Model PE-740

Interprocessor Bus Interface

Technical Manual

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REVISION HISTORY

ECO No.	Date	Description	Pages
0328	6/28/84	New ZETACO Cover	
0523	3/3/86	New Cover	
0584	4/4/86	Update Manual and Board Cover	

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1.0 PRODUCT OVERVIEW

ZETACO's Model PE-740 Interprocessor Bus Interface provides a means for high speed asynchronous communications between two Data General Nova 3 or Nova 4 minicomputers. The two controllers in this set support bidirectional, half-duplex or full-duplex communications and have the ability to interrupt the program in the event that a loss of signal from the other computer is detected.

The controllers tranfer two types of information between them, data and status, without an intermediate storage device. Data is transferred between an accumulator in one processor to the accumulator in the other, under direct program control in one 16-bit word at a time. Status information is transferred by the setting of Busy and Done flags. By checking Busy and Done status the processors can achieve data transfer rates of 100,000 sixteen-bit words per second. Using program interrupts, the data transfer rate is limited by the time required to service the interrupts.

2.0 SYSTEM CONFIGURATION

The controllers occupy I/O slot 10 in each Nova 3 computer. Slot 10, via the backplane, is connected to a board-edge connector designated P4. An external cable is provided that mates with the board-edge connectors, establishing the communications system. The controller can also be used in any I/O slot of a Nova 3 or Nova 4. This configuration does require internal and external cabling. The PE-740 is a direct replacement for the Data General 4240 Interprocessor Bus Controller and is compatible with Operating, Reliability and Diagnostic Software.

The system configuration is determined by the external cable, which establishes which controller is the right and which is the left. Full-duplex registers on the left-side controller are not used. All data is latched (stored) on the right-side controller.

There are no switch or jumper selectable options on this product.

2.1 OPERATIONAL CHARACTERISTICS

As shown in Figure 2.1, the controllers are designated left and right. The right controller serves as the data holding area, while the left controller serves in a gating capacity. The designation of right and left does not affect the programming, or the communications abilities, of either computer in the system.

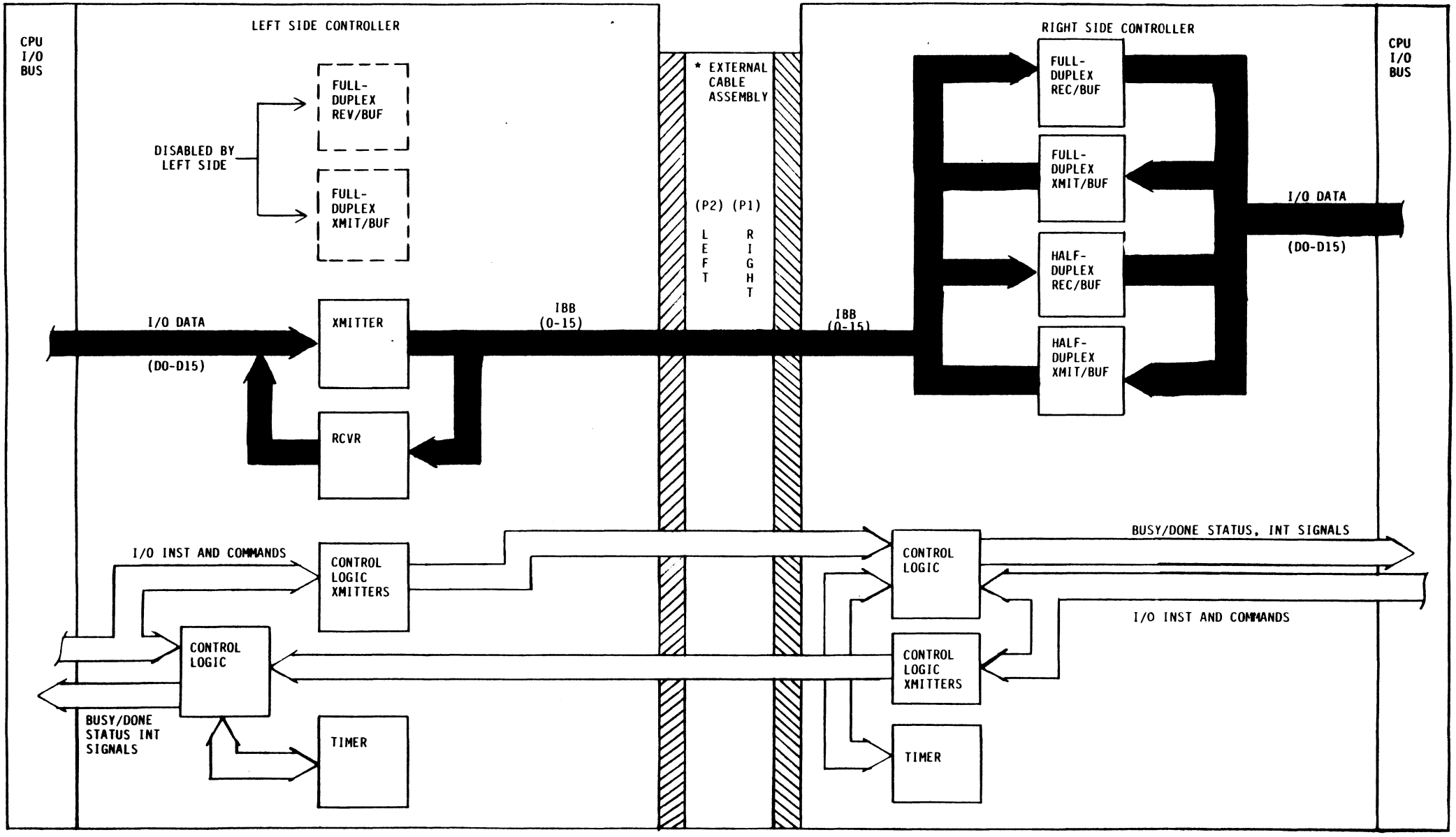
The data holding areas of the right-side controller consist of four 16-bit storage buffers and associated receivers.

The storage buffers are under control of one processor while the receiver is under control of the other processor. Each processor controls one full-duplex and one half-duplex storage buffer and one full-duplex and one half-duplex receiver.

In full-duplex communications, the full-duplex storage buffer is referred to as a 16-bit full-duplex transmitter and responds to device code 41. The processor's full-duplex receiver is referred to as a 16-bit full-duplex receiver and responds to device code 40.

In half-duplex communications, the processor's half-duplex storage buffer and half-duplex receiver are referred to as a 16-bit half-duplex transmitter/receiver and respond to the same device code 36.

Device code 37 is used by the missing pulse detectors of each controller. Each detector consists of a one-second timer that is continually restarted by the execution of the appropriate I/O instruction, in the other computer, at regular intervals of one second or less. When one computer fails to restart the timer in the other computer within the specified time period, that timer's Done flag is set to one, generating a program interrupt request in the computer in which the timer is installed. Additionally, when a computer knows that it is about to cease functioning, that computer may set the other computer's timer Done flag directly by executing the appropriate I/O instruction.



* CABLE DETERMINES LEFT/RIGHT CONTROLLER

FIGURE 2.1 PE-740 Configuration/Designation

3.0 TROUBLE-SHOOTING, TEST PROGRAMS AND CUSTOMER SERVICE

3.1 TEST PROGRAMS

This controller is software compatible with DG Model 4240 Interprocessor Bus and runs DG DTOS Diagnostic and Reliability programs provided on the DTOS tape. These programs should be run to verify the status of the controller.

3.2 CUSTOMER SUPPORT HOTLINE

ZETACO, Inc. provides a Customer Support Hotline (612-941-9480) to answer technical questions and to assist with installation and trouble-shooting problems. The Hotline is manned by a technical team from 8:00 a.m. to 5:00 p.m. (Central Time) Monday through Friday.

To facilitate over-the-phone trouble-shooting, please fill out the checklist on the following page before placing your call.

HOTLINE TROUBLE-SHOOTING CHECKLIST

CPU_____Operating System and Rev._____

Is this Controller replacing a previously installed subsystem?_____

Device Code of new Controller:_____ Any similar subsystem in the CPU? YES NO If yes, then its Device Code:_____

Configuration Facts_____

Problem Description_____

Problem happens when (in use by Operating System, Reliability, etc.)?

Intermittent or consistent problem?_____

Priority of Board in CPU (Slot)_____

Reviewed Interrupt and Priority Jumpers on Vacant Slots?_____

Tried Different Slot?_____

Cleaned DG gold-fingered contact points of board and reset board?___

Does DTOS tape "BOOT" correctly?_____

Result of DG DTOS Reliability or Diagnostic:_____

3.3 PRODUCT RETURN AUTHORIZATION

When controller malfunction has been confirmed using the tests outlined in Section 3.0, the board can be returned to ZETACO for warranty repair or for time-and-material repair if the product has been damaged or is out of warranty. A Return Material Authorization (RMA) number is required before shipment and should be referenced on all packaging and correspondence.

To ensure prompt response, the information outlined in the Material Return Information form on the following page should be gathered before calling the ZETACO Hotline for the RMA number. Please include a completed copy of the Material Return Information form with the product. Each product to be returned requires a separate RMA number and Material Return Information form.

To safeguard the Controller during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

3.4 WARRANTY INFORMATION

All ZETACO controllers and couplers are warranted free from manufacturing and material defects, when used in a normal and proper manner, for a period of up to two years from date of shipment. Except for the express warranties, stated above, ZETACO disclaims all warranties including all implied warranties of merchantability and fitness. The stated express warranties are in lieu of all obligations of liabilities on the part of ZETACO for damages, including but not limited to, special, indirect or consequential arising out of or in connection with the use or performance of ZETACO's products.

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to ZETACO for repair. This will: 1) Determine if the board is actually defective. 2) Increase the speed and accuracy of a product's repair, which is often dependent upon a complete understanding of the user's checkout test results, problem characteristics, and the user system configuration. Test results for the disk controller should be obtained by performing the tests below. (Use back of page if more space is needed.)

TEST	RESULT
Diagnostics	_____
Reliability	_____

Other tests performed (system operation, errors, etc.):

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this information with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain.)

2. Under which operating system are you running? Include Revision number.

3. Describe the system configuration, (i.e. peripherals, controllers, model of computer, etc.).

4. Has the controller been returned before? Same problem?

To be filled out by CUSTOMER:

Model #: _____
Serial #: _____
RMA #: _____ (Call ZETACO to obtain an RMA number.)

Returned by:

Your name: _____
Firm: _____
Address: _____
Phone: _____

4.0 PROGRAMMING NOTES

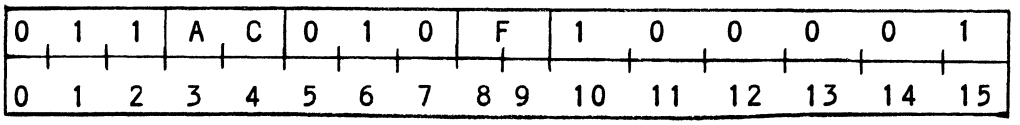
4.1 FULL-DUPLEX COMMUNICATIONS

The full-duplex communications link provides for high speed, bi-directional communications between processors. Each processor controls one full-duplex transmitter/buffer and one full-duplex receiver/buffer, which allows data to be transferred between processors. Because of the high-speed data transfer rate, the PE-740 appears to be full-duplex. Actually, data is transferred over the half-duplex bi-directionally data bus (IBB0-IBB15). Data transfer is accomplished by one processor executing a Write Data instruction (which loads data into buffer) and the other processor does a Read Data instruction (gates buffer data onto I/O bus).

4.1.1 TRANSMIT DATA

When a Write Data instruction (DOA AC, DP0) is executed, the transmitting processor transfers data from the specified accumulator to the PE-740. If the instruction was initiated by left processor, the data passes through the left controller to the storage buffer on the right controller. If the right CPU initiated the instruction, data is loaded directly into the buffer on the right controller.

DOA AC, DP0 (WRITE)



FUNCTIONS

S In the computer executing the instruction, the DP0 Busy flag is set to 1 and the DP0 Done flag is set to 0. In the other computer, if the DP1 Busy flag is 1, the DP1 Done flag is set to 1 and DP1 Busy flag remains unchanged.

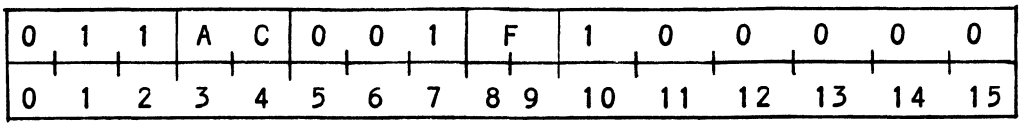
C In the computer executing the instruction, the DP0 Busy and Done flags are both set to 0.

P This command has no effect.

4.1.2 RECEIVE DATA

When a Read Data Instruction (DIA AC, DPI) is executed, the receiver passes the contents of the storage buffer to the specified accumulator of the processor. If the instruction was initiated by the right processor, the receiver passes data directly to the I/O bus. If the left processor initiated the instruction, the buffer data of the right controller is passed to the receiver of the left controller and on to the I/O bus.

DIA AC, DPI (READ)



FUNCTIONS

S In the computer executing the instruction, the DPI Busy flag is set to 1 and the DPI Done flag is set to 0. If the DPI Busy was 1 before this instruction was issued, then, in the other computer, the DPO Busy flag is set to 0 and the DPO Done flag is set to the prior value of the DPO Busy flag.

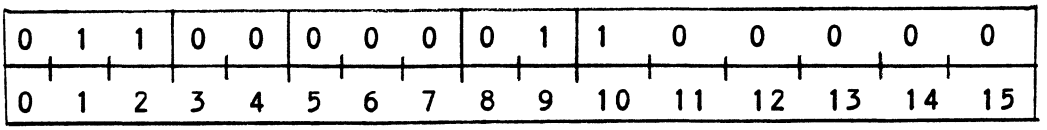
C In the computer executing the instruction, the DPI Busy and Done flags are both set to 0. In the other computer, the DPO Busy flag is set to 0 and the DPO Dong flag is set to the prior value of the DPO Busy flag.

P This command has no effect.

4.1.3 INITIATE RECEIVE

Before a transfer begins, the computer has no way of knowing whether or not its receiver (DPI) buffer contains meaningful information. Therefore, the computer executing the DPI instruction issues an initiate receiver instruction (NIOS DPI) and waits until the other computer has placed meaningful data in the buffer before doing a Read.

NIOS DPI



In the computer executing the instruction, the DPI Busy and Done flags are set to 1 and 0 respectively. If the DPO Busy flag of the other computer is 1, the DPI Done flag of the computer executing the instruction is set to 1 immediately. If the DPO Busy flag of the other computer is 0, the DPI Busy and Done flags of the computer executing the instruction will remain set to 1 and 0 until the DPO Busy flag of the other computer is set to 1.

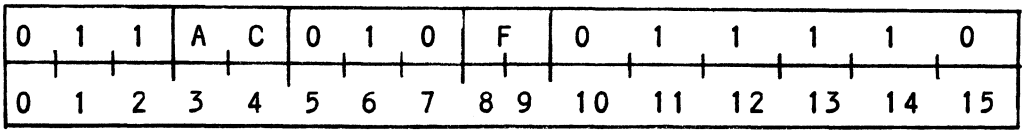
4.2 HALF-DUPLEX COMMUNICATIONS

The half-duplex communications link provides the facilities for bi-directional, half-duplex communications between processors. The half-duplex facility also provides, when appropriate software is used, the logic that governs the setting of Busy flags of both half-duplex devices, allowing the program to establish an "interlock". Each processor controls one half-duplex transmitter/receiver. While the transmitter/receiver is actually two separate devices, they both respond to the same device code and thus can only assume one role at a time. This arrangement allows for transfer of information in one direction at a time.

4.2.1 TRANSMIT DATA

When a Write Data instruction (DOA AC, IPB) is executed, the transmitting processor transfers data from the specified accumulator to the PE-740. If the instruction was initiated by the right-side processor, the data is loaded directly into the half-duplex buffer on the right controller. If the instruction was initiated by the left-side processor, the data passes from the I/O data bus through the left-side controller to the buffer on the right-side controller.

DOA AC, IPB (WRITE)



FUNCTIONS S In the computer executing the instruction, the IPB Busy flag is set to 1 if the IPB Busy flag of the other computer is 0. Even if both computers issue a Start at exactly the same time, only one IPB Busy flag will be set to 1.

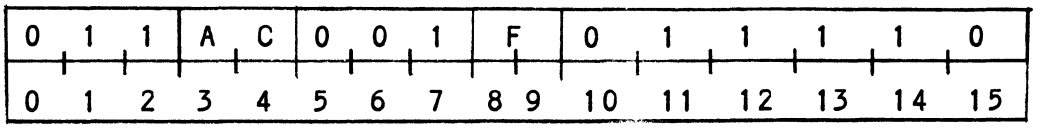
C In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Busy flag is set to 0.

P In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Done flag is set to 1.

4.2.2 RECEIVE DATA

When a Read Data instruction (DIA AC IPB) is executed, the receiver passes data from the storage buffer to the I/O bus, which passes data to the specified accumulator. If the instruction was initiated by the right-side processor, the data is passed directly from the buffers of the right-side controller to the I/O bus. If the left-side processor initiated the instruction, data is passed from the buffers on the right-side controller, across the cable (IBB Bus) to the left controller, and then to the I/O bus.

DIA AC, IPB (READ)

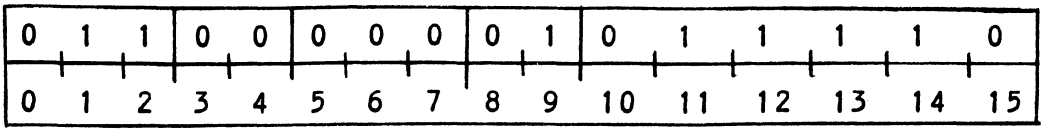


FUNCTIONS The functions are the same as described for Receive (Write). (See Section 3.2.2.1.)

4.2.3 REQUEST BUS

The Request Bus instruction (NIOS IPB) is used by an initiating processor to gain access to the half-duplex bus. Upon issuing the Request Bus, the Busy flag of the requesting processor will be set to a 1 if the Busy flag of the other processor is not set. If the Busy flag of the other processor is set, the Busy flag of the requesting processor is not set. If the Busy flag of the other processor is set, the Busy flag of the requesting processor is not set and the requesting processor must bid for bus again at a later time, after the other computer releases its lock.

NIOS IPB

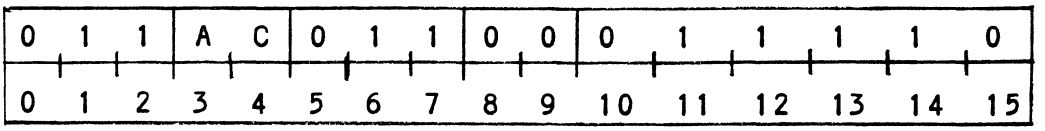


In the computer executing the instruction, the IPB Busy flag is set to 1 if the IPB Busy flag of the other computer is 0.

4.2.4 CLEAR FLAGS

When a processor has completed transferring a block of data, it issues a Clear Flags (DIB) instruction to set its IPB Busy and Done flags to 0. This unlocks the system and prepares it for another lock procedure.

DIB IPB



The IPB Busy and Done flags in the computer executing the instruction are both set to 0.

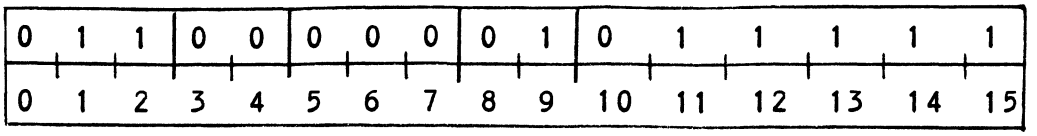
4.3 TIMER OPERATION

The Timer provides a means for generating an interrupt in either computer when the other computer fails to execute a specific instruction or generates a signal indicating probable power fail condition. This capability is implemented by a missing pulse detector on each controller, along with the Timers Done flag.

Each detector consists of a one-second timer that is normally restarted by the execution of a Start Timer. Another means of setting a timer is the Set Timer instruction, used to notify the other computer when a computer is about to cease operations. Once a Timer Done flag is set, the computer should issue a Clear Timer instruction to set the Done flag to 0; otherwise, the processor will be continually notified of a failure.

4.3.1 START TIMER

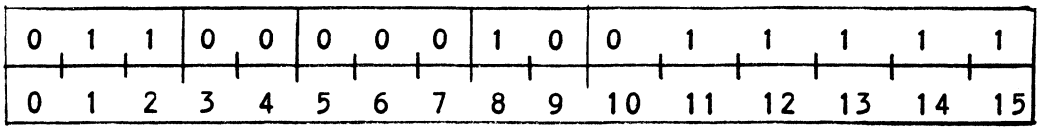
NIOS IVT



The one-second timer in the other processor is started.

4.3.2 CLEAR TIMER

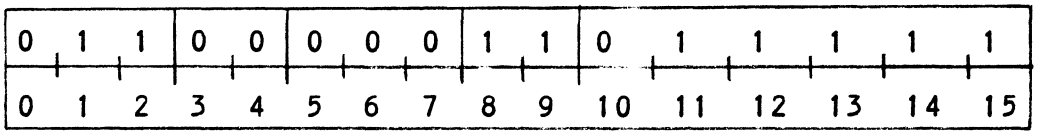
NIOC IVT



In the computer executing the instruction, the IVT Done flag is set to 0.

4.3.3 SET TIMER

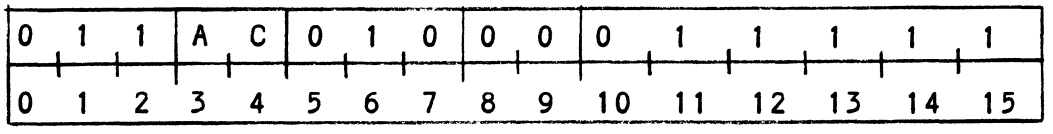
NIOP IVT



The IVT Done flag in the other processor is set to 1.

4.3.4 START OWN TIMER

DOA IVT



In the computer executing the instruction, the timer is started.