Model 480

Slot Saver II Controller

600-210-00 A

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REVISION HISTORY		
ECO #	DATE	DESCRIPTION
0328	6/28/84	New ZETACO Cover

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PRODUCT RETURN AUTHORIZATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to ZETACO for repair. However, if controller or module malfunction has been confirmed, you should return the part to ZETACO. If the part is no longer under warranty, or if the problem is not warranted, then repair will be on a time-and-material basis. A Return Material Authorization (RMA) number is required before shipment and should be referenced on all packaging and correspondence.

To ensure prompt response, the information outlined in the Material Return Information form on the following page should be gathered before calling the ZETACO Hotline for the RMA number. Please include a completed copy of the Material Return Information form with the product. Each product to be returned requires a separate RMA number and Material Return Information form.

To safeguard the product during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to ZETACO, Inc. for repair. The speed and accuracy of a product's repair is often dependent upon a complete understanding of the user's checkout test results, problem characteristics, and the user system configuration. Use the form below to record the results of your trouble-shooting procedures. If more space is needed, use additional sheets.

FUNCTION	TEST	RESULT
Serial Port	GNSTP	_____
Real Time Clock	RTCD	_____
Line Printer	LPTD	_____
MUX	QTYDR	_____

Other tests performed:

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this information with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain.)

2. Under what operating system are you running? (AOS, AOS/VS, RDOS, etc.)

3. Describe the system configuration (i.e.; peripherals, controllers, model of computer, etc.)

4. Has the unit been returned before? Same problem?

To be filled out by CUSTOMER:

Model #: _____
Serial #: _____
RMA #: _____ (Call ZETACO to obtain an RMA number.)

Returned by:

Your name: _____
Firm: _____
Address: _____
_____
Phone: _____

TABLE OF CONTENTS

The Slot Saver II does not limit your choice of peripheral device manufacturers. The logic for each interface controller offers you extensive flexibility in your selection. You can choose the model of each peripheral device that best fits your application, although the model must be specified at the time of order. This same flexibility is offered in your choice of device codes for special system applications.

Software compatibility is a key feature of the Slot Saver II controller board. And, in some cases, an expanded instruction set is designed into the logic which, at the option of the programmer, permits use of special features available in certain peripheral equipment.

Board Layout

Individual controllers included on the Slot Saver II are listed below and include a brief description.

Basic Interface Subassembly

The general interface subassembly consists of the 15-inch by 15-inch printed circuit board upon which the other controllers are mounted. This assembly also includes certain I/O command and data bus buffering logic common to all the controllers on the board.

Console Terminal Controller

This controller provides interface logic for the system serial console terminal (device code 10/11) which can be either a current loop or RS-232 device operating in a full duplex mode. Baud rates (110 to 19.2K) and data format are selectable with jumpers on the board. Flexible interface logic permits the use of a CRT, teletype or teleterminal device as the system console.

Second Console Terminal Controller

This option contains the logic for a second serial terminal device channel with an RS-232C or current loop interface. Clocking of data is controlled by an internal clock signal. The desired baud rate should be specified at the time of order but is easily changeable by jumper on the board. The device code is normally

set at 50/51 unless a special code is requested. This controller is frequently used to control a line printer with a serial interface.

Programmable Real Time Clock

The Real Time Clock controller provides four frequencies selectable under program control: 60Hz, 10Hz, 100Hz and 1000Hz. Frequency sources are the AC lines for 60Hz and a crystal oscillator for the other frequencies.

Parallel Line Printer Controller

The controller operates with a line printer containing a parallel interface made by Centronics, Data Products, Control Data, Printronix, General Electric and others. The controller includes all required cabling (20 feet standard; longer lengths available at extra cost). Specify printer manufacturer and model number when ordering.

Four Channel Multiplexer

This controller provides control for four serial ports which may be teleterminals or CRT's. Baud rates and data formats are selectable on an individual channel basis. Full modem control, including Ring Indicator, Data Terminal Request, etc., for use for remote communications terminals is available for a few of the four channels.

For larger systems, the four channel multiplexer is compatible with additional four or eight channel multiplexer boards built by ZETACO, Inc.

Documentation Package

The controller board is shipped with a complete documentation package, including installation instructions, programming instructions, diagnostic software and logic schematics.

2.0 Installation Instructions for Slot Saver II Controller

2.1 Unpacking

Upon receiving the interface package, unpack the contents and inspect the board and cable assembly for visual damage. If any damage is apparent, do not attempt to install the controller and notify ZETACO, Inc. immediately.

2.2 Board Installation

The Slot Saver II controller board is usually installed in the general input/output slot of a Data General Nova or Eclipse minicomputer. In the case of a Nova 1200 Series or Nova 2, this is the third board slot from the bottom of the computer. For a Nova 3 or an Eclipse, the general I/O slot is slot 4.

An alternative way of determining the general I/O slot is to examine the end plane of the computer as indicated in Figure 2-1. For the Nova 2 or later models, the general I/O slot has two extra pins between the A and B connectors.

Although in principle the Slot Saver II can be inserted into any slot above slot 2, unless the general I/O slot is used problems can occur unless proper jumpering is made on the end plane of the Data General minicomputer. Leaving a blank slot between boards can interrupt the continuity of the data channel and interrupt priority lines, thereby preventing operation under interrupt control.

Once the slot to insert the board has been selected, the interrupt and data channel priority pins A94 and A96 on the computer back plane should come from the card below it. If there is no card below it, A94 and A96 should be wirewrapped to A93 and A95, respectively, of the first active slot below it.

In order to prevent printed circuit boards from being accidentally inserted into slots in which they may be damaged, there are keys in the female edge connectors on the back panel. A key is a small obstruction (usually made of nylon) that prevents a board from being inserted into a female edge connector unless the board has a matching slot cut into it.

The board should be carefully inserted into the proper slot in the computer with the locking tabs extended (see Figure 2-2). If the card is properly seated in the track, very little pressure is required to seat the board in the

edge plane connectors. The card should be removed and the alignment checked if resistance to seating is observed.

2.3 Cable Installation

Electrical connections between the Slot Saver II controller board and peripheral equipment located outside the minicomputer chassis are made with external cable assemblies to the back plane of the computer. The design and installation of these cable assemblies vary with each model of Data General minicomputer and peripheral device.

2.3.1 Computer Back Panel

The back panel of the computer provides a means for interconnecting the computer, memory, console and various controller boards and cabling to external peripheral equipment. The back panel is the vertical printed circuit board mounted on the left side of the computer chassis when viewed from the front.

On the side of the back panel facing into the chassis are 10 or 12 pairs of printed circuit board female edge connections, one pair for each slot (Figure 2-2). The contacts of these connectors protrude through the back panel to the left side of the minicomputer chassis.

When the male edge connectors of a printed circuit board are inserted into the female edge connectors of a slot, finger contacts on the male edge connectors meet contacts in the female edge connectors. Electrical connections to boards can, therefore, be made to pins on the back panel.

For each controller card slot, there are two horizontal parallel rows of 100 pins on the back plane. The left group of pins is the A connector, and the right group (as viewed from the left side of the computer) is called the B connector. Numbering of each group of 100 pins is as indicated below (shown only for A connector).

BACK PANEL NUMBERING

A1	A3	A5	A7	A9	A11	A13	A15	A17	A19	A21	A23	A25	A27	A29	A31	A33	A35	A37	A39	A41	A43	A45	A47	A49	A51	A53	A55	A57	A59	A61	A63	A65	A67	A69	A71	A73	A75	A77	A79	A81	A83	A85	A87	A89	A91	A93	A95	A97	A99
A2	A4	A6	A8	A10	A12	A14	A16	A18	A20	A22	A24	A26	A28	A30	A32	A34	A36	A38	A40	A42	A44	A46	A48	A50	A52	A54	A56	A58	A60	A62	A64	A66	A68	A70	A72	A74	A76	A78	A80	A82	A84	A86	A88	A90	A92	A94	A96	A98	A100

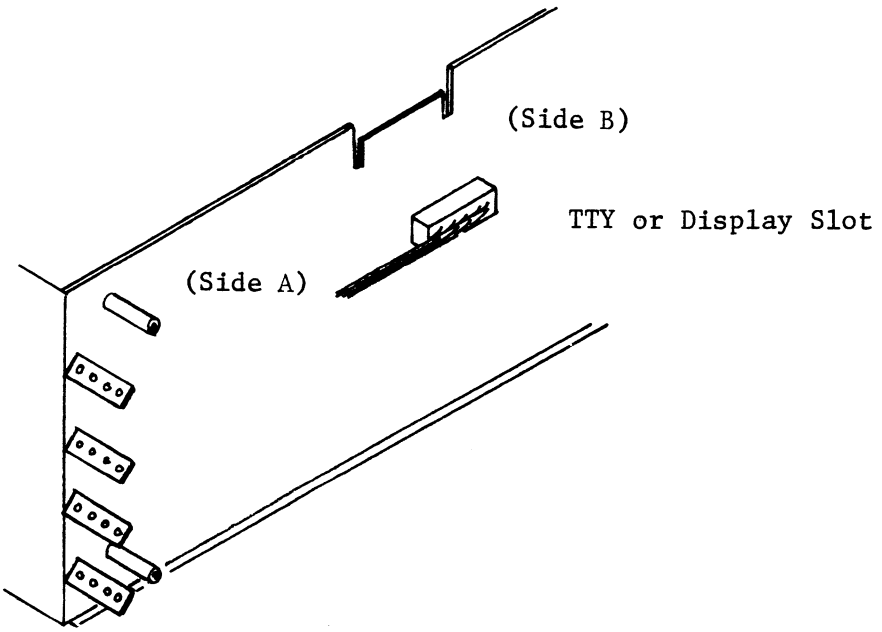


Figure 2-1

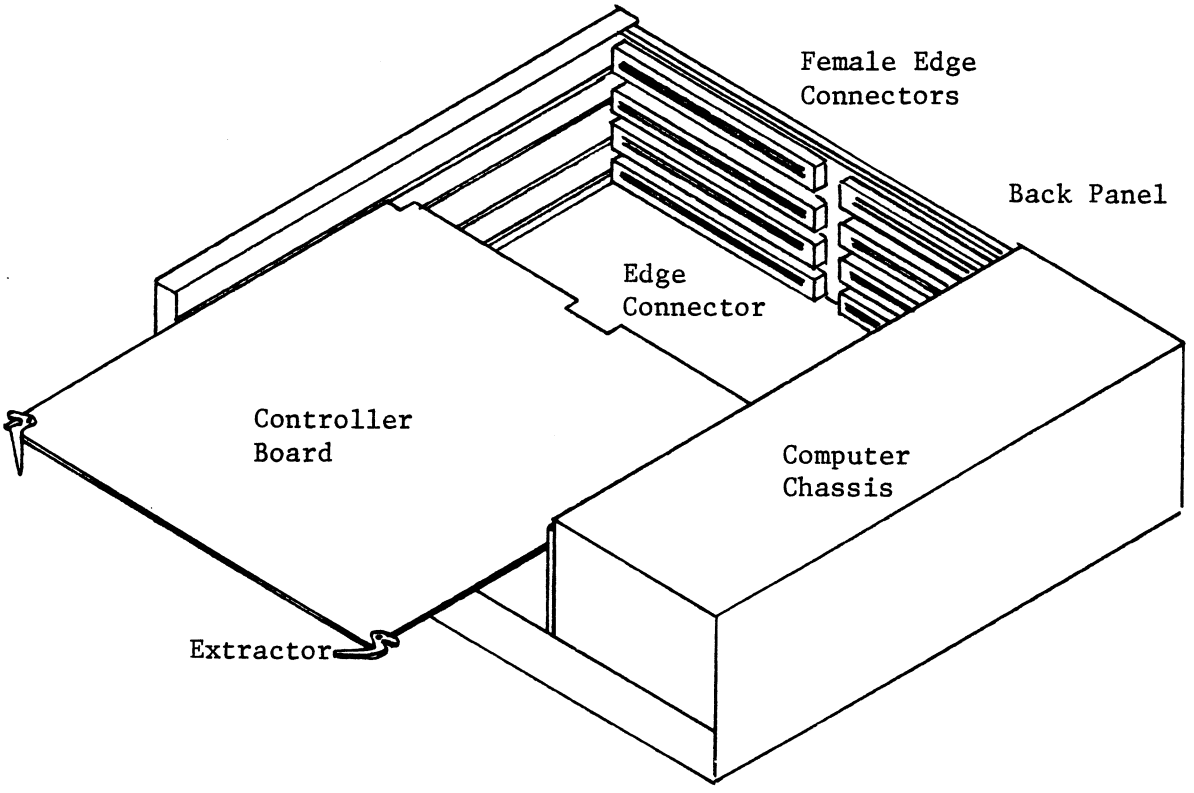


Figure 2-2: Board Installation

Pin 1 is on the top left of the connector; pin 2 is on the bottom left directly below pin 1. Pin 99 is the top right pin of the connector, and pin 100 is the bottom right.

2.3.2 External Cable Assemblies

Because of the variations in mechanical design of the connector mounting area at the rear of the various models of computer, several cable assembly designs are employed. These basically fall into two categories:

1. Single piece cable assemblies
2. Two piece cable assemblies

The single piece cable assemblies (Figure 2-3) consist of a single cable which plugs on to the computer end plane at one end and on to the external peripheral device (such as a line printer) on the other end. Stress relief for the cable is provided with a ty wrap at the rear of the computer. This type of cabling is most often used with the Nova 3 and Eclipse models where the room to mount connectors at the rear of the computer is severely limited.

Two piece connector assemblies (Figure 2-4), on the other hand, consist of a short (18-inch) cable which plugs on the computer end plane and terminals, with a connector at the rear of the computer, plus a longer external cable which goes from the rear of the computer to the external peripheral device. These two piece assemblies are used most frequently with the Nova 1200 and Nova 2 models. The two piece assemblies are more difficult to install but offer the advantage that the minicomputer can be easily uncabled from the peripheral equipment and removed from the cabinet for service.

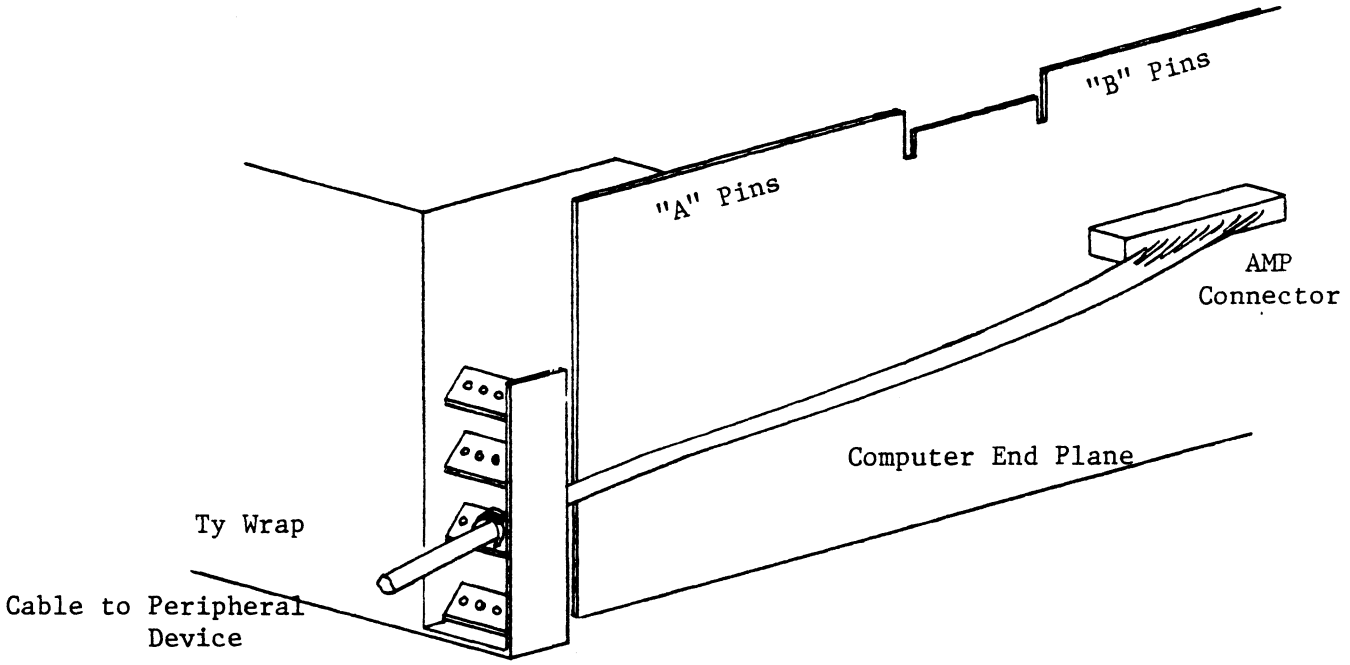


Figure 2-3: Typical Single Piece Peripheral Cable Assembly

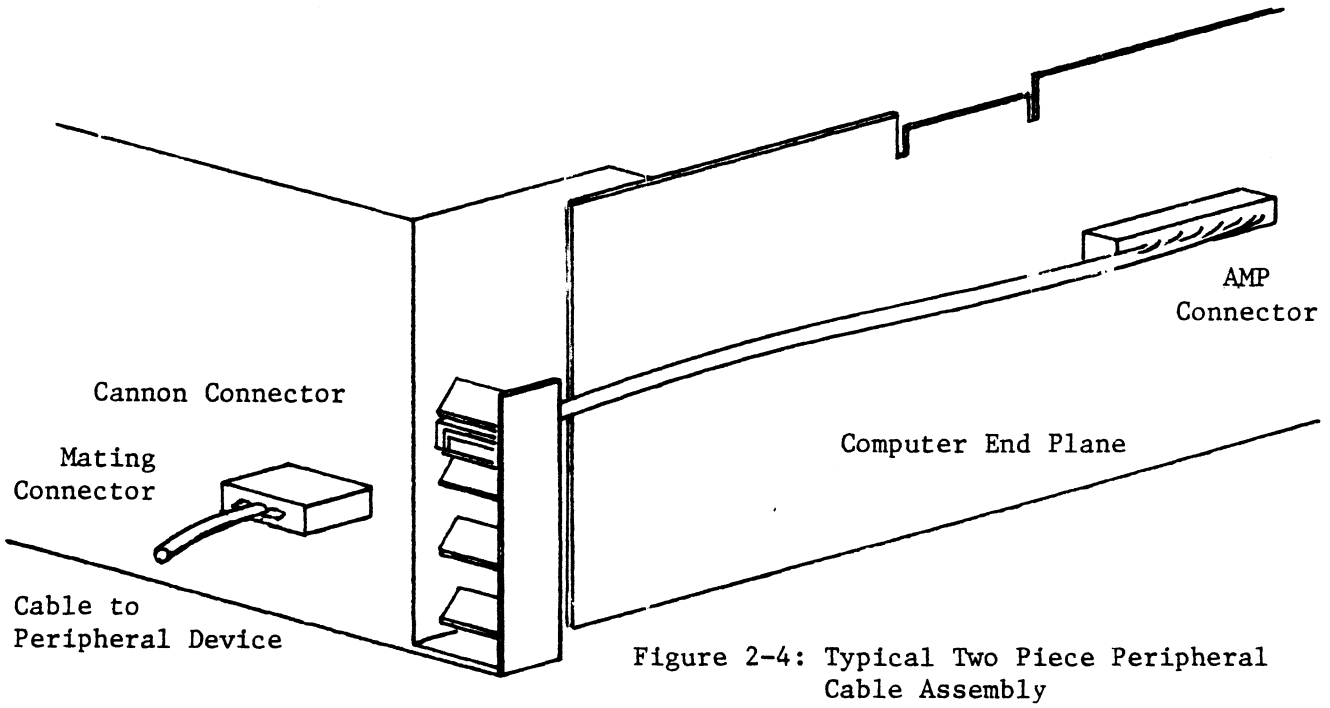


Figure 2-4: Typical Two Piece Peripheral Cable Assembly

3.0 Loading of Diagnostic Programs

3.1 Auto Binary Loader

Prior to loading a controller diagnostic program tape, it is necessary to read in a paper tape binary loader. For machines equipped with the Automatic Program Load option, the Data General Auto Loader Binary program should be used. The procedure for loading this tape is as follows:

1. Load the loader in the paper tape reader (or teletype reader).
2. Preset the console data switches to octal 12, the device code of the paper tape reader (switches 12 and 14 up, all others down). If a teletype reader is used, then an octal device code 10 should be set (switch 12 up).
3. Hit the reset and then the program load switches. The tape should read in and will stop on the last punched frame on the tape.
4. If a proper read operation has occurred, remove the loader tape from the reader.

3.2 Manual Program Loading

If the minicomputer is not equipped with the Automatic Program Load option, the operator must use the data switches to load the bootstrap loader, which is used only to bring in a more extensive binary loader. This latter program resides in high core and is used to read in the controller diagnostic program.

There are two versions of the bootstrap loader; one for the teletype reader, the other for the high speed paper tape reader. In the following listing, the first two columns indicate the memory location (shown for a 4K system) and its contents. To load the program, simply use the console switches to place the octal numbers in the locations specified. For a memory of any other size, load the bootstrap program beginning at a location whose address is 20_8 less than the largest address.

Bootstrap Loader

```
X7757    126440    GET:    SUBO   1,1        Clear AC1, carry
X7760    06361Y             SKPDN  TTI
X7761    000777             JMP    .-1        Wait for DONE
X7762    06051Y             DIAS   0,TTI      Read into ACo and restart reader

X7763    127100             ADDL   1,1        Shift AC1 left 4 places
X7764    127100             ADDL   1,1
X7765    107003             ADD    0,1,SNC    Add in new word
X7766    000772             JMP    GET+1      Full word not assembled yet
X7767    001400             JMP    0,3        Got full word, exit

X7770    06011Y    BSTRP:   NIOS   TTI        Enter here, start reader
X7771    004766             JSR    GET        Get a word
X7772    044402             STA    1,.:2      Store it to execute it
X7773    004764             JSR    GET        Get another word
                            ...                This will contain an STA (first
                                                 STA 1,.+1)
                            ...                This will contain JMP .-4
```

Y = 0 for teletype reader
Y = 2 for paper tape reader

X is determined by the computer memory size according to the following table:

Memory Size	X
8K words	1
16K words	3
24K words	5
32K words	7

Once the bootstrap loader has been entered, the binary loader (DGC #091-000036) is then placed in the teletype reader or high speed reader. Set the data switches to X7770. Then press the START switch. The loader will read in and halt on the last punched frame. You are now ready to load a diagnostic tape.

3.3 Loading the Diagnostic Tape

Once the binary loader has been read into the computer, the next step is to read in the diagnostic program tape. The starting address for the binary loader is determined by the size of the core memory in the minicomputer as indicated in the following table.

Core Size	Octal Starting Address
8K words	*117777
16K words	137777
24K words	157777
32K words	177777

*NOTE: If a teletype reader is used instead of a paper tape reader, switch zero must be down in the starting address.

3.4 Diagnostic Operating Instructions

The operating instructions for the controller diagnostic are included in the comments section in the beginning of each diagnostic program listing.

4.0 Common Peripherals

The Common Peripheral section includes the Slot Saver II printed circuit board with extractors and handle and contains the logic required by all the other controllers.

4.1 Theory of Operation

The common peripheral logic in this section is used primarily for buffering command signals from the computer data buses. As an example, a signal such as STRT is used on all of the controllers included on the Slot Saver II board. Attaching each of the circuits requiring this signal directly to the CPU bus (pin A52) would impose a substantial load since similar loads could also be applied to this same pin on all available I/O slots within the computer. Therefore, the design approach used on this board is to present only one load (receiver) to each CPU signal. The single receiving circuit then in turn drives all loads requiring the signal on a single I/O board. This approach is not used with circuits which drive the computer buses since drivers impose different load conditions than do receivers.

The Common Peripheral section also provides the interrupt priority logic for the various controllers on the Slot Saver II board. The console serial terminal has the highest priority and the four channel multiplexer the lowest.

Buffering of the device code select lines is also provided by the common peripheral logic. There are actually two sets of device code selection logic on the Slot Saver II board. The first set of gates handles the device codes for the console serial device (teletype or CRT), real time clock, four channel multiplexer and line printer. Since the controllers for these devices must use a standard set of device codes to maintain software compatibility, all of these device codes are essentially fixed.

The common peripheral logic decodes the three most significant bits of the device code with the least significant three bits included in the logic of each peripheral controller (001 XXX).

The device code for the second serial channel is selectable with a series of jumpers. This device code is normally set up for 50/51 but may be modified for any desired code.

The final section of logic in the Common Peripheral section is associated with placing the device code of an interrupting device on the data bus lines in response to an interrupt acknowledge instruction from the computer.

4.2 Checkout Procedure

Checkout of the common peripheral logic is not required unless none of the peripheral controllers on the board are operable. The checkout procedure listed below requires the use of an oscilloscope and board extender and requires a technical understanding of the operation of the computer.

The short test programs listed below should be entered into the computer memory through the console data switches. Each program then allows the technician to focus on a particular portion of the common peripheral logic and to confirm its operation. Refer to the logic schematic for gate and pin references.

Test 1: Verify Receipt of Data From the Data Bus

Location	Octal Program	Pneumonic	Comments
100	062677	IORST	
	060477	RDS 0	Read switches
	061010	DOA 0,10	Output data word
	000775	JMP *-3	

The program starts at location 100. When the program is running, console switches 8 through 15 can be raised and lowered one at a time while looking for a pulse on the data 8 through data 15 signals. Trigger oscilloscope from I/O Reset A (gate H1-6).

Test 2: Device Code Logic

Using the same program as above, signals DS3, 4, 5 and their complements can be checked with a scope. Pin N1-12 should also be viewed to confirm the presence of the common select pulse.

Test 3: Verify Presence of Command Pulses

Octal Program		Pin
063677	IORST	N1-3
060110	NIOS,TTI	D1-3
060210	NIOC,TTI	C1-11
060310	NIOP,TTI	E1-3
060410	DIA 0,TTI	C1-8
061010	DOA 0,TTI	D1-8
061410	DIB 0,TTI	C1-6
061477	INTA	C1-3
062077	MSKO 0,CPU	B1-10
000767	JMP *-9	---

By triggering on Pin H1-6 ($\overline{\text{I/O Reset B}}$), the command functions listed below will be successively displayed in time. Request enable signal D1-2 can be checked any time the computer is in the run mode. The presence of INTA signal should also be checked on G1-11.

Note that a short pulse appears on the clear line shortly following each IORST as well as from the NIOS instruction. A pulse appears on the Data In B line during the MSKO instruction too. This is just the way the logic within the computer works and is not a function of the I/O board.

Test 4: Verify Basic Board Timing

The basic timing for the Slot Saver II board is generated by a 3.072MHz oscillator. This signal is shaped by the inverter A2-12 and then divided by two and ten, respectively, to give frequencies of 1536KHz (A3-12) and 307.2KHz (A3-11).

Test 5: Interrupt Priority Logic

Pin D1-11 should be at ground if the board is placed in the lowest available slot in the machine. If no devices are requesting an interrupt, pin K2-6 will also be at ground. By selectively touching the various device interrupt request lines (example: Pin L2-1) to ground with a jumper wire, pin K2-6 should go high (+3V).

CKT-PIN	Signal
L2-1	$\overline{\text{TTI(1) INT REQ}}$
L2-13	$\overline{\text{TTO(1) INT REQ}}$
M2-1	$\overline{\text{TTI(2) INT REQ}}$
M2-13	$\overline{\text{TTO(2) INT REQ}}$
L2-5	$\overline{\text{LPT INT REQ}}$
M2-9	$\overline{\text{CLK INT REQ}}$
K2-4	$\overline{\text{MUX INT REQ}}$

4.3 Schematic Drawing

The logic for the Common Peripheral option is included on ZETACO's drawing number 700-210-00.

5.0 Serial Communication Devices

5.1 Introduction

The Slot Saver II controller can be configured for up to two serial peripheral devices. Most commonly, this will consist of the system console teletype or CRT (device 10/11) and, in a slightly larger system, a second CRT (device 50/51). Either of the two channels may be configured for a current loop or RS232C interface. Available baud rates cover the range from 110 baud to 19.2K baud.

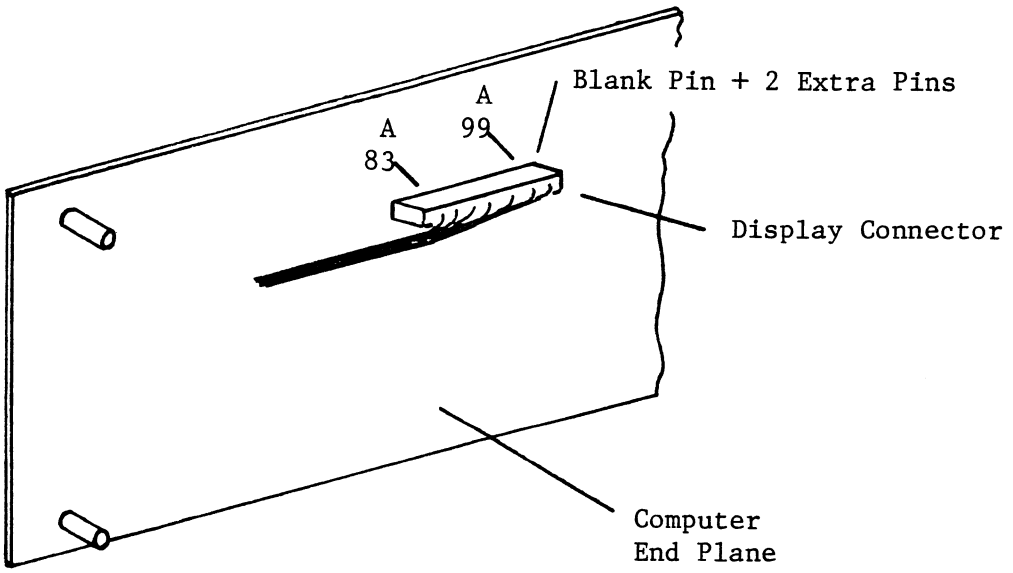
The second serial device can also be used for serial models of line printer; such as, GE Terminet 300 or Terminet 1200. In this application, the device code for the second serial channel should be changed by jumper to 17 and the mask bit to 12. The parallel line printer controller must then be disabled or its device code changed.

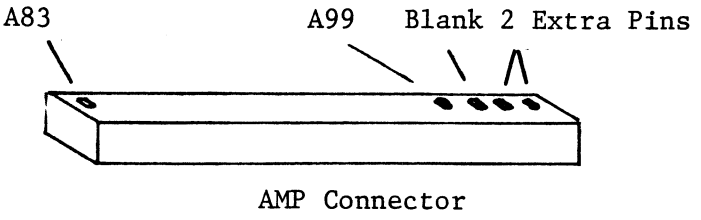
5.2 Installation

The installation instructions for the Slot Saver II controller board are included in Section 2.0 of this manual.

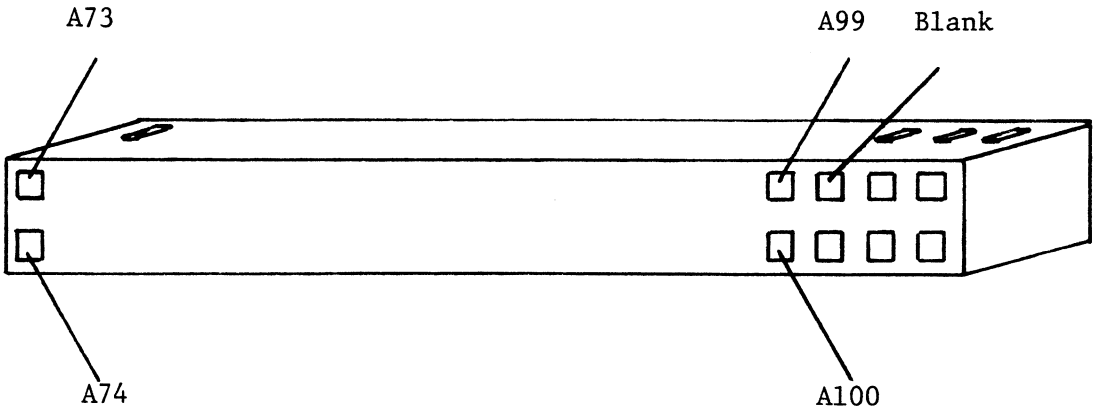
Display Terminal Cable

The system console CRT or teletype is most frequently cabled using a single piece cable assembly. Slot 3 of a Nova 1200 or Nova 2 or slot 4 of the Nova 3 or Eclipse contains two extra pins between the A and B connectors on the computer end plane. Installation of the cable consists of pushing the single row AMP connector located on the computer end of the cable over these end plane pins and then securing the cable to the rear of the computer with a ty wrap. The relationship between the AMP connector and the end plane pins is shown in the following sketches.





If the system contains two serial devices (CRT or teletype), a dual row AMP connector is used. A sketch indicating the place to plug this connector is shown below.



Baud Rate Jumpering

Baud rates for the two serial devices on the Slot Saver II controller board are selectable with hard wire jumpers or switches. Eight available frequency options include:

19.2K baud
9600
4800
2400
1200
600
150
110

The jumpers consist of two parallel rows of pads located on chip position L12. Jumpers for serial channel #1 are on the left (towards column K) and on the right (near column M) for serial channel #2. A shorting jumper wire is inserted horizontally on the board for the desired baud rate. The frequency options are etched on the circuit board. Nearest the card handle is 110 baud, and 19.2K baud is nearest chip row 11.

Device Code Selection (Serial Channel #2)

The device code for the first serial channel is usually set at 10/11. Unless otherwise specified, the second channel comes wired as 50/51. For special applications, other device codes may be used for the second serial channel. The device code is determined by five hard wire jumpers J302 through J306. The table provides a guide to selecting non-standard device codes.

Device Code Selection Table

CRTII	J302 (DS0)	J303 (DS1)	J304 (DS2)		J305 (DS3)	J306 (DS4)
0X	IN	IN	IN	X0+1	IN	IN
1X	IN	IN	OUT	X2+3	IN	OUT
2X	IN	OUT	IN	X4+5	OUT	IN
3X	IN	OUT	OUT	X6+7	OUT	OUT
4X	OUT	IN	IN			
5X	OUT	IN	OUT			
6X	OUT	OUT	IN			
7X	OUT	OUT	OUT			

Jumper OUT = 1 bit; Jumper IN = 0 bit. Reference the Slot Saver II assembly drawing for the location of these jumpers.

RS232C/Current Loop Jumpering

Each Console Serial Port may be selected for either RS-232C(EIA) or current loop input/output by jumper changes. (Reference jumper option sheet).

Serial Console Port 1

RS-232C	Current Loop
J204 In	J204 Out
J205 Out	J205 In
J210 Out	J210 In

Serial Console Port 2

RS-232C	Current Loop
J310 In	J310 Out
J311 Out	J311 In
J312 Out	J312 In

5.3 Programmers Reference Information

The Console Serial Device controller is set up to handle full duplex communications with Model ASR-33, KSR-33 or KSR-35 teletypes at a speed of 10 characters per second or a CRT at speeds up to 19.2K baud. Each serial device controller has separate input and output functions and is really two distinct devices. Each has its own device code, BUSY, DONE and INTERRUPT DISABLE flags.

Output To The Terminal

Output from the computer to the console terminal requires only one I/O instruction. The device code is 11 and the interrupt priority mask bit is 15. A character is transferred to the display terminal with a Data Out A instruction. The ASCII character code is placed in bits 8-15 of the selected accumulator. The START function is used to set BUSY which in turn causes the contents of the controller output buffer to be serially shifted out to the terminal. The terminal displays or prints the character or performs the indicated control function. In the case of a teletype terminal, if the punch is on, the character is also punched on the tape with accumulator bit 15 corresponding to channel 1 (a 1 in the accumulator produces a hole in the tape). Completion of transmission clears BUSY, sets DONE and requests an interrupt if the INTERRUPT DISABLE flag is clear.

Input From The Terminal

Input to the computer from the terminal also uses only one I/O instruction. The device code is 10 and the interrupt priority mask bit is 14. The logic of the input controller is slightly different than other input controllers in that striking a key on the keyboard will cause the code from the terminal to be serially shifted into the controller input buffer. This will occur irrespective of whether the program has previously set the BUSY flag or not.

Under normal operation, the BUSY flag is set with a NIOS instruction prior to when data is expected to be received from the terminal. In the case of a teletype, if a paper tape is loaded in the reader, the START function causes the next character to be read. The DONE flag is set, BUSY cleared and an interrupt generated (unless the DISABLE flag is set) when the character has been serially shifted into the teletype controller buffer. The eight bits which comprise the

character are brought into the accumulator with a Data In A instruction. Tape channel 1 on a teletype reader corresponds to AC bit 15.

5.4 Theory of Operation: Serial Devices

The first serial interface controller is generally the system console device (device codes 10 and 11) and is either a CRT terminal or teletype. The second serial interface device controller is generally set up as device codes 50 and 51 and becomes the second input terminal although it can be jumpered to any other desired device code.

The following description of the operation of serial input and output channels is written as for a teletype although the description applies equally well to a CRT terminal.

Much of the logic of the serial input and output interface is provided by a UART (Universal Asynchronous Receiver Transmitter L10). The bit timing for these controllers is derived from a 307.2KHz clock which is located on the common peripheral section of the board. The UART requires a clocking signal which is 16 times the actual communication bit rate (L10-17). The 307.2KHz clock is successively divided by two in the counters F11 and G11 through eight stages of division for a total of 256, and all intermediate frequencies are brought out to jumper points. The 1200 baud frequency is then further divided by a factor of 11 in counter J12 to give a baud rate slightly greater than 109. The error in this baud rate from the desired baud rate of 110 extends only over the span of one character time and does not result in data errors.

Console Input Controller

The Console Terminal controller uses many of the same signals as the terminal output controller. The console input and output controllers are independent to the extent that they both have separate BUSY and DONE logic and device codes and hence, from the standpoint of the computer, act as two totally independent peripheral devices.

A data input cycle begins with the execution of a NIOS instruction. As always, this sets the BUSY flip flop. No further action occurs until a character is sent by the teletype. Data enters the input controller as a serial bit stream at the selected baud rate.

The serial data stream from the terminal enters through external pin B69. The voltage at this point is normally -5 volts if the cable is connected and the power turned on. When the start bit of a character is received, the voltage at B69 goes to a high value. The Schmidt trigger N12-6 turns on, and gate N12-11 goes to ground. It should be noted that an inverse situation actually exists at B69 with respect to the voltages for space and marking bits. When L10-20 drops to ground, the received data clock (L10-17) is continuously running at 16 times the selected baud rate and will, upon the next positive going transition, begin to clock the character into the serial data register within the UART. When all data and parity bits have been received, L10-19 goes high and sets TTI DONE (1) high (L5-5) and clears TTI BUSY (1) (L4-5). If interrupts have been enabled in the processor, the next positive transition of REQUEST ENABLE (L3-3) will cause a program interrupt to be generated.

The received character can then be read into an accumulator of the processor by executing a Data In A instruction. The appropriate output pins (5-12) of the UART are high if the corresponding bit in the received character was a binary one.

Console Output Controller

Output of data from a Data General computer and a console terminal device is asynchronous on a character-by-character basis. Each character is sent as a serial bit stream at the selected baud rate. Each 8-bit character is preceded by a marking bit and followed by two space bits. This results in a character data transfer rate of the selected baud rate divided by 11.

The process of sending out a character begins by sending out a Data Out A START command. The ASCII code equivalent of the desired character must have been previously placed in bit 8-15 of the selected accumulator. When a DOAS instruction is executed, pulses appear on both the DOA and START lines. The DOA pulse precedes the START pulse by a few hundred nanoseconds and the two signals do not overlap. Since the START signal sets the BUSY flip flop, the DOA operation will have been completed before BUSY is set.

The Data Out A pulse causes a negative going pulse on the output register load line (L10-23) of the UART. The character being sent is loaded in parallel through pins 26-33 of the UART. Clocking of the output process (L10-40) requires that the CLEAR TO SEND signal (A90) is high. For teletype and most CRT connections, this signal is tied to five volts through a 3K resistor and is not used by the terminal.

The serial data stream leaves the UART on pin 25. For a teletype, the 20 mil current loop is provided through external pins A85 and A83. For an RS-232 type interface, jumper J204 is used in place of J205, and the discrete circuitry is used to provide a ± 5 volt swing to the output signal.

When the START bit, 7-bit character, parity and two stop bits have been shifted from the UART, pin 24 goes high and sets TTO DONE which also clears TTO BUSY. As with the teletype input channel, a program interrupt will be generated if interrupts have been enabled in the processor.

5.5 Schematic Drawings

Logic for the two serial peripheral devices are included on ZETACO's drawing 700-210-00.

5.6 How To Check Out A Teletype (Or CRT)

Improper functioning of the console serial device can be caused either by a malfunction in the device itself, the serial device controller located in the computer or by faulty software (including a malfunctioning CPU or memory). Of these, the more likely is a problem in either the serial device or the controller board. Resolving this situation then is a matter of isolating the area of the problem.

Local Mode Testing

The first step to be taken is to place the terminal in the local (off-line) mode. In local, the keys which are struck will appear on the screen (or be printed in the case of a teletype) if the terminal is in the half duplex mode.

If a teletype is being used, the punch can be turned on and a short leader generated by holding down the HERE IS key for a few seconds and then typing a short message on the keyboard (e.g., The quick brown fox. . .). The message should be followed by a carriage return and line feed. When the message has been completed, generate a short trailer with the HERE IS key. The punched tape can then be looped into the paper tape reader without tearing it from the paper tape punch. (The reader switch should be in the STOP or FREE position at this time.) When the tape is secured, place the reader switch in the START position. The message which has been typed will be repeatedly printed and punched. Let this tape run for several minutes and then review the printout for errors. If no errors are observed, the terminal should then be placed on line to the computer.

On-Line Testing

Detailed tests to be run in conjunction with the computer are outlined in two writeups entitled:

1. Diagnostic Programs: Serial Device Input
2. Diagnostic Programs: Serial Device Output

These tests require that the processor be stopped and that several short test programs be loaded into memory through the console data switches. These programs use a proven set of instructions (if entered properly) and, if all tests run properly, may indicate that the problem is in the customer's applications software. These programs check teletype and controller operation under interrupts as well as BUSY and DONE logic. If the programs do not run satisfactorily, check to see if the board is wired for device codes 10 and 11 (see notes below).

On-Line Checkout

A few short diagnostic routines entered through the data switches of the computer console will establish within minutes whether the controller, cables and CRT have been properly connected and are functioning correctly. These programs should be run prior to proceeding to ZETACO's Serial Device Diagnostic.

Test A: Program To Repeatedly Output A Single Character Using BUSY/DONE Logic

The octal program listed below is entered through the console data switches starting at location 100. The starting address (100) is set in the switches and then the EXAMINE switch is hit to load this address. The console switches can then be reset to the ASCII value of the character to be printed (e.g., octal 100 = @, octal 101 = A, etc.) The program is started by pressing the CONTINUE switch.

The program reads the selected character from the computer data switches, sends out the character to the teletype or CRT and then waits in a SKIP BUSY (or DONE) loop for the serial shifting of the character to the terminal to be completed. The process requires no response from the terminal and will repeatedly send out the same character. If the terminal does not have an automatic line feed, it will be necessary to take the terminal off line to advance the line. If proper transmission is occurring, the console switches can be changed on the fly to change the character sent out.

Memory Location	Octal Program	Symbolic Code	Comments
100	062677	IORST	
101	060477	READS 0,CPU	Reads console switches
102	061111	DOAS 0,TTO	Send out character
103	063511	SKPBZ TTO	
104	000777	JMP .-1	Wait for completion
105	773	JMP .-5	Repeat

To run under DONE logic, change the instruction in location 103 to 063611.

If no output occurs, a problem exists with one of the following:

1. The cable has been improperly installed. Carefully check installation.
2. Terminal not on line.
3. Wrong baud rate selected.
4. A problem exists with the controller. Check that controller and cable are plugged to the same slot.

Test B: Device Output Under Interrupt Control

Memory Location	Octal Program	Symbolic Code	Comments
1	70	JMP Location 70	
60	062677	IORST	
	060177	INTEN	Enables interrupts
	072077	MSKO 2,CPU	Mask instruction
	061111	DOAS 0,TTO	Output a character
	400	JMP *	Wait for interrupt
70	065477	INTA 1,CPU	Device code AC1
	063077	HALT	

The program is started at location 60, and the interrupt processing routine is placed at location 70. Before starting the program, the operator must first place a mask word (all zeros for normal operation or 000001 for teletype output disable) in accumulator 2. The character to be printed must also be placed in AC0.

The program sends out one character and then waits for an interrupt. When the interrupt occurs, the program passes through location 1 to get to the interrupt routine at location 70. The INTA instruction places the device code of the interrupting device (device 11 in this case) in AC1 and then halts. By changing the halt to JMP 60 or JMP *-8 (770), the program will run continuously.

If bit 15 in the mask word is equal to one, the TELETYPE OUTPUT flag is disabled and the program will hang on the JMP * instruction at location 64. If bit 15 is unequal to one, the program will run normally.

Test C: Read One Character Under Either BUSY or DONE Logic

Memory Location	Octal Program	Symbolic Code	Comments
110	062677	IORST	
	060110	NIOS	Enable CRT Interface Controller
	063510	SKPBZ	Wait for character to be struck on keyboard
	777	JMP *-1	
	060410	DIA 0,TTI	Read character AC0
	063077	HALT	Halt, display AC0
	773	JMP *-5	

The program enables the controller and then waits for a key to be struck on the keyboard. The ASCII code for the character is placed in the accumulator zero (e.g., A = 101). By hitting the CONTINUE switch, the next character on the tape is read. By changing the third instruction to 063610 SKPDN, you may run under DONE logic.

Test D: Read One Character Using INTERRUPT Logic

The program is started at location 60, and location 70 contains the interrupt processing routine. Before starting the program, the operator must first place a mask word (all zeros for normal operation or 000002 for teletype input disable) in accumulator 2. After the program is started at location 40, the operator should strike a key on the keyboard.

Memory Location	Octal Program	Symbolic Code	Comments
1	50	JMP Location 50	
40	062677	IORST	
	060177	INTEN	Enable interrupts
	072077	MSKO 2,CPU	Mask instruction
	060110	NIOS TTI	Start paper tape reader
	400	JMP *	Wait for interrupt
50	065477	INTA 1,CPU	Device code AC1
	060410	DIA 0,TTI	Character AC0
	063077	HALT	
	060210	NIOC TTI	Clear interrupt and continue
	41	JMP Location 41	

The character read and the device code are placed in accumulators 0 and 1, respectively. If mask bit 14 = 1, the reader will advance tape to the next character and load the controller registers, but it will not generate an interrupt. The program will hang on the JMP * instruction at location 64.

5.7 Diagnostic Description: Serial Device Exerciser Program

The Serial Device Exerciser program (ZETACO's tape #702-010-00) is a diagnostic program which will check a single or multiple serial port device in both an input and output mode. The user can select and change both the type of logic (BUSY, DONE and INTERRUPT) and the terminal device code addresses as the program operates.

Operating Instructions

A listing is not included for the program since the instructions listed below are adequate for the program operation.

The program is loaded via a paper tape reader using the binary loader. The starting address of the diagnostic is 2_8 (switch 14 only up). To activate the program, strike any key on the desired terminal. The program will then print appropriate statements, and the user may then select the desired tests (B = BUSY, D = DONE, I = INTERRUPT). Each of the three tests provides a direct echo back from the keyboard for testing of all keys.

Certain additional control codes are available for function changing or testing. They are as follows:

CTRL-C When struck during any of the selected tests, allows for changing to other tests.

CTRL-A When struck during any of the selected tests, allows for changing to a different terminal by striking any key on the desired terminal.

CTRL-X When struck during the interrupt test, will automatically test the mask logic. When struck, the program will immediately ring the bell. The keyboard should then be disabled for approximately 5 seconds, after which time the bell will ring again and the echo will be activated.

SS II CONNECTOR PANEL

SER 25S	FUNCTION	PORT 1 BP	PORT 1 AMP	PORT 2 BP	PORT 2 AMP	COLOR
2	TRANSMITTED DATA	A85	1-13	B13	SGL	GRAY
12	(+) CURRENT SOURCE	A83	1-11	A77	SGL	ORANGE
3	RECEIVED DATA	B69	1-31	B11	SGL	WHITE
13	RECEIVED (-)	A6	SGL	A6	SGL	BLUE
5	CLEAR TO SEND	A90	1-18	B67	SGL	PURPLE
7	GROUND	A99	1-27	B1	SGL	BLACK
	KEYWAY		1-29			

MUX 25S	FUNCTION	LINE 0 BP	LINE 0 AMP	LINE 1 BP	LINE 1 AMP	LINE 2 BP	LINE 2 AMP	LINE 3 BP	LINE 3 AMP	COLOR
2	TRANSMITTED DATA	A79	1-7	A86	1-14	A78	1-6	A89	1-17	BROWN
7	GROUND	A1	SGL	A1	SGL	A2	SGL	A2	SGL	BLACK
3	RECEIVED DATA	A87	1-15	A88	1-16	A81	1-9	A92	1-20	YELLOW
5	CTS	A75	1-3	A84	1-12	A76	1-4	A73	1-1	BLUE

NOTE:

The terms "Received Data" and "Transmitted Data" are assigned in accordance with the EIA standard RS-232-C.

When operating in a non-modem environment, it will be necessary to adjust these two lines to meet your configuration.

Definition to this product:

Received Data - Data going into the multiplexer.
Transmitted Data - Data coming out of the multiplexer.

This information applies directly to the connector panel manufactured by ZETACO, Inc. If this item has not been purchased, then refer only to the "FUNCTION" and "BP" columns for your cable connection.

6.0 Model 225 Real Time Clock

6.1 General Description

The Real Time Clock controller provides a series of timing pulses which are independent of the minicomputer processor timing. The clock option consists of four frequencies (10, 60, 100, 1000Hz) which are selectable under program control and can provide program timing and scheduling interrupts at the pre-selected rate. The 60 cycle frequency is derived from the line frequency which operates the computer. The other three frequencies are derived from a crystal controlled oscillator.

6.2 Installation

The Slot Saver II controller board is generally installed in board slot 3 of a Nova 1200 or Nova 2 computer or slot 4 of a Nova 3 or Eclipse. The Real Time Clock controller picks up a clipped 60Hz signal from pin B6 of the general I/O slot designated for the minicomputer. If the Slot Saver II is inserted in a different slot, then a jumper wire must be placed on the end plane from pin B6 on the general I/O slot (#3 or #4) to pin B6 on the slot containing this controller.

6.3 Programmers Reference Information

The controller for the Real Time Clock options uses the standard clock instruction set as outlined in the Nova Programmers Reference Manual. The Real Time Clock option consists of four frequencies (10, 60, 100, 1000Hz) which are selectable under program control.

One I/O instruction is required to set the clock frequency. BUSY and DONE are controlled or sensed by bits 8 and 9 in all I/O instructions. The device code is 14 and the interrupt priority mask bit is 13.

The clock frequency to be used is selected with a DATA OUT A instruction to the Real Time Clock. The referenced accumulator will contain the desired frequency in bits 14 and 15 as follows:

AC Bits 14-15	Frequency
00	AC Line Frequency
01	10Hz
10	100Hz
11	1000Hz

As with all other peripheral controllers, the BUSY flip flop is set by the START signal (NIOS instruction). The next pulse from the selected clock will then set DONE, requesting an interrupt if INTERRUPT DISABLE is clear. A DOA instruction to select the frequency need be given only once; following each interrupt a NIOS sets up the clock for the next pulse.

When BUSY is first set, the first interrupt can come up at any time up to the clock period. But, once one interrupt has occurred, further interrupts are at the clock frequency selected, provided the program always sets BUSY before the next period expires.

The Real Time Clock option is used for low resolution timing compared to processor speed, but it has high long-term accuracy. Power turn on or the RESET function generated by either the program or the minicomputer console will reset the clock to line frequency. Following power turn on, the line frequency pulses are available immediately, but up to five seconds may elapse before a steady pulse train is available from the crystal for other frequencies.

6.4 Theory of Operation: Real Time Clock Logic

The logic in this section of the Slot Saver II controller board is designed to provide program or event timing at any one of four frequencies which are selected by program control. The frequencies provided by the clock controller are 10, 60, 100 and 1000Hz. The 60Hz signal is obtained from the line voltage which operates the Data General Nova computer. The frequencies of 10, 100 and 1000Hz are obtained by counting down a 1536KHz crystal oscillator.

The clock controller is easily understood by examining the logic diagram for the drawing 700-210-00. Both the crystal oscillator and associated counting circuitry as well as the 60Hz circuitry are free running and operate independent of the computer instruction timing. The oscillator runs at 1536.000KHz with an accuracy of 0.05%. This signal is then divided by 16, 16 and 6 to produce a frequency of 1KHz. This frequency is further divided twice by 10 to give frequencies at 100 and 10Hz.

The 60 cycle signal is generated within the Nova power supply and is carried on the back plane to pin B6 of slot 3 (slot 4 of Nova 3 or Eclipse). Note that if this board if plugged into other than the designated I/O slot, the 60 cycle signal will not be present and must be jumpered on the computer end plane. This signal has a period of 16.7 milliseconds and varies between 4.5 and 5.0 volts. The two transistor circuits convert this to an 0-4.5 volt signal which drives an integrated circuit.

All four frequencies continuously appear on gate E3. The program can select which one of the four frequencies is used to provide elapsed time information. It should be noted that only one of the four frequencies can be selected at any one time. Frequency selection is accomplished by executing a Data Out A instruction to the Real Time Clock as follows:

Bit 14	Bit 15	Selected Frequency
0	0	60Hz
0	1	10Hz
1	0	100Hz
1	1	1000Hz

The Real Time Clock controller will operate under BUSY, DONE or INTERRUPT logic. Once the desired frequency has been selected, operation begins with a NIOS instruction which sets the BUSY flip flop. On a positive transition of the selected clock signal BUSY is reset, DONE is set and the INTERRUPT REQUEST flip flop set. A NIOC instruction will clear DONE and INTERRUPT REQUEST or a NIOS can be used if another clock period is required.

Since the clock frequencies are not slaved to the computer, the timing on the very first clock cycle can occur anywhere between 1 microsecond and the selected clock period. All succeeding clock interrupts will, of course, occur spaced in time by the selected clock period.

Checkout of the interface consists primarily of monitoring the various clock frequencies with an oscilloscope at gates E3-13, E3-12, E3-11 and E3-10. Selection of the four frequencies with the Data Out A instruction can be verified at E3-9. Proper operation of the BUSY, DONE and INTERRUPT logic can be verified using a scope using the diagnostics listed below. Accuracy of the clock can be verified with a sweep second hand on a watch using the clock timing diagnostic.

6.5 Schematic Drawing

The logic for the Real Time Clock controller is included on ZETACO's drawing 700-210-00. As a prerequisite, this logic must be used in conjunction with the Common Peripheral option (drawing 700-210-00).

6.6 Checkout of Real Time Clock Option

Following installation of the Slot Saver II controller into the general I/O slot of the computer, the machine should be powered up. Proper functioning of the Real Time Clock controller can be determined within a few minutes by entering a few octal diagnostic routines through the computer console data switches. These routines should be checked using all selectable frequencies before proceeding to ZETACO's RTC(Real Time Clock)Timing Diagnostic program.

The Real Time Clock has four operating frequencies; namely, 60, 10, 100 and 1000Hz, which are selectable under program control. The diagnostic programs should be run for all frequencies to verify proper operation.

Bit 14	Bit 15	Selected Frequency
0	0	60Hz
0	1	10Hz
1	0	100Hz
1	1	1000Hz

Test A: Program to Test BUSY/DONE Logic

The octal program is entered through the console data switches starting at location 100. The starting address is also 100. Before beginning the program, the operator must first place the code for the selected clock frequency in accumulator 0. The program will then start the clock. If the clock is operating properly, the BUSY flip flop will be reset and the program will halt at location 105. Accumulator 0 can then be changed to a different frequency selection. Operation using DONE logic can be determined by changing the SKIP instruction to SKPDN (063614).

Memory Location	Octal Programs	Symbolic Code	Comments
100	062677	IORST	
	061014	DOA 0,RTC	Select frequency from AC0
	060114	NIOS RTC	Start clock
	063514	SKPBZ	
	777	JMP *-1	Wait for clock response
	063077	HALT	
	772	JMP *-6	Repeat if desired

Test B: Clock Operation Under Interrupts

Memory Location	Octal Programs	Symbolic Code	Comments
1	70	JMP 70	
60	062677	IORST	
	061014	DOA 0,RTC	Select frequency
	072077	MSKO 2,CPU	Mask instruction
	060177	INTEN	Enable interrupts
	060114	NIOS RTC	Start clock
	400	JMP *	Wait for interrupts
70	065477	INTA 1,CPU	Device code AC1
	603077	HALT	
	60	JMP 60	

The program is started at location 60 and location 70 contains the interrupt processing routine. Before starting the program, the operator must first place a mask word (all zeros for normal operation or 000004 for clock disable) in accumulator 2.

After receiving the interrupt, the device code is placed in accumulator 1. If mask bit 13 = 1, the reader will not generate an interrupt. The program will hang on the JMP * instruction at location 65.

6.7 Real Time Clock Timing Diagnostic

When the controller has successfully executed Tests A and B, you are now ready to check the accuracy of the various clock frequencies. ZETACO's diagnostic #900-014-00 is supplied for this purpose. This program permits the checking of the accuracy of each of the four clock frequencies against the sweep second hand of the operator's watch. A listing and separate binary tape are included with this documentation.

The paper tape containing the diagnostic must first be loaded into the memory of the computer through a Paper Tape Reader or Teletype Reader. The clock frequency is selected by the operator through the selection of one of four program starting addresses (10, 11, 12, 13).

The diagnostic starts the clock operating at the selected frequency and then counts interrupts. Every five seconds the bell on the system console (CRT or teletype) is rung. At the same time, the CARRY bit on the processor changes state. By comparison of the bell (or carry light) to a sweep second hand on your watch, the accuracy of the Real Time Clock controller can be verified.

A computer listing of the clock diagnostic is contained on the following page.

7.0 Line Printer Controller

7.1 General

ZETACO's printer controller permits use of most popular brands of line printer containing a parallel type interface with a Data General Nova or Eclipse or Nova-emulating minicomputer. The controller is a programmed I/O (character-by-character) transfer device and is software compatible with the Data General operating systems and printer instruction set. When ordering a line printer, a standard Centronics or Data Products interface should be specified. Brands of printers available with these types of interface cards are Centronics, Data Products, Printronix and Control Data.

For line printers which have a serial RS-232C rather than a parallel interface, the printer should be connected to the second serial channel on the Slot Saver II board rather than to the parallel printer controller. Accomplishing this requires that the following changes be made on the board:

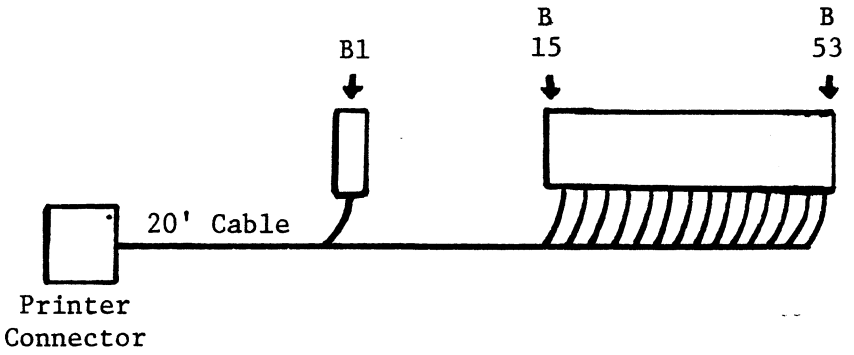
1. Change the device code on the second serial channel to 17 and the mask bit to 12.
2. Disable the parallel printer interface (connect jumper on K1-1) so two controllers do not respond to the same device code.

7.2 Line Printer Cabling

External connections for a line printer controller are located between pins B15 and B54 on the computer back plane. A separate ground pin on B1 is also required. The cable assembly on the computer end contains a 20/40 pin AMP connector which is slid over the appropriate pins on the computer end plane (see sketch). This connection should be made with AC power off to the computer. The cable should be plugged on the B connector corresponding to the card slot containing the Slot Saver controller.

NOTE: The mounting of the AMP connector should be double checked since circuitry in both the computer and printer will be destroyed if the cable is improperly plugged.

Single piece cable assemblies are stress relieved at the rear of the computer with a ty wrap. The other end of the cable mounts directly to the interface connector on the line printer. Two piece cable assemblies have a cannon connector which is mounted at the rear of the Nova. Special mounting hardware is included with the cable assembly.



7.3 Programmers Reference Information

Data transfer between a Nova or Eclipse minicomputer and the printer is performed on a character-by-character basis. Programmed output to the controller is generated by a Data Out A and a START command. Bits 8-15 of the selected accumulator contain the ASCII code of the character to be transfered.

The interface board can be wired to operate with any of 62 possible peripheral device select codes. To ensure software compatibility, the board is jumpered to device 17 unless otherwise specified. For a system which includes two line printers, device code 57 is used for the second printer. The standard mask bit for a line printer is bit 12.

The start (bit 9 of the instruction word) must be set on each Data Out instruction. This pulse is used to set the BUSY flag to the "1" state. Upon completion of the transfer or at the end of the printing or function operation, the DONE flag is set and BUSY goes to the zero state. Program control of the interface can use any of the standard Data General I/O instructions:

SKPBN	Skip if BUSY flag is 1
SKPBZ	Skip if BUSY flag is 0
SKPDN	Skip if DONE flag is 1
SKPDZ	Skip if DONE flag is 0

When transfer of each character is complete and if the INTERRUPT logic for the computer has been enabled, the interface will command a standard program interrupt. An INTA (interrupt acknowledge) instruction places the device code of the interrupting device into the selected accumulator. If the device does not need further service at this time, a NIOC instruction to the device clears the DONE flag and prevents further interrupts. If, on the other hand, another character is to be transferred immediately, the CLEAR instruction is not required as a DOAS instruction clears DONE, sets BUSY and transfers the new character. Disabling the interrupt capability for this device can be controlled by a mask instruction with the printer mask bit 12 selected.

Data is transferred to the printer with DOAS instructions at a rate of up to one character every 1.5 microseconds. Status of the printer is read into the computer using a Data In A (DIA) instruction. Bit 15 is a binary one when the printer is ready, on line and has paper.

Command Codes

Several special command codes are decoded by the printer controller logic. The way these codes are handled differs depending on whether the line printer to be used contains a Centronics or Data Products interface. These differences are indicated below.

Line Feed (Code 012)

For a Data Products type interface, the line feed code is strobed directly over to the printer. This causes the printer to go into the print mode and the paper to advance one line.

For a Centronics interface, the line feed code (012) is converted by the controller to a carriage return character (015) which causes the print cycle and line advance by the printer. If there are no characters in the printer buffer, this character is ignored by the Centronics printer. Note that although a CR,LF character sequence in the software is converted to a CR,CR sequence, only one print cycle and line advance occurs.

Vertical Tab (Code 013)

Some Centronics printers have a two channel vertical format unit (channels 5 and 7). Channel 7 is used for top of form and is used in conjunction with a form feed code. Channel 5 is used with the VTAB code to accomplish special line spacing while printing.

For a Data Products printer with a 12 channel tape-controlled VFU, a two character sequence is used which consists of a VTAB code (013) followed by the channel select character. Upon receipt of the VTAB command, the controller inhibits the strobe line to the printer, sets the DONE flip flop and waits for the next character. The character following a VTAB will be the paper feed code. The lower five bits of the character determine the paper advance. The VFU option will provide the capability of controlling forms advance in either a tape or line count mode. The VFU operates at either six or eight lines per inch. Special tape preparation methods are not required for eight LPI.

Table 1 shows the forms advance when the paper tape reader is used to control duration of slew (bit 5 false). Table 2 shows the forms advance when the data code is used to control duration of the slew (bit 5 true).

Table 1

Selected Tape Channel	Character Following VTAB						
	7	6	5	4	3	2	1
0	x	x	0	0	0	0	0
1	x	x	0	0	0	0	1
2	x	x	0	0	0	1	0
3	x	x	0	0	0	1	1
4	x	x	0	0	1	0	0
5	x	x	0	0	1	0	1
6	x	x	0	0	1	1	0
7	x	x	0	0	1	1	1
8	x	x	0	1	0	0	0
9	x	x	0	1	0	0	1
10	x	x	0	1	0	1	0
11	x	x	0	1	0	1	1

Table 2

Number Lines Slewed	Character Following VTAB 7	6	5	4	3	2	1
0	x	x	1	0	0	0	0
1	x	x	1	0	0	0	1
2	x	x	1	0	0	1	0
3	x	x	1	0	0	1	1
4	x	x	1	0	1	0	0
5	x	x	1	0	1	0	1
6	x	x	1	0	1	1	0
7	x	x	1	0	1	1	1
8	x	x	1	1	0	0	0
9	x	x	1	1	0	0	1
10	x	x	1	1	0	1	0
11	x	x	1	1	0	1	0
12	x	x	1	1	1	0	0
13	x	x	1	1	1	0	1
14	x	x	1	1	1	1	0
15	x	x	1	1	1	1	1

x = don't care

Form Feed (Code 014)

This code is strobed over to the printer and causes the paper to advance to the top of form.

Carriage Return (Code 015)

For a Data Products interface the carriage return character is strobed over to the printer and causes it to go into the print mode and results in no forms advance.

For a Centronics interface the carriage return code is strobed over to the printer and causes it to go into the print mode, the carriage to return and the paper to advance one line. If a carriage return and line feed or two line feeds or two carriage returns are sent to the printer, the printer will perform one print, one carriage return and one line advance. If there are no characters in the printer buffer, this code will be ignored by the printer.

7.4 Theory of Operation: Parallel Line Printer Controller

This section provides a description of the logic of the parallel line printer controller and is intended as a supplement to the schematic diagram. This controller has been designed for compatibility with the printer software and operating systems currently offered by Data General.

The logic of this controller can be looked upon as in two parts; the Printer Common logic and the Printer Interface logic. As the names imply, the Printer Common logic contains the basic data buffering, timing and circuits which interface with the minicomputer bus structure and are common to all printer controllers. The Printer Interface logic contains the circuitry which interfaces with the cable to the printer and contains logic to accommodate special features of a Data Products or Centronics line printer.

Description of Printer Common Logic

The Printer Common logic is contained on the left half of the printer schematic.

The Device Select logic provides a means of decoding those control and data signals which are meant for the printer controller. The device selection gate K1-6 is normally jumpered for device code 17. If a second line printer is used in the system, the jumper on K1-1 can be changed to set the parallel printer controller to device code 57.

The Interrupt Priority logic (located on the Common Peripheral drawing) is a means of maintaining continuity of the interrupt and data channel priority lines between this controller board and the boards placed in the computer above the printer board. If the printer is not requesting an interrupt, pin G3-13 will also be at ground, thereby passing the interrupt priority along to the next lower device. If, on the other hand, the printer controller is requesting interrupt recognition by the processor, then G3-13 is high and G3-11 will be high.

The status device code (gate H3) is used when the controller is run under interrupt control. When the processor recognizes an interrupt, the software must execute an INTA (interrupt acknowledge) instruction. This instruction causes the device code for the interrupting device (17, in this case) to be placed on the

data bus. As with the Device Select logic, these gates are normally wired for device 17 but automatically compensate for a device code 57.

The BUSY/DONE/INTERRUPT logic is a standard set of circuits used in all controllers on the Slot Saver board. The BUSY flip flop in the controller is set when the computer executes a START instruction with the printer device code (e.g., DOAS 1,LPT). The controller remains BUSY until a response is received at a later time from the printer. This response (LPT COMPLETE) resets BUSY, sets DONE and will cause an interrupt if the processor's INTERRUPT flag has been enabled. Interrupts may be disabled if the printer INTERRUPT flag has been enabled. Interrupts may be disabled on the printer controller through the use of a Mask Out instruction with bit 12 set equal to one.

Character Transfer and Buffering

Characters are actually sent from the computer to the printer controller with a Data Out A instruction. The START bit must be included with this instruction to set the BUSY flip flop. The signal $\overline{\text{LPT DOA}}$ (K4-3) initiates a series of our timing pulses used throughout the controller logic. The 8-bit ASCII character from the accumulator selected in the DOAS instruction is loaded into registers J10 and J11. Gate H12 decodes the characters as they are received and are set up to look for the printer control character line feed.

The timing on the one shots F4, G4 and G5 is described below. The register CLEAR signal sets the character storage registers to zero before each new character. The clock pulse signal then loads the new character into the registers and simultaneously starts the strobe delay circuit G4-7. This delay is used to allow the data to settle prior to initiating a load (strobe) pulse to the line printer. At the completion of the strobe delay pulse, the strobe signal G5-1 is generated.

Two types of capacitors are used on the board to provide filtering between power and ground (6.8 microfarad tantalum capacitors for power supply noise and .05 microfarad capacitors for high speed decoupling).

Printer Interface Logic

The right half of the schematic contains the logic which drives the lines to the printer and accommodates special characteristics of the different brands of line printer.

The chips J6 and J7 drive the eight data lines. The character data from the buffer registers J10 and J11 are presented to the driver chips as DB1 through DB8. These signals are high for a binary one condition. The jumper near J6-6 is not used in the case of a Data Products type interface which requires a high on the data lines as a true condition. When this jumper is in place, the data signals on the cable are ground true.

Gates J5-9, H12 and J9 are used to detect a line feed code (012) and convert it to a carriage return code (015). This code conversion is used for a standard Centronics printer. The jumper on J5-10 is used to disable this feature.

The BUSY signal from the line printer K5-9 is high when the printer is ready, has paper and has been placed on line. The demand or acknowledge line K4-12 from the printer corresponds to a character request line. This cycles low as each character is received and processed and goes high when the printer is ready for the next character. This causes LPT complete to go high which clocks the DONE flip flop, resets the BUSY flip flop (J5-5) and causes an interrupt to the computer.

The logic in the upper right hand corner of the schematic is used for a Data Products printer with a vertical format unit. A vertical tab character is decoded by gate K7-8. This character is trapped by the controller and is not sent over to the printer. A means of setting the DONE flip flop is artificially provided by the one shot H6.

The next character sent out from the computer is assumed by the controller to be the channel select command. This triggers a sequence of events which starts with the setting of flip flop G8-5. At the same time, the INHIBIT flip flop H8-9 is cleared by the rising $\overline{\text{VTAB}}$ signal. The VFU line J8-5 (B36) to the printer rises simultaneously with the channel character on the data lines. The print and paper feed cycle is thus completed.

Upon receipt of the next character from the computer (which may be the first character of the next line), flip flop G8-9 is set. Approximately 75 nanoseconds later, a RESET pulse appears at G6-11 which presets the logic to its pre-VFU state.

7.5 Schematic Reference

Logic for the line printer controller is contained on ZETACO's drawing #710-L06-JJ1-00.

Several different designs of cables may be used with this controller. The drawing for the one piece cable assembly is #122-C02-M1-00.

7.6 Checkout Of A Line Printer And Controller

The majority of the causes of not being able to print data from a computer lie with the printer itself. The first things to check when first hooking up a printer are the obvious; such as,

1. Is the printer powered?
2. Has the printer been placed on line?
3. Is there paper in the unit?
4. Is the cable from the computer plugged in tightly?
5. Is the front gate closed?

If these conditions are satisfied, the next step is to exercise the printer by itself. Many models of line printer can be ordered with the self-test option. If this option is not available, an external exerciser test box may be available from your serviceman. If no printing occurs using the self-test option, a malfunction exists within the printer. Please note which lights work, whether the motor comes on and any other symptoms before calling for service. If, on the other hand, the printer operates satisfactorily with the self-test feature, then you should proceed to the next step of the checkout process.

Initial Checkout of Computer Controller

Following installation of the controller board and cable (see installation instructions), the next step in the checkout process is to power up the computer with the cable to the printer disconnected at the printer end. If no adverse effects are noted, the computer should be turned off and the cable connected to the printer. The computer can then be turned on again and power applied to the printer.

A few short diagnostic routines entered through the data switches of the computer console will establish within minutes whether the controller, cable and printer have been properly connected and are functioning correctly. These programs should be used to verify proper operation before proceeding to ZETACO's Comprehensive Printer Diagnostic program.

Test A: Program To Repeatedly Print A Single Character Using BUSY/DONE Logic

The octal program is entered through the console data switches starting at location 100 through location 110. The starting address (100) is set in the switches and then the EXAMINE switch is hit to load this address. The console switches can then be reset to the ASCII value of the character to be printed (e.g., octal 100 = @, octal 101 = A, etc.) The program should be started by pressing the CONTINUE switch.

The program reads the data switches, sends out the character to the printer and then waits in a SKIP BUSY (or DONE) loop for the printer to request the next character. When the printer acknowledges, a line feed character is sent, thereby initiating a print cycle and advancing the paper. The selected letter will be printed in the first column of the paper. If proper printing is occurring, the console switches can be changed on the fly to change the character printed.

Note that a line feed code octal 012 must be loaded into accumulator 1 before the program is started.

Memory Location	Octal Program	Symbolic Code		Comments
100	062677	IORST		
101	060477	READS	0	Read console switches into AC0
102	061117	DOAS	0,LPT	Output character
103	063517	SKPBZ	LPT	Wait for printer response
104	000777	JMP	.-1	
105	065117	DOAS	1,LPT	Send line feed
106	063517	SKPBZ		
107	777	JMP	.-1	Repeat
110	771	JMP	.-1	

To run under DONE logic, change the instruction in location 103 to 063617.

If the program does not cause printing, hit the console stop switch. Then press the instruction step switch several times and observe the program addresses being executed. If the program just cycles in the two instruction BUSY loops (locations 103 and 104), then a problem exists with one of the following:

1. The printer is not working. Test by itself with self test feature or external test plug.
2. The cable has been improperly installed. Carefully check installation.
3. A problem exists with the controller. Check that controller is in the correct slot.

Prior to calling ZETACO, Inc., run Test A and Test B and note results of these tests plus all symptoms (lights on in printer, prints but doesn't advance paper, runs Tests A and B but not C, etc.)

Test B: Program To Read Printer Status Bit

Memory Location	Octal Program	Symbolic Code		Comments
120	062677	IORST		
	064417	DIA	1,17	
	063077	HALT		
	000775	JMP	.-3	

Enter octal program into memory through console data switches. Start at location 120. The program reads a printer status word and then halts. If the printer is powered, has paper and is on line, examine bit 15 of AC1. The result should be a binary one.

Test C: Operation Under Interrupts

Memory Location	Octal Program	Symbolic Code	Comments
1	210	JMP 210	
200	062677	IORST	
	076077	MSKO 3,CPU	Mask out device
	061117	DOAS 0,LPT	
	063617	SKPDN LPT	
	777	JMP .-1	
	065117	DOAS 1,LPT	
	060177	INTEN	Enable interrupts
	400	JMP .+0	Wait
210	071477	INTA 2,CPU	Acknowledge
	060217	NIOC LPT	
	063077	HALT (or JMP .-10, 000766)	

The program starts at location 200. Prior to beginning, a printable character must be placed in AC0 and a line feed code (012) in AC1. A mask word must also be placed in AC3. The program outputs the first character under DONE logic and then waits for an interrupt from the print cycle at the JMP .+0 instruction. Upon receiving the interrupt, the program goes through location 1 to the interrupt processing routine at location 210. The INTERRUPT ACKNOWLEDGE instruction should place the printer octal device code (017) in AC2 and then halt. By changing the halt to a jump instruction, the program can be made to run continuously.

The printer mask bit is bit 12. If there is a binary one in bit 12 of AC3, the printer interrupt scheme is disabled and the program will loop on the JMP .+0 instruction. If bit 12 of AC3 is zero, the program runs normally.

Test D: Program To Print Characters From Data Switches

Memory Location	Octal Program	Symbolic Code		Comments
100	062677	IORST		
	063077	HALT		Set data switches, press CONTINUE
	020115	LDA	0,CNT	
	040116	STA	0,TEMP	
	060477	READS	0	Read console switches
	061117	DOAS	0,LPT	Output a character
	063617	SKPDN	LPT	
	777	JMP	.-1	
	014116	DSZ	TEMP	Decrement counter
	774	JMP	.-4	
	065117	DOAS	1,LPT	LF character
	063617	SKPDN		
	777	JMP	.-1	
	765	JMP	.-11	
	10	CNT:	10	# characters to be printed
	0	TEMP:	0	

This program has proven useful in printing out the full character set, since the character to be printed can be changed on the fly by changing the console data switches. A line feed code (012) must be set into AC1 before beginning. The program starts at location 100 and halts immediately for a character to be set on the data switches. Press the CONTINUE switch to start again. The program then sends out eight characters followed by a line feed, thereby causing a print cycle. After each line, the character to be printed is read from the code set in the console data switches. The number of characters printed on a line can be varied by changing the octal constant CNT in core.

Test E: Program To Output Four Characters

This program provides a means of selectively sending out various combinations of letters, control characters and paper feed commands to test the VFU and paperfeed characteristics of the printer.

Memory Location	Octal Program	Symbolic Code		Comments
100	062677	IORST		
	061117	DOAS	0,LPT	
	063517	SKPBZ	LPT	
	777	JMP	.-1	
	065117	DOAS	1,LPT	
	063517	SKPBZ	LPT	
	777	JMP	.-1	
	071117	DOAS	2,LPT	
	063517	SKPBZ	LPT	
	777	JMP	.-1	
	075117	DOAS	3,LPT	
	063517	SKPBZ	LPT	
	777	JMP	.-1	
	763	JMP	.-13	

The four characters to be printed are placed in AC0-AC3. A typical example is A, B, VTAB, CC (101, 102, 013, 002). Here the letters AB are printed on each line, and the control code for a double line feed is used.

Special Notes: Common Difficulties

The most frequent reason for an inoperable interface is an internal cable which has been improperly plugged onto the computer end plane. Double checking of this cable cannot be overstressed.

The second most common difficulty encountered is caused by operating the printer board. This can occur quite by accident long after the interface has been fully verified if another controller or memory board is temporarily removed from the computer. The symptom of this condition is that the printer will run using BUSY/DONE logic but will not operate under interrupt control. The cause is the fact that the interrupt priority continuity is broken by an empty board slot. The condition is corrected by replacing a missing board or jumpering the INTP and DCHP lines (see section on installation).

7.7 Printer Diagnostic Program

ZETACO, Inc. offers separate diagnostic programs for both the Centronics and Data Products line printers. The detailed operating instructions are summarized in the comments in the front of the program listing. Sample printouts are also provided. The general operating instructions are described below.

Diagnostic Requirements

Equipment

Data General Minicomputer (any model)
Line printer with parallel interface
Custom Systems printer controller
Paper tape reader (optional)
Teletype or CRT

Storage

This diagnostic requires locations 0 through 2000 octal. A buffer area starting at about 700 octal is used for the teletype or CRT input test.

Operating Procedure

Loading Method

Use standard binary loader to load binary diagnostic tape through the teletype reader or high speed reader.

Operator Action Required

Set the data switches to the starting address indicated for the selected test.

Test 1	S.A.	00010	On Line Status Check
2		11	Operation Using BUSY Logic
3		12	Auto Carriage Return Test
4		13	Operation Under Interrupt Control
5		14	Print From Data Switches
6		15	Input From Teletype
7		16	Vertical Format Unit Test

Press EXAMINE switch to load starting address. Then set program looping switches and press CONTINUE. Each subtest will repeat continuously if SWØ = 1. If SWØ = Ø, the program makes one pass and halts. To go on to the next subtest without changing the starting address, set switch SW1 = 1. When the processor halts, set SW1 = Ø and press CONTINUE, and the next test will begin.

Test Descriptions

On Line Status Check

The diagnostic reads in the printer status word with a Data In A instruction to determine whether the printer is powered, has paper and has been selected by the operator. If bit 15 is unequal to 1, the program halts at STATER (location 000033). If status is valid, the program continues to loop until SWØ is set to Ø by the operator.

Operation Using BUSY Logic

This subtest puts out a short canned message followed by a carriage return and line feed. Alternate lines of data are preceded by an octal 16 code which gives enlarged size characters. Timing of characters is under the control of the BUSY flip flop in the printer controller.

Auto Carriage Return Test

This test prints a title using BUSY logic and then alternately sends out the letter A followed by a blank code. This test will cause a print cycle to occur whenever a full line (80 or 132) of characters has been received by the printer.

Operation Under Interrupt Control

This test prints a single title line using BUSY logic and then follows with the ASCII character set (octal 40-177) using INTERRUPT logic. The character set pattern shifts by one character from line to line. Carriage return and line feed characters are sent after each 128 alphanumeric characters.

Print From Data Switches

This routine advances paper to the top of form and then halts. An ASCII character code can then be set into console data switches 8-15 and the CONTINUE switch pressed. The selected character is then continuously sent to the printer and the auto carriage return feature of the printer used to cause a print cycle. The character in the data switches can be changed on the fly as the printer runs.

Input From Teletype (or CRT)

This routine executes a top of form code to the printer and then sits in a wait loop for input from the teletype. The operator can type a message followed by a rubout character. The message will be printed on each line using BUSY logic. It is not necessary for the operator to add line feed or carriage return characters as these are inserted by the program.

If the rubout key is struck before entering another character on the teletype, a canned message is printed.

Vertical Format Unit Test

This routine is used to test the optional tape controlled 12 channel vertical forms feature. Note that most printers are not ordered with this option.

A standard 12 channel IBM format tape is mounted in the forms tape reader on the printer. The diagnostic will halt immediately after the program is started. The operator places the octal value of the number of channels punched on the forms tape and then presses the CONTINUE switch on the computer console. The program then prints a line and advances to the next hole on channel zero. Again a line of print occurs and the advance is to the next hole on channel one, etc.

Error Stops

STATER

If the computer halts at STATER, the indication is that an unexpected status has been read from the printer. Examination of register indicates error.

AC0 = Read Status
AC1 = Expected Status

Status Bits:
Bit 15 = If set to a binary one, indicates printer on line and ready.

IRRER

If the computer halts at IRRER, the indication is that an illegal device

code has been detected during an interrupt. Examination of registers indicates the device.

AC3 = Illegal Device Code
AC2 = Line Printer Device Code

DBER

If the computer halts at DBER, the error indication is that the device responded unexpected BUSY (BUSY flag set).

8.0 Four Line Asynchronous Multiplexer

8.1 Introduction

ZETACO's Asynchronous Multiplexer Controller enables any Data General Nova or Eclipse line computer to communicate with and control four serial terminal devices (i.e., CRT, teletype). The multiplexer controller contains all the circuitry necessary to receive, transmit and buffer the data characters between the terminal devices and the computer. This controller can be used in conjunction with additional multiplexer cards to serve up to 64 lines operated together as a multiplexing system. The multiplexer is compatible with Data General's operating system and diagnostic software.

8.2 Configurations

The multiplexer controller is configured into the following models and cable assemblies:

Model No.	Description
480-4	Four (4) channel multiplexer with individual baud rate, data format selection and RS-232 or current loop interface. Baud rate selection using dip switches is available as an option.
480-C	Internal cable and panel assembly.

8.3 Programming Notes

A receiver indicator (RI) and a transmit indicator (TI) are associated with each line. The receiver indicator is set when a character has been assembled from the serial input stream. It is cleared under program control. The transmit indicator is set whenever the line unit circuitry has accepted a character for transmission and is ready to accept another. I/O RESET clears all transmit and receive indicators. Since the transmitter circuitry includes double buffering, the transmit indicator is set almost immediately after accepting the first character following a long idle period. At maximum transmission rate, the transmit indicator is set once per character time; it is cleared under program control.

The four-line receiver/transmitter multiplexer controller contains conventional DONE flags for interface to a Nova line I/O bus. These are logically

ored together to get a system DONE. To the programmer, DONE appears set if any input lines have completely assembled characters ready for reading by the processor (some RI = 1) or if any output lines have transmitted characters and can accept new characters (some TI = 1).

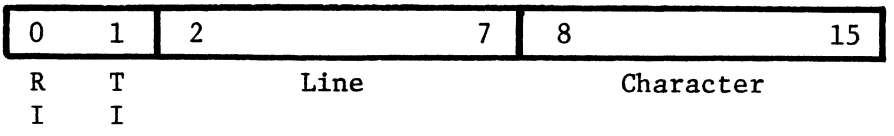
The DIAC instruction, which reads input characters and line control information, also clears the receiver indicator of the line just read. Upon issuance of DIAC AC QTY, DONE will be cleared if there are no other lines with data to be read and if all transmit indicators (for all lines) are 0. If there are additional lines to be read or character completions which need to be handled, DONE will remain set.

The DOA AC QTY instruction, which supplies a character for output on a selected line, also clears the transmit indicator for that line. If no new character is to be outputted, the DOB AC QTY instruction may be used to clear the transmit indicator without sending a new character. While DOA or DOB clears the transmit indicator for a line, they will clear DONE only if there are no other lines on which transmission has completed and if no receivers have assembled characters for the processor to read. The S-pulse is not microcoded as a part of an instruction.

The BUSY flag is set whenever output is occurring on any of the lines. It clears when all characters on all lines awaiting transmission have been sent.

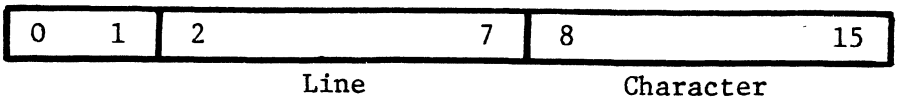
I/O Instructions

DIAC AC QTY reads the following word:



RI	Receive indicator--a character has been assembled and appears in bits 8-15, right justified.
TI	Transmit indicator--a character previously sent to the transmitter has been accepted for transmission and a new character may be sent.
Line	The line number to which the indicators apply.
Character	The character just received on the indicated line if RI is set; undefined is RI is not set.

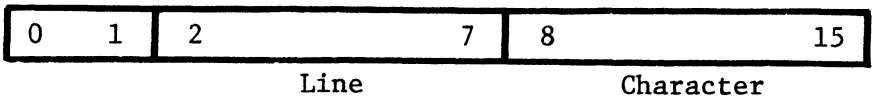
DOA AC QTY assumes the following word in an accumulator:



Line — The line number on which the character is to be transmitted and for which the transmit indicator is to be cleared. Bits 0 and 1 are ignored.

Character — The character to be transmitted, right justified in the byte if less than 8 bits.

DOB AC QTY assumes the following word in an accumulator:



Line — The line number (0 through 7 for a single card system) for which the transmit indicator is to be cleared. Bits 0, 1 and 8 through 15 are ignored.

8.4 Theory of Operation

8.4.1 General

In communicating with the serial terminal devices, the multiplexer hardware performs all character assembly and disassembly into the serial bit streams required. START and STOP bits are inserted on transmission and stripped out on reception. Character buffering is provided on both reception and transmission so that the program has a full character time to respond without losing input data or reducing transmission rate.

The multiplexer system is flexible in line capacity, transmission code and line speed. It can accommodate from four to 64 full duplex lines, in multiplex of four or eight at speeds including 19200 baud. The transmission code structure (character size and number of STOP bits) and line speeds are selectable by the user so that an installation can be reconfigured with minimal hardware change.

A number of four or eight line multiplexer cards appear as if they were a single I/O device connected to the computer under a single device code. On

reception, an I/O instruction reads words containing the line number in the left half and a character in the right. At the completion of transmission of a character, an I/O instruction reads a similar word containing the line number indicating that a character has been transmitted. The program responds by outputting a word containing the appropriate line number and new character. Multiplexing occurs since the I/O instruction to read a line number/character word and control information always affects only one line on one of several cards. The choice of which of several cards is made automatically by the hardware in priority order, lower line numbers having the higher priority.

8.4.2 Circuit Descriptions

Clock Oscillator and Baud Rate Divider Chain

The basic multiplexer timing is generated by a crystal-controlled series resonant oscillator which operates at 3.072MHz. Chip A3 (on the Common Peripheral logic) divides the clock oscillator frequency by 10 and then feeds the baud rate divider chain and the I/O RESET logic.

The baud rate divider chain (chips F11, G11 and J12) further divides the clock oscillator into the frequencies required for the various baud rates. Note that the clock frequency is 16 times the baud rate. Divider chain outputs are connected to the baud rate jumpers or optional switches to accommodate jumpering the requires baud rates for each line. Baud rate jumper locations and line numbers are listed.

Jumper Location	Line No.
B12	0
C12	1
D12	2
E12	3

The I/O RESET logic is a pulse-forming network on the computer interface I/O term IORST.

Computer I/O Interface

The interface provides decoding of the I/O instructions, multiplexer selection, line selection and data interface.

Multiplexer selection (MUX SEL) and line selection (SEL GROUP) are gated with the necessary I/O instructions to insure the correct communications link is established.

Mask bit 14 is used to mask interrupts from the multiplexer.

The multiplexer selection logic decodes the DSO-DS5 lines for either a 30_8 or 70_8 device code. When selection is made, chip M1-pin 8 goes low and stays low as long as the proper decode is maintained.

The Line Selection logic exclusive ores data lines bits 2 through 5 and the hard wired line addresses on the board. When the data lines match the hard wired address, chip C5-pin 6 goes low. This indicates a particular group of four lines has been selected. C5-6 is added with MUX SEL at chip F7; and, when pin 13 becomes active (SEL GROUP), it indicates that the MUX and a group of lines are selected.

The data interface is an open collector interface connected to the computer's common data bus. The multiplexer uses the data interface for received data, transmitted data, line number and the transmit/receive indicator.

Data Transfer

This section encompasses the Character Assembly and Disassembly logic, the BUSY/DONE logic and the Line Priority logic.

The heart of the Character Assembly and Disassembly logic is the universal asynchronous receiver/transmitter chip (UART). The UART can be separated into a transmitter section and a receiver section and is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

All lines operate similarly; and, therefore, line 0 will be used as a representative line in the descriptions.

(Reference transmitter timing diagram for following description.)

The transmitter section basically assembles parallel data from the computer into serial asynchronous data for the terminal device.

The data lines, bits 8 through 15, are connected to all the UART's. Data is loaded into the UART's by the DATA OUT A command. Loading the correct UART is accomplished by a 1 of 4 decoder (chip E5) which provides a THRL pulse only for the addressed line. In our example, TRL0 would become active and load UART 0 buffer register (chip B10).

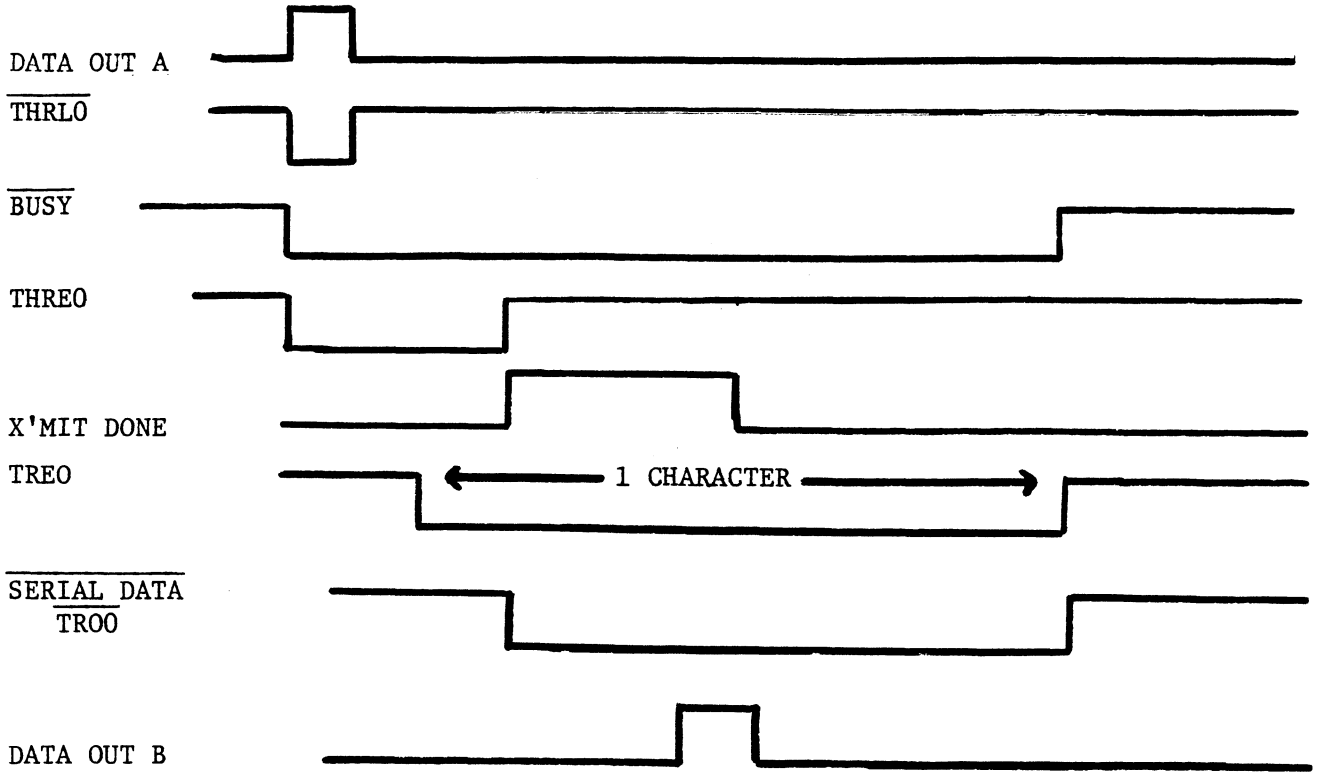
THRL0 also sets the BUSY flip flop (chip B8) indicating a data transfer is in progress. Data is then transferred from the UART's buffer register to its transmitter register. At this time, THRE0 becomes active and sets the X'MIT DONE flip flop (chip C7). Data begins to serially shift out of the transmitter register (TR0) and is outputted at current loop or RS-232 logic levels. The START, PARITY and STOP bits are automatically appended to the serial data by the UART's control circuitry which is jumper controlled. UART control pins 35 through 39 are jumperable so that the characters may be 5, 6, 7 or 8 bits in length, have 1, 1½ or 2 STOP bits and have odd, even or no parity bit.

As previously mentioned, THRE0 sets the X'MIT DONE flip flop. This flip flop can be cleared by IORESET or DOB0--DOB0 being DATA OUT B gated by the selected line (chip E5).

At the completion of the transmission of a data character, TRE0 becomes active and clears the BUSY flip flop. This completes the transmission cycle.

(Reference the receiver timing diagram for the following description)

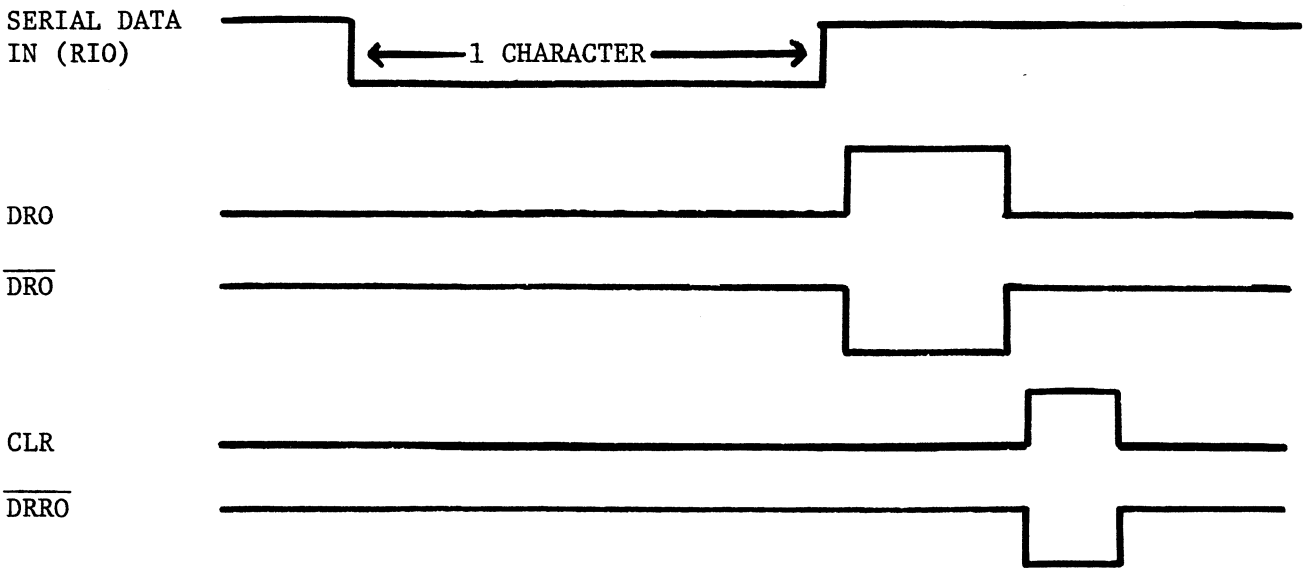
The receiver section disassembles the asynchronous data characters into a parallel character and outputs the character to data bits 8 through 15 with the START, PARITY and STOP bits removed.



Transmitter Timing

Serial data (RIO) enters the UART buffer register from the line receiver. When an entire character has been assembled, DRO goes high indicating that the character has been transferred to the UART's holding register. DRO is equivalent to a RECEIVE DONE flip flop. The RECEIVE DONE (DRO) is processed through the priority chain and DRO enables the parallel output of UART 0 holding register. (All the UART's holding registers are wired together, and enabling the DRX input enables that particular UART to output its holding register on the DATA BUS bit 8 through 15.)

A CLEAR pulse (chip A10) DRRO disconnects UART's 0 holding register from the data bus and resets DRO (the RECEIVE DONE flip flop).



Receiver Timing

The BUSY gate is an "OR" gate of the four individual lines TRANSMIT BUSY. Any line being BUSY produces a multiplexer BUSY signal (chip C5-pin 8).

The multiplexer DONE may be either a TRANSMIT DONE (TDO) or a RECEIVE DONE (DRO). Any line with TRANSMIT DONE or RECEIVE DONE active produces a card DONE (chip A11-pin 15).

The Priority logic is priority on the TRANSMIT or RECEIVE DONE. It assigns the highest priority to the lower number lines (i.e., line 0 has higher priority than line 2). TRANSMIT DONE (TDO) or RECEIVE DONE (DRO) is continuously strobed by REQB in the priority network. If a higher priority DONE does not exist, a lower order $\overline{DRX}$ is allowed. As previously mentioned, the four lines of $\overline{DRX}$ connect to chip A11 to provide a card DONE. Chip A11 also encodes the $\overline{DRX}$ into a binary representation. This binary representation (IN0, IN1) provides selection logic to chip A6 to select the transmit/receive indicator and line address information during a Data In A instruction.

Terminal Device Interface

The terminal device output can be either 20 MA current loop or RS-232C output. A jumper option is available for ease of conversion. If this option is required, inform ZETACO at the time of ordering. If ZETACO is

not informed that this conversion is a customer requirement, the boards will be shipped as RS-232C output only.

8.4.3 Installation and Options

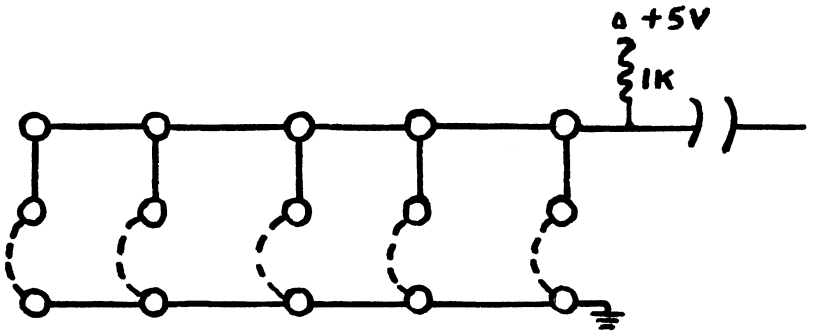
Recheck option requirements to ensure the options originally specified are still correct. Install and recheck cabling to the board to ensure correct connections. Install multiplexer board in the Nova or Eclipse logic chassis.

Note that when using ZETACO's internal cable and panel assembly 480-C, the following interface circuits cabling should be noted:

Internal Cable	Description	Connect to External Cable (Customer Supplied)
Connecting CRT's to the cable and panel assembly:		
Pin 2	Transmitted Data	Pin 3
Pin 3	Received Data	Pin 2
Connecting modems to the cable and panel assembly:		
Pin 2	Transmitted Data	Pin 2
Pin 3	Received Data	Pin 3

Jumper Options (Reference Jumper Option Sheet)

UART Jumpering



____ = Primary Jumper

---- = Alternate Jumper

To install alternate jumper, cut primary jumper (foil) and install insulated wire as shown.

Listed below are the jumper options associated with each UART:

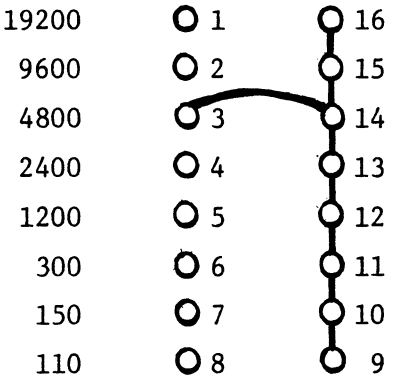
UART Pin #	Primary (Hi)	Alternate (Lo)
35	Inhibits parity generation and verification	Allows parity generation and verification
36	Two stop bits (When 5-bit word is programmed, 1.5 stop bits are generated.)	One stop bit

UART Pin #37	UART Pin #38	Word Length
Alternate (Lo)	Alternate (Lo)	5 bits
Alternate (Lo)	Primary (Hi)	6 bits
Primary (Hi)	Alternate (Lo)	7 bits
Primary (Hi)	Primary (Hi)	8 bits

UART Pin #	Primary (Hi)	Alternate (Lo)
39	Even Parity	Odd Parity

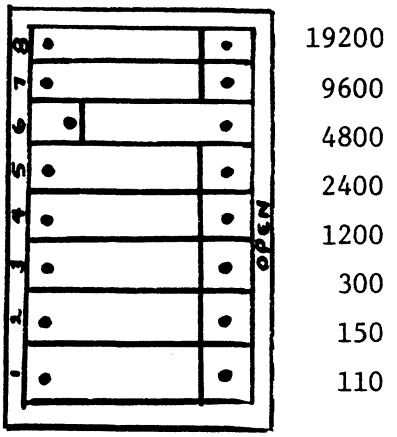
Unless specified, primary jumpers are installed at the time of shipment.

Baud Rate Jumpering (Reference Jumper Option Sheet



4800 baud shown
pin 3 to pin 14

Optional Switch



4800 baud shown
Switch 6 closed

For each line, eight baud rates are selectable. Listed are the pins to jumper for each baud rate.

Baud Rate	Jumper Pins	Switch Closed
19200	1 to 16	8
9600	2 to 15	7
4800	3 to 14	6
2400	4 to 13	5
1200	5 to 12	4
300	6 to 11	3
150	7 to 10	2
110	8 to 9	1

Unless specified, 4800 baud is selected at the time of shipment.

Multiplexer Address Jumpering (Reference Jumper Option Sheet)

Two addresses are available - 30_8 and 70_8

30_8 - No jumper

70_8 - Insulated jumper installed

Unless specified, address 30_8 is selected at the time of shipment.

RS-232C/Current Loop Jumpering (Reference Jumper Option Sheet)

Each line may have either RS-232C(EIA) or current loop input/output. The capability to field change between RS-232C and current loop must be specified at the time of the order. If not specified at the time of order, the conversion must be done at the factory. If the board is ordered as field convertible, use the next page instructions. (Reference Jumper Option Sheet) Do not install both jumper choices.

RS-232C to Current Loop

1. Install/remove jumper per below:

	Current Loop Install Jumper	RS-232C Install Jumper
Line 0	SJ700	SJ701
1	SJ710	SJ711
2	SJ800	SJ801
3	SJ810	SJ811

2. Resistor - 470 ohm

	Current Loop Install	RS-232C Remove
Line 0	SJ705	SJ705
1	SJ715	SJ715
2	SJ805	SJ805
3	SJ815	SJ815

Current Loop to RS-232C

1. Install/remove jumpers per below:

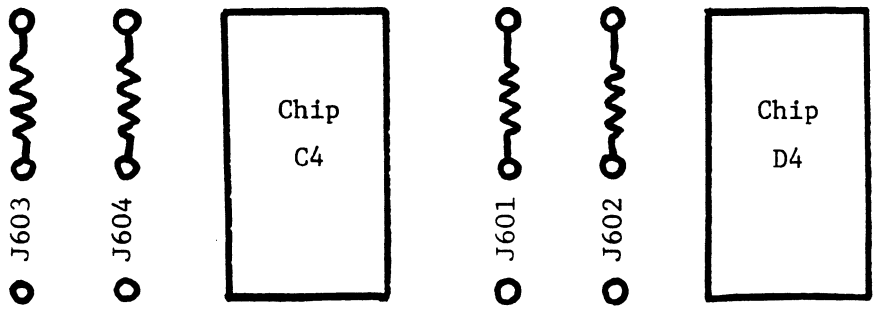
	Install Jumper	Remove Jumper
Line 0	J701	J700
1	J711	J710
2	J801	J800
3	J811	J810

2. Remove 470 ohm resistors.

Line 0 - R706
1 - R713
2 - R806
3 - R813
} 4 Channel

Line Address Jumpering (Reference Jumper Option Sheet)

Up to 64 addresses are available (4 addresses per multiplexer board).



Line Selection

	J604	J603	J602	J601
Line 0 → 3	-	-	-	-
4 → 7	J	-	-	-
8 → 11	-	J	-	-
12 → 15	J	J	-	-
16 → 19	-	-	J	-
20 → 23	J	-	J	-
24 → 27	-	J	J	-
28 → 31	J	J	J	-
32 → 35	-	-	-	J
36 → 39	J	-	-	J
40 → 43	-	J	-	J
44 → 47	J	J	-	J
48 → 51	-	-	J	J
52 → 55	J	-	J	J
56 → 59	-	J	J	J
60 → 63	J	J	J	J

- = 3K Resistor
J = Insulated Jumper

Unless specified, lines 0-3 are selected at time of shipment.

Priority Jumper When There Are Multiple Multiplexer Boards Per Computer

This back panel jumper allows priority assignment. Jumper pin A91 of higher priority board to A92 of a lower priority board.

Terminal Device Interface

CLEAR TO SEND CH 0	A75
CH 0 SERIAL DATA IN	A87
CH 0 SERIAL DATA OUT	A79
CLEAR TO SEND CH 1	A84
CH 1 SERIAL DATA IN	A88
CH 1 SERIAL DATA OUT	A86
CLEAR TO SEND CH 2	A76
CH 2 SERIAL DATA IN	A81
CH 2 SERIAL DATA OUT	A78
CLEAR TO SEND CH 3	A73
CH 3 SERIAL DATA IN	A92
CH 3 SERIAL DATA OUT	A89

9.0 Interface Signals, Pin Assignments, Optional Cabling Assembly

Listed below are the computer interface and external interface signals used by the Slot Saver II controller board. A brief description of the optional cable panel assembly available for the Slot Saver II is also included.

9.1 Computer Interface Signals

Signal	Back Panel Pin
CLR	A50
$\overline{\text{DATA 0}}$	B62
$\overline{\text{DATA 1}}$	B65
$\overline{\text{DATA 2}}$	B82
$\overline{\text{DATA 3}}$	B73
$\overline{\text{DATA 4}}$	B61
$\overline{\text{DATA 5}}$	B57
$\overline{\text{DATA 6}}$	B95
$\overline{\text{DATA 7}}$	B55
$\overline{\text{DATA 8}}$	B60
$\overline{\text{DATA 9}}$	B63
$\overline{\text{DATA 10}}$	B75
$\overline{\text{DATA 11}}$	B58
$\overline{\text{DATA 12}}$	B59
$\overline{\text{DATA 13}}$	B64
$\overline{\text{DATA 14}}$	B56
$\overline{\text{DATA 15}}$	B66
DATIA	A44
DATOA	A58
DATOB	A56
* $\overline{\text{DCHP IN}}$	A94
* $\overline{\text{DCHP OUT}}$	A93
$\overline{\text{DSO}}$	A72
$\overline{\text{DS1}}$	A68
$\overline{\text{DS2}}$	A66
$\overline{\text{DS3}}$	A46
$\overline{\text{DS4}}$	A62

Signal	Back Panel Pin
$\overline{\text{DS5}}$	A64
INTA	A40
* $\overline{\text{INTP IN}}$	A96
* $\overline{\text{INTP OUT}}$	A95
$\overline{\text{INTR}}$	B29
IORST	A70
$\overline{\text{MSKO}}$	A38
$\overline{\text{RQENB}}$	B41
$\overline{\text{SELB}}$	A82
$\overline{\text{SELD}}$	A80
STRT	A52

*For the two pairs of priority-determining signals, the IN signal comes from the processor or the preceding device, the OUT signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), jumper pin A93 to A94 and A95 to A96 to maintain bus continuity.

9.2 Device Interface Signals

Signal	Back Panel Pin
SERIAL PORT #1	
SERIAL DATA OUT	A85
SERIAL DATA IN	B69
CLEAR TO SEND	A90
READER RUN (Optional Jumper)	A89
SERIAL PORT #2	
SERIAL DATA OUT	B13
SERIAL DATA IN	B11
CLEAR TO SEND	B67
REAL TIME CLOCK	
50/60Hz SIGNAL	B6

Signal	Back Panel Pin
PRINTER	
Bit 1	B15
Bit 2	B19
Bit 3	B23
Bit 4	B25
Bit 5	B27
Bit 6	B31
Bit 7	B49
Bit 8	B51
SELECTED	B54
STROBE	B53
BUSY	B52
PAPER EMPTY	B48
DEMAND	B38
VFU	B36
FOUR CHANNEL MULTIPLEXER	
LINE 0 SERIAL DATA OUT	A79
LINE 0 SERIAL DATA IN	A87
LINE 0 CLEAR TO SEND	A75
LINE 1 SERIAL DATA OUT	A86
LINE 1 SERIAL DATA IN	A88
LINE 1 CLEAR TO SEND	A84
LINE 2 SERIAL DATA OUT	A78
LINE 2 SERIAL DATA IN	A81
LINE 2 CLEAR TO SEND	A76
LINE 3 SERIAL DATA OUT	A89
LINE 3 SERIAL DATA IN	A92
LINE 3 CLEAR TO SEND	A73

9.3 Optional Cable Panel Assembly

An optional cable panel assembly (Model 480-C) is offered by ZETACO as a convenient means to attach external cables to the Slot Saver II board. The cable panel consists of a 19-inch wide by 3½-inch high metal panel which can be mounted in the rear of your computer cabinet. This panel contains six standard RS-232C type 25-pin female connectors plus a cable harness assembly approximately five feet in length which runs up to and plugs on to the side plane of the mini-computer. In this manner, external cables to the two console CRT's and four multiplexed terminals can be easily connected or disconnected at the rear of the computer cabinet. The pin outs of the six serial plugs are detailed on the next page.

Note that the line printer cabling which comes with the Slot Saver II is a direct single piece cable assembly which plugs into a separate area of the computer end plane and does not pass through the Model 480-C panel.