Model 270

10 MB Disk Controller

200-T39-HH4-01

REVISION HISTORY		
ECO #	DATE	DESCRIPTION
0328	6/28/84	New ZETACO Cover

CUSTOMER SERVICE

Our warranty attests the quality of materials and workmanship in our products. If malfunction does occur, our service personnel will assist in any way possible. If the difficulty can not be eliminated by use of the following service instructions and technical advise is required, please phone the Custom Systems sales department (612-941-9480) giving the serial number, board name, model number, and problem description. You will be placed in contact with the appropriate technical assistance.

PRODUCT RETURN

Pre-return Checkout.

If controller malfunction is suspected, the use of test software is needed to determine if the controller is the problem and what in particular is wrong with the controller. The tests applicable to this board are listed on the next page of the manual. Please run the test sequence before considering product return.

Returned Material Authorization.

Before returning a product to Custom Systems for repair, please ask our sales secretary for a "Returned Material Authorization" number. Each product returned requires a separate RMA number. Use of this number in correspondence and on a tag attached to the product will ensure proper handling and avoid unnecessary delays.

Returned Material Information.

Information concerning the problem description, system configuration, diagnostic program name, revision level, and results, i.e., error program counter number should be included with the returning material. A form is provided for this information on the next page of the manual.

Packaging.

To safeguard your materials during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

(Include with returning material)

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to Custom Systems, Inc. for repair. This will: 1) Determine if in fact the board is defective (many boards returned for repair are not defective, causing the user unnecessary system down-time, paper work, and handling while proper testing would indicate the board is working properly). 2) Increase the speed and accuracy of a product's repair which is often dependent upon a complete understanding of the user checkout test results, problem characteristics, and the user system configuration. Checkout results for the 10 Megabyte Disk Controller should be obtained by performing the following tests. (Include error program counter #'s and accumulator contents if applicable).

FUNCTION	TEST	RESULTS
Formatting	D.G. PDKP FMTR	
Data or other errors	D.G. DKT Diag. D.G. PDKP Reli.	

Other tests performed:

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this sheet with the mal-functioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain).

   _____

2. What operating system are you running under? (AOS RDOS, DDOS, DTOS).

   _____

3. Describe the system configuration (i.e., peripherals, I/O controllers, model of computer, etc.

   _____

   _____

4. Has the controller been returned before? _____ Same problem?_____

To be filled out by CUSTOMER:

Model #: _____

Serial #: _____

RMA #: _____

Returned by: _____
(company name)

TABLE OF CONTENTS

1.0 GENERAL DESCRIPTION

The Custom Systems Model 270 Cartridge Disk Controller is designed to interface to any of the Data General Nova or Eclipse Model Minicomputers, with up to four top or front loading type cartridge disk drives.

Specifications of the disk drives are as follows:

Loading	-	Top/Front
Tracks/In	-	200
Total Tracks	-	408
Density	-	2200 BPI
Discs	-	1 removable and 1 fixed
Speed	-	2400 RPM
Sectors	-	12
Data Format	-	Double Frequency
Data Capacity	-	10 Megabyte Per Drive

Some representative Cartridge disk drive manufacturers that the disk controller will interface to are:

1. Diablo Series 40 and (44B)
2. Western Dynex Series 6000
3. Ampex Series DM 440
4. EMM (CAELUS) Series 306
5. Wangco Series T&F
6. CDC Series 9427

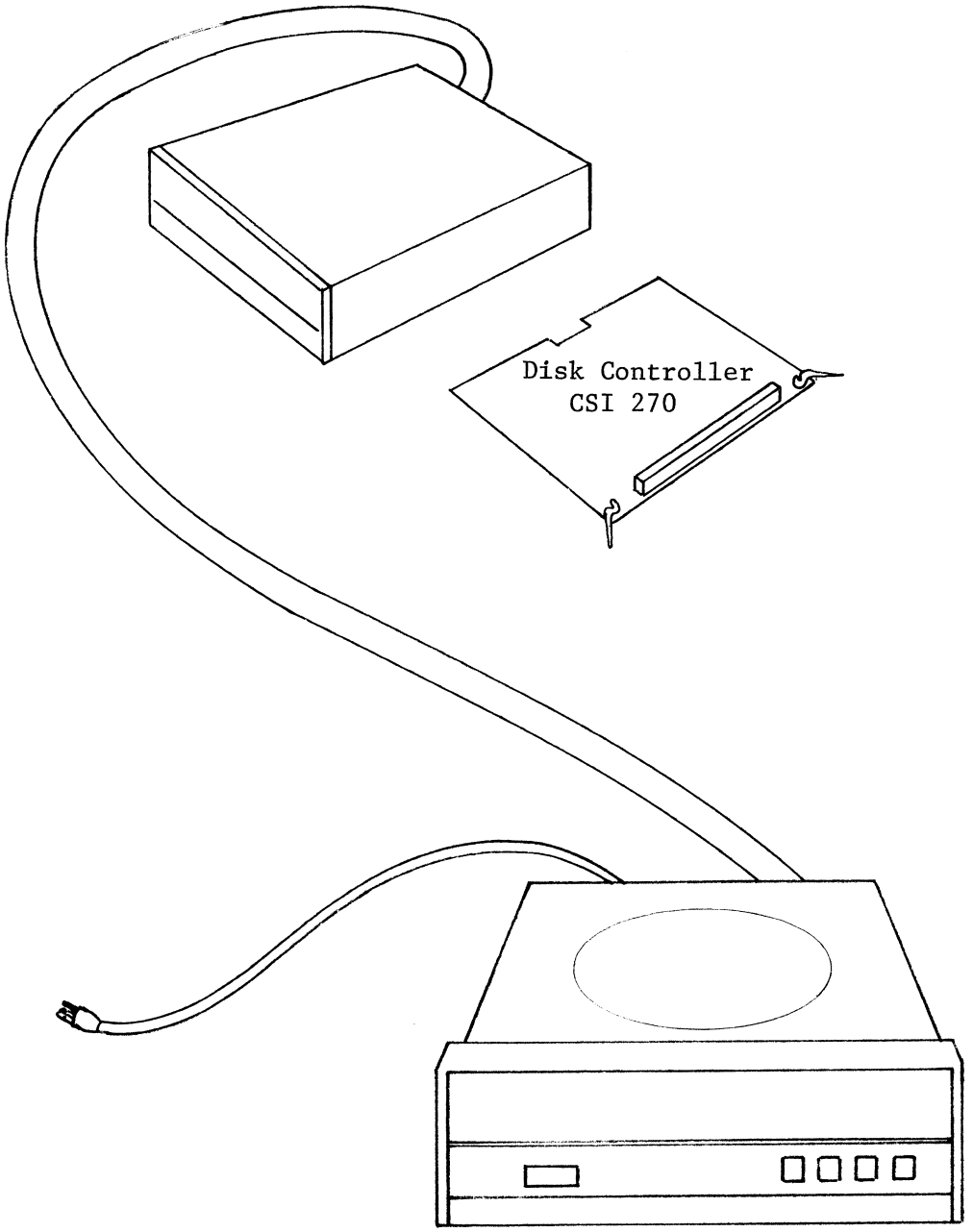
These drives use either the 5440 (Top Loading) or 2315 (Front Loading) style removable disk cartridges.

In addition to the above disks, the controller can be jumper modified to interface with the Diablo Series 30 drives. Therefore, both 10 Megabyte and 2.5 Megabyte Diablo disks can be interfaced with the same controller.

The Model 270 Cartridge Disk Controller is incorporated on a single 15"x15" printed circuit card that plugs directly into any spare slot available within the mini-computer (Reference Figure 1). The controller requires + 5 volts and receives its power from the computer +5V supply.

BASIC DISK CARTRIDGE SYSTEM

FIGURE 1



Specifications for the Model 270 disk controller are:

Data Transfer Rate	-	2.5 MHZ
Words Per Sector	-	256 (16 bit)
Sectors Per Track	-	12
Heads Per Disk	-	2
Number Of Disks	-	2
Drives Per Controller	-	4
Data Per Disk	-	5.0 Million Bytes
Power Requirements	-	+5.0 Volts (± 0.25V) 5.0 Amps
Dimensions	-	15" x 15" x ½"

The disk controller transfers data through the processor's data (DMA) channel, allowing the processor to perform other calculations or I/O operations while the data is being transferred. To read a file from the disk to the processor or to write a new file on the disk, the programmer need only specify the locations on the disk and in memory for the data transfer, the number of blocks of data involved in the transfer and the direction of the transfer.

The disk controller includes address verification circuitry that increases system reliability by ensuring the proper cylinder, head and sector destination was achieved before the data transfer is started. Further data integrity is ensured by appending a cyclic redundancy checkword (CRC) to every data field during a write operation. The CRC is regenerated during a read operation, and the regenerated CRC is bit by bit compared to the written CRC. If they compare, the record is error free. If they do not compare, a data error exists and a retry on that particular record should be made.

The cartridge disk controller has device code 33_8. If a second cartridge disk controller is connected to the bus, it would have device code 73_8.

The controller employs TTL integrated circuits exclusively and uses standard, off-the-shelf chip types. Each controller is rigorously tested to reduce early life and thermal failures.

A 6-8 foot interface cable is supplied with each controller. This interface cable has mating connectors to connect the disk drive to the disk controller.

The disk controller is compatible to Data General's system and diagnostic software.

TABLE 1

DIABLO 44B DISK

Board Type	Jumpers/Switches
SO	No jumpers/switches on this board
AL	SW1 - OFF (Off=200TPI ON=100TPI)
	2- OFF (OFF=NEG. ATTN ON=POS. ATTN)
	3, 4 FILE ADDRESS (CONTROLLER DOESN'T CARE)

SW3	SW4
ON	ON-FILE 1
ON	OFF-FILE 2
OFF	ON-FILE 3
OFF	OFF-FILE 4

LO	SW1 - OFF	ON=INDEX ONLY (UPPER DISK)
	2 - OFF	ON=1500 RPM
	3 - OFF	
	4 - ON	
DT	SW1 - ON	ON=SEPARATE WRITE/ERASE
	2 - ON	OFF=WRITE PROTECT UPPER DISK
	3 - ON	OFF=WRITE PROTECT LOWER DISK
	4 - OFF	OFF=SEPARATED DATA

TABLE 1 (continued)

WESTERN DYNEX OR AMPEX

Board Type	Jumpers/Switches	
SERVO PWB	H_c-H_1	Allow 408 tracks
DATA PWB	A_c-A_1	Selects top head on low input
	D_c-D_1	Allow sending of write check status
SECTOR COUNTER	B_c-B_2	Sends data pulse between data clocks
	C_c-C_2	Allow sending of decoded data
	D_c-D_1	Allow sector count to be sent
	E_c-E_1	Allow sector count to be sent
	F_c-F_1	Allow sector count to be sent
CONTROL PWB	A_c-A_1	Gated restore
	B_c-B_2	
	D_c-D_1	Selects RMVBL disk on low I/O input
	GC_2-G_2	
	GC_1-G_1	
	H_c-H_1	
	J_c-J_1	Latched illegal address
	K_c-K_2	
	L_1-L_2	
	M_c-M_1	
	N_c-N_1	Busy on all seek commands
	O_c-O_1	
	S_c-S_2)	Leading edge seek strobe
	T_c-T_1)	

TABLE 1 (continued)

WESTERN DYNEX OR AMPEX (continued)

Board Type	Jumpers/Switches
CONTROL PWB	W_c-W_1 Latched Stop Load
	V_c-V_2

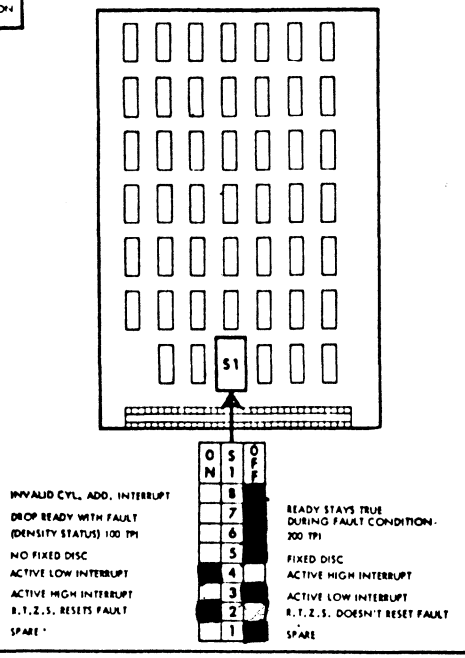
Western Dynex/Ampex have assigned interface configuration 223 to their drives to work with Custom Systems' controller.

EMM (CAELUS) SERIES 306

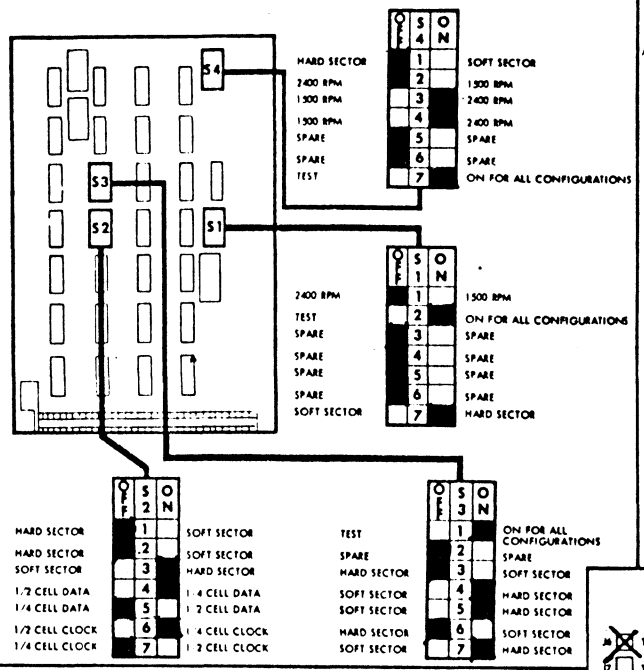
Board Type	Jumpers/Switches
DRIVE CONTROL BOARD	E1-E2 TOP LOAD
CONTROL SECTOR BOARD	E2-E1 Sect Cnt on leading edge of notch
	E5-E4 Sect Cnt on leading edge of notch
	E8-E7 Sect Cnt on leading edge of notch
	E11-E10 Sect Cnt on leading edge of notch
DATA TRANSLATOR BOARD	E5-E6 Double frequency data in
	E2-E4 Diablo formatted data out
READ/WRITE BOARD	E3-E5 Write inhibit switch on
INPUT/OUTPUT BOARD	E41-E40
	E44-E43 Illegal address/address acknowledge
	E47-E46
	E49-E48 With sector multiplexing
	E20-E21 Seek complete
	E52-E51 No retraction with controller power less
	E32-E33 Inverted head select
	E29-E28 Inverted disk select
	E16-E17 Address clear gated with seek pulse
	E1-E2 Full capacity
	E3-E4 Full capacity
	E25-E26 Double frequency in
	E23-E24 Diablo out
	E11-E12 200 TPI (STD)
	E34-E35 200 TPI(-)

■ INDICATES SWITCH POSITION

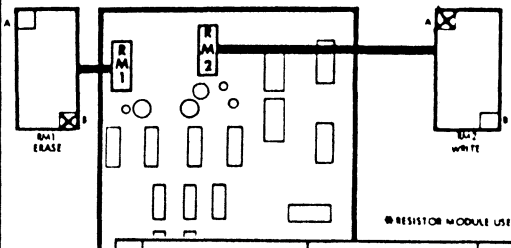
CONTROL BOARD



DATA RECOVERY BOARD

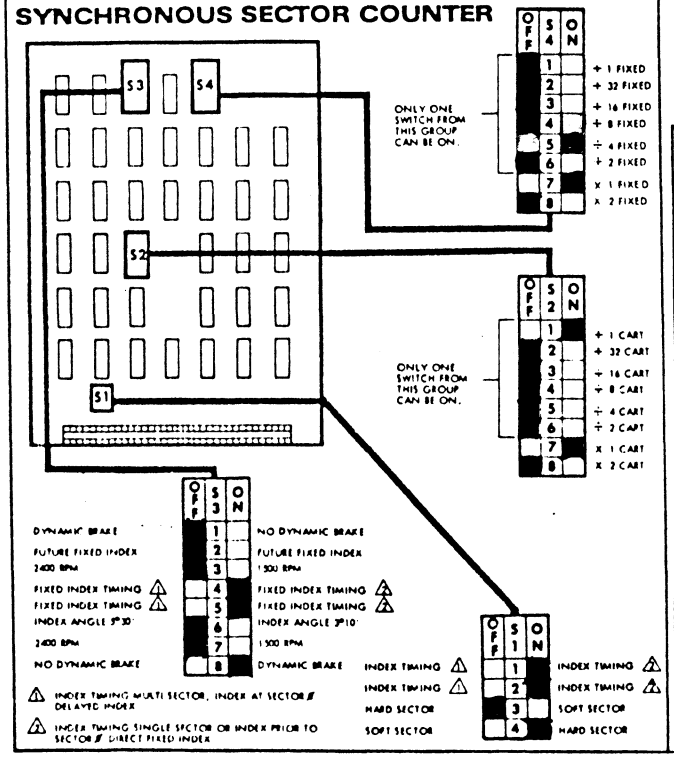


R/W/E BOARD

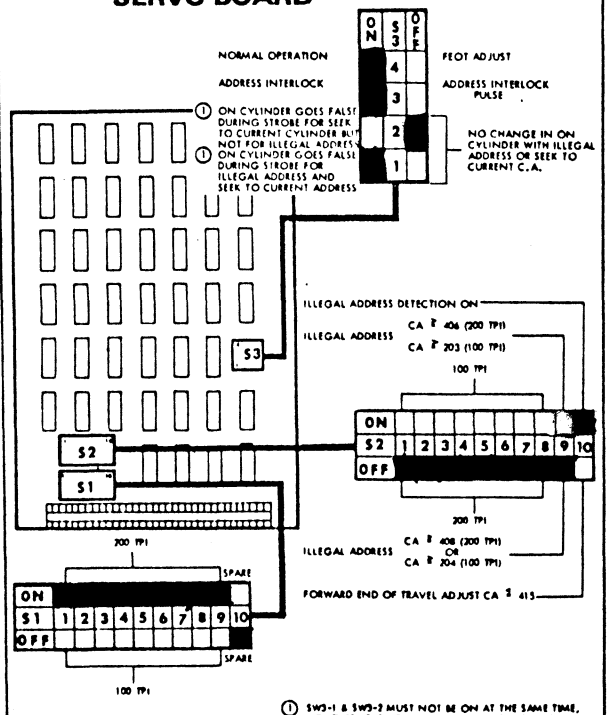


*	DESCRIPTION		RM1 – (ERASE)		RM2 – (WRITE)	
	TPI	ERASE TYPE	MOD. TYPE	PIN 1	MOD. TYPE	PIN 1
	100	PRE-ERASE	*5300130	B	*5300130	A
	100	STRADDLE ERASE	NONE		*5300130	A
	200	PRE-ERASE	75300100	A	NONE	
■	200	STRADDLE ERASE	75300200	B	*5300200	A

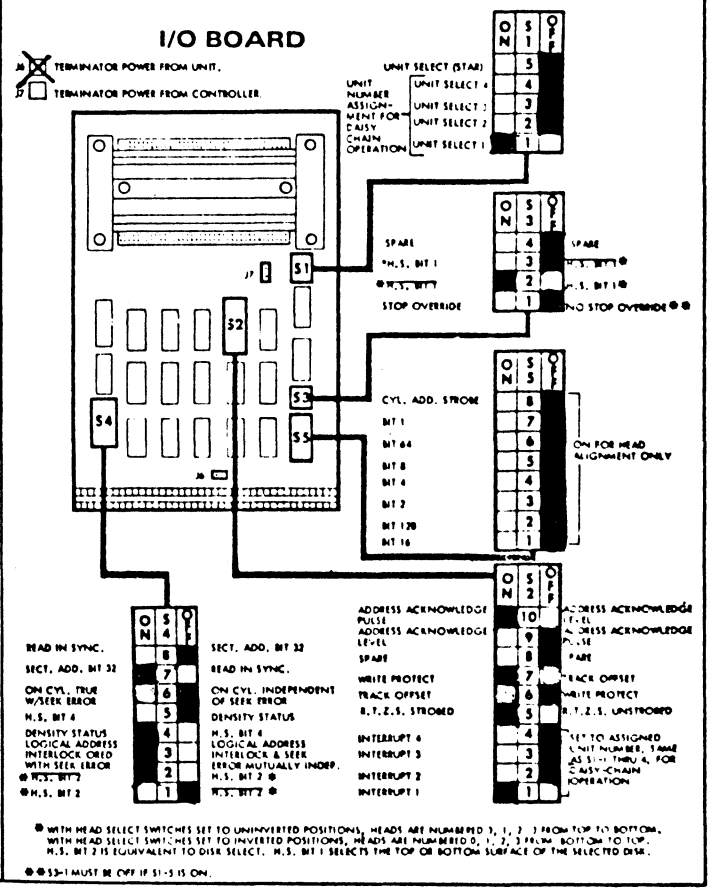
SECTOR BOARD - SYNCHRONOUS SECTOR COUNTER



SERVO BOARD



I/O BOARD



● WITH HEAD SELECT SWITCHES SET TO UNINVERTED POSITIONS, HEADS ARE NUMBERED 3, 1, 2, 3 FROM TOP TO BOTTOM. WITH HEAD SELECT SWITCHES SET TO INVERTED POSITIONS, HEADS ARE NUMBERED 0, 1, 2, 3 FROM BOTTOM TO TOP. H.S. BIT 2 IS EQUIVALENT TO DISK SELECT. H.S. BIT 1 SELECTS THE TOP OR BOTTOM SURFACE OF THE SELECTED DISK.

●● S3-1 MUST BE OFF IF S1-5 IS ON.

2.0 INSTALLATION AND OPTIONS

2.1 INSTALLATION

This section provides detailed information for installing the Custom Systems Series 270 Disk Controller.

Inspect the controller board for any in-transit damage. Contact the carrier and Custom Systems if any damage is discovered, specifying the nature and extent of the damage.

Installation of the disk controller involves installing the logic card into the Data General computer, interfacing the controller to the disk drive with the supplied interface cable, and configuring jumper options in the drive and the controller. Table 1 is available as a guide to the disk jumper options. For those drives not listed call Custom Systems or send your particular drive to Custom Systems to ensure controller/disk compatibility. Section 2.2 lists the controller board options.

Before proceeding, ensure the primary power is removed from each element of the system.

2.1.1 LOGIC CARD INSTALLATION

The disk controller is designed to install directly into any spare slot on the bus after the CPU, MEMORY and I/O board. Before installation:

1. Review Section 2.2 (Options) for your option requirements.

If with the selection of the I/O slot a vacant slot or slots exist between the disk controller and the board below it, the DCHP (Data Channel Priority) and INTP (Interrupt Priority) signals must be physically jumpered on the computer backpanel to maintain priority interrupt continuity. Install one end of a wire-wrap jumper to the DCHP - OUT signal at pin 93 of the "A" connector occupied by the device below the disk controller. Connect the remaining end to the DCHP - IN signal at pin 94 of the "A" connector occupied by the disk controller, bridging the vacant slot or slots. Similarly, connect

the INTP-OUT signal (pin A-95) from the lower device to the INTP-IN signal at pin A-96 of the disk controller. This will complete the priority interrupt continuity to the card. If vacant slots exist between the disk controller and the device above the disk controller, perform similar strapping of the DCHP and INTP signals to maintain interrupt priority.

The disk controller should now be inserted, component side up, into the selected I/O slot and locked into position with the release levers.

2.1.2 CABLING INSTALLATION

The disk controller and disk drive are interconnected with the supplied interface cable. The disk controller end of the cable is either a 100 pin brown connector that plugs on to the Data General paddleboard or a cable assembly that plugs on the computer backpanel I/O pins. The disk drive end of the cable has the appropriate disk interface connector to mate with the specified drive.

After the controller and cable have been installed and disk jumper options verified, power may be restored to the system. At the customer's discretion diagnostics may be run on the disk subsystem or on line operation pursued.

2.2 OPTIONS (Reference Jumper Option sheet in Schematic Section for Jumper/Switch locations).

2.2.1 DEVICE CODE

J200, J202 Installed = 33_8
J200, J201 Installed = 32_8
J200 Not Installed J202 Installed = 73_8
J200 Not Installed J201 Installed = 72_8

2.2.2 ATTENTION POLARITY

The controller will accept either negative or positive attentions from the disk drive. S4 closed = positive attention from drive.
S4 open = negative attention from drive.

2.2.3 RECALIBRATE ON RESET

This option repositions the disk drive heads to track 000 on each activation of the reset switch.

S3 closed = Recalibrate heads on activation of reset switch or normal commanded restore.

S3 open = Recalibrate heads on normal commanded restore.

2.2.4 MASK ADDRESS ERRORS

This option allows the capability of the disk controller to prohibit address errors. This option may allow a user to recover data that may have ordinarily been unrecoverable.

S2 closed = Prohibit address errors

S2 open = Allow address errors

2.2.5 SELECT FIXED DISK

This option allows selecting only the fixed disk. This option may be useful if hipboot is not installed on your removable pack, but on your fixed pack.

S1 closed = Select fixed disk only

S1 open = Select both fixed and removable disk

2.2.6 DIABLO SERIES 30 SELECT (This Option Must Be Ordered)

This option allows the controller to interface with the Diablo Series 30 drives. To convert from 10 Megabyte to 2.5 Megabyte perform the following:

1. Remove J907 and Add J908
2. Add 2024
3. Remove J1822 and Add J1823

3.0 PROGRAMMING NOTES

This section outlines the disk controller formatting and programming conventions.

3.1 FORMAT

The sector format allocates a 256, 16-bit word block of data to each sector. In addition to the 256 - word block of data, each sector contains a 16-bit address and error checking information and is organized as illustrated in figure 4.

GAP 1 - SYNC BIT — Gap 1 consists of 23 words of zero's (368 BITS) followed by a ONE-BIT that permits the controller's logic to synchronize itself with the address when a read or write operation is initiated.

ADDRESS - The address contains one word. During both read and write operations the address information is compared with the address the controller is seeking to ensure that the correct cylinder, head and sector are located. If the address information does not compare an address error is indicated.

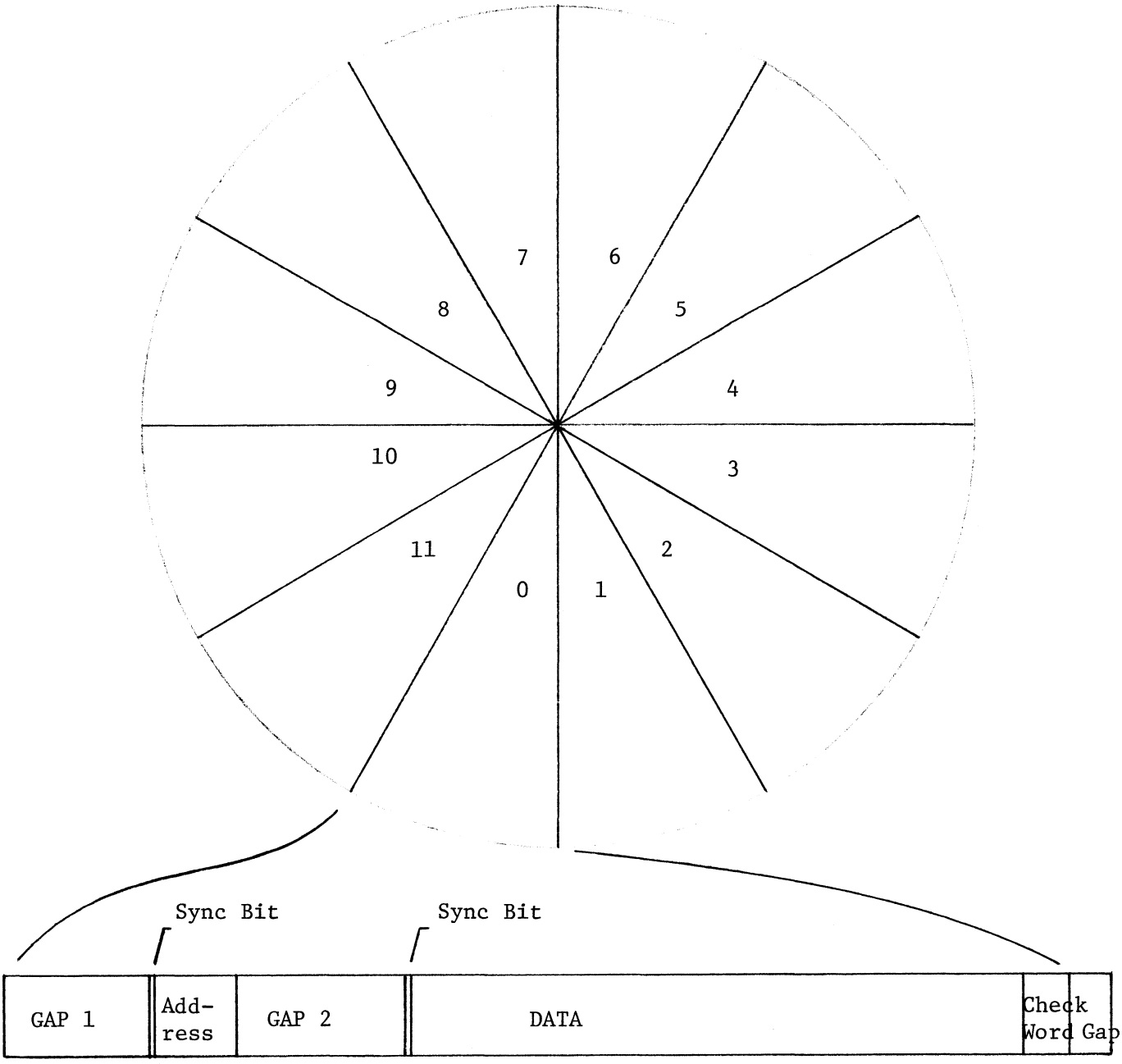
GAP 2 - SYNC BIT — Gap 2 consists of 18 usec of decision time for doing a write or read operation plus 120 usec of zero's data followed by a one-bit. As with Gap 1, the 120 usec of zero's permits the controller to synchronize itself with the read data during a read operation.

DATA - The data consists of a string of 4096 BITS (256, 16-bits words).

CHECKWORD - The error checkword or cyclic redundancy check (CRC) word is a 16-bit polynomial derived from the data written. During subsequent read operations this word is compared with a similar word derived from the data read. If the two words do not agree, data has been lost and an error is indicated.

GAP - This gap is comprised of all zero's and is required for accumulated disk tolerances.

SECTOR ORGANIZATION
FIGURE 4



Gap 1	=	23 words zeroes
Sync Bit	=	Single Data Bit (Start of Data)
Address	=	1 Word
Gap 2	=	22 Words Zeroes
Sync Bit	=	Single Data Bit (Start of Data)
Data	=	256 - 16 Bit Words
Check Word	=	1 Word
Gap	=	Zeroes till sector pulse.

3.2 PROGRAMMING

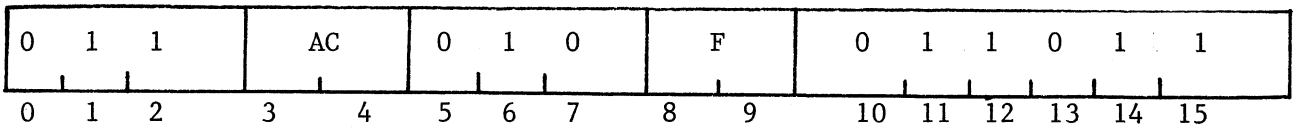
Before reading or writing, the program must give a seek command to position the heads at the desired cylinder; once the seek is done the program can then give a read or write command. Information the program must supply for a disc operation is the drive, cylinder, head and sector, the (two's complement) negative of the number of sectors to be processed, and an initial address (to the core address counter) for data channel access. In a single read or write, the hardware automatically counts from one sector to the next and from one surface to the next until the sector count is zero. However, data operations always stop at the end of a cylinder, and the program must reposition the heads to go on to the next cylinder.

The disc cartridge system has device code 33, mnemonic DKP, and uses all six of the I/O transfer instructions. Busy and Done are sensed by bits 8 and 9 in the I/O skip instructions. The Clear and Start functions control these flags in the usual fashion, but the I/O Pulse function (F=11) is also used. Interrupt disable is controlled by interrupt priority mask bit 7. A second controller connected to the bus would have device code 73.

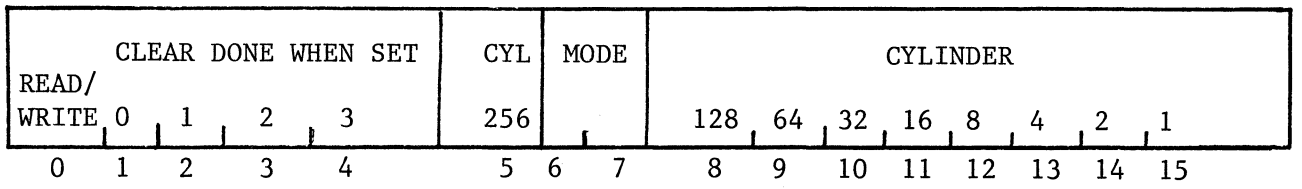
The clear function clears busy, done and the other flags in the controller, and terminates operations if the controller is currently processing data. Start and Pulse are both used to start disc commands, but the command is determined by the mode of the controller; in other words the program specifies a command by placing the controller in the appropriate mode and actually begins the command by giving Start or Pulse. When the seek or recalibrate mode is selected, the program starts the command by giving Pulse, as this function does not set Busy (although it does clear Done), hence while the heads are being positioned on one drive the control is free for a command on another. For Read or Write mode, the program gives Start to set Busy, and thus prevents the control from beginning any other command while processing data. An interrupt is requested as usual by the setting of Done, but there are also separate done flags that indicate the completion of a seek command in any drive or the completion of a Read or Write command in the drive currently selected by the controller. The setting of any Seek Done flag or the READ/WRITE Done flag requests an interrupt, and Read/Write Done also clears Busy and sets Done in the controller.

The I/O mnemonics code and description for each disk controller instruction are listed below:

DOA - DKP Data Out A, Disc Command Register



Clear the Done flags selected by one bits in AC bits 0-4 and select the mode and cylinder according to the contents of AC bits 5-15 as shown. Perform the function specified by F as explained above.



0-4 Clear the Done flags when set

6-7 These bits select the mode:

0-0 READ

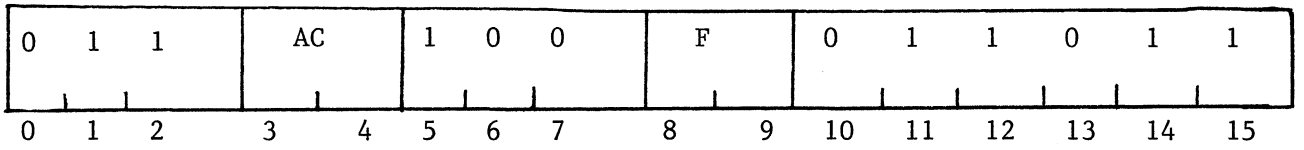
0-1 WRITE

1-0 SEEK - POSITION THE HEADS TO THE CYLINDER SPECIFIED BY BITS 8-15

1-1 RECALIBRATE - FORCE THE HEADS TO CYLINDER 0 INDEPENDENTLY OF THE HEAD-POSITIONING CIRCUITS

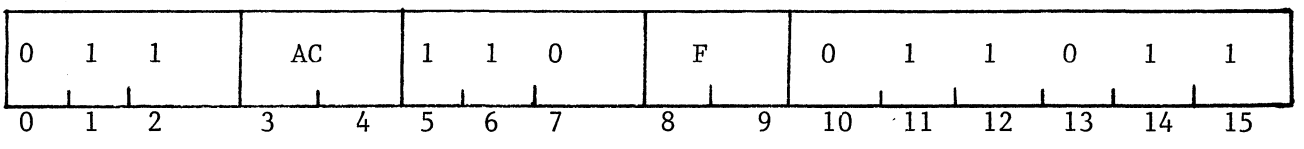
5, 8-15 CYLINDER ADDRESS SELECTION (630_8 MAXIMUM)

DOB - DKP Data Out B, Address Register



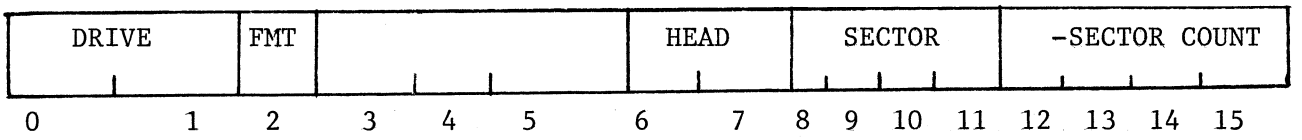
Load the contents of AC into the address counter (AC bit 0 should be 0), and perform the function specified by F as explained above.

DOC - DKP Data Out C



Select the drive, surface and sector, and the number of sectors to be

processed, according to the contents of AC as shown; perform the function specified by F as explained.



BITS

0-1 Select drive units as follows:

00 UNIT 0
01 UNIT 1
10 UNIT 2
11 UNIT 3

2 Modify Write operation to write address word in preamble. Formats Sector Header with word rqual to cylinder address Sector, and head contents.

6-7 Select head specified by binary representation of this field.

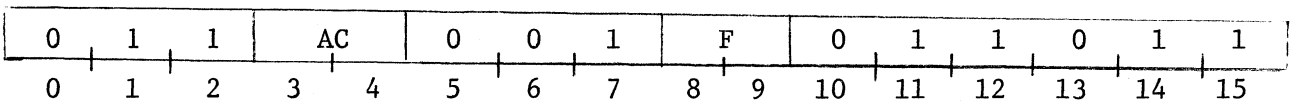
00 - HEAD 0
01 - HEAD 1
10 - HEAD 2
11 - HEAD 3

BITS 6-7 (3_8 MAXIMUM)

8-11 Select Sector to start a Read or Write operation.

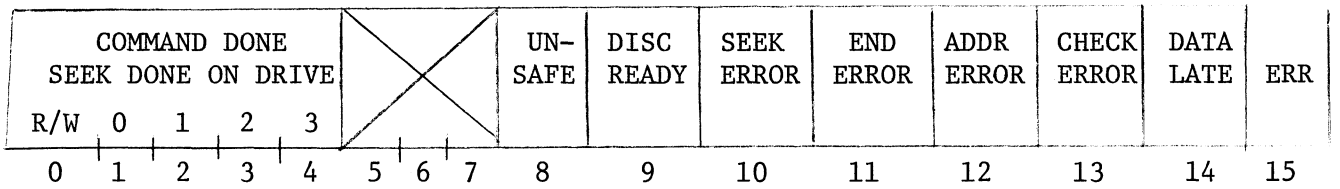
12-15 The 2's complement of the number of sectors to be processed by a Read or Write operation. (MAXIMUM: Sixteen)

DIA - DKP Data in A



Read the status of the disc system into AC as shown. (Perform the function specified by F.)

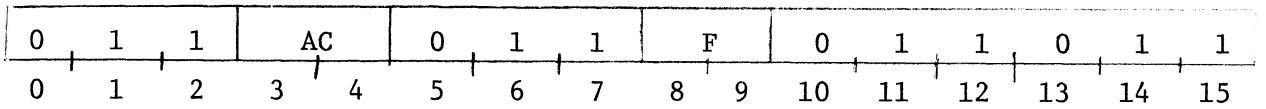
DIA Disc Status Register



The Clear function clears all of the done and error flags; Start and Pulse clear the error flags.

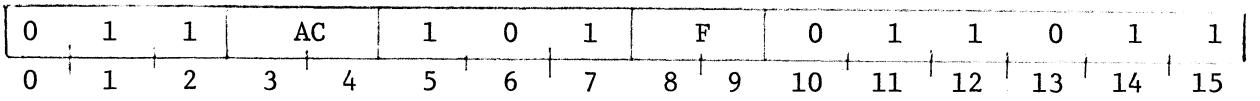
BITS	
0-4	A drive has completed a command as indicated by a 1's condition in these bit positions. The setting of any of these flags requests an interrupt.
8	Unsafe, the drive has a malfunction.
9	The selected drive is available to the program.
10	The selected drive failed to position heads as requested.
11	Controller has reached the end of cylinder, but the sector count is not zero.
12	Address Error - Header word does not compare with expected position.
13	The cyclic redundancy word read from disc does not compare to character computed by the controller for the data in the block.
14	The Data Channel failed to respond in time to a request for access.
15	The 'OR' condition of bits 8, 10, 11, 12, 13, 14 above.

DIB - DKP Data in B

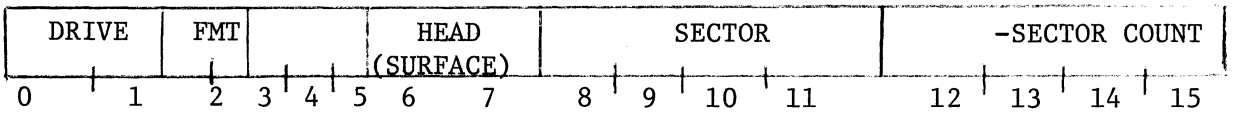


Read the present contents of the address counter into AC. (Perform the function specified by F.) At the end of a Write command, the address counter is 2 greater than the address of the last word written.

DIC - DKP Data in C, Disc Pack



Read the address status of the presently selected drive into AC as shown. (Perform the function specified by F.)



The normal programming procedure for operating a single drive is to give a DOC to select the drive, surface, sector and sector count, and then give a DIA to check whether the disc is ready (status bit 9). If it is, the program should give a DOAP to select the cylinder, and to select and initiate the Seek command. When the heads are properly positioned the drive sets its Seek Done flag requesting an interrupt. The program should respond with a DIA to check status bit 10, Seek Error, to ensure that the heads have positioned properly. A DOA is then given to clear Seek Done and select the Read or Write mode as desired. Finally a DOBS specifies the initial address and starts the Read or Write. For Write the controller immediately makes two data channel requests to fill two buffers before writing begins.

The controller waits until the drive encounters the selected sector on the selected surface, it then verifies the correct destination was achieved by comparing the 16 bit address written on the pack with the destination registers within the controller. If the addresses don't compare the Address

Error F/F sets, the Done F/F is set and the data transfer never starts. If the addresses compare the data block is processed making a pair of data channel requests whenever it has two words ready for memory in reading or both buffers are free in writing. As each sector is completed, the sector counter is incremented by one; and upon completing the final sector in the track, the head register is incremented by one while the sector counter is returned to zero, so the operation continues from surface to surface in the cylinder. For each sector, the controller also increments the sector count. When the sector count reaches zero the controller terminates the command (with the counters pointing to the last block processed) and sets Read/Write Done, which in turn clears Busy and sets Done requesting an interrupt.

The setting of the Data Late during a block indicates that information has been lost, but data transfers continue until the controller processes the entire block, at which time it terminates the command. At the completion of a data block in Write, the controller writes a computed check word at the end of the sector; in Read, the controller compares the check word read from the disc with one it has computed from the data read, and if they differ, sets Check Error and terminates the command. If the controller reaches the end of the cylinder (ie the end of the last sector on surface 3) and the sector count is not zero, the controller sets End Error and terminates the command.

Although the program can process data with only one drive at a time, it can position the heads on several drives simultaneously. After given a Seek for one drive, the program can select another and give a Seek for it. This means that the surface, sector and sector count information cannot be given when the drive is selected initially for seeking, and each time the program wishes to handle a particular drive it must reselect that drive. (eg. if several drives are seeking simultaneously and there is an interrupt, the program should give a DIA to determine which drive interrupted, then give a DOC to select that drive, and give another DIA to check Seek Error for that drive). To read or write, the program must give all three output commands, DOA, DOB and DOC to supply all the necessary information (the order of the instructions is not important, but Start should be given with the last of the three in order for the command to start properly.)

4.0 THEORY OF OPERATION

In the theory of operations section each sheet of the logic will be individually discussed.

SHEET 1 - COMPUTER IN BUS

Each receiver input is R/C filtered to improve noise margins and gated with Controller Selected or Data Channel Selected to ensure the proper device communication link is established. One shot H7 and F/F K9 provide logic that enables recalibrating disk heads when the computer reset switch is activated.

SHEET 2 - CONTROLLER SELECTION

Chip C2 monitors the Device Select lines (DSO-DS5) for a device code. D2-4 is true (+3V) when the disk controller is selected.

SHEET 3 - CORE ADDRESS REGISTER

A 15 bit register that contains the memory address. The register is parallel loaded by the Data Out B command and is incremented during data channel access by the Data Channel Out (DCHO) or Data Channel In (DCHI) commands. Chip P1 is used only when the controller is interfaced to a Diablo Series 30 Drive.

SHEET 4 - HEAD/SECTOR/DISK REGISTER

The logic contains 4 registers:

1. The Sector Count Register which contains the two's complement of the number of sectors to be used in a data transfer.

2. The Sector Number Register which contains the starting sector address.

3. The Head (surface) Register which contains the starting head address.

4. Disk Address Register which contains one of the four possible disk addresses.

The Registers are parallel loaded by the Data Out C command prior to the data transfer. At the end of every sector of data

transferred, the increment sector (INC SC) advances the Sector Count and Sector Number Registers. When transferring more sectors of information than on a surface, the head number is advanced when the last sector of a particular surface has been transferred. INC HEAD advances the head register and resets the sector number register.

SHEET 5 - DATA CHANNEL, BUSY/DONE

To present a Data Channel Request (DCHR) the Flag F/F B4-5) must be set. On a write operation the Flag F/F is initially set by the Start command and then for either a read or write command the Shift Done clocks the Flag F/F set and the Data Channel Acknowledge (DCHA), via the Req. 1 and Req. 2 F/F resets it. The Data Channel Request along with DCHA set the Data Channel Select F/F (D4-5) if the request is the highest priority. When Data Channel selection is established two 16 bit data request are made for each Data Channel Request. Req. 1 and Req. 2 F/F generate Clk B and Clk A to load the two 16 bit transfers.

The Busy F/F is set by Start and enables Done to be set by an error condition, format done or data transfer done. Done is cleared by Data Out A and Bit 0.

SHEET 6 - BIT/WORD COUNTER

The bit counter counts at the bit rate (400 NSEC) and the word counter counts at the word rate (6.4 USEC). Shift Done and Load become active every 2 words (32 bits) to respectively start the next Data Channel Request and load the write data. Format Done to active only during a format operation whenever 32 words have been written (23 zeros, 1 address and 8 zeros). INC SC is active during normal read/write operations to indicate 256 data words have been transferred and we need to go to the next sector to continue the data transfer.

SHEET 7 - DATA LATE, END OF CYLINDER, INCREMENT HEAD

The End of Cylinder F/F is set whenever we try to advance the head beyond head 3.

The Data Late circuitry ensures the computer supplies or receives data at an acceptable rate without losing data. Each Data Channel Request sets the Data Late enable F/F and each time the computer responds (INC CA) the F/F is cleared. If the F/F is not cleared by the shift done time the Data Late F/F will set indicating the computer did not respond in time.

The increment head O.S. increments the head register when we have completed reading or writing the 12th sector of a particular track. It also clocks the End of Cylinder F/F and if we have reached the last available head the End of Cylinder F/F will set.

This sheet also contains the error collection circuitry. The following error conditions will cause an error status:

1. CHECKWORD ERROR
2. SEEK ERROR FROM DRIVE
3. WRITE CHECK OR PROTECT FROM DRIVE
4. DATA LATE ERROR
5. ADDRESS ERROR
6. END OF CYLINDER

SHEET 8 - READ TIMING AND READ DATA CIRCUITRY

Before the data field in a sector is read or written, the address of that sector is checked to ensure proper orientation. The address check F/F is set by Sector Compare which indicates the desired sector and mechanical sector compare. The address check F/F triggers a 60 usec one-shot (A8-9 SYNC DELAY), which after the 60 usecs sets the Transfer Enabled F/F (D7-9). The first "ones" data (SYNC BIT) then sets the Xfer F/F (E8-5) in-

dicating the SYNC BIT has been found and the address (16 bits) is to follow. The address check F/F also triggers a 35 msec O.S. which delays activating read gate. After the address has been checked the address check F/F is cleared which triggers a 18 usec one-shot. When the 18 usec one-shot times out and a read operation is desired the 60 usec and the 35 msec one-shots are again triggered and the Xfer F/F starts looking for the SYNC bit. If it is a write operation the 18 usec one-shot would set the Write Enable F/F instead of triggering the 60 usec one-shot. Write will be discussed on Sheet 9.

The read data received by the controller must be in separated clock and data format. The Data F/F (A1-9) provides NRZ data which is used in the checkword generator, sector address verification and serdes circuitry.

SHEET - 9 WRITE TIMING AND DOUBLE FREQUENCY ENCODING

Before data on a sector is written the address must be verified. Once verified a 18 usec one-shot is triggered (read delay) and when it times out sets the Write Enable F/F (A9-5). The setting of the Write Enable F/F triggers a 120 usec one-shot. During this 120 usec, an all zeros data pattern is written on the disk. At the end of the 120 usec the SYNC bit F/F sets and the SYNC bit is written. Following the SYNC bit, 256 computer words of data from serdes (sheets 14 and 15), the checkword generator and the tolerance gap are written. The tolerance gap is an all zeros data pattern, following the checkword until the next sector pulse.

The heart of the write timing is a 20MHZ crystal ascillator. This ascillator is logically gated to produce two 100 nsec pulse trains of a 400 nsec period. The two pulse trains are displaced 200 nsec from each other and form logic terms State 1 and State 3. The Double Frequency Encoding is performed by these States with clocks being written at State 1 time and data being written at State 3 time.

SHEET 10 - ATTENTION LATCHES, COMMAND DECODE

The attention latches indicate when a drive has completed its seek operation. There are four attention latches supporting four disk drives. Any attention latch set or a Read/Write operation done (CTLR Done) will set the Interrupt Request F/F (G3-9) providing the mask interrupt F/F (G3) is not set.

The attention logic levels from the drive may be either negative (0V) or positive (+3V) attentions. Via a switch either attention polarity can be accommodated.

S4 closed = Positive attention
S4 open = Negative attention

The command decode logic decodes and holds data bits 6 and 7 on a Data Out A command.

6	7	
0	0	READ
0	1	WRITE
1	0	SEEK
1	1	RECALIBRATE

J1000 Installed for Odd Device Codes and Removed for Even Device Codes

SHEET 11 - SECTOR COMPARE, CRC GENERATOR, CHECKWORD ERROR

The sector compare logic samples at each sector pulse if the desired sector and the actual (mechanical) sector are equal. If they are, the Sector Compare F/F will set.

The CRC (Cyclic Redundancy Character) is used in both write and read operations. The CRC is used to verify the 256 word data field transferred correctly. On a write operation the write data is clocked through the CRC generator and the contents of the generator are appended at the end of every data field. On a read operation the read data is clocked through the CRC generator. When the previously written CRC is read it is checked against what the CRC generator predicted. Any deviation and the Checkword Error F/F sets.

SHEET 12 - TIMING GENERATION, DATA DONE, ADDRESS CHECK DONE.

Various clocks and strobes are generated on this sheet.

CW STB - Strobe for Checkword Error F/F

CLOCK SHIFT - Clock Serdes

CHK CHAR - Strobes CRC to be appended to the write data

STROBE CHK CHAR - Clocks CRC Generator

STROBE CYL - Clock Physical Address Register and Address Error F/F

BIT COUNT - Clocks bit/word counters

The Data Done Counter (E12) counts when the Data Done F/F (D12) is set. The Data Done F/F is set by the INC. SC logic term, indicating we have read 256 data words and that the next 16 bits will be the CRC. When the Data Done Counter (E12) overflows Read Gate is removed.

The Address Counter (C12) counts during the address portion of a data record. Since the address is 16 bits in length the Address Check Over F/F (D12) will be set following the sixteenth data bit indicating we should have read the address.

SHEET 13 - PHYSICAL ADDRESS REGISTER

This register stores the desired cylinder, head, and sector information. This same information is written on the disk at each sector when the pack is formatted. Before the data field is written or read the Physical Addrdss Register is compared with the physical address written on the disk. If they compare the data in the data field is transferred. If they don't compare, an Address Error status is posted and the data transfer is stopped.

SHEET 14, 15 - SERIALIZER/DESERIALIZER (SERDES)

On a write operation the Serdes logic converts the 16 bit parallel data transfers from the computer and transforms it into the serial format required by the disk drives.

On a read operation the Serdes logic converts the serial data from the disk drives into the 16 bit parallel format required by the computer.

SHEET 16, 17 - BUS-IN ASSEMBLER

Six signals gate data unto the data bus.

1) DATIA - DRIVE AND CONTROLLER STATUS
2) DATIB - CONTENTS OF THE CORE ADDRESS REGISTER
3) DATIC - DRIVE, HEAD, SECTOR, SECTOR COUNTER REGISTER INFORMATION
4) DCHI - PARALLEL READ DATA TO THE COMPUTER
5) DCHA - CONTENTS OF THE CORE ADDRESS REGISTER
6) INTA - DEVICE ADDRESS

SHEET 18 - DISK DRIVE TRANSMITTERS

The disk drive transmitters are gated with a voltage monitor circuit that prevents logic transients during power up and power down.

Switch S3, when closed, will position the heads to track zero whenever an I/O RESET command occurs. This switch should be open when running the diagnostics.

Switch S1, when closed, allows selection of only the fixed disk.

J1822 Installed for 10 MBYTE Drives
J1823 Installed for 2.5 MBYTE Drives

SHEET 19 - ADDRESS ERROR/START SEEK

The Address Error F/F is set by either

1) A sector pulse occurs during an address check.
2) Data read from the address portion of a record does not compare with the physical address register (Sheet 13).

Switch S2 when closed prohibits detections of address errors. The Start F/F holds the Start command until the drive unit is ready. This logic allows the computer operator to do a program load before the disk unit is ready and when the unit becomes ready the system will automatically load.

The Start Seek F/F is set whenever the program initiates a seek or recalibrate command and stays set until Address Acknowledge is received from the disk drive or the 90 USEC One Shot times out. The Start Seek F/F is the TRACK ADDRESS STROBE (TAS) to the disk drive, which loads the drive cylinder address register.

SHEET 20 - 2.5/10 MEGABYTE CONVERSION

Multiplexors M12, D11, and F9 provide the status and timing multiplexing required to convert the controller from interfacing with 10 megabyte drives to 2.5 megabyte Diablo Series 30 drives.

5.0 INTERFACE

5.1 COMPUTER INTERFACE

	Signal	Backpanel Pin
	CLR	A50
	DATA 0	B62
	DATA 1	B65
	DATA 2	B82
	DATA 3	B73
	DATA 4	B61
	DATA 5	B57
	DATA 6	B95
	DATA 7	B55
	DATA 8	B60
	DATA 9	B63
	DATA 10	B75
	DATA 11	B58
	DATA 12	B59
	DATA 13	B64
	DATA 14	B56
	DATA 15	B66
	DAT1A	A44
	DAT1B	A42
	DAT1C	A54
	DAT0A	A58
	DAT0B	A56
	DAT0C	A48
	DCHA	A60
	DCHI	B37
	DCHMO	B17
	DCHO	B33
*	DCHP IN	A94
*	DCHP OUT	A93
	DCHR	B35

	Signal	Backpanel Pin
	$\overline{\text{DS0}}$	A72
	$\overline{\text{DS1}}$	A68
	$\overline{\text{DS2}}$	A66
	$\overline{\text{DS3}}$	A46
	$\overline{\text{DS4}}$	A62
	$\overline{\text{DS5}}$	A64
	INTA	A40
*	$\overline{\text{INTP IN}}$	A96
*	$\overline{\text{INTP OUT}}$	A95
	$\overline{\text{INTR}}$	B29
	IOPLS	A74
	IORST	A70
	$\overline{\text{MSKO}}$	A38
	$\overline{\text{RQENB}}$	B41
	SELB	A82
	SELD	A80
	$\overline{\text{STRT}}$	A52

*For the two pairs of priority-determining signals, the IN signal comes from the processor or the preceding device; the OUT signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), jumper Pin A93 to A94 and A95 to A96 to maintain bus continuity.

5.2 DISK DRIVE INTERFACE

Signal (to Disk)	Backpanel Pin
$\overline{\text{SELECT FILE 0}}$	A81
$\overline{\text{SELECT FILE 1}}$	B13
$\overline{\text{SELECT FILE 2}}$	A85
$\overline{\text{SELECT FILE 3}}$	A88
DISK SELECT	B11
HEAD SELECT	A83
$\overline{\text{TRACK ADDRESS 1}}$	A89
$\overline{\text{TRACK ADDRESS 2}}$	A84
$\overline{\text{TRACK ADDRESS 4}}$	A87
$\overline{\text{TRACK ADDRESS 8}}$	A91
$\overline{\text{TRACK ADDRESS 16}}$	A63
$\overline{\text{TRACK ADDRESS 32}}$	A73
$\overline{\text{TRACK ADDRESS 64}}$	B31
$\overline{\text{TRACK ADDRESS 128}}$	A71
$\overline{\text{TRACK ADDRESS 256}}$	B19
$\overline{\text{TRACK ADDRESS STROBE}}$	A86
$\overline{\text{RESTORE}}$	A77
$\overline{\text{WRITE GATE}}$	B23
$\overline{\text{WRITE DATA AND CLOCK}}$	B27
$\overline{\text{READ GATE}}$	B15

Signal (from Disk)	Backpanel Pin
$\overline{\text{DRIVE UNIT READY}}$	B34
$\overline{\text{SEEK ERROR}}$	A79
$\overline{\text{WRITE CHECK}}$	B53
$\overline{\text{READ CLOCK}}$	A61
$\overline{\text{READ DATA}}$	A59
$\overline{\text{ATTENTION DEV 0}}$	B48
$\overline{\text{ATTENTION DEV 1}}$	B49
$\overline{\text{ATTENTION DEV 2}}$	A78
$\overline{\text{ATTENTION DEV 3}}$	A76

Signal (from Disk)	Backpanel Pin
$\overline{\text{SECTOR PULSE}}$	A49
$\overline{\text{SECTOR BIT 1}}$	B38
$\overline{\text{SECTOR BIT 2}}$	B51
$\overline{\text{SECTOR BIT 4}}$	B69
$\overline{\text{SECTOR BIT 8}}$	B67