Model 120

Mag Tape Controller

181-T22-FF1-01

REVISION HISTORY		
ECO #	DATE	DESCRIPTION
0112	3/29/83	Changed Page 2-2
0328	6/28/84	New ZETACO Cover

CUSTOMER SERVICE

Our warranty attests the quality of materials and workmanship in our products. If malfunction does occur, our service personnel will assist in any way possible. If the difficulty can not be eliminated by use of the following service instructions and technical advise is required, please phone the Custom Systems sales department (612-941-9480) giving the serial number, board name, model number, and problem description. You will be placed in contact with the appropriate technical assistance.

PRODUCT RETURN

Pre-return Checkout.

If controller malfunction is suspected, the use of test software is needed to determine if the controller is the problem and what in particular is wrong with the controller. The tests applicable to this board are listed on the next page of the manual. Please run the test sequence before considering product return.

Returned Material Authorization.

Before returning a product to Custom Systems for repair, please ask our sales secretary for a "Returned Material Authorization" number. Each product returned requires a separate RMA number. Use of this number in correspondence and on a tag attached to the product will ensure proper handling and avoid unnecessary delays.

Returned Material Information.

Information concerning the problem description, system configuration, diagnostic program name, revision level, and results, i.e., error program counter number should be included with the returning material. A form is provided for this information on the next page of the manual.

Packaging.

To safeguard your materials during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to Custom Systems, Inc. for repair. This will: 1) Determine if in fact the board is defective (many boards returned for repair are not defective, causing the user unnecessary system down-time, paper work, and handling while proper testing would indicate the board is working properly). 2) Increase the speed and accuracy of a product's repair which is often dependent upon a complete understanding of the user checkout test results, problem characteristics, and the user system configuration. Checkout results for the NRZI Mag Tape Controller should be obtained by performing the following tests. (Include error program counter #'s and accumulator contents if applicable).

TEST	RESULTS
Data General Mag Tape Diagnostic	
Data General Reliability Test	

Other tests performed:

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this sheet with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain).

   _____

2. What operating system are you running under? (AOS RDOS, DDOS, DTOS).

   _____

3. Describe the system configuration (i.e., peripherals, I/O controllers, model of computer, etc.

   _____

   _____

4. Has the controller been returned before? _____ Same problem?_____

To be filled out by CUSTOMER:

Model #: _____

Serial #: _____

RMA #: _____

Returned by:_____
(company name)

TABLE OF CONTENTS

1.0 GENERAL DESCRIPTION

The Series 120 Magnetic Tape Controller is physically located on one printed circuit board assembly which is mounted within the Data General minicomputer. (Reference Figure 1) The Magnetic Tape Controller can be plugged into any spare slot available within the minicomputer. The electrical position of the Magnetic Tape Controller is between the Processor and the Tape Transport. The Series 120 Magnetic Tape Controller features Data Verification Logic in the form of the following check circuitry:

1. Vertical Parity Check.
2. Vertical Parity Generator.
3. Longitudinal Parity Check.
4. Cyclic Redundancy Check Character Generator.

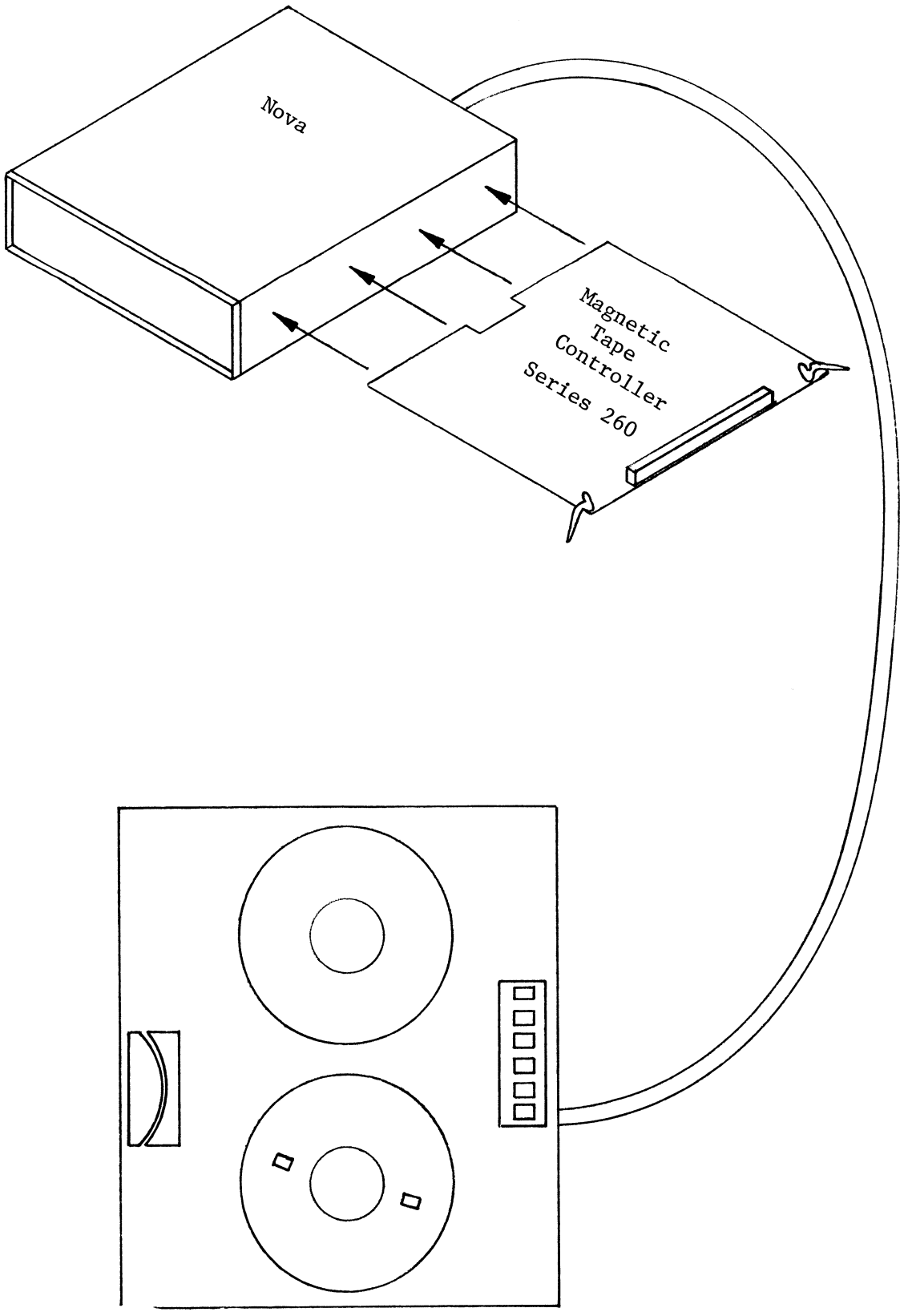
The Magnetic Tape Controller is used to synchronize and control a maximum of four separate tape transports. The Magnetic Tape Controller is able to accommodate 9-track, 800 bpi tape units with different operational speed characteristics (12.5 ips to 75 ips) with the normal operational constraints which allow only one operation (either a read, write or space operation) to be performed in any one tape unit at a time. The Magnetic Tape Controller can be operated with a wide variety of industry compatible tape transports, and these may also be intermixed on any one tape controller. Double buffered data storage registers facilitate the smooth transfer of data between high speed tape units and the I/O data channels.

The Magnetic Tape Controller is capable of odd or even parity mode of operation, which is selectable within the Magnetic Tape Controller under program control. In accordance with the standard recording format, 9-track tapes are written only in odd lateral parity (for binary data). In addition to the lateral parity bit, 9-track tapes are verified in the longitudinal direction by the inclusion of a longitudinal parity check character (LPCC) written as the last character before the inter-record gap and a cyclic redundant check character (CRCC), which is recorded midway between the last data character and the LPCC.

NO TEXT OR FIGURES TO APPEAR ON

THIS PAGE

BASIC
MAGNETIC TAPE SYSTEM



Tape Control Status Registers are provided in the Magnetic Tape Controller to store information defining error conditions and operational status. The Status Registers can be monitored to simplify error recovery operations performed under program control.

The Magnetic Tape Controller contains the standard BUSY and DONE Logic indicators along with the routine program interrupt facilities. The Magnetic Tape Controller can request servicing in any of the three following ways:

1. The Tape Controller can be programmed to produce an interrupt upon the completion of any commanded operation,
2. The program can sense the status of the BUSY and DONE lines to determine when a command operation has been completed; or
3. The program can monitor the tape unit READY bit of the Status Register.

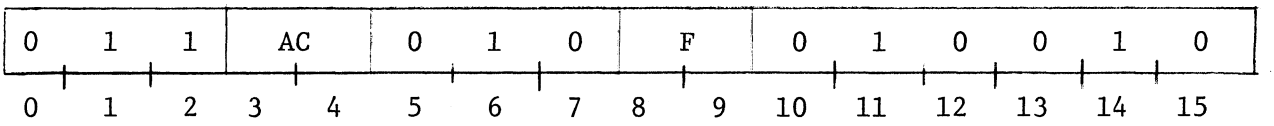
The programmed interrupt method of service is generally used as this type of servicing is most readily compatible with the queuing of any data requests that may be present. The Tape Controller may also interrupt in the event an illegal command was given. In this case, the interrupt will occur with the error status bits set in the Status Register.

The Device Selection Code for the Magnetic Tape Controller is octal 22. If a second Tape Controller is subsequently added to the same processor, it is assigned the Device Selection Code of octal 62.

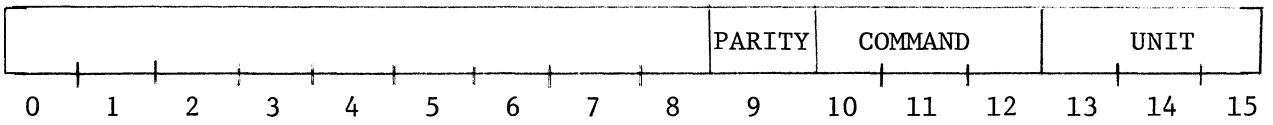
The Tape Controller uses all of the I/O instructions except the DATIC instruction. BUSY and DONE are sensed by bits 8 and 9 in the I/O skip instruction. The CLEAR function (F=10) clears BUSY and DONE and also clears the Command Register and the status flags in the control. START (F=01) clears DONE, sets BUSY, clears many of the flags and places the control and the selected transport in operation. INTERRUPT DISABLE is controlled by Interrupt Priority Mask bit 10.

The I/O mnemonics code and description for each tape control instruction are listed below.

DOA - MTA Data Out A, Magnetic Tape



Load the contents of AC bits 9-15 into the Tape Command Register as shown and perform the function specified by F.



9 0 selects odd parity, 1 selects even.

10-12 These bits select the command as follows. (See Table 1 for expanded definition of each command).

0 Read
1 Rewind
2
3 Space Forward
4 Space Reverse
5 Write
6 Write End of File
7 Erase

13-15 Numbers 0-7 address Transports 0-7.

Table 1

TAPE COMMANDS

To perform any operation, the program must select the unit while giving a command, and all commands are initiated by giving START. The REWIND commands do not actually place the Controller in operation, but for all other commands START clears DONE and sets BUSY. At the termination of the command the control clears BUSY and sets DONE, requesting an INTERRUPT if the MASK INTERRUPT F/F is clear.

WRITE. The program must specify parity, a (negative) word count and an initial address. If the Write Protect Ring is installed, START sets ILLEGAL and DONE and the controller does not go into operation. Otherwise, the control makes an immediate data request for the first word, and it writes the words it receives via the data channel from the locations specified by the address counter until either the word counter overflows or DATA LATE sets, at which time the control terminates the record and sets DONE.

WRITE END OF FILE. The program must specify odd parity for a 9-track tape or the controller will not write a file mark properly. If Write Protect is true, START sets ILLEGAL and DONE and the controller does not go into operation. Otherwise, the controller erases 2½ inches of tape (i.e., it extends the present record gap to 3 inches, writes a file mark and then sets DONE).

ERASE. If Write Protect is true, START sets ILLEGAL and DONE and the controller does not go into operation. Otherwise, the controller erases 2½ inches of tape and then sets DONE. This command is used primarily to skip sections of tape on which the program has found it impossible to write data correctly. i.e., without parity errors or a bad tape indication.

READ. The program must specify parity, a (negative) word count and an initial address. The controller reads a single record from tape and sends the data via the data channel to the locations specified by the address counter until it encounters the EOR gap or the word counter overflows, whichever occurs first. Giving a large word count (e.g., giving zero) ensures that the entire record will be read even if its length is unknown. If the record contains an odd number of data characters, the final one is sent to memory

in the left half of a separate word. The setting of DATA LATE during the record indicates that information has been lost, but data transfers continue until overflow or the record ends. After completing the record, the Controller sets DONE.

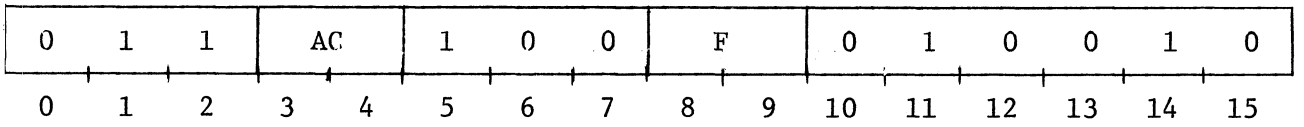
If the record read is a file mark, its single "data" character is sent to memory via the data channel. The length of a record of unknown size can be determined after it is read by giving a DIB to check the contents of the address counter, which will be one greater than the address to which the last word in the record was sent (provided, of course, the word count was large enough).

SPACE FORWARD. The program should give a (negative) word count equal to the number of records to be spaced. The controller spaces forward over the given number of records unless it encounters a file mark or the end of tape, in which case it stops at the mark or at the end of the record in which the EOT marker is encountered. To space a file of up to 4096 records, the program can simply give a zero word count.

SPACE REVERSE. The program should give a (negative) word count equal to the number of records to be spaced. If load point is true, START sets ILLEGAL and DONE and the controller does not go into operation. Otherwise, the controller spaces reverse over a given number of records, but it stops the tape automatically upon encountering a file mark or the load point. To space a file of up to 4096 records, the program can simply give a zero word count.

REWIND. START does not affect the Controller but simply initiates the REWIND in the addressed transport and the controller is free for further use by the program. The addressed transport rewinds the tape at high speed onto the supply reel and stops at load point.

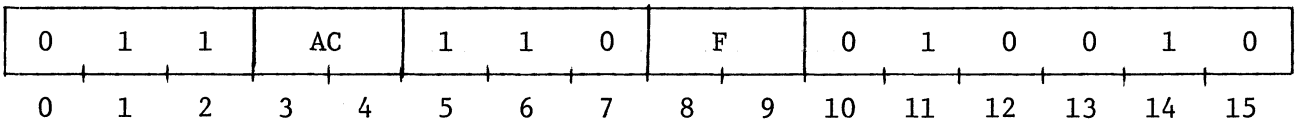
DOB - MTA DATA OUT B, MAGNETIC TAPE



Load the contents of AC bits 1-15 into the address counter (AC bit 0 should be 0) and perform the function specified by F.

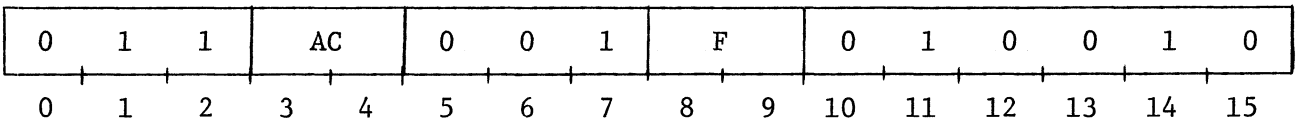
NOTE: If this instruction is given with a 1 in AC bit 0 and if the control then executes a READ command in which the word counter does not overflow, the control reads the CRC at the end of the record and sends it to the next memory location specified by the address counter. This is primarily for maintenance, for the program to check whether the CRC is being generated properly.

DOC - MTA DATA OUT C, MAGNETIC TAPE



Load the contents of AC bits 4-15 into the word counter and perform the function specified by F.

DIA - MTA DATA IN A, MAGNETIC TAPE



Read the status of the tape system into AC as shown and perform the function specified by F.

ERROR	DATA LATE	REWIND	ILLEGAL	HIGH DENSITY	PARITY ERROR	END OF TAPE	END OF FILE	LOAD POINT	9 TRACK	BAD TAPE	SEND CLOCK	FIRST CHAR	WRITE LOCK	ODD CHAR	UNIT READY
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bits 11 and 12 are for maintenance only. START clears ERROR, DATA LATE, PARITY ERROR, END OF FILE and BAD TAPE. CLEAR clears these plus ILLEGAL. The remaining flags are supplied by the addressed transport (which is automatically unit 0 after CLEAR is given).

0 Bit 1, 3, 5, 6, 7, 8, 10 or 14 are true.

1 The data channel has failed to respond in time to request for access.

2 The addressed transport is now rewinding.

3 This bit sets if the program gives START when any of the following conditions holds:

--The command is WRITE, ERASE or WRITE END OF FILE and WRITE LOCK (bit 13) is true.

--The command is SPACE REVERSE and Load Point (bit 8) is true.

--BUSY is false and Tape Unit Ready (Bit 15) is also false.

The setting of ILLEGAL prevents the tape controller from going into operation and sets DONE, requesting an INTERRUPT if the INTERRUPT DISABLE F/F is clear. The program must give CLEAR before proceeding.

4 The addressed transport is set to high density. The Controller only handles high density (800 bpi). This status is held high within the Controller.

5 In READ or WRITE, the controller has encountered a data character whose lateral parity differs from that specified with the command or has discovered a track with odd parity the length of the record. Incorrect parity in a CRC or LPCC does not set this bit, but specifying the wrong parity when reading a file mark does.

6 The addressed tape is beyond the EOT marker. (Reverse motion clears this bit).

7 The controller has written a file mark or has encountered one in reading or spacing. If there is an error in a file mark, it is not recognized as such; i.e., the controller interprets it as a very short data record.

8 The addressed tape is at load point.

9 The addressed transport handles 9-track tape. The Controller only handles 9-track tape. This status is tied high within the Controller.

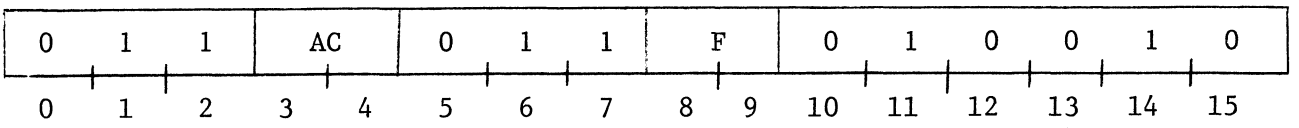
10 The controller has encountered either data in a record gap or a false end of record (two or more continuous blank characters). Spacing reverse over an unrecognized file mark also sets BAD TAPE.

13 The Write Enable Ring is not in the supply reel on the addressed transport.

14 An odd number of characters were detected while reading or writing.

15 The addressed transport is ready for operation by the program.

DIB - MTA DATA IN B, MAGNETIC TAPE



Read the present contents of the address counter into AC bits 1-15 and perform the function specified by F. Clear AC bit 0.

2.0 TAPE FORMAT

The Custom Systems Tape Controller writes 9-track, NRZI, 800 bpi tapes only. A data record consists of data and error checking characters. Every data character consists of the 8-bit data byte plus a parity bit that is generated by the controller to conform with odd or even parity as specified by the program. Every character is in either a data record or a file mark. A block of words from memory to the controller is represented by the data bytes in a record taken together. The controller separates adjacent records by automatically erasing a segment of tape to form a record gap between them. The controller always stops the magnetic tape in a record gap.

The maximum record length is 4096 words (or 8192 data characters). In writing, the controller divides the words into two data bytes. In reading the bytes are reassembled. Figure 3 represents the manner in which the data is disassembled on a WRITE or reassembled on a READ.

NINE-TRACK FORMAT

FIRST CHARACTER								SECOND CHARACTER							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 3

In 9-track format, each word is written as two 8-bit characters. After the last line of a record is written, the controller writes three blank lines, a Cyclic Redundancy Character (CRC), three blank lines and a Longitudinal Parity Check Character (LPCC). (Reference Figure 4).

The LPCC (always odd) produces even longitudinal parity in each of the tracks along the length of the tape. Minimum record gap is 0.6 inch. Reading or writing, the controller checks to ascertain that the lateral parity of every data line agrees with that specified by the program and that every track has even longitudinal parity.

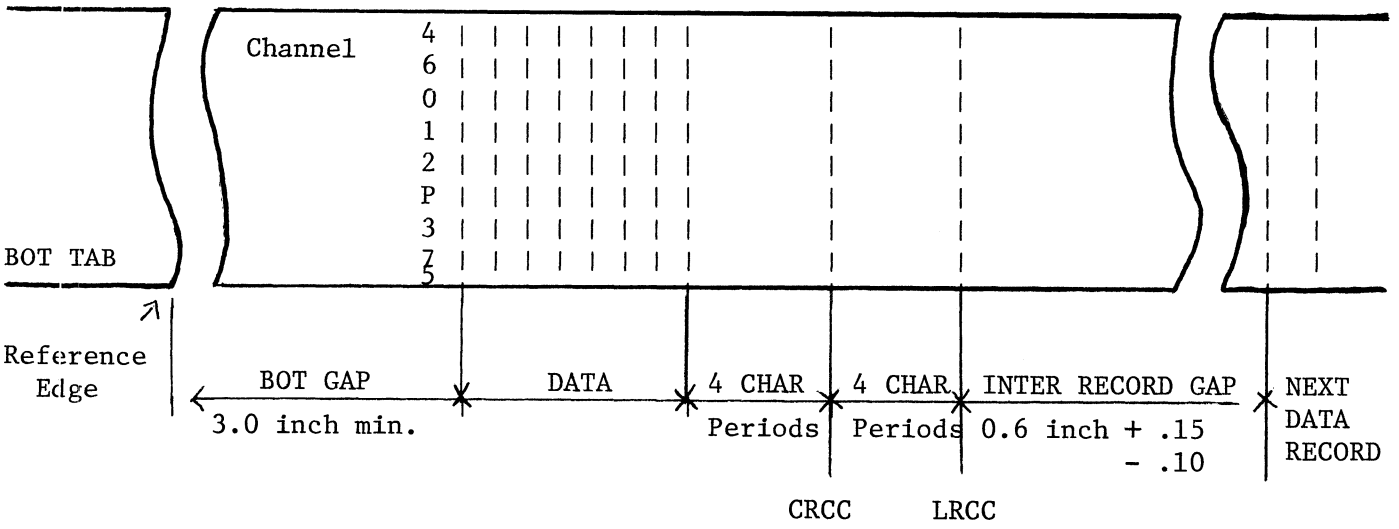
Care must be taken to avoid words containing a zero data byte in 9-track recording format. A zero data byte would be read as a missing character (blank line). No words beyond that point would reassemble correctly.

The program can group sets of data records into files. The end of a file is indicated by a File Mark. The File Mark is a special record containing one special data character and its LPCC. A SPACE command automatically terminates when a File Mark is detected.

The ends of all tapes contain reflective strips that are detected by photo cells in the transport. The Load Point marker is located at least ten feet in from the beginning of the tape and constitutes the logical beginning of tape (BOT). REVERSE commands stop automatically at this marker. At least three inches of tape intervene between BOT and the first record.

EOT, or end-of-tape reflective strip, is located at least 14 feet from the end of the tape. The program should not record more than a few feet beyond EOT, leaving at least ten feet of the tape for trailer. A status bit indicates when the tape is beyond EOT, but this condition only stops the tape automatically when it is spacing forward.

FORWARD MOTION (HEAD RELATIVE TO TAPE)



NOTES:

1. Tape shown with oxide side up.
2. Channels 0 through 7 contain data bits in descending order of significance.
3. Channel P (parity) always contains odd data parity.
4. Each bit of the LRCC is such that the total number of "1" bits in that track (including the CRCC and the LRCC) is even. In the 9-track format. the LRCC will never be an all-zeroes character.
5. A file mark is a single character record having "1" bits in channels 3, 6 and 7 for both the data character and the LRCC. The CRCC contains all zeroes. This record is separated by 3.5 inches from the previous record and by a normal IRG (0.6 inch) from the following record.
6. Data packing density is fixed at 800 bits per inch.

Figure 4

3.0 INSTALLATION

3.1 CARD INSTALLATION

This section provides detailed information for installing the Custom Systems Series 120 Magnetic Tape Controller.

Inspect the controller board for any in-transit damage. Contact the carrier and Custom Systems if any damage is discovered, specifying the nature and extent of the damage.

Reference Figure 5 to insure the controller addressing is correct.

Reference Figure 6 to insure speed setting of the tape controller is appropriate for your tape drive(s).

Install the controller in any spare slot on the bus after the CPU, memory and I/O boards.

Install priority jumpers to the tape controller and around any unused card slots.

Jumper Pin A94 (DCHPIN) to Pin A93 (DCHPOUT).
Pin A96 (INTPIN) to Pin A95 (INPOUT).

Reverify all your connections before applying power to the computer or tape drives.

3.2 CABLING

Custom Systems provides the necessary cabling to connect the magnetic tape unit to the computer. The cabling is of a single piece construction which plugs directly on the computer backpanel at one end and directly to the tape drive unit at the other end.

A. Connection at the Computer End

The connection at the computer end is made directly to the computer backpanel via connector blocks. Align the labels on the connectors with the respective pins on the computer backpanel.

B. Connection at the Magnectic Tape Drive End
(Reference Figure 7)

Three connectors are present at the tape drive end of the cable. They are labeled

J1 or J16 = Control Cable

J3 or J6 = Read Cable

J2 or J1 = Write Cable

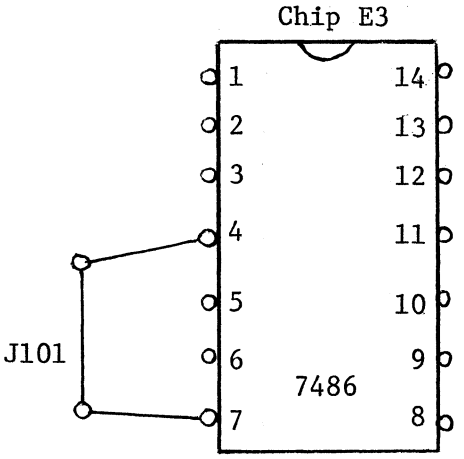
Control Cable
J16 = WANGCO
J1 = Kennedy
J101 = Cipher

Read Cable
J6 = WANGCO
J3 = Kennedy
J103 = Cipher

Write Cable
J1 = WANGCO
J2 = Kennedy
J102 = Cipher

Connect these three cable connectors to the tape drive ensuring correct cable mating (ie read cable (J6) connects to the read cable input point of the tape drive).

CONTROLLER ADDRESSING 22/62



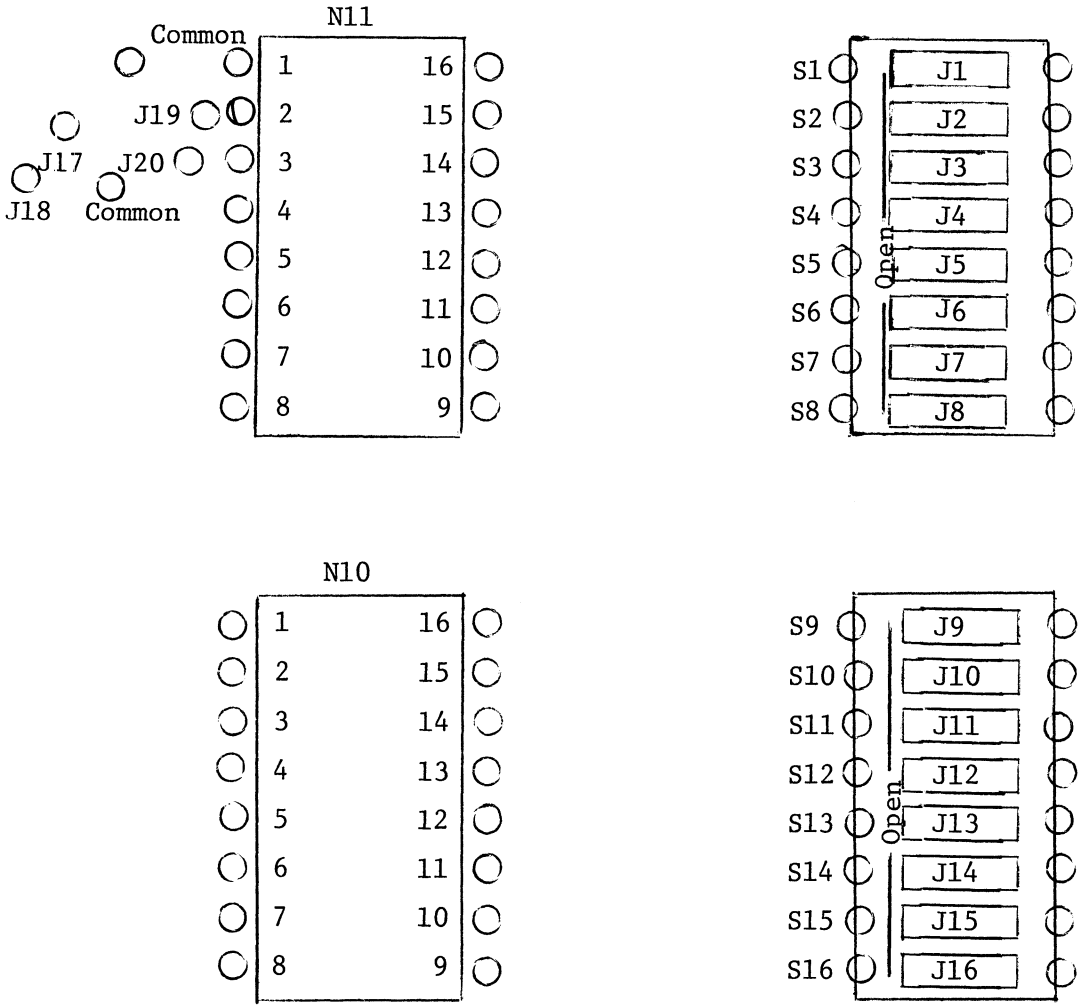
J101 Installed = Address 22

J101 Cut = Address 62

J101 is a foil jumper

Figure 5

TAPE CONTROLLER SPEED



TAPE SPEED	SWITCHES CLOSED
12.5 ips	S2, S3, S6, S7, S10, S11, S14, S15, J18, J20
25 ips	S2, S3, S6, S7, S10, S11, S14, S15, J17, J19
37.5 ips	S1, S4, S5, S8, S9, S12, S13, S16, J17, J19
45 ips	S2, S4, S5, S8, S10, S11, S13, S16, J17, J19
75 ips	S1, S3, S6, S8, S9, S11, S14, S16, J17, J19

Figure 6

MAG TAPE CONTROLLER INSTALLATION

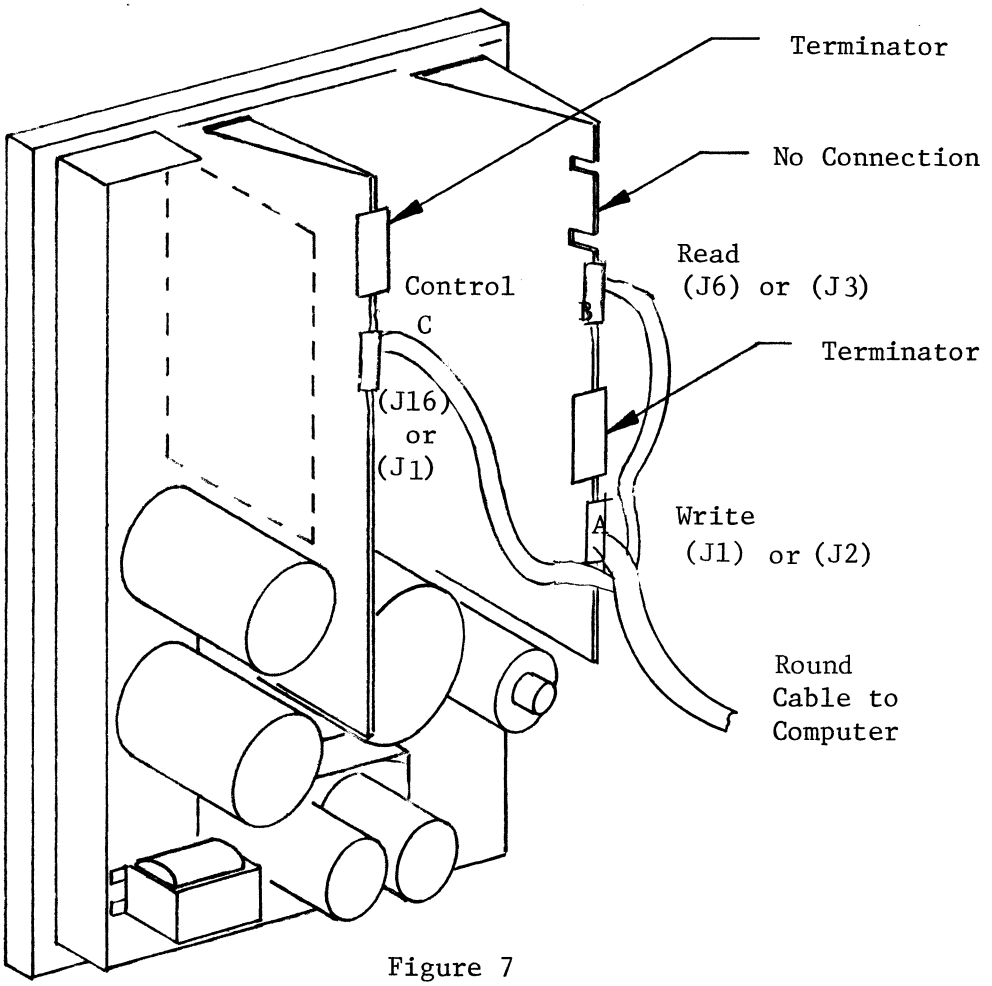


Figure 7

Ensure your particular tape drive has ERASE gated with WRITE gate; i.e., reference Figure 8 for Wangco Model 1045).

Run diagnostic and reliability programs if available.

Install the Jumper from RR to SS on the Transport Control Board as shown on the drawing below:

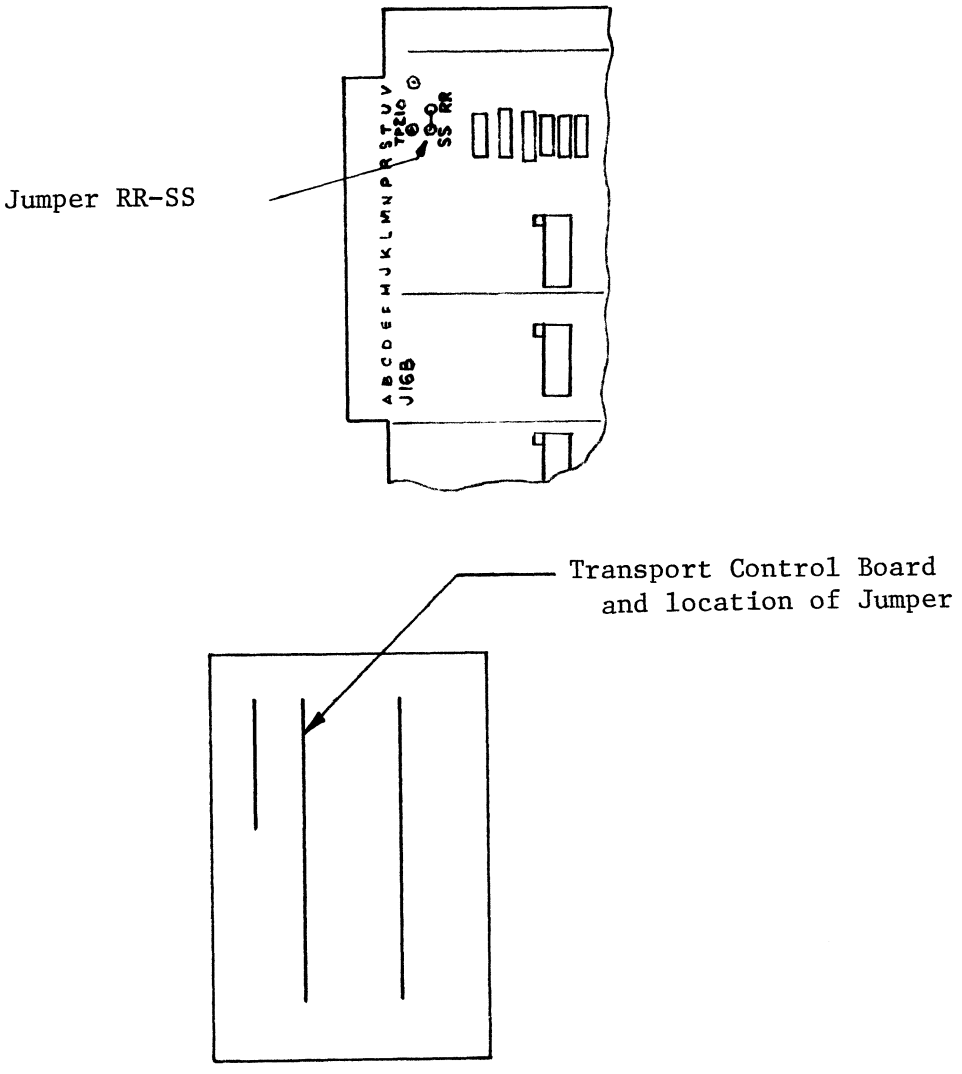


Figure 8

4.0 THEORY OF OPERATION

In the Theory of Operations section, the Tape Controller is subdivided into small sections. Each section will be discussed separately and then tied together by discussing a WRITE/READ operation.

4.1 MAIN OSCILLATOR AND TAPE SPEED SELECTION (Sheet L04)

The Main Oscillator is a crystal-controlled series resonant oscillator and operates at 3.072 MHZ (period = 325.5 NSeC). The main oscillator provides all of the timing required by the Tape Controller.

The 3.072 MHZ signal is buffered by N12-6, which provides clock pulses to the Tape Speed Selection Counters N10,N11. (Reference installation instructions for jumper options for the various tape speeds).

N11-4 receives its clock pulses from N12-6 (J17) except for 12½ ips tape speeds. It then receives the clock pulses from P1-5(J18).

N10-13provides clock pulses at the character transfer rate to another set of counters M12 and L12. These counters provide a clock ($\overline{\text{DLYCT}}$) to the gap timing counters (J12, H12) which control timing of the inter-record gap. N11-2 (N11-3 for 12½ ips) supplies a clock to shift register J9. This register provides three consecutive clock pulses (DLY 1, DLY 2, DLY 3) every character time and provides the timing requirements of a WRITE operation.

4.2 WORD COUNTER (Sheet L02)

The Word Counter is comprised of chips N4, M4 and K4 (chip G4 is for special application). These counters hold the negative word count of the number of 16-bit words to be transferred. $\overline{\text{DATOC}}$ command loads bits 4-15 and each DCHO (WRITE) or DCHI (READ) or BUMP (SPACE) increment the word counter. When the counter overflows, K4-7 goes low ($\overline{\text{ENDB}}$) setting the word count overflow F/F (M8-5). The setting of the word count overflow F/F prevents further data channel transfers.

4.3 ADDRESS COUNTER (Sheet L02)

The Core Address Counter is comprised of chips N3, L4, J4 and H4. These counters hold the memory address used in data channel transfers. $\overline{\text{DATOB}}$ command loads bits 1-15 and each DCHO (WRITE) or DCHI (READ) increment the address counter.

4.4 CONTROLLER SELECTION (Sheet L02)

The Controller Selection logic monitors device selection lines DS0-DS5. When DS0-DS5 = 22_8, chip D3-6 is true enabling communications with the Tape Controller. If jumper J101 is cut, the controller address becomes 62_8.

4.5 DIRECTION CONTROL AND GAP TIMING (Sheet L04)

All the tape commands except REWIND and SPACE BACK move tape in the forward direction. Tape motion can only occur if the GO F/F sets. The GO F/F (G12-5) is set by the $\overline{\text{START}}$ command if the command is not REWIND or the ILLEGAL F/F is not set.

The ILLEGAL F/F is set by START if any of the following three conditions are true:

1. WRITE or ERASE command and the WRITE ring is removed.
2. SPACE BACK command and at the beginning of the tape.
3. BUSY and TAPE UNIT READY are false.

When the GO F/F sets, SFC (H11-8) goes true for all forward commands, and SRC (H11-3) goes true for the SPACE BACK command. SFC and SRC are gated directly to the tape unit and control the tape motion.

The setting of the GO F/F sets the START DELAY F/F (G129) which initializes the gap timing counters J12 and H12. These counters are used to establish the inter-record gap and position the heads within the inter-record gap upon stopping tape motion. The START DELAY F/F is reset by the gap timing counters timing out (DLY-OV). The resetting of the START DELAY F/F enables

the controller to accept read data or start writing data, depending upon the command issued.

The GO F/F is reset by the setting of the STOP F/F (A12-9) or $\overline{\text{DELAY}}$ on an ERASE command. The STOP F/F is set by one of the following conditions.

1. SPACE BACK command and tape positioned at the beginning of tape.
2. Inter-record gap found following READ or WRITE record command.
3. File mark found during spacing command.
4. Desired number of records encountered during a spacing command.

4.6 END OF RECORD DETECT AND CHARACTER COUNTER (Sheet L04)

To find the inter-record gap, several things must be validated:

First: Verify that three data characters have been read from the tape.

Second: Verify that the missing characters are not the product of a defective tape.

The first three Read Strobe Pulses (RDS) will sequentially step the character counter (B11). The primary function of this counter is to remember that three data characters have been read from the tape.

A two-stage counter, RED1 and RED2, (C9) is used to detect the inter-record gap in the following manner. Each DLY1 pulse increments the two-stage counter. However, each Read Strobe (RDS) resets the counter and on a one-for-one pulse basis the counter never progresses beyond a count of one. When a gap occurs, RED1 and RED2 will both be set (3 missing characters) and product an $\overline{\text{ERF}}$ signal (D9-8). This $\overline{\text{ERF}}$ signal indicates a possible inter-record gap has been found. $\overline{\text{ERF}}$ starts the gap timing counters, and when the counters time out (DLYOV) and if $\overline{\text{ERF}}$ is still active (no additional RDS pulses), the STOP F/F sets and tape motion is halted (clears GO F/F).

With the 9-track format, the controller will sense the inter-record gap before the CRCC. A character (CRCC) read after the first missing three characters will cause the character counter to reset. The next Read Strobe (LPCC) will set the first character in the character counter. If a second data character is received, the RESET ERF F/F (L9-5) will set and in turn set the BAD TAPE F/F (L9-9). The output of the BAD TAPE F/F enables bit 10 to the Bus-In Assembler.

4.7 FILE MARK DETECT (Sheets L03 and L04)

A file mark is a single character record having "1" bits in channels 3, 6 and 7 for both the data character and the LRCC. The CRCC contains all zeroes.

On Sheet L03, EOF C (K9-6) goes true when only bits 3, 6 and 7 contain data. Since there are only two characters in a file mark (one data and one LPCC), the first $\overline{\text{EOF}}$ F/F (F12-5) sets on the first character and $\overline{\text{EOF}}$ F/F (F12-9) sets on the second character (Sheet L04). Tape motion is always halted if a file mark occurs with the end-of-file status available as bit 7 to the Bus-In Assembler.

4.8 READ CHAIN (Sheet L03)

The Read Chain is comprised of the Read Data Receivers, the Read Registers and the Parity Checker Circuitry.

Read Data enters the Tape Controller as eight bits of data (a character), one parity bit and a read strobe. The parity bit is not a usable data bit but is used in the Parity Checker.

The first character of the data is parallel loaded into registers E5 and K7 by the first (odd) Read Strobe $\overline{\text{(CLKBF)}}$ The second character along with the first character are parallel loaded into registers F5, H5, K5 and M5 by the second (even) read strobe. Data is now ready for input into the computer. At this time, a Data Channel Request Sequence is started, and the Read Data is strobed over to the computer by the DCHI signal. This procedure continues until the word counter overflows or an interrecord gap is encountered.

As previously mentioned, the parity bit is used in the Parity Checker

Circuitry. Each character is processed through the Vertical Parity Generator (chip K8) and the Longitudinal Parity Generator (chip L8).

The Vertical Parity Generator output should be low at each character time to indicate odd parity was achieved. If the Vertical Parity Generator is high at the character time, the PARITY ERROR F/F (D4-5) will set.

The data continues to be clocked into the Longitudinal Generator and is checked only after the DATA, CRC and LPCC characters have been received. Chip L8-9 being high at this time indicates a parity error and in turn will set the PARITY ERROR F/F (D4-5).

4.9 WRITE CHAIN (Sheet L03)

The Write Chain is composed of two ranks of Write Registers, Data Multiplexers, Vertical Parity Generator, CRC Generator and Write Data Transmitters.

Write Data (16 bits) is parallel loaded into the first rank of the Write Registers (G6, L6, J6 and N6) by the DCHO signal (OUTDT). Data is then parallel loaded into rank two by the $\overline{\text{SDATF}}$ signal which also starts a new data transfer request to the computer. Multiplexers F7 and J7 essentially divide the 16-bit word into two 8-bit words. The first 8-bit word is from data bit 0-7 and the second 8-bit word from data bit 8-15. Each 8-bit word is applied to the Vertical Parity Generator (G8) which provides a parity bit if the total number of bits in the 8-bit word is even. Each 8-bit word is also loaded into the CRC Generator (H8). The CRC is appended to the record four character times after the last character of data. Multiplexers G7 and H7 control the write data going to the tape drive, selecting either data from the Write Registers or data from the CRC generator.

4.10 WRITE OPERATION (Reference Figure 9)

The first step is for the computer to establish contact with the Magnetic Tape Controller. The controller is selected by the computer issuing device code 22_8 (62_8 for second controller), which is decoded in the controller to produce a controller select signal (D3-6). The controller select signal enables a communication link between the computer and the controller.

Next, the computer would issue a DATOB command and load the core address registers and a DATOC command and load the word count registers.

After the word count and core address registers are loaded, the computer would issue a DATOA command, selecting the operation to be performed (WRITE, READ, ERASE, SPACE, REWIND) and the tape unit to perform the specified operation. Next, the computer should read the status registers, via a DATIA command, to verify the tape transport is ready (indicated by bit 15). If the selected transport is ready, the computer can issue a I/O instruction with a START function; e.g. NIOS.

The $\overline{\text{START}}$ signal generates a CLRAL signal (D5-8 and A10-4) which clears out the controller functional F/F and registers preparatory to the start of the actual operation. The $\overline{\text{START}}$ pulse sets the GO F/F which actually transmits the FORWARD and REVERSE commands to the tape unit to start the tape moving. The START pulse also sets the BUSY F/F (M7-9), if not a REWIND command. The setting of BUSY enables the DONE F/F (M7-5) to become set when the TAPE UNIT READY (TUR) signal becomes true when the WRITE operation has been completed.

START is also gated with WRITE to set the DATA FLAG F/F (L11-5). The DATA FLAG F/F set output synchronizes the DATA CHANNEL REQUEST F/F (A3-5) with the REQUEST ENABLE (REQUEN) I/O BUS signal. The output from the DATA CHANNEL REQUEST F/F causes the DATA CHANNEL REQUEST (DCHR) line to the computer to become active, requesting WRITE data.

In response to the DCHR pulse the processor will send back a DCHA pulse which will allow the data channel select (DCH SEL) to become set. The set output from the DCH SEL F/F disables the DCHMO line because a write operation is present. DCHA is gated with DCH REQ to produce a $\overline{\text{ENADX}}$ signal which clears the data flag F/F. DCHA also places the current address on the data channel bus. This information plus the high state of DCHMO specifies the memory location data is to be fetched from for the write operation.

The processor will enable the DCHO line when data is ready for transfer to the tape controller. DCHO produces an increment pulse for the word count register and the core address register. DCHO also produces OUTDT which gates the 16 bits of write data into the first rank of the write registers.

At this point in time the tape is coming up to speed and the timing of the interrecord gap is continuing. When the gap timing counters time out the write enable F/F sets and along with logic term DLY1 form $\overline{\text{SDATF}}$. $\overline{\text{SDATF}}$ loads rank two of the write registers and write data starts to flow to the tape unit. The $\overline{\text{SDATF}}$ pulse also set the data flag F/F which starts another data channel request cycle for the next 16 bit data word.

If the tape unit is a dual gap (separate read and write heads) unit, the written data will start to enter the read chain, and will be checked for proper parity.

The data channel request cycles continue until the word count register overflows indicating that we have written the desired number of words. The CRC/LRCC timing network takes over now and writes the CRC 4 character times after the last data word and an additional 4 character times later the write reset pulse occurs creating the LRCC.

As previously mentioned the written data enters the read chain. When the read chain circuitry detects the last data word it presets a timing value in the gap timing counters. When the gap timing counter times out it sets the stop F/F which in turn clears the go F/F which drops the forward command to the tape drive. When tape motion has stopped TUR becomes active and sets the Done F/F. The write operation has been completed and the tape head is positioned in the middle of the interrecord gap.

5.0 INTERFACE

5.1 COMPUTER INTERFACE

Signal	Backpanel Pin
CLR	A50
$\overline{\text{DATA 0}}$	B62
$\overline{\text{DATA 1}}$	B65
$\overline{\text{DATA 2}}$	B82
$\overline{\text{DATA 3}}$	B73
$\overline{\text{DATA 4}}$	B61
$\overline{\text{DATA 5}}$	B57
$\overline{\text{DATA 6}}$	B95
$\overline{\text{DATA 7}}$	B55
$\overline{\text{DATA 8}}$	B60
$\overline{\text{DATA 9}}$	B63
$\overline{\text{DATA 10}}$	B75
$\overline{\text{DATA 11}}$	B58
$\overline{\text{DATA 12}}$	B59
$\overline{\text{DATA 13}}$	B64
$\overline{\text{DATA 14}}$	B56
$\overline{\text{DATA 15}}$	B66
DATIA	A44
DATIB	A42
DATIC	A54
DATOA	A58
DATOB	A56
DATOC	A48
$\overline{\text{DCHA}}$	A60
$\overline{\text{DCHI}}$	B37
$\overline{\text{DCHMO}}$	B17
DCHO	B33
*$\overline{\text{DCHP IN}}$	A94
*$\overline{\text{DCHP OUT}}$	A93
$\overline{\text{DCHR}}$	B35

Signal	Backpanel Pin
$\overline{\text{DS0}}$	A72
$\overline{\text{DS1}}$	A68
$\overline{\text{DS2}}$	A66
$\overline{\text{DS3}}$	A46
$\overline{\text{DS4}}$	A62
$\overline{\text{DS5}}$	A64
INTA	A40
*$\overline{\text{INTP IN}}$	A96
*$\overline{\text{INTP OUT}}$	A95
$\overline{\text{INTR}}$	B29
IORST	A70
$\overline{\text{MSKO}}$	A38
$\overline{\text{RQENB}}$	B41
$\overline{\text{SELB}}$	A82
$\overline{\text{SELD}}$	A80
STRT	A52

*For the two pairs of priority-determining signals, the IN signal comes from the processor or the preceding device, the OUT signal goes to the next device. If the computer is operated with an interface board removed (or a slot is not used), jumper pin A93 to A94 and A95 to A96 to maintain bus continuity.

5.2 MAGNETIC TAPE INTERFACE

	Signal	Backpanel Pin
Control & Status	$\overline{\text{SELECT 0}}$	A69
	$\overline{\text{SELECT 1}}$	A71
	$\overline{\text{SELECT 2}}$	A65
	$\overline{\text{SELECT 3}}$	A67
	$\overline{\text{FORWARD}}$/STOP	A78
	$\overline{\text{REVERSE}}$/STOP	A76
	$\overline{\text{REWIND}}$	A73
	$\overline{\text{WRITE ENABLE}}$	A63

	Signal	Backpanel Pin
Control & Status (Cont.)	FILE PROTECT STATUS	A47
	BOT STATUS	A49
	EOT STATUS	A84
	READY STATUS	A81
	REWIND STATUS	A57
Write Data	WRITE DATA STROBE	A86
	WRITE RESET	A85
	WRITE DATA PARITY	A90
	WRITE DATA 0	B6
	WRITE DATA 1	B11
	WRITE DATA 2	B13
	WRITE DATA 3	B15
	WRITE DATA 4	B19
	WRITE DATA 5	B23
	WRITE DATA 6	B25
	WRITE DATA 7	B27
	LOW READ THRESHOLD	A87
Read Data	READ STROBE	B54
	READ DATA PARITY	B67
	READ DATA 0	B53
	READ DATA 1	B52
	READ DATA 2	B51
	READ DATA 3	B49
	READ DATA 4	B38
	READ DATA 5	B36
	READ DATA 6	B34
	READ DATA 7	B31