NOVA 4/X I/C's

25509 1048		
AY-3-1015 1234	1	
2901 1073	4	
2910 1074	3	
301 207	1	
339 479	2	
MK4116P-3 1100	64	
555 173	1	
723 094	1	
728-002	1	
4747 416	2	
8406 133	1	
7427 260	1	
7486 ~~448~~ 068	1	
74LS02- 1020	1	
74LS05 - 798	2	
74LS08 595	1	
74LS29 -	1	
74LS74-476	2	
74LS93-	1	
74LS158-~~1250~~ 1211	3	
74LS161-581	2	
74LS164-1231	4	
74LS194 580	1	
74LS244-1253	1	
74LS373-~~1279~~ ~~1375~~	8	
74LS377-~~1277~~ 1266 ~~1004~~	2	
74LS390-1232	2	
74S00 156	3	
74S02 ~~366~~ (366)		
74S04 159	4	
74S05 188	2	
74S08 - 537	5	
74S09 - 1529	1	
74S11 237	1	
~~74S14 096~~	1	
74S15-259	1	
74S17-	1	
74S20 249	1	
74S22 174	2	
74S30 -1045	1	
74S32-180	4	
74S37 472	2	
74S38-779	3	
74S51-504	2	
74S64 182	1	
74S74- 300	11	
74S86- 365	1	
74S112- ~~1772~~	13 172	
74S113 160	1	
74S138 223	6	
74S139 185	1	
74S153 166	11	
74S158-1211	1	
74S161-1524	5	
74S182-170	1	1080N
74S240-1522	~~1~~	
74S241-1521	18	
74S251- 165	6	
74S253-~~1373~~ 1355	2	
74S260-305	5	
1046N 74S373-1018	2	
74S374-1019	39	
74S375-1265	1	
74S399 -	1	
75150- 146	1	
75451- 625	2	
75452 -626	1	
93422-1497	4	
93S46 - 540	3	
DG		
641	14	
74LS299	1150	
74LS14	576	

D3-4702-9-795

AM

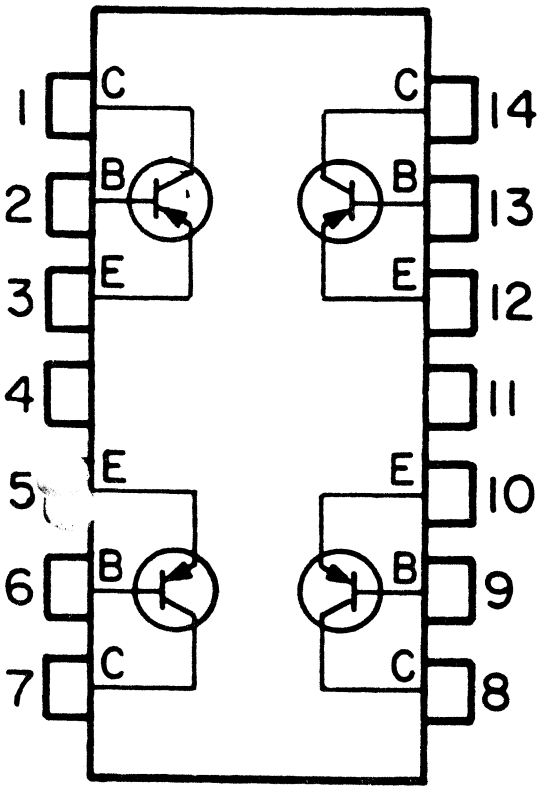
74S240

74S241

100000001

PNP Quad Core Driver

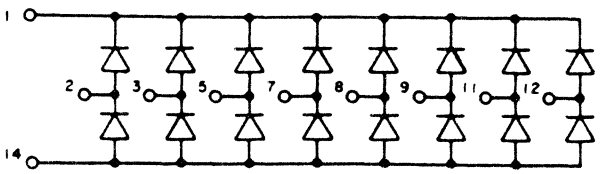
PIN CONFIGURATION



100000002

16 Diode Array

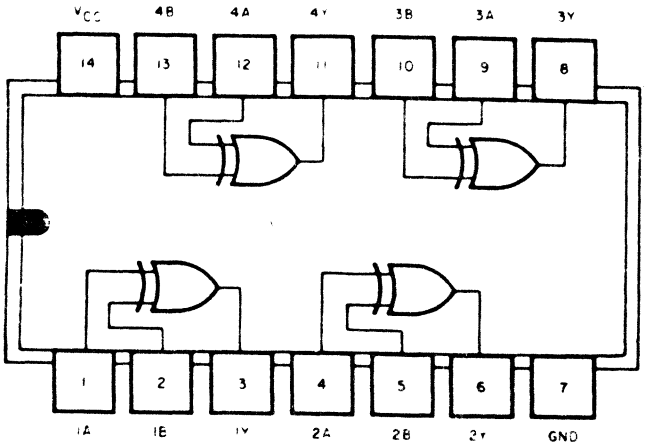
LOGIC DIAGRAM



100000068

Quad 2-Input Exculsive-OR Gate

PIN CONFIGURATION

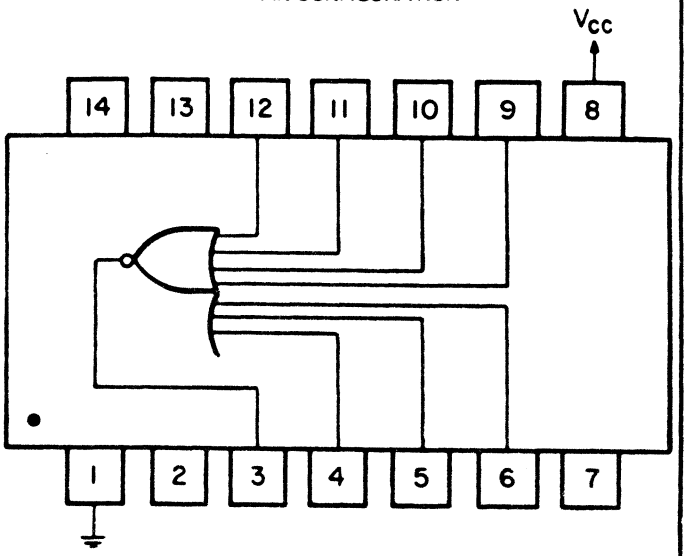


Positive logic: $Y = A \oplus B$

100000069

Single 7-Input NOR Gate

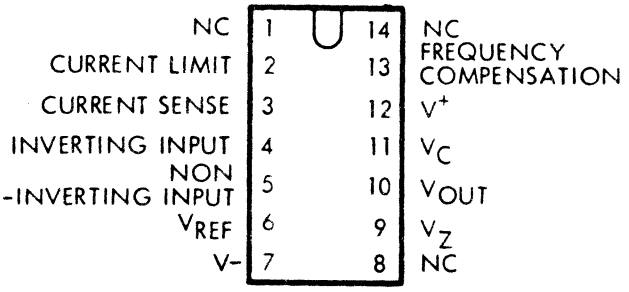
PIN CONFIGURATION



100000094

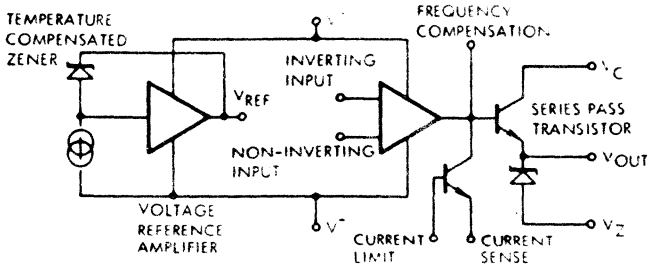
Precision Voltage Regulator

PIN CONFIGURATION



The 1000000094 is a precision voltage regulator consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

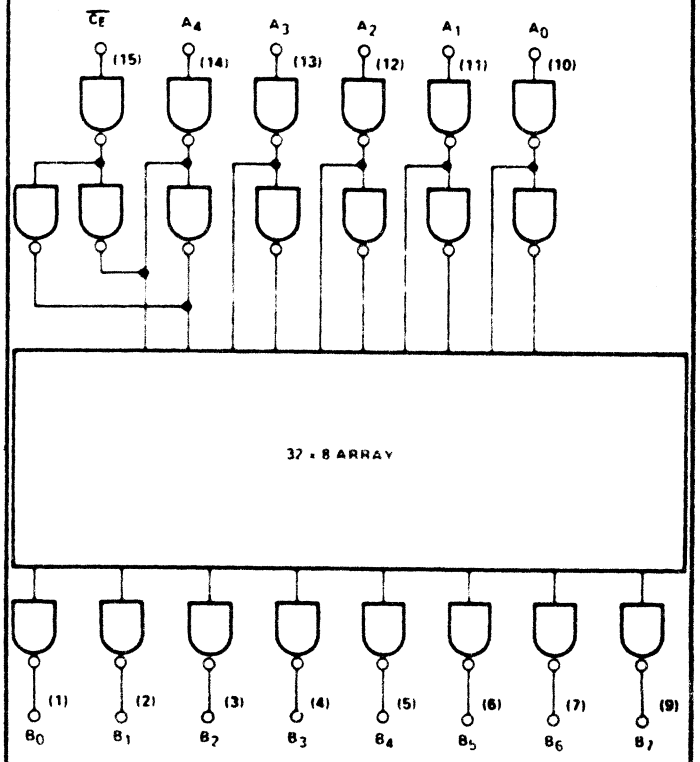
Equivalent Circuit



100000095 and 100000096

256-Bit Bipolar ROM

LOGIC DIAGRAM



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

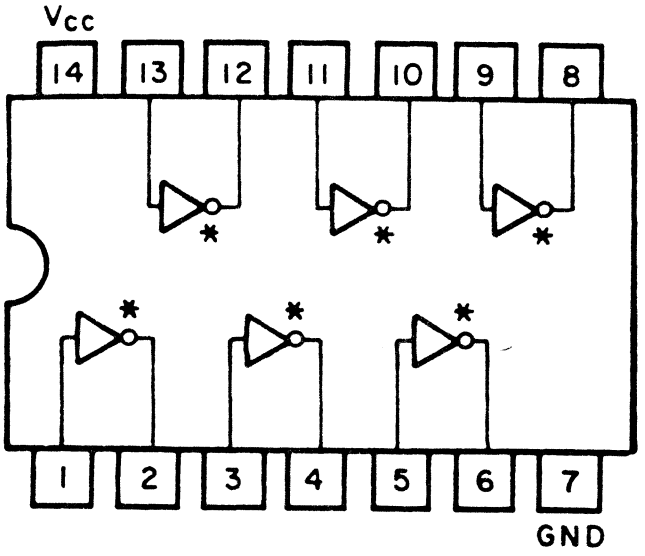
These TTL 256-bit read only memories are organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Enable input is taken high.

The 100000095 and 100000096 are fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-AND operation with the outputs of other TTL or DTL devices.

100000133

Hex Inverter

PIN CONFIGURATION



DIP (TOP VIEW)

*Open collector

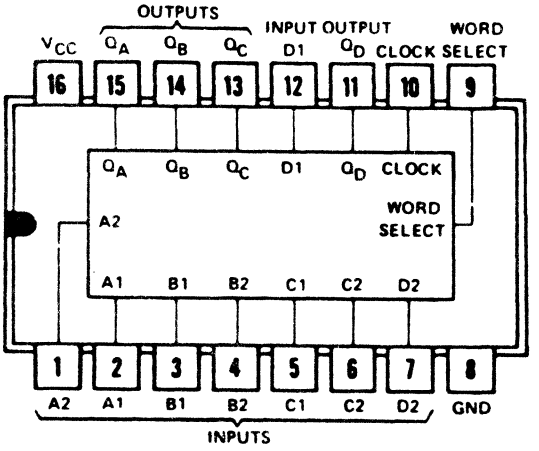
V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: $Y = \overline{A}$

100000134

4-Bit Data Selector/Storage Register

PIN CONFIGURATION



V_{CC} = Pin 16
Gnd = Pin 8

Positive logic: word select low for word 1, word select high for word 2.

This monolithic data selector/storage register is composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer and six inverter/drivers.

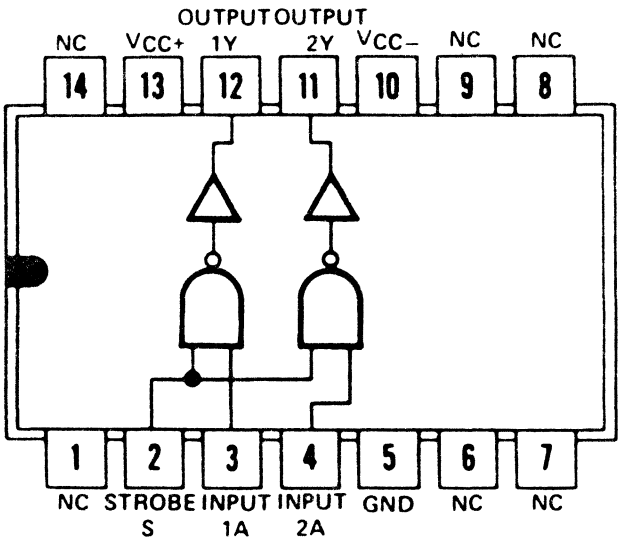
When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

NOTE *The 100000134 is a low power TTL device.*

100000146

Dual Line Driver

PIN CONFIGURATION



V_{CC+} = Pin 13

V_{CC-} = Pin 10

Gnd = Pin 5

NC = No Internal Connection

Positive logic: $Y = \overline{AS}$

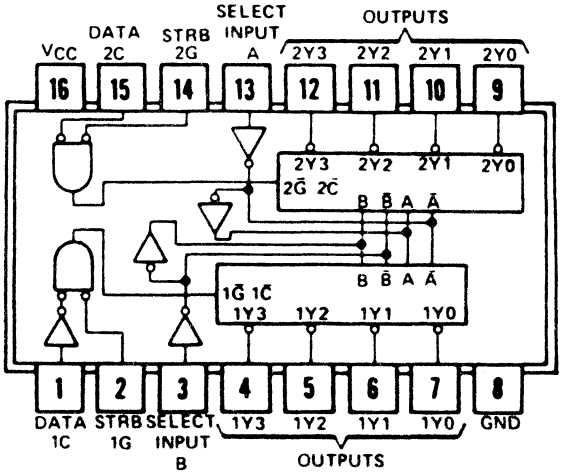
This device is a monolithic dual line driver which satisfies the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C.

A rate of 20,000 bits per second can be transmitted with a full 2500pF load.

100000147

Dual 2-Line-To-4-Line Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

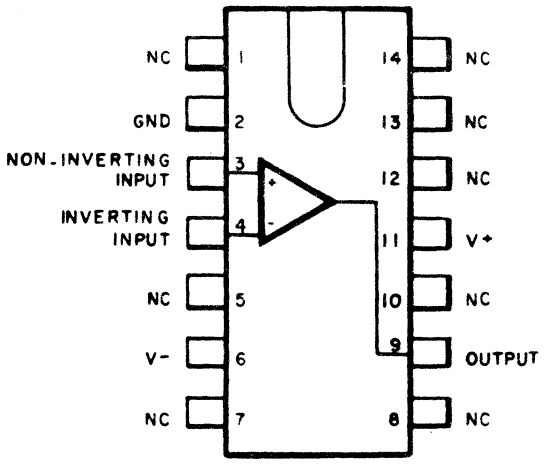
Inputs				Outputs			
Select		Strobe	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

100000157

High Speed Differential Comparator

PIN CONFIGURATION

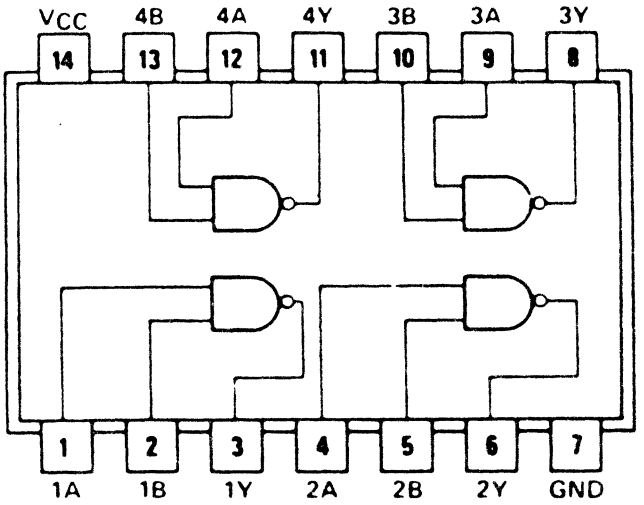


The 100000157 is a differential voltage comparator intended for applications requiring high accuracy fast response times. Constructed on a single silicon chip, the device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier, or a high-noise immunity line receiver.

100000158

Quad 2-Input Positive-NAND Gate

PIN CONFIGURATION



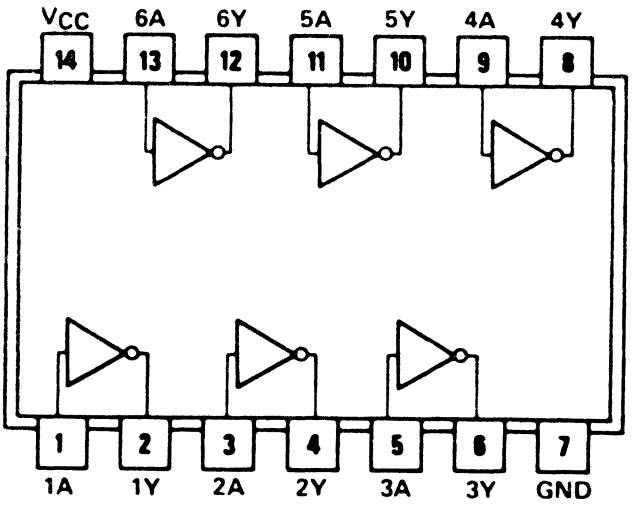
Positive logic: $Y = \overline{AB}$

NOTE *The 100000158 is a Schottky device.*

100000159

Hex Inverter

PIN CONFIGURATION



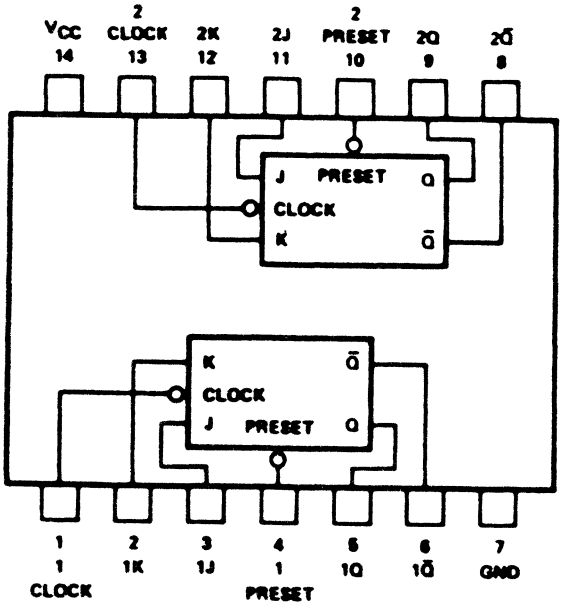
Positive logic: $Y = \overline{A}$

NOTE *The 100000159 is a Schottky device.*

100000160

Dual J-K Edge-Triggered Flip-Flop

PIN CONFIGURATION



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes:

t_n = bit time before clock pulse.

t_{n+1} = bit time after clock pulse.

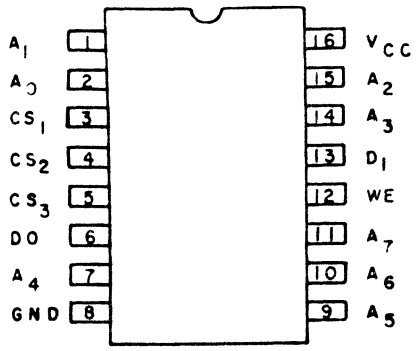
These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bi-stable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

NOTE *The 100000160 is a Schottky device.*

100000164

256-Bit Bipolar RAM

PIN CONFIGURATION



FUNCTION TABLE

Chip Selects	Write Enable	Operation	Output
All "0"	"0"	Write	Logical "1" State
All "0"	"1"	Read	Complement of data written in memory
One or More "1"	X	Hold	Logical "1" State

he 10 0164 integrated circuit is a high speed, lly decoded, static bipolar 256-bit random cess memory in a 256x1 organization. This vice provides uncommitted collector output d three chip selects.

peration

Read

he memory is addressed through the A_0-A_7 puts which select one of the 256 words. The ip is enabled by placing all chip selects (CS) logic "0". If any or all CS inputs are logic 1", then the device will be disabled. If the rite enable (WE) is at logic "1" the stored bit read out of DO.

Write

he memory is addressed through the A_0-A_7 puts which select one of the 256 words. The ip is enabled by placing all the CS inputs to gic "0". If the WE input is at logic "0", the ta on terminal DI is written into the addressed ord.

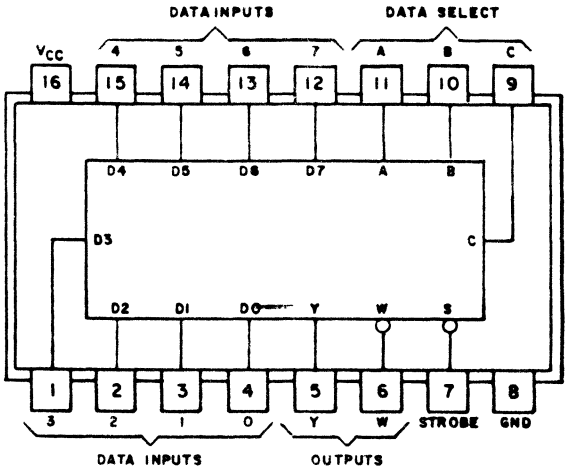
hen WE returns to logic "1", the information at was written in is now read out; however, ch word read out is the complement of what as en in.

NOTE *The 100000164 is a low power Schottky device.*

100000165

Data Selector/Multiplexer with 3-State Outputs

PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

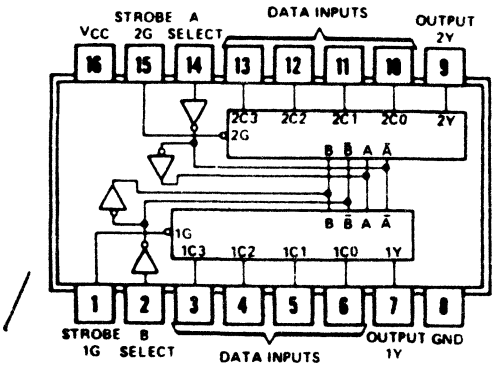
H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off).
D0, D1 .... D7 = the level of the respective D input.

NOTE *The 100000165 is a Schottky device.*

100000166

Dual 4-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select Inputs A and B are common to both sections.

H = high level; L = low level; X = irrelevant.

This monolithic, data selector-multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates.

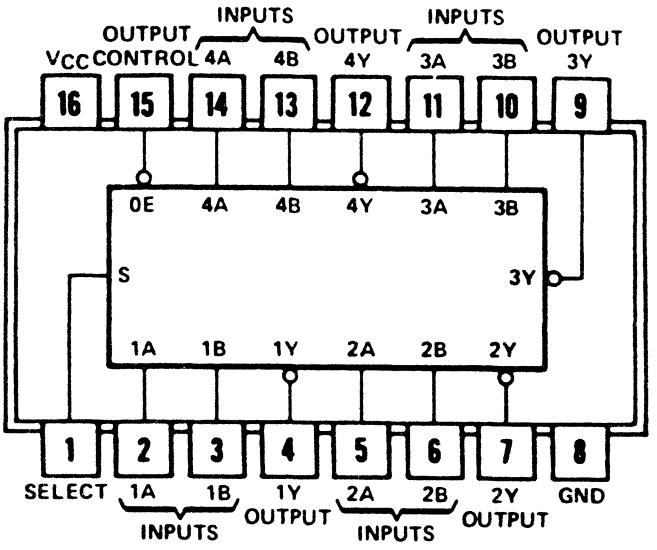
Separate strobe inputs are provided for each of the two four-line sections.

NOTE *The 100000166 is a Schottky device.*

100000167

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Output Y
Output Control	Select	A B	
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

These Schottky-clamped multiplexers have three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

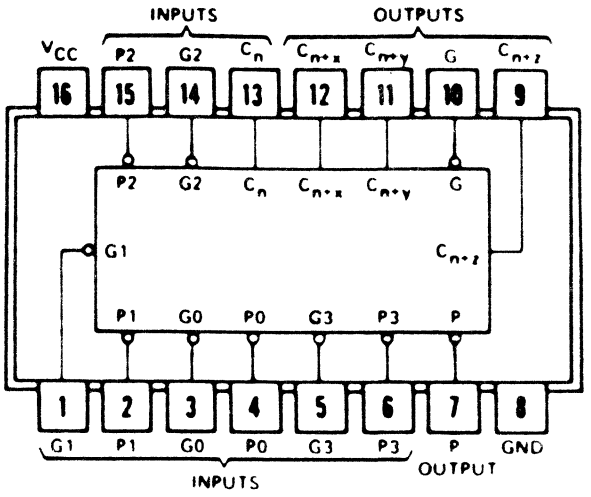
This three-state output means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

NOTE *The 100000167 is a Schottky device.*

100000170

Look-Ahead Carry Generator

PIN CONFIGURATION



Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
Gnd	8	Ground

Positive Logic:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$

$$C_{n+y} = \overline{G}_1 + \overline{P}_1\overline{G}_0 + \overline{P}_1\overline{P}_0 C_n$$

$$C_{n+z} = \overline{G}_2 + \overline{P}_2\overline{G}_1 + \overline{P}_2\overline{P}_1\overline{G}_0 + \overline{P}_2\overline{P}_1\overline{P}_0 C_n$$

$$\overline{G} = \overline{G}_3(\overline{P}_3+\overline{G}_2)(\overline{P}_3+\overline{P}_2+\overline{G}_1)(\overline{P}_3+\overline{P}_2+\overline{P}_1+\overline{G}_0)$$

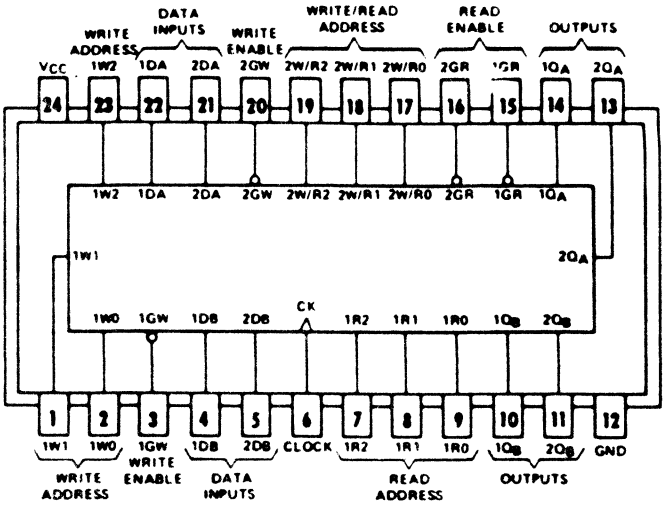
$$\overline{P} = \overline{P}_3\overline{P}_2\overline{P}_1\overline{P}_0$$

NOTE *The 100000170 is a Schottky device.*

100000171

16-Bit Multiple-Port Register File with 3-State Outputs

PIN CONFIGURATION



The 100000171 is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits.
2) Reading from two bits.
3) Writing into and simultaneously reading from the same two bits.

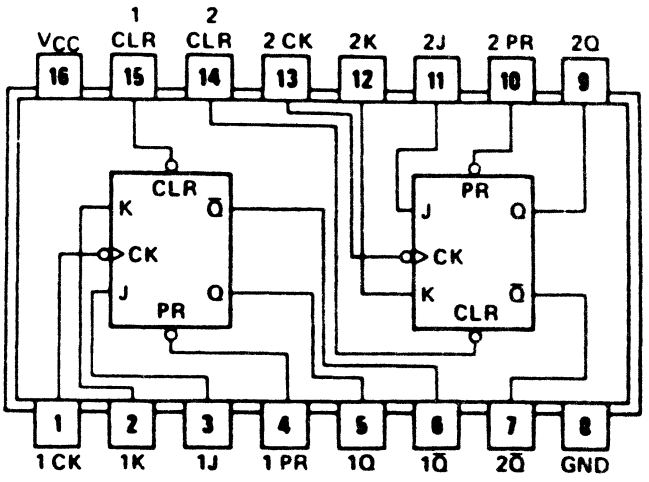
Regardless of the mode, the operation of section 2 is entirely independent of section 1.

Functions of the inputs and outputs are as shown in the following table:

100000172

Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes:

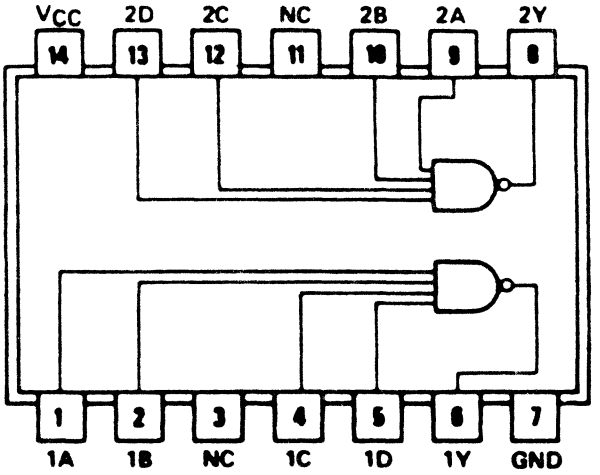
H = high level (steady state).
L = low level (steady state).
X = irrelevant.
↓ = transition from high to low level.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000172 is a Schottky device.*

100000173

Dual 4-Input Positive-NAND 50 Ohm Line Driver

PIN CONFIGURATION



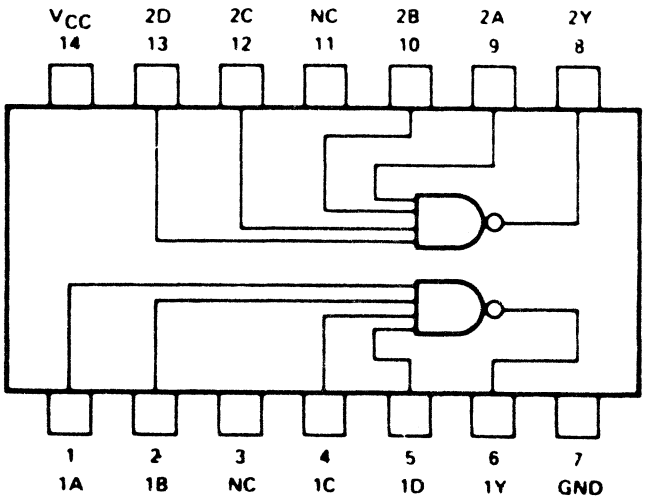
Positive logic: $Y = \overline{ABCD}$

NOTE *The 100000173 is a Schottky device*

100000174

Positive-NAND Gate with Open-Collector Outputs

PIN CONFIGURATION

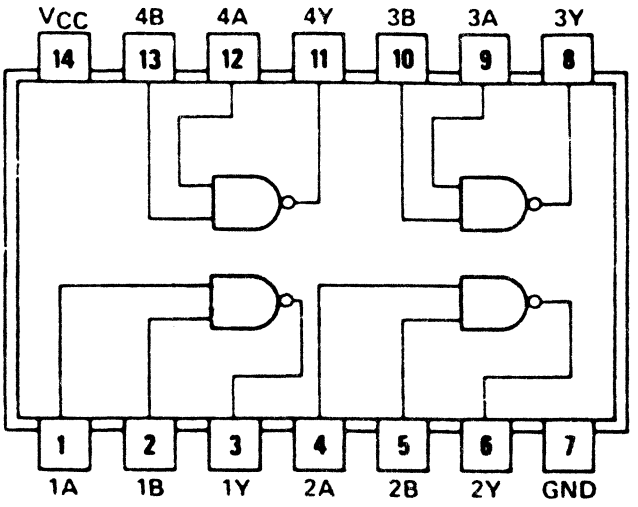


NOTE *The 100000174 is a Schottky device.*

100000175

Quad 2-Input Positive-NAND Gate with Open-Collector Outputs

PIN CONFIGURATION



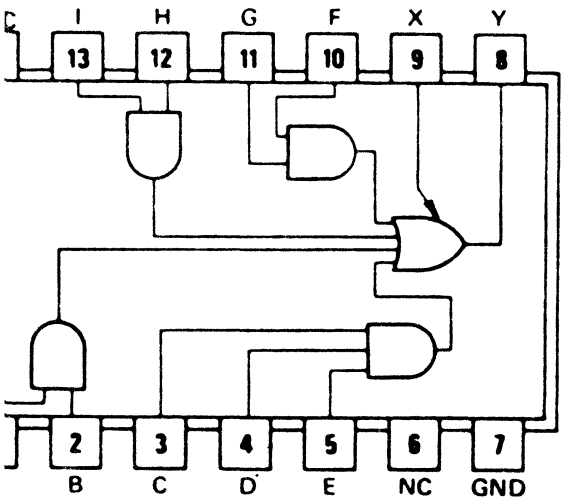
Positive logic: $Y = \overline{AB}$

NOTE *The 100000175 is a Schottky device.*

100000181

Expandable 4-Wide AND-OR Gate

PIN CONFIGURATION

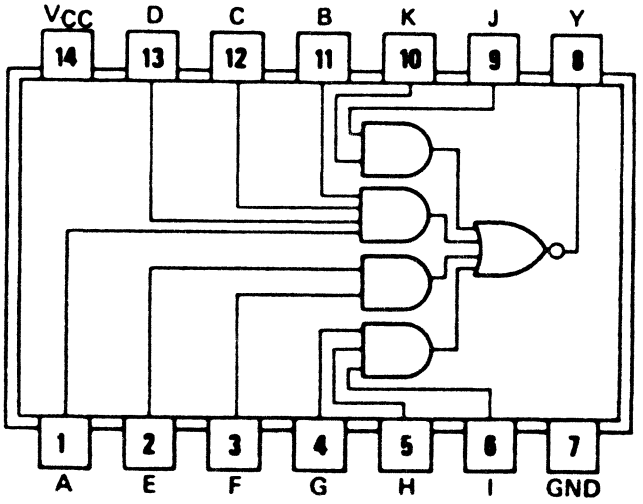


Positive logic: $Y = AB+CDE+FG+HI+X$

100000182

4-2-3-2-Input AND-OR-INVERT Gate

PIN CONFIGURATION



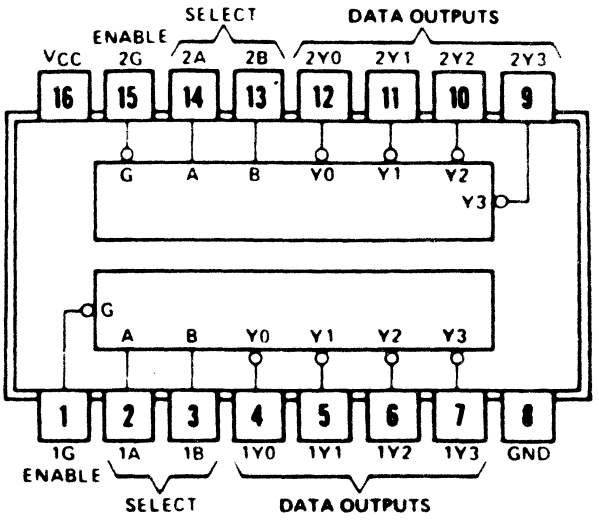
Positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

NOTE *The 100000182 is a Schottky device.*

100000185

Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

(Each Decoder/Demultiplexer)

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level; L = low level; X = irrelevant

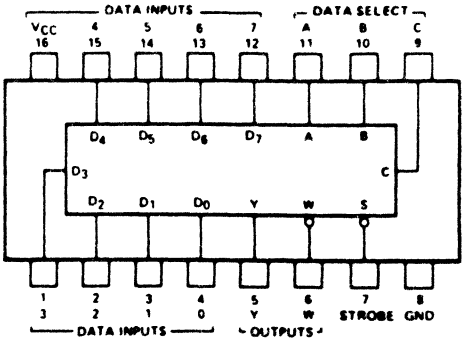
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

NOTE *The 100000185 is a Schottky device.*

100000186

8-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



TRUTH TABLE

Inputs										Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

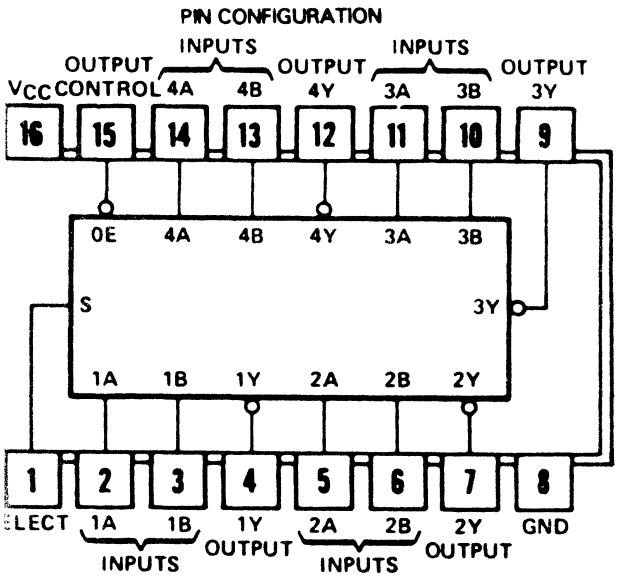
Note: When used to indicate an input, X = irrelevant.

The 100000186 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

100000187

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Output Y
Output Control	Select	A B	
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

= high level, L = low level, X = irrelevant,
= high impedance (off).

ese Schottky-clamped multiplexers have three-
ıte outputs which can interface directly with
d drive data lines of bus-organized systems.
th all but one of the common outputs disabled
a high-impedance state), the low impedance
the single enabled output will drive the bus
e to a high or low logic level.

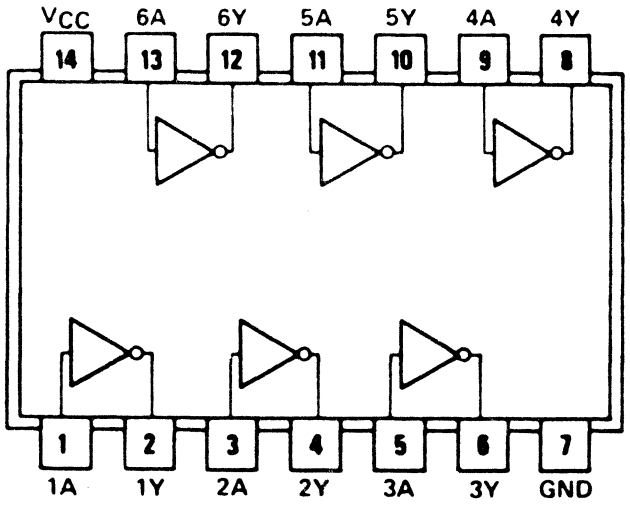
is three-state output means that n-bit (para-
led) data selectors with up to 258 sources can
imp ıented for data buses. It also permits
use of standard TTL registers for data re-
tio roughout the system.

NOTE *The 100000187 is a Schottky device.*

100000188

Hex Inverter with Open-Collector Outputs

PIN CONFIGURATION



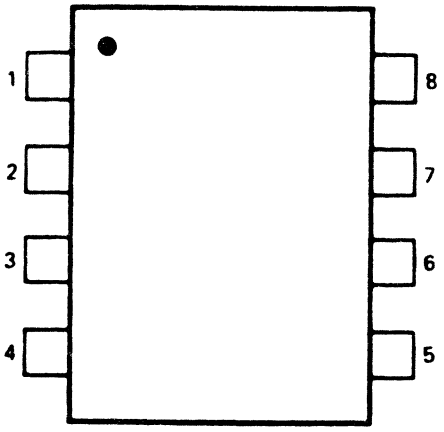
Positive logic: $Y = \overline{A}$

NOTE *The 100000188 is a Schottky device.*

100000193

Timer

PIN CONFIGURATION



PIN DESIGNATIONS

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

The 100000193 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting, if desired.

In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. For a stable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

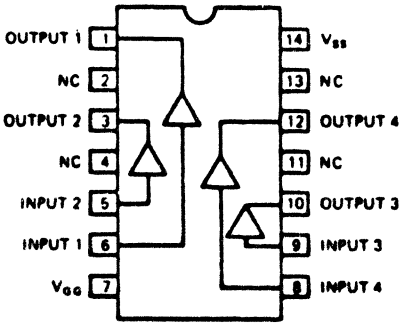
The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

NOTE *The 100000194 is a Schottky device.*

100000194

Quad MOS Clock Driver

PIN CONFIGURATION

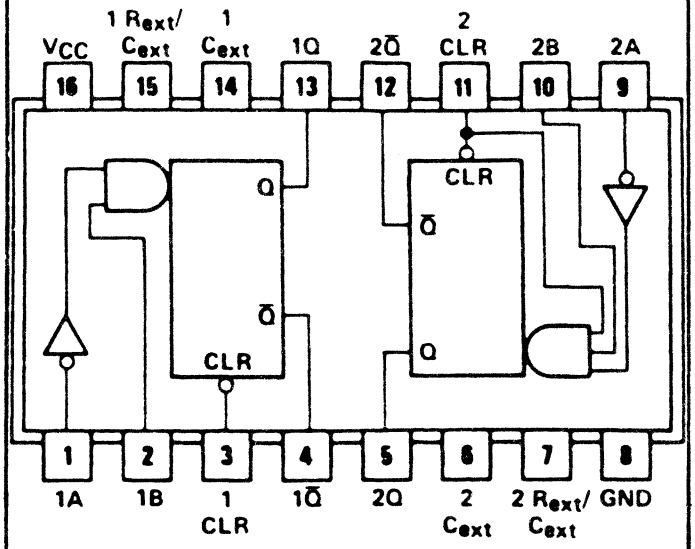


The 100000194 is a monolithic quad driver designed primarily for use as a MOS clock driver. It can be driven by high current TTL buffers or drivers, either directly or through input coupling capacitors, if level shifting is required.

100000222

Dual Retriggerable Monostable Multivibrator with Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Notes:

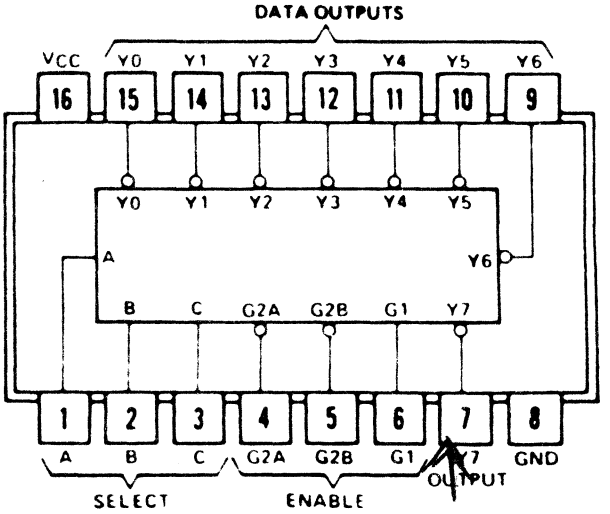
H = high level (steady state).
L = low level (steady state).
↑ = transition from low to high level.
↓ = transition from high to low level.
⎍ = one high-level pulse.
⎎ = one low-level pulse.
X = irrelevant (any input, including transitions).

An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

100000223

Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level; L = low level; X = irrelevant

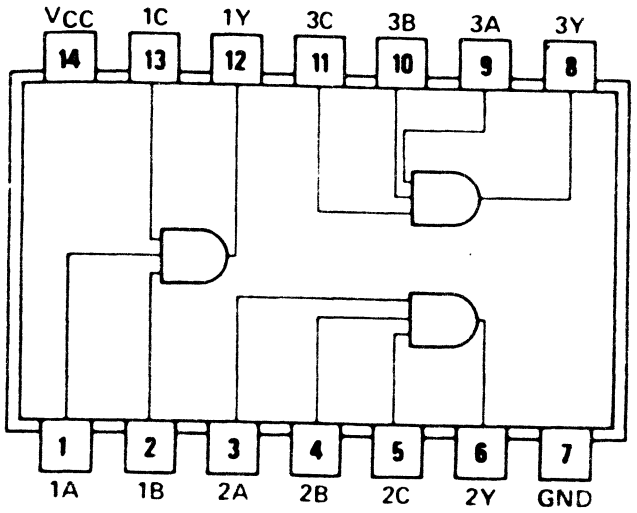
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

NOTE *The 100000223 is a Schottky device.*

100000237

Triple 3-Input Positive-AND Gate

PIN CONFIGURATION



V_{CC} = Pin 14

Gnd = Pin 7

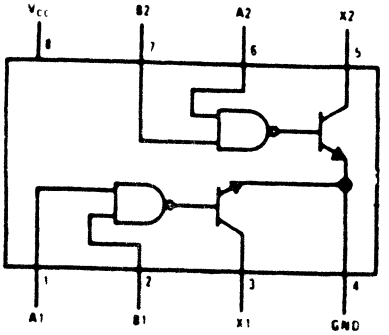
Positive logic: Y = ABC

NOTE *The 100000237 is a Schottky device.*

100000238

Dual Peripheral Driver

PIN CONFIGURATION



TRUTH TABLE

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

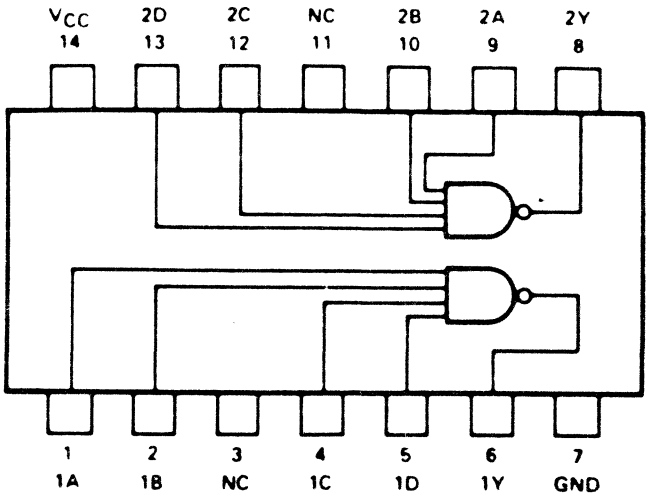
*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000249

Positive-NAND Gate

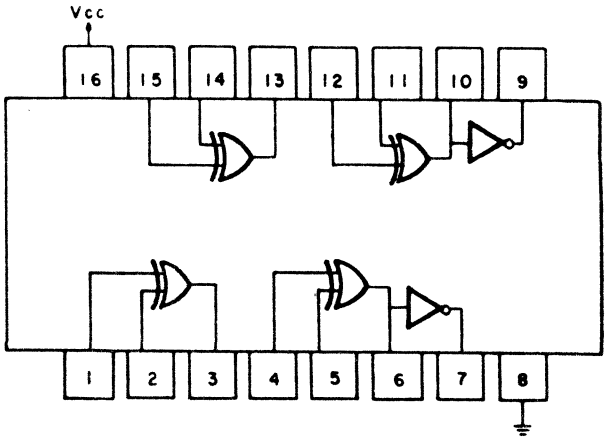
PIN CONFIGURATION



100000250

Quad Exclusive-OR Gate

PIN CONFIGURATION



TRUTH TABLE

A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = High Voltage Level
L = Low Voltage Level

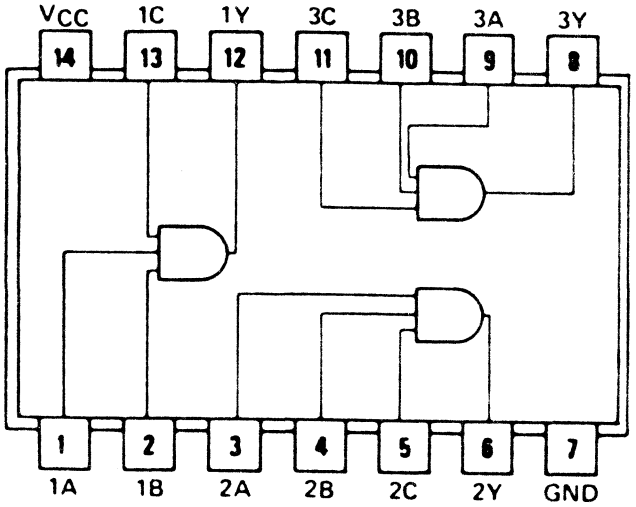
The exclusive OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expressions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{A}\overline{B}$.

NOTE The 100000249 is a Schottky device.

100000259

Triple 3-Input Positive-AND Gate with Open-Collector Outputs

PIN CONFIGURATION



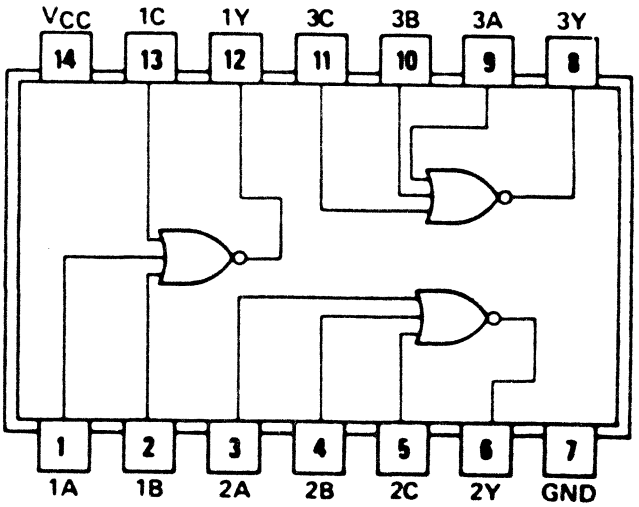
Positive logic: $Y = ABC$

NOTE *The 100000259 is a Schottky device.*

100000260

Triple 3-Input Positive-NOR Gate

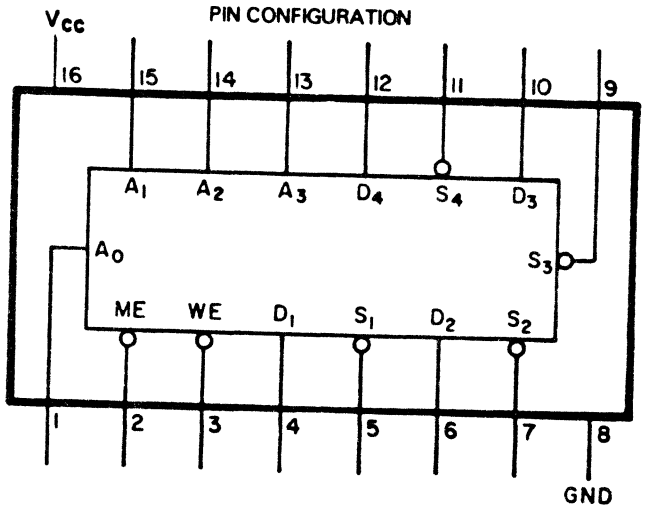
PIN CONFIGURATION



Positive logic: $Y = \overline{A+B+C}$

100000266

64-Bit RAM



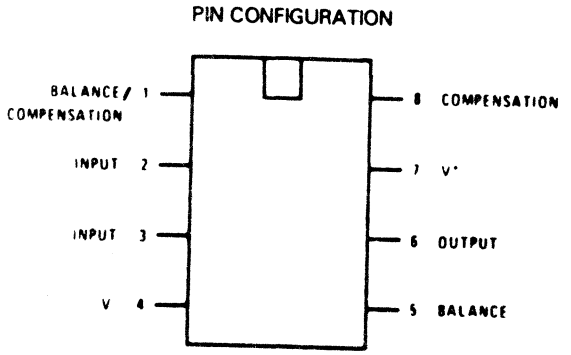
TRUTH TABLE

Memory Enable	Write Enable	Operation	Outputs
	0	Write	Hi-Z State
	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

The 100000266 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of T[illegible]

100000267

Operational Amplifier



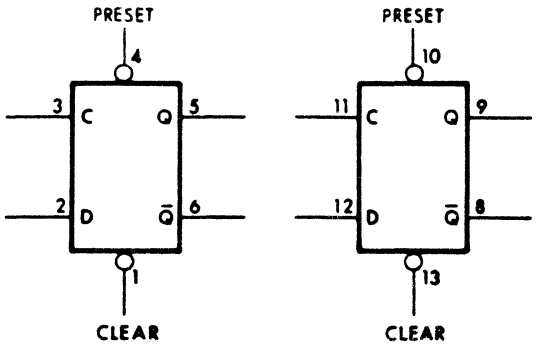
The 100000267 is a general purpose operational amplifier. This amplifier offers overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30pF capacitor.

In addition, the circuit can be used as a comparator with differential inputs up to ±30V, and the output can be clamped at any desired level to make it compatible with logic circuits.

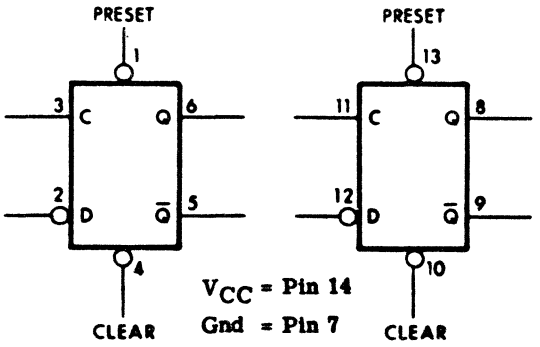
100000300

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



ALTERNATE PIN CONNECTIONS



FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

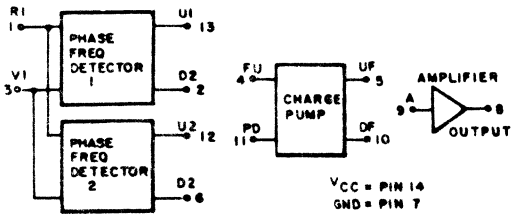
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000300 is a Schottky device.*

100000301

Phase-Frequency Detector

LOGIC DIAGRAM



FUNCTION TABLE

INPUT STATE	INPUT		OUTPUT			
	RI	VI	U1	D1	U2	D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

1. X indicates output state unknown
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

TRUTH TABLE

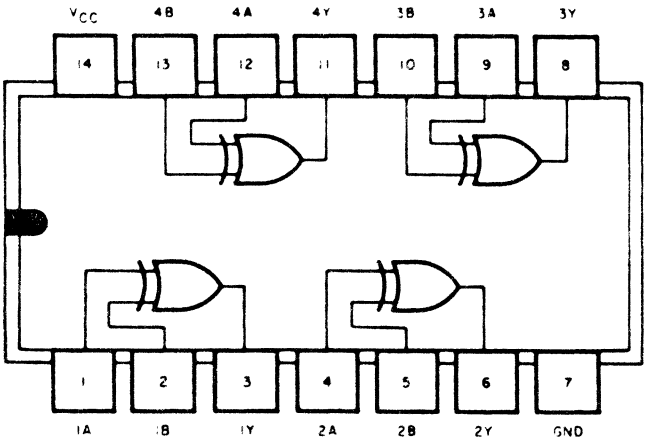
This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

The 100000301 contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked loop applications.

100000365

Quad 2-Input Exclusive-OR Gate

PIN CONFIGURATION

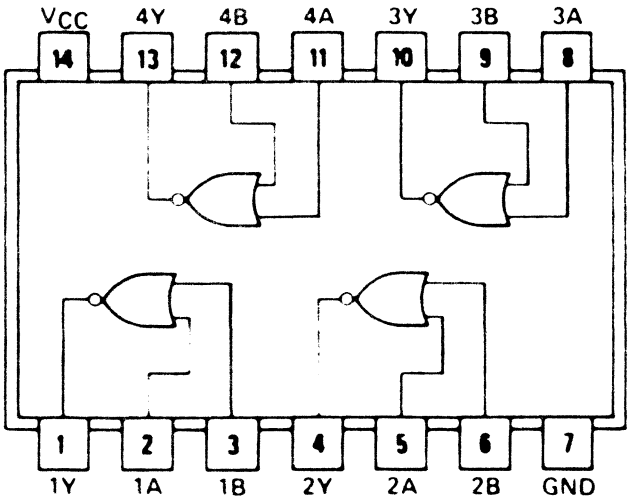


NOTE *The 100000365 is a Schottky device.*

100000366

Quad 2-Input Positive-NOR Gate

PIN CONFIGURATION

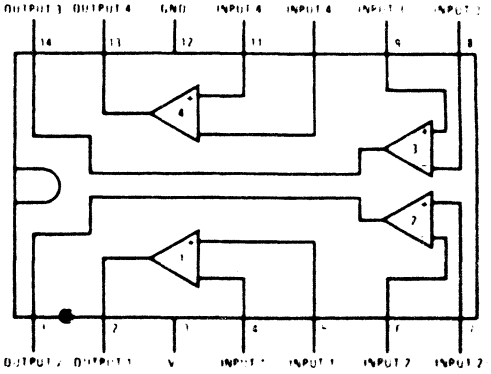


NOTE *The 100000366 is a Schottky device.*

100000470

Voltage Comparator

PIN CONFIGURATION



The 100000470 operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. The input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Pin Designations

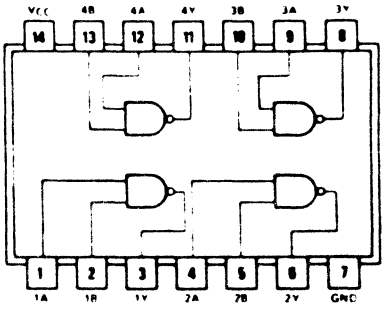
V+ = Pin 3

Gnd = Pin 12

100000472

Quad 2-Input Positive NAND Gate

PIN CONFIGURATION

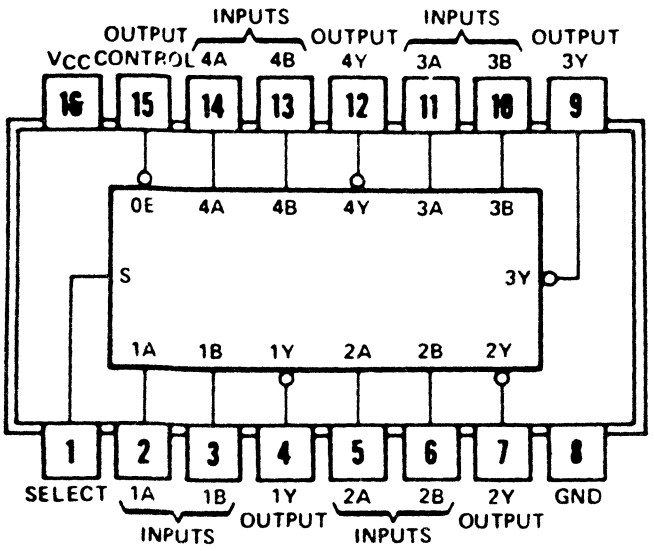


NOTE *The 100000472 is a Schottky device.*

100000475

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE

Inputs			Output
Output Control	Select	A B	Y
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

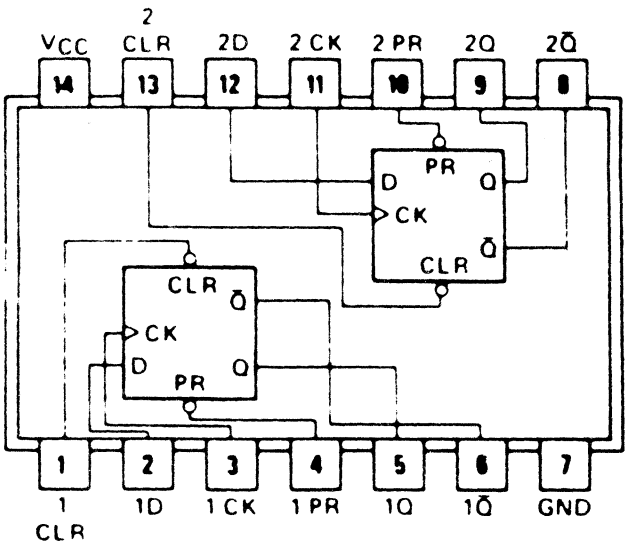
H = high level, L = low level, X = irrelevant,
Z = high impedance (off).

NOTE *The 100000475 is a low power Schottky device.*

100000476

Dual D-Type Positive-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



Logic Diagram Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

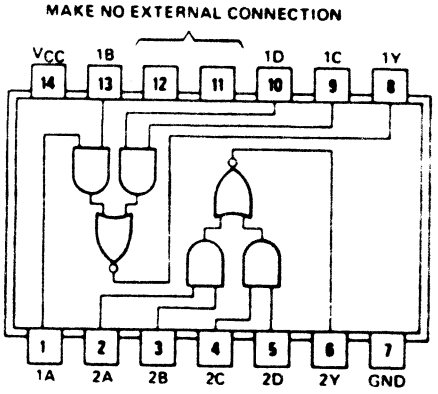
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable: that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000476 is a low power Schottky device.*

100000504

Dual 2-Wide 2-Input AND-OR-INVERT Gates

PIN CONFIGURATION



Positive logic: $Y=\overline{AB+CD}$

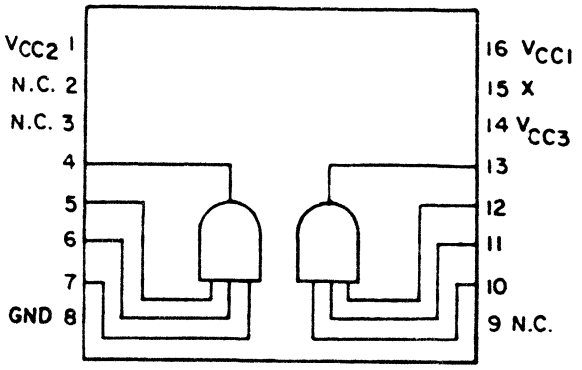
NOTE

The 100000504 is a Schottky device.

100000505

Clock Driver

PIN CONFIGURATION



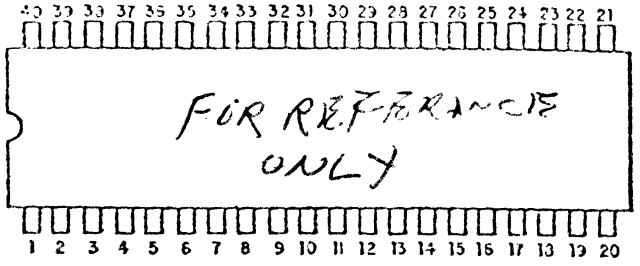
10000080 10000350

UART.

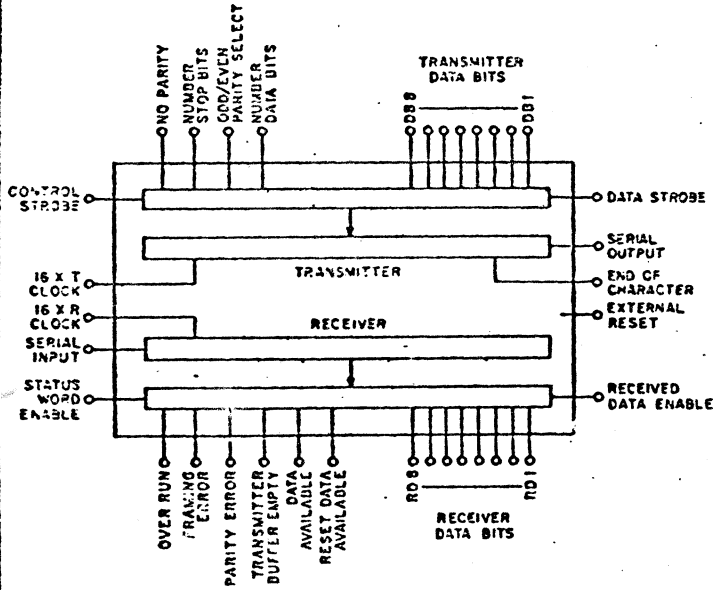
Asynchronous Receiver/Transmitter

The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

Pin Configuration



Block Diagram

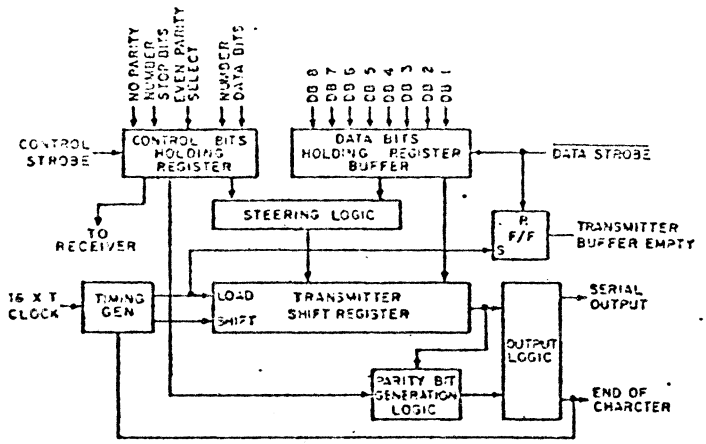


Description of Pin Functions

Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{ss}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.

Continued ....

Transmitter Block Diagram



Description of Pin Functions (Continued)

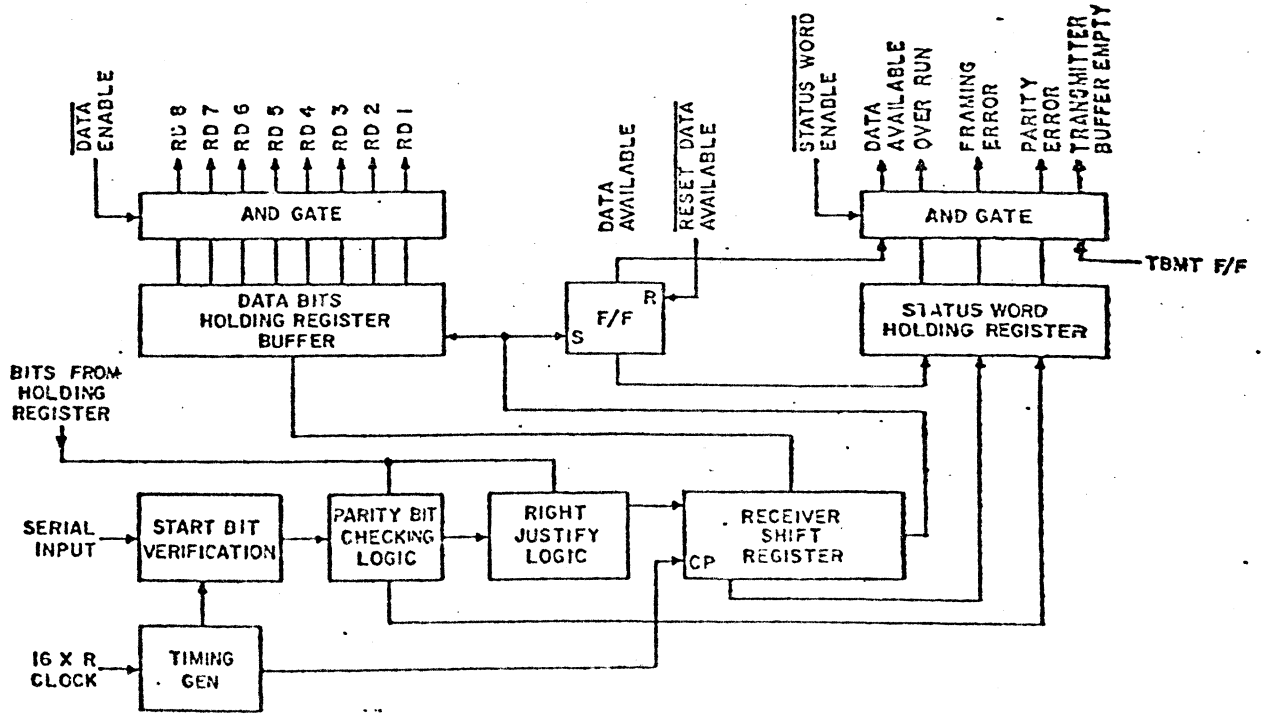
Pin No.	Name	Symbol	Function
25-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
31	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
34	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indications). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
35	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character.

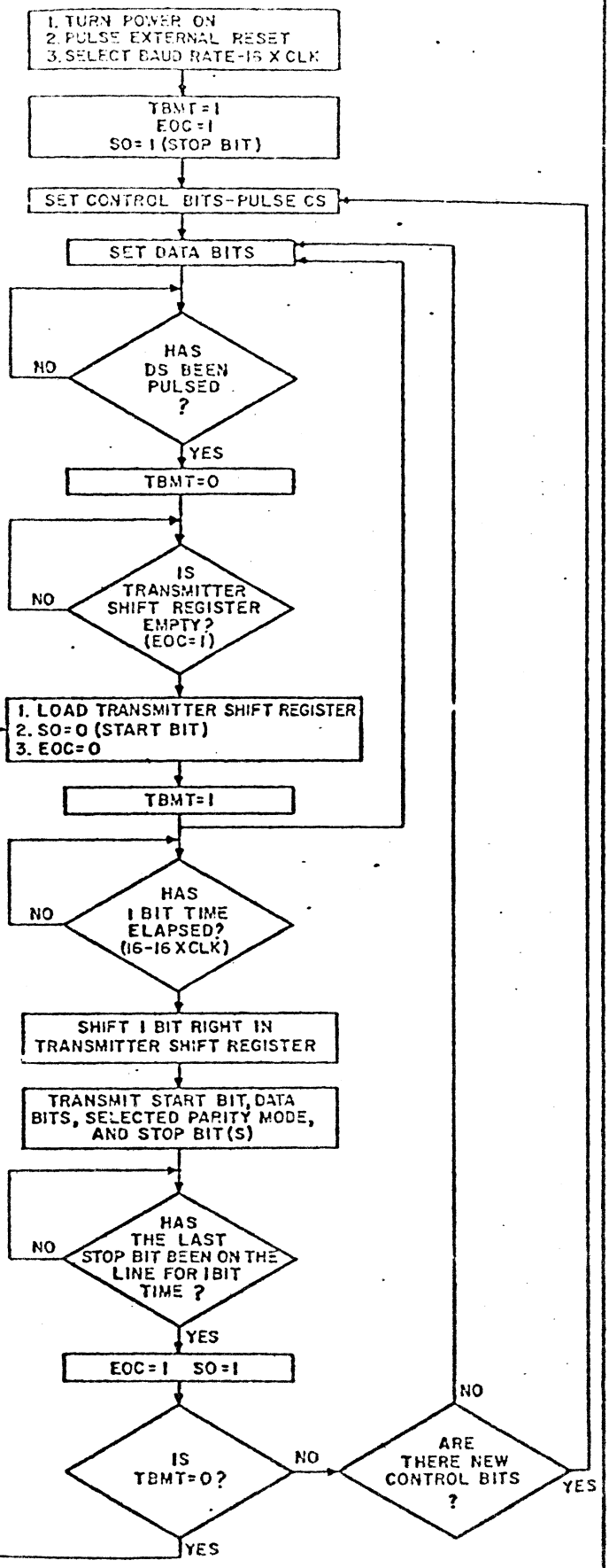
NB1	NB2	Bits Character
0	0	5
1	0	6
0	1	7
1	1	8

39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

Continued....

Receiver Block Diagram





Transmitter Operation

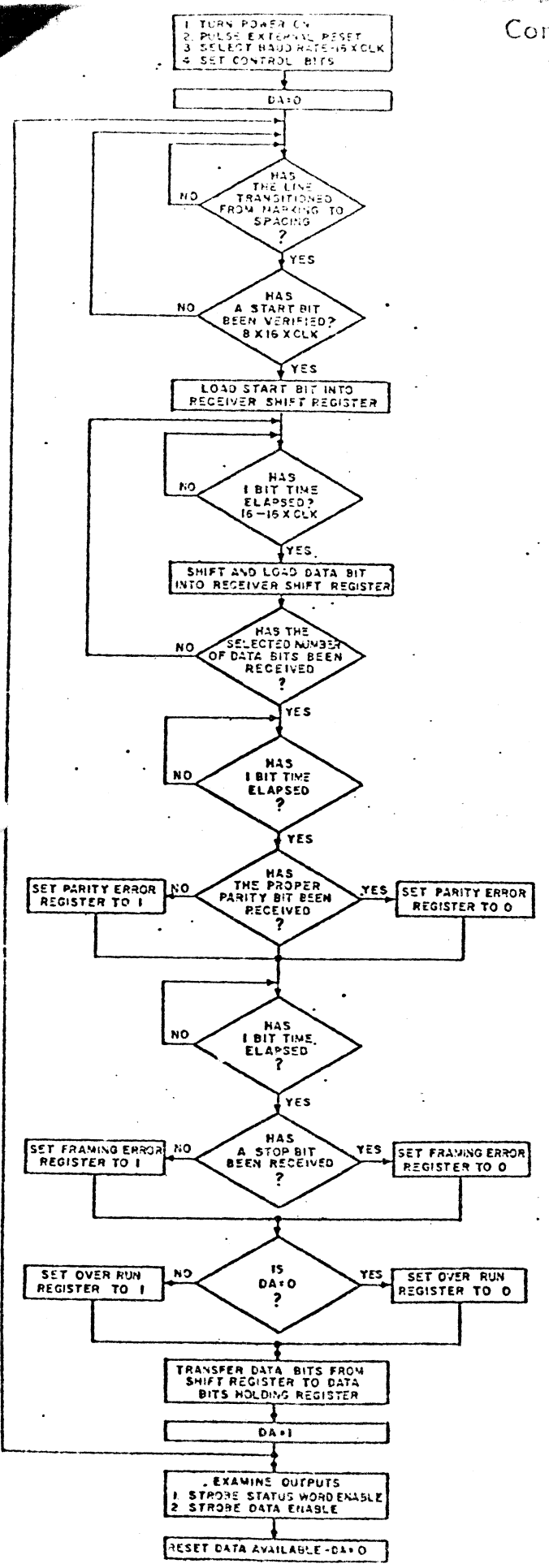
Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously mentioned.

Continued....



Receiver Operation

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

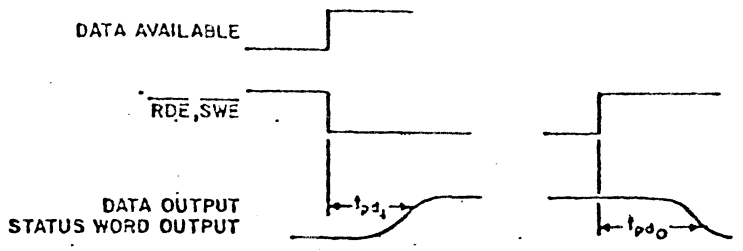
After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16X clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditioning set to a logic "0".

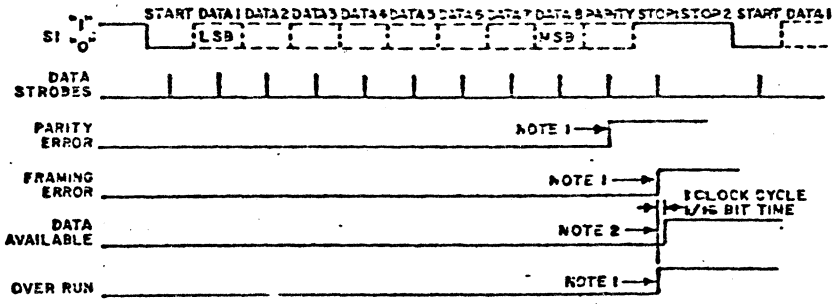
Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

Continued....

Receiver Propagation Delay Timing Diagram



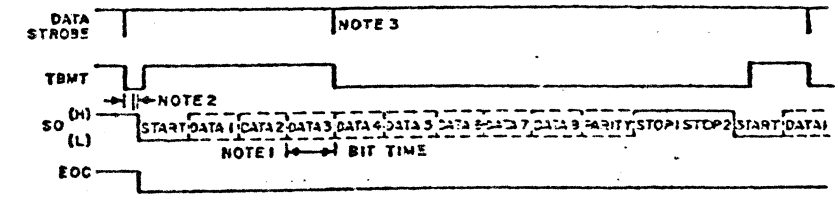
Receiver Timing Diagram



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Transmitter Timing Diagram



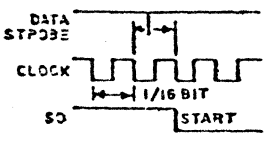
NOTE: TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1.

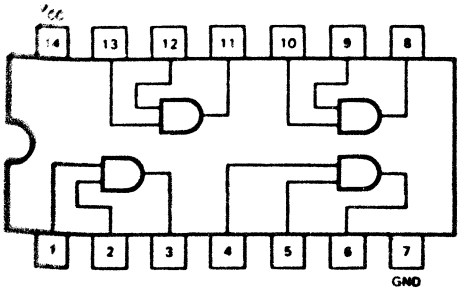
DETAIL:



100000537

Quad 2-Input AND Gate

PIN CONFIGURATION

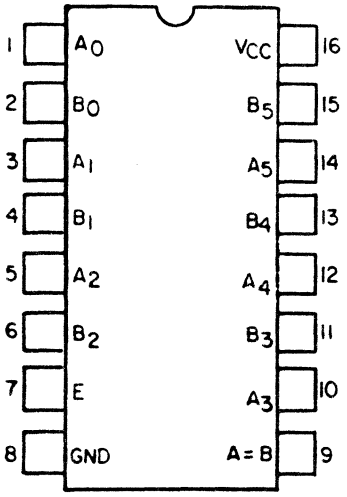


NOTE *The 100000537 is a Schottky device.*

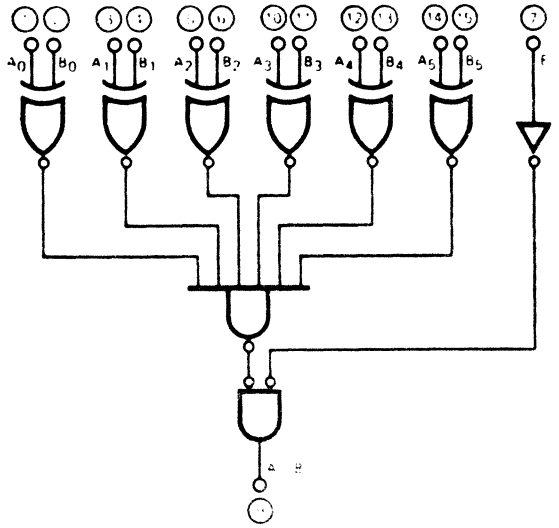
100000540

High Speed 6-Bit Identity Comparitor

PIN CONFIGURATION



LOGIC DIAGRAM



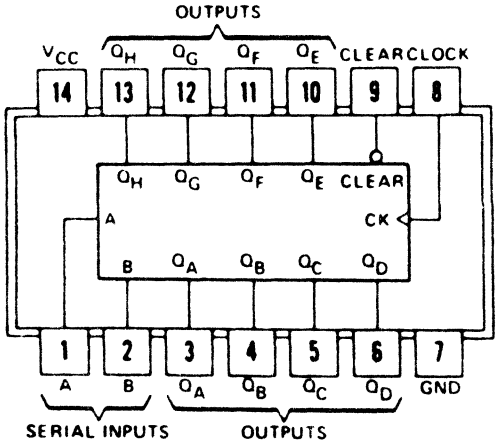
The 100000540 is a very high speed 6-Bit Identity Comparator. The device compares two words of up to 6-bits and indicates identity in less than 12 ns It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable Input (E) is LOW, it forces the output LOW. The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL product families.

NOTE *The 100000540 is a Schottky device.*

100000541

8-Bit Parallel-Out Serial Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

Notes:

H = high level (steady state),
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

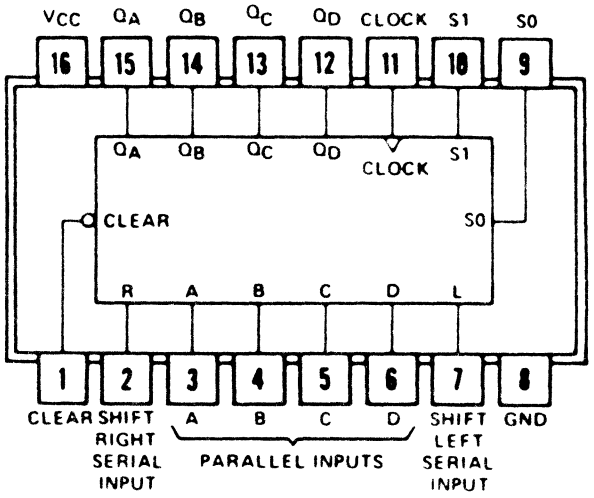
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

The 100000541 features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the set-up requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock

100000580

4-Bit Bidirectional Universal Shift Register

PIN CONFIGURATION



FUNCTION TABLE

CLEAR	MODE S_1	MODE S_0	CLOCK	SERIAL LEFT	SERIAL RIGHT	PARALLEL A	B	C	D	OUTPUTS Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

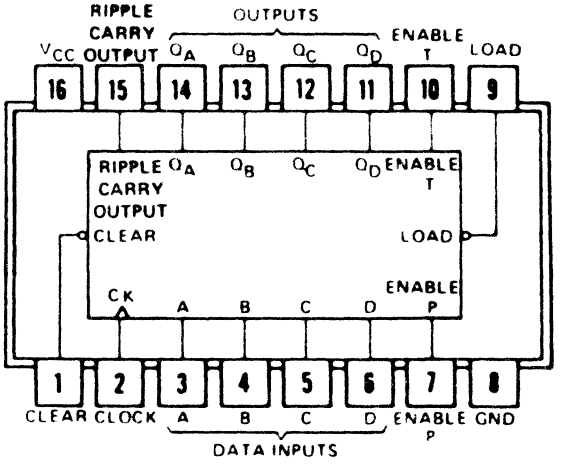
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

NOTE *The 100000580 is a low power Schottky device.*

100000581

Synchronous 4-Bit Counter

PIN CONFIGURATION



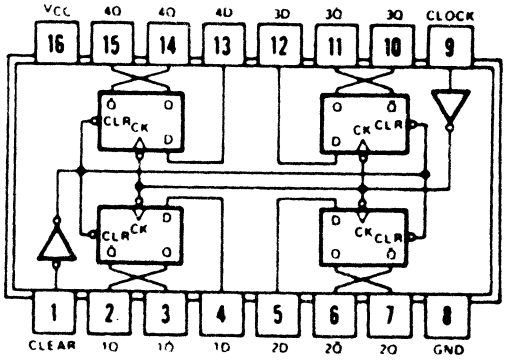
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

NOTE *The 100000581 is a low power Schottky device.*

100000594

Quad D Flip Flop with Clear



FUNCTION TABLE

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

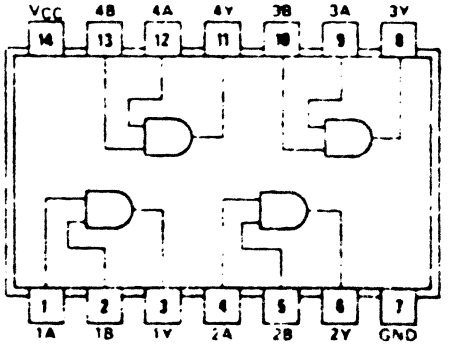
Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

NOTE *The 100000594 is a low power Schottky device.*

100000595

Quad 2-Input Positive-AND Gate



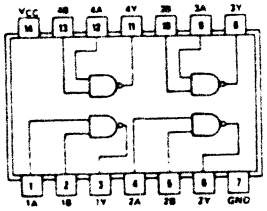
NOTE *The 100000595 is a low power Schottky device.*

100000779

74 S 38

Quad 2-Input NAND Buffer

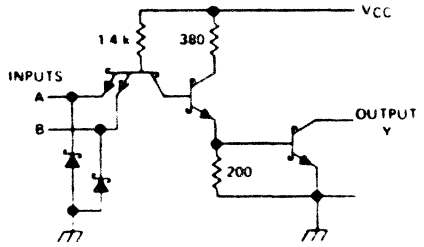
PIN CONFIGURATION



positive logic:

$Y = \overline{AB}$

LOGIC DIAGRAM



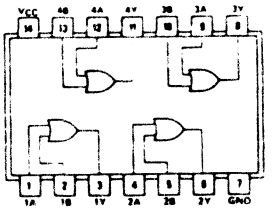
The 100000779 consists of four 2-input NAND buffers with open collector-outputs.

NOTE *The 100000779 is a Schottky device.*

100000780

Quad 2-Input OR Gate

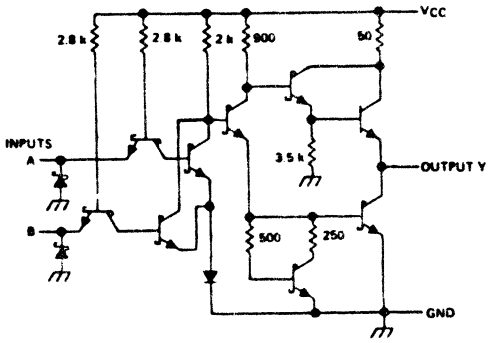
PIN CONFIGURATION



positive logic:

Y = A+B

LOGIC DIAGRAM



The 100000780 consists of four 2-input OR gates with totem-pole outputs.

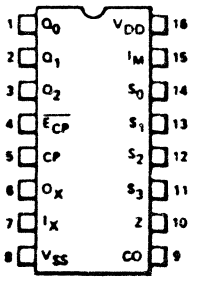
NOTE *The 100000780 is a Schottky device.*

100000795

DS-4701-?

Programmable Bit Rate Generator

PIN CONFIGURATION



PIN NAMES

CP	External Clock Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_7	Scan Counter Outputs
Z	Bit Rate Output

CLOCK MODES AND INITIALIZATION

I_X	$\overline{E_{CP}}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎍	Reset During First CP = HIGH Time

Note : Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576 MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = 1st HIGH Level Clock Pulse After $\overline{E_{CP}}$ Goes LOW
⎍⎍⎍ Clock Pulses

TRUTH TABLE FOR RATE SELECT INPUTS

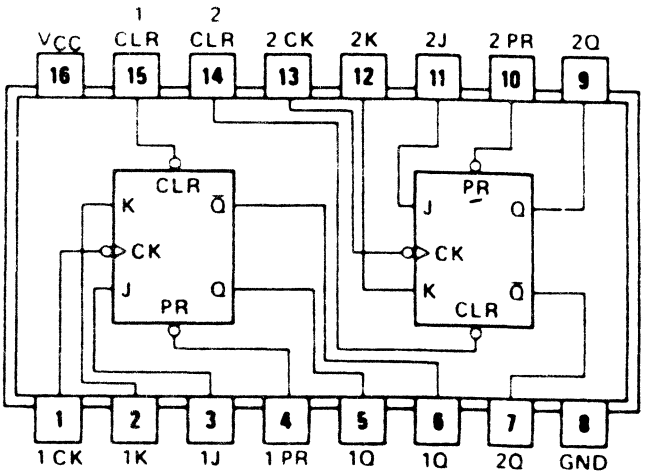
S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

100000796

5472

Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes:

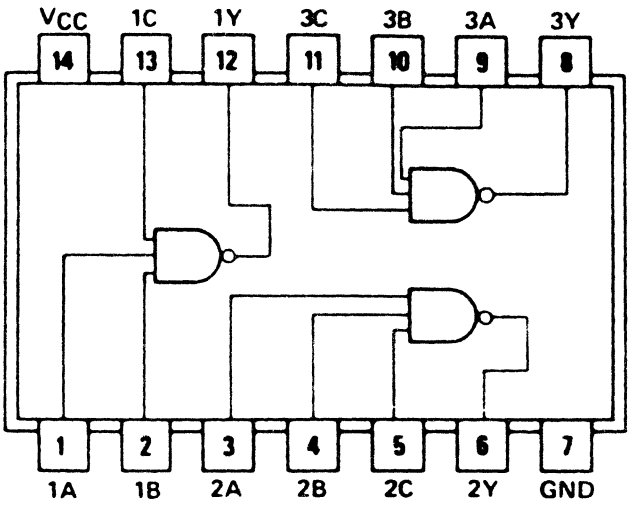
H = high level (steady state).
L = low level (steady state).
X = irrelevant.
↓ = transition from high to low level.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000796 is a low power Schottky device.*

100000797

Triple 3-Input Positive-NAND Gate

PIN CONFIGURATION



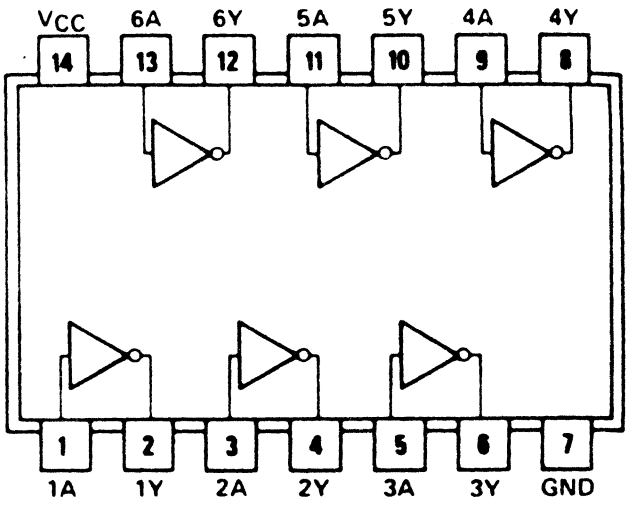
Positive logic: $Y = \overline{ABC}$

NOTE *The 100000797 is a low power Schottky device.*

100000798

Hex Inverter with Open Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{A}$

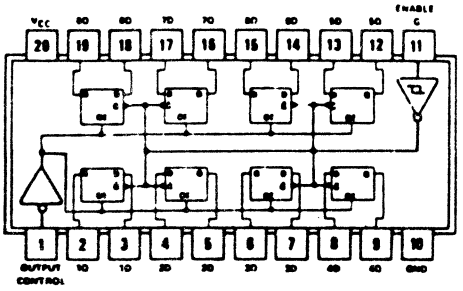
NOTE *The 100000798 is a low power Schottky device.*

100001018

Octal D-Type Transparent Latches

74 : 373

PIN CONFIGURATION



TRUTH TABLE

OUTPUT $\overline{\text{CONTROL}}$	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 = the level of Q before the indicated steed-state input conditions were established.
H = high level
L = low level
Hi-Z = high impedance
X = irrelevant
↑ = transition from low to high level

The 100001018 contains eight D-type latches. When the enble G is high, the Q outputs follow the D inputs. When this enable goes low, the outputs are latched at the data states that were setup.

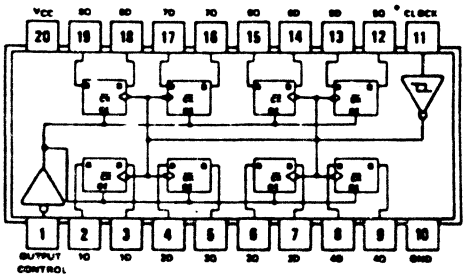
These latches have totem-pole 3-state outputs for driving highly-capacitive or relatively low-impedance loads.

NOTE *The 100001018 is a Schottky device.*

100001019

Octal D-Type Edge-Triggered Flip-Flops

74S374



TRUTH TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 = the level of Q before the indicated steed-state input conditions were established.
H = high level
L = low level
Hi-Z = high impedance
X = irrelevant
↑ = transition from low to high level

The 100001019 contains eight edge-triggered D-types flip-flops. On the low-to-high clock transition, the Q outputs are set to the data states setup on the D inputs.

These flip-flops have totem-pole 3 state outputs for driving highly-capacitive or relatively low-impedance loads.

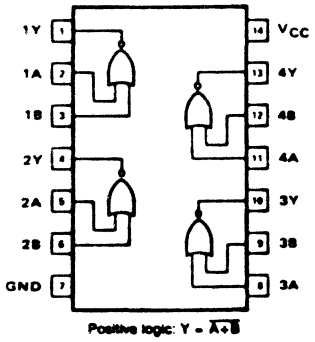
NOTE *The 100001019 is a Schottky device.*

100001020

74LS02

Quad 2-Input NOR Gate

PIN CONFIGURATION



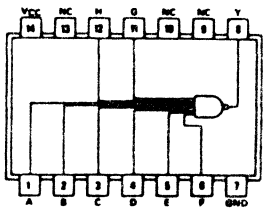
NOTE *The 100001020 is a low power Schottky device.*

74LS32

100001045

8-Input NAND Gate

PIN CONFIGURATION



positive logic:
$Y = \overline{ABCDEFGH}$

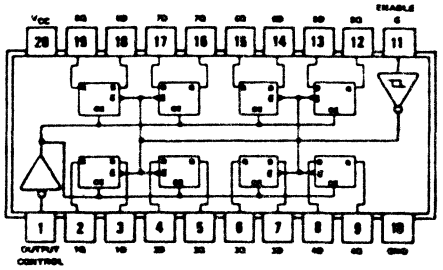
NOTE *The 100001045 is a Schottky device.*

100001046

373

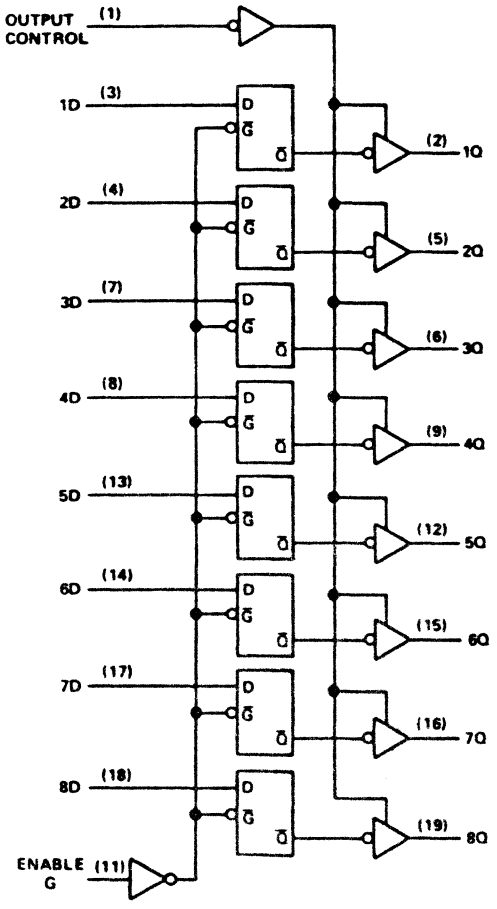
Octal D-Type Transparent Latch

PIN CONFIGURATION



BLOCK DIAGRAM

TRANSPARENT LATCHES



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

The 100001046 consists of eight, transparent D-type latches with totem-pole three-state outputs. When the enable (G) is high the Q outputs will follow the data ((D) inputs. When the enable goes low, the output will be latched at the level of the data that was setup.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

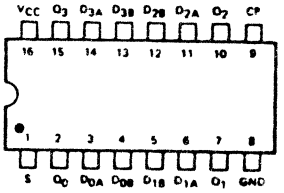
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

NOTE *The 100001046 is a low power Schottky device.*

100001047 and 100001048

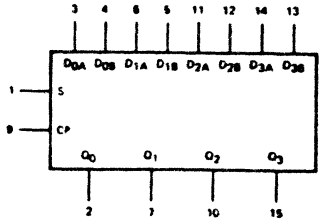
Quad Two-Input Registers

PIN CONFIGURATION



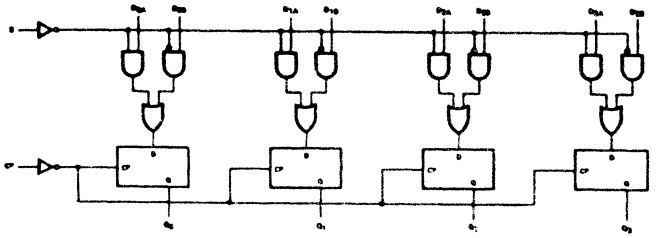
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



The 100001047 and 100001048 are registers containing four D flip-flops with a buffered common clock and a two input multiplexer at the input of each flip-flop. The multiplexers are controlled by the common select line S. Data selected by S is stored in the flip-flops on the low-to-high transition of the clock. When the S input is low, the DiA data is stored in the register; when it is high, the DiB data is stored.

NOTE *The 100001047 and 100001048 are Schottky devices. The 100001047 is a lower power component.*

PRELIMINARY DATA
JANUARY, 1977

Four-Bit Bipolar Microprocessor Slice
Advanced Micro Devices
Bipolar Microprocessor Circuits

DISTINCTIVE CHARACTERISTICS

- Plug-in replacement for standard Am2901
- 20% to 30% faster than standard Am2901
- Major improvements in D input and carry paths
- I_{OL} raised to 20mA on Y outputs — 30% more drive than standard Am2901
- I_{CC} reduced to 190mA at 125°C — 30% less than standard Am2901
- V_{IL} raised to 0.8V over full military range for increased noise immunity

Note: $Q' \leftarrow Q/2$ means
$Q' \leftarrow (1, Q)$

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901A will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip. The Am2901A is a plug in replacement for the Am2901. For detailed description and applications see the Am2901 Data Sheet.

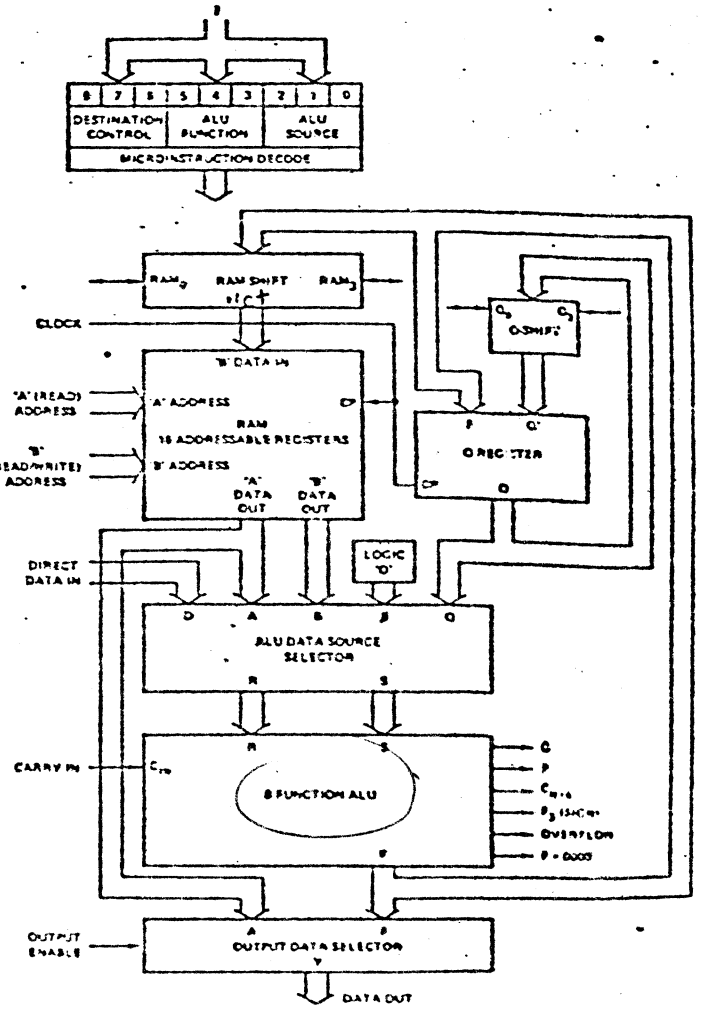
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to 70°C	AM2901APC
Hermetic DIP	0°C to 70°C	AM2901ADC
Hermetic DIP	−55°C to +125°C	AM2901ADM
Hermetic Flat Pack	−55°C to +125°C	AM2901AFM
Dice	0°C to +70°C	AM2901AXC

Note: The Data in this data sheet contains expected typical performance for the Am2901A. As a rule, worst case AC limits will be approximately 1.6 times typical over the commercial range and approximately 2.0 times typical over the military range. Be sure to contact Advanced Micro Devices for the latest data.

AVAILABLE FEBRUARY, 1977

MICROPROCESSOR SLICE BLOCK DIAGRAM



MICRO CODE			ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

ALU Source Operand Control.

MICRO CODE				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R+S
L	L	H	1	S Minus R	S−R
L	H	L	2	R Minus S	R−S
L	H	H	3	R OR S	R∨S
H	L	L	4	R AND S	R∧S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$∧S
H	H	L	6	R EX-OR S	R∨S
H	H	H	7	R EX-NOR S	$\overline{R \vee S}$

ALU Function Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

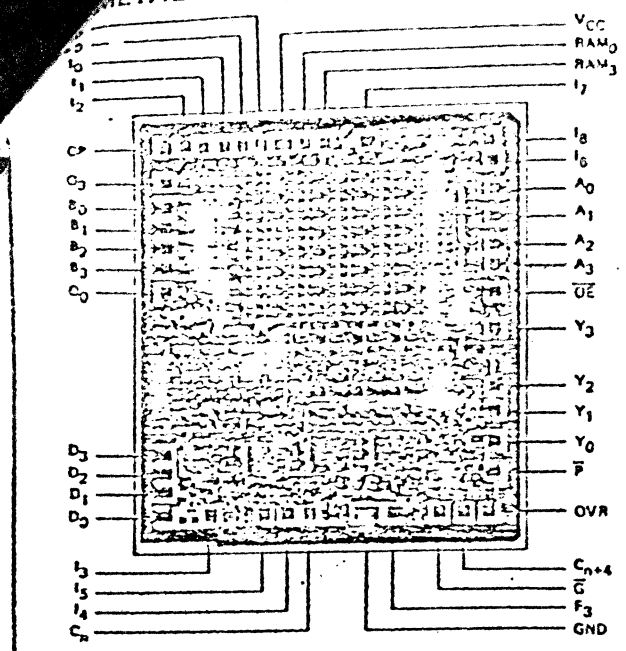
ALU Destination Control.

OCTAL	I_{210} OCTAL / I_{543} ALU Source / ALU Function	0	1	2	3	4	5	6	7
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L, R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L, S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L, R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	$\overline{A}$∧B	Q	B	A	$\overline{D}$∧A	$\overline{D}$∧Q	0
6	R EX-OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
7	R EX-NOR S	$\overline{A \vee Q}$	$\overline{A \vee B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \vee A}$	$\overline{D \vee Q}$	$\overline{D}$

+ = Plus, − = Minus; ∨ = OR, ∧ = AND; ∨ = EX-OR

Source Operand and ALU Function Matrix.

METALLIZATION AND PAD LAYOUT

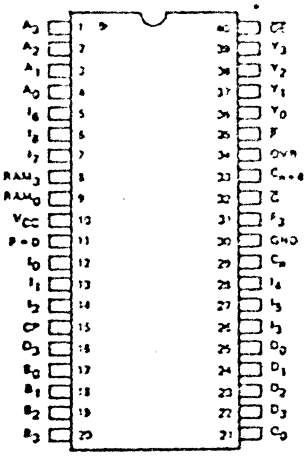


DIE SIZE 0.132" X 0.149"

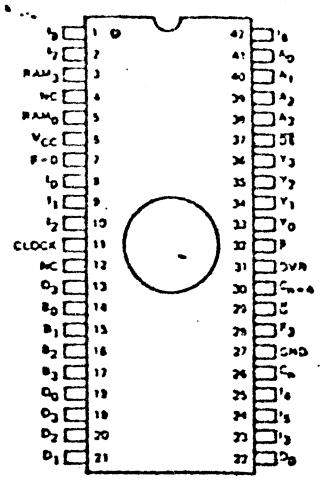
CONNECTION DIAGRAMS

Top View

DIP



Top View



Note:
Pin 1 is marked for orientation.

Caution: Am2901AFM pinout differs from Am2901FM on pins 4, 11, 12 and 13.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines to the Am2901, used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the Am2901A. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the Am2901A. D_0 is the LSB.

Y_{0-3} The four data outputs of the Am2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Am2901A's ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Figure 8 for logic equation.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n The carry-in to the Am2901A's ALU.

C_{n+4} The carry-out of the Am2901A's ALU. See Figure 8 for equations.

CP The clock to the Am2901A. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

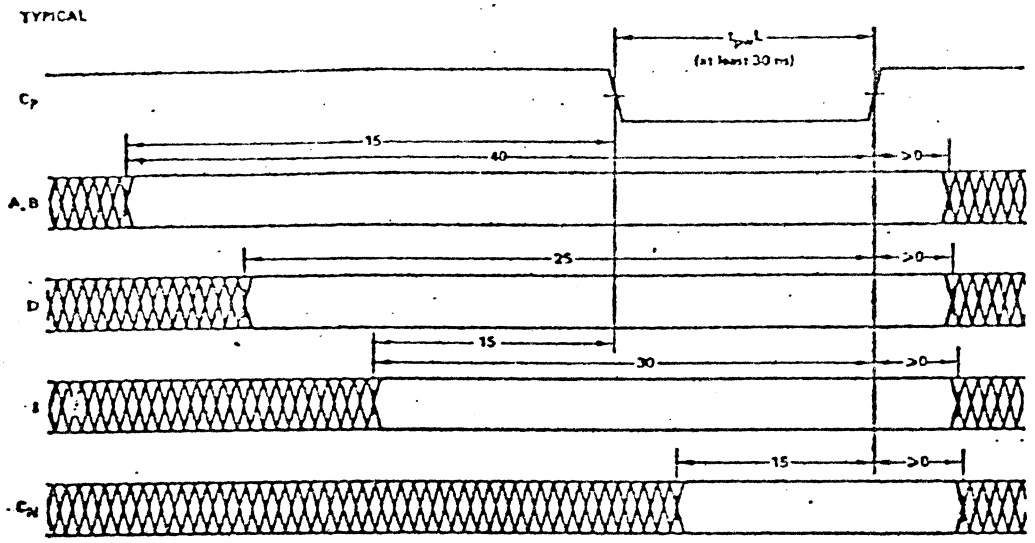
...CAL CHARACTERISTICS OVER ...

(Subgroups 1, 2, and 3) Data in bold face is changed from Am2901

Symbols	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800µA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600µA, F_3	2.4			
				I_{OH} = −600µA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	µA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V			50	µA
				V_O = 0.5V			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V, V_O = 0.5V	$Y_0, Y_1, Y_2, Y_3, \overline{G}$		−30		−85	mA
			C_{n+4}		−30		−85	
			OVR, $\overline{P}$		−30		−85	
			F_3		−30		−85	
			$RAM_{0,3}$, $Q_{0,3}$		−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.	Am2901APC, DC	T_A = 25°C		160	250	mA
				T_A = 0°C to +70°C		160	265	
				T_A = +70°C		160	220	
			Am2901ADM, FM	T_C = −55°C to +125°C		160	280	
				T_C = +125°C		160	190	

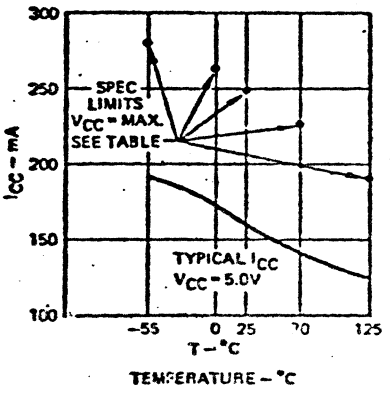
Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901AXM, DM, FM. "COM'L" = Am2901AXC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

old times are defined relative to the clock LOW-to-e. Inputs must be steady at all times from the set-up operation on the correct data so that the correct ALU data can be written into one of the registers.



Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for AM2901ADC, in ns. See Table III for Detailed Information.

Typical I_{CC} Versus Temperature



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...es I, II, and III below define the timing characteristics of ...e Am2901A at 25°C. The tables are divided into three types ...of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

All values are at 25°C and 5.0V. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V.

TIME	TYPICAL	GUARANTEED
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	55ns	
Maximum Clock Frequency to Shift Q Register (50% duty cycle) I = 432 or 632	40MHz	
Minimum Clock LOW Time	30ns	
Minimum Clock HIGH Time	30ns	
Minimum Clock Period	75ns	

Note: The Data in this data sheet contains expected typical performance for the Am2901A. As a rule, worst case AC limits will be approximately 1.5 times typical over the commercial range and approximately 2.0 times typical over the military range. Be sure to contact Advanced Micro Devices for the latest data.

TABLE II

COMBINATIONAL PROPAGATION DELAYS (all in ns, $C_L \leq 50pF$)

From Input \ To Output	TYPICAL 25°C, 5.0V								GUARANTEED 25°C, 5.0V							
	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	45	45	45	40	65	50	60	—								—
D (arithmetic mode)	30	30	30	25	45	30	40	—								—
D (I = X37) (Note 5)	30	30	—	—	45	—	40	—			—	—		—		—
C_n	20	20	10	—	35	20	30	—				—				—
I_{012}	35	35	35	25	50	40	45	—								—
I_{345}	35	35	35	25	45	35	45	—								—
I_{678}	15	—	—	—	—	—	20	20		—	—	—	—	—		
$\overline{OE}$ Enable/Disable	20/20	—	—	—	—	—	—	—		—	—	—	—	—	—	—
A bypassing ALU (I = 2xx)	30	—	—	—	—	—	—	—		—	—	—	—	—	—	—
Clock (Note 6)	40	40	40	30	55	40	55	20								

TABLE III

SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	TYPICAL 25°C, 5.0V		GUARANTEED 25°C, 5.0V	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
A, B Source	2, 4 3, 5	40 $t_{pw}L + 15$	0		0
B Dest.	2, 4	$t_{pw}L + 15$	0		0
D (arithmetic mode)		25	0		0
D (I = X37) (Note 5)		25	0		0
C_n		15	0		0
I_{012}		30	0		0
I_{345}		30	0		0
I_{678}	4	$t_{pw}L + 15$	0		0
$RAM_{0, 3}$. $Q_{0, 3}$		15	0		0

Notes: 1. See next page.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B test" set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. DV 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

Am2901B

Four-Bit Bipolar Microprocessor Slice

Advanced Micro Devices
Bipolar Microprocessor Circuits

DISTINCTIVE CHARACTERISTICS

- Plug-in replacement for Am2901 and Am2901A
- Up to 27% faster than Am2901A, up to 50% faster than 2901
- High reliability plastic and cerdip packages
- Available now

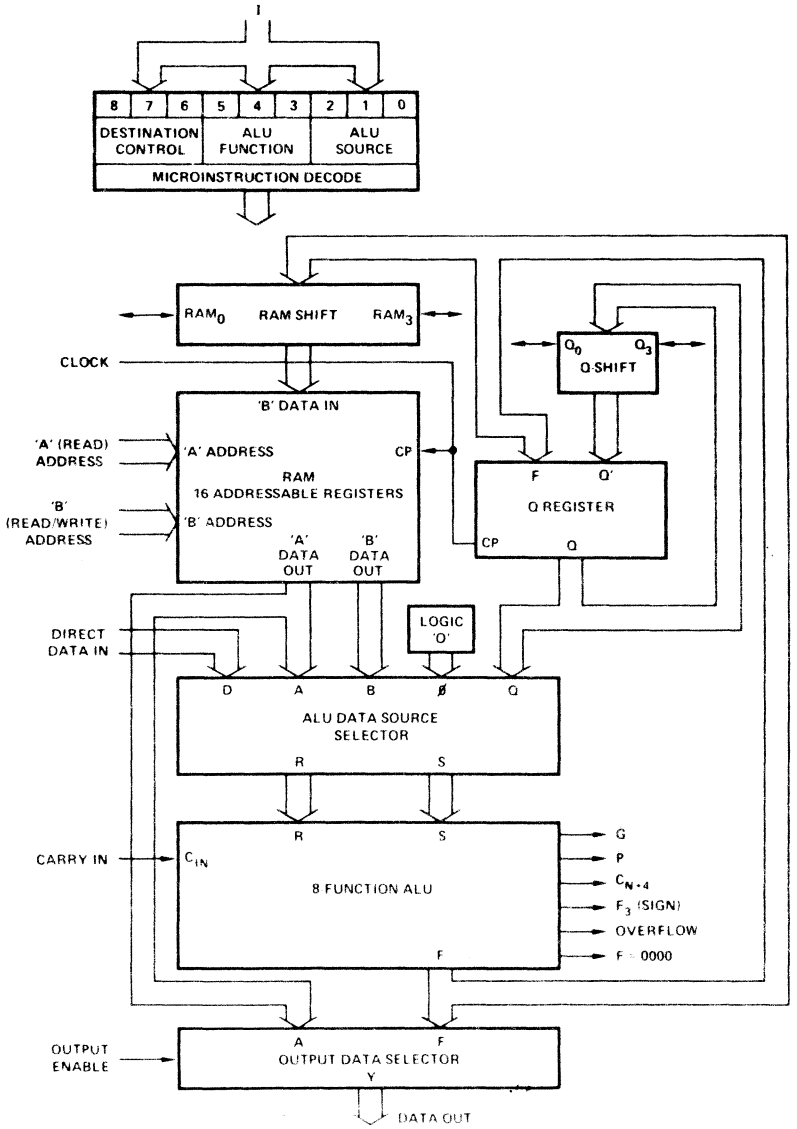
For applications information see the Am2900 Family Data Book and Chapters III and IV of "Build a Microcomputer", AMD's application series on the Am2900 family.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901B will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip. The Am2901B is a plug in replacement for the Am2901 or Am2901A.

MICROPROCESSOR SLICE BLOCK DIAGRAM



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Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

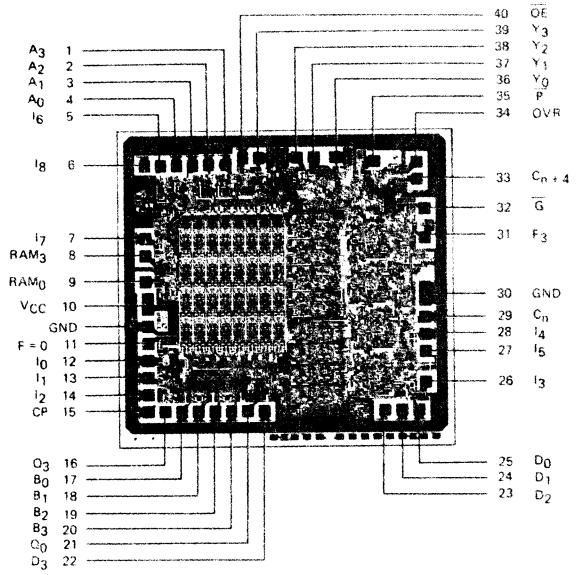
Figure 4. ALU Destination Control.

OCTAL I_{210} / I_{543} / ALU Source / ALU Function	OCTAL 0	1	2	3	4	5	6	7
	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	Q	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus, − = Minus, ∨ = OR, ∧ = AND, ∀ = EX OR

Figure 5. Source Operand and ALU Function Matrix.

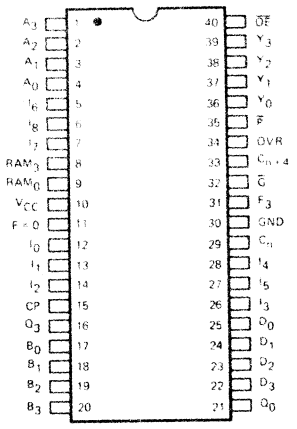
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.117" X 0.128"

Top View

DIP



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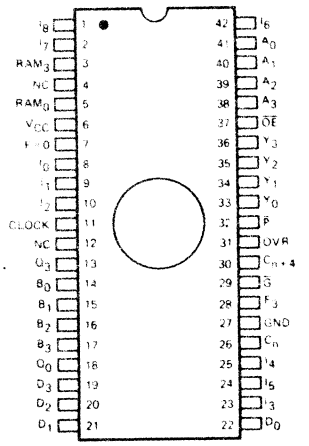
Top View



MPR-007

Note: Pin 1 is marked for orientation.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$,$\overline{G}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) i the data on the four ALU outputs F_{0-3} are all LOW. I positive logic, it indicates the result of an ALU operation i zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outpu change on the clock LOW-to-HIGH transition. The clo LOW time is internally the write enable to the 16 x 4 R/ which compromises the "master" latches of the regis stack. While the clock is LOW, the "slave" latches on RAM outputs are closed, storing the data previously the RAM outputs. This allows synchronous master-sl operation of the register stack.

transition occurs.

PRELIMINARY DATA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX. (See Fig. 12)	Am2901BPC, DC	T_A = 25°C		160	250	mA
				T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am2901BDM, FM	T_C = −55°C to +125°C			265	
				T_C = +125°C			198	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901BXM, DM, FM. "COM'L = Am2901BXC,•PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

I. Typical Room Temperature Performance

The tables below specify the typical performance of the Am2901B at 25°C and 5.0V. All data are in ns, with inputs changing between 0V and 3V at 1V/ns and measurements made at 1.5V. For guaranteed data, see following pages.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	51ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	33MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	60ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	38	41	39	33	44	44	50	–
D	22	23	24	20	28	29	31	–
Cn	17	19	13	–	22	19	26	–
I012	30	30	29	22	34	34	38	–
I345	32	32	30	25	32	30	34	–
I678	17	–	–	–	–	–	16	16
A Bypass ALU (I = 2XX)	22	–	–	–	–	–	–	–
Clock ↓	29	31	29	23	33	35	40	19

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	51 (Note 4)	0
B Destination Address	11	Do Not Change		0
D	–	–	39	0
Cn	–	–	33	0
I012	–	–	46	0
I345	–	–	42	0
I678	5	Do Not Change		0
RAM0, 3, Q0, 3	–	–	9	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	12	27

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5.

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	77ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	77ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	23	–	37	29	38	–
I012	50	47	45	35	56	53	57	–
I345	49	48	44	45	54	49	53	–
I678	28	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37		55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	25	0 (Note 3)	77 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	57	0
Cn	–	–	53	0
I012	–	–	70	0
I345	–	–	66	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

III. Guaranteed Military Range Performance

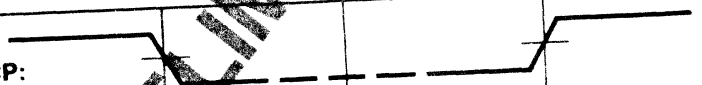
The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	97ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	97ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	–
D	44	38	39	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	37	59	55	58	–
I345	53	50	46	44	58	50	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ↓	53	50	49	41	63	58	61	31

C. Set-up and Hold Times Relative to Clock (CP) Input.

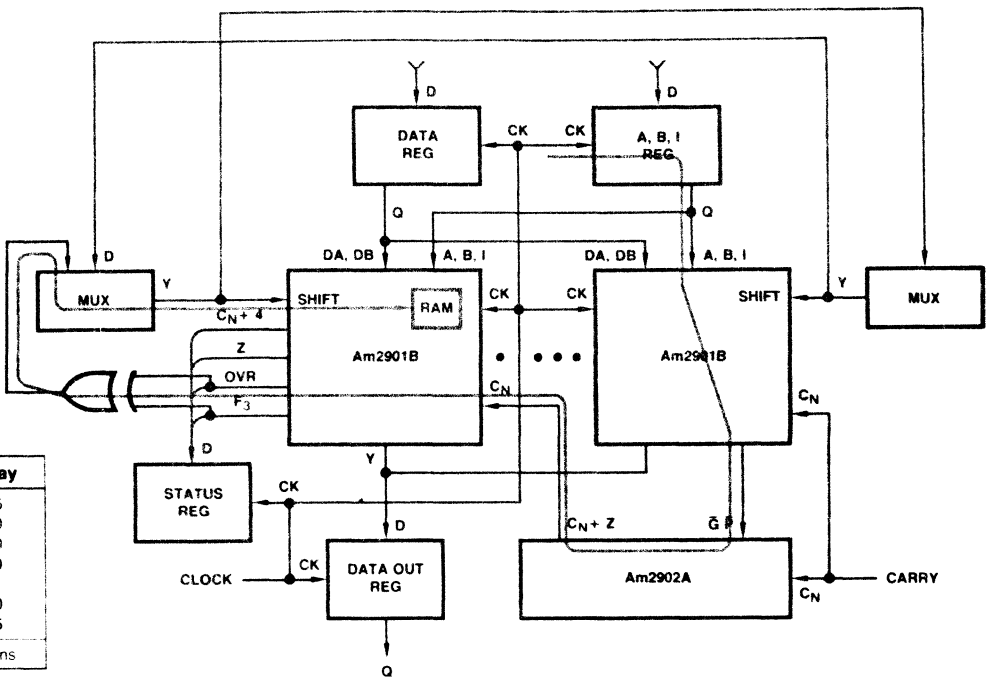


Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	97 (Note 4)	0
B Destination Address	15	Do Not Change		0
D	–	–	60	0
Cn	–	–	55	0
I012	–	–	73	0
I345	–	–	73	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	40	35

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

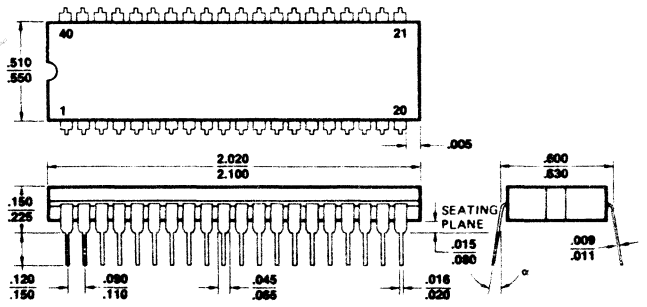


Device	Path	Delay
Register	Cp to Q	15
2901B	A, B to $\overline{G}$, $\overline{P}$	50
2902A	$\overline{G}$, $\overline{P}$ to C_{n+z}	10
2901B	C_n to F_3, OVR	29
XOR gate	in to out	11
Mux	D to Y	10
2901B	RAM_3 set-up	15
Total		140ns

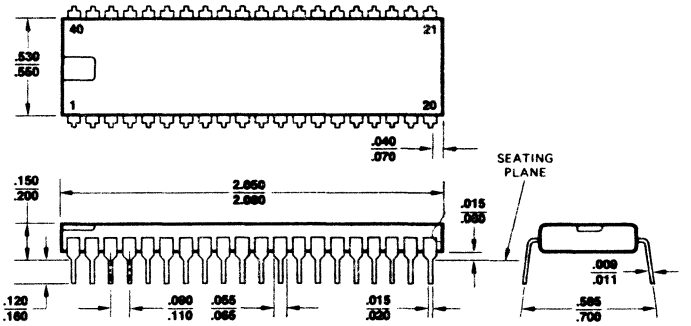
Example of speed calculation for two's complement arithmetic operation with shift down. The worst case speed path is shown in half-tone. For more detailed timing analysis, see Chapter III of "Build a Microcomputer," AMD's application series on the 2900 family.

PACKAGE OUTLINES

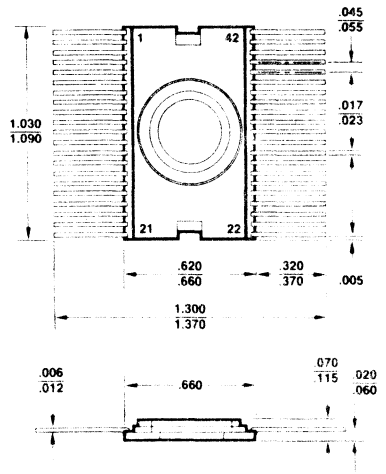
Cerdip
D-40-1



Molded
P-40-1



Flatpack
F-42-1



ORDERING INFORMATION

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2901BPC	P-40	C	C-1
AM2901BDC	D-40	C	C-1
AM2901BDC-B	D-40	C	B-1
AM2901BDM	D-40	M	C-3
AM2901BDM-B	D-40	M	B-3
AM2901BFM	F-42	M	C-3
AM2901BFM-B	F-42	M	B-3
AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2901BXM	Dice	M	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

ADVANCED MICRO DEVICES, INC.,

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National Semiconductor

IDM2901A 4-Bit Bipolar Microprocessor

General Description

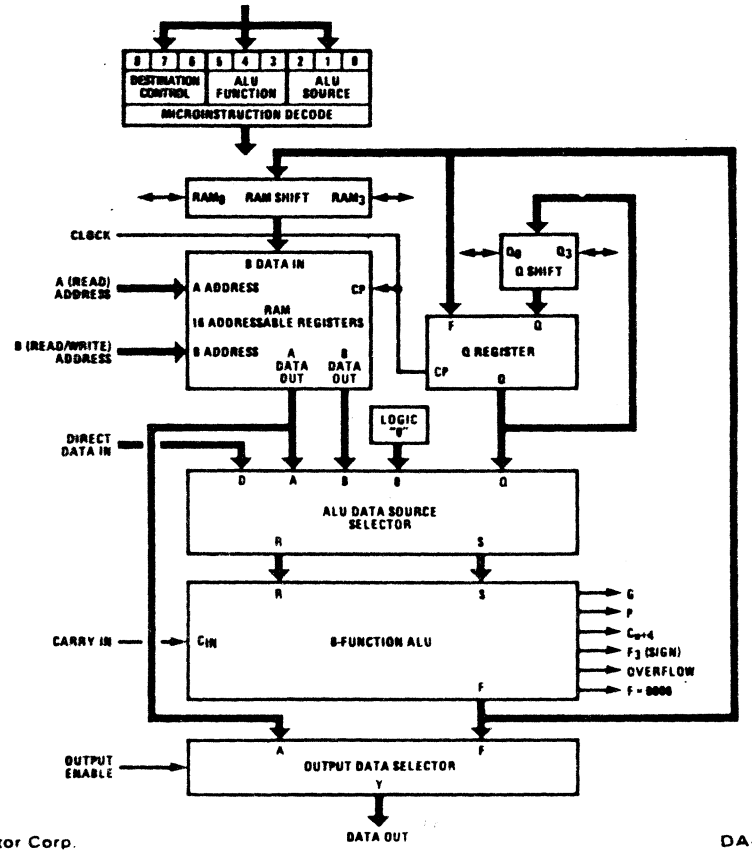
The IDM2901A 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisites. The building-block architecture and microinstruction format of the IDM2901A permits efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901A device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each – the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using state-of-the-art (Low-Power Schottky) technology.

Features and Benefits

- **Multiple-address architecture** – improves sys... speed by providing simultaneous yet independ... access to two working registers.
- **Multifunction ALU** – performs addition, two's... traction operations, and five logic functions on ... source operands.
- **Flexible data-source selection** – for every A... function, data is selected from five source ports fo... total of 203 source operand pairs.
- **Left/right shift independent of ALU** – an arithme... operation and a left or right shift can be obtained ... the same machine cycle.
- **Four status flags** – carry, overflow, zero, and fu... tional sign are available as outputs.
- **Expandable** – Connect any number of IDM2901... together for longer word lengths.
- **Microprogrammable** – three groups of 3 bits each f... source operand, ALU function, and destinati... control.

Block Diagram



DA-B20M77/Printed in

olute Maximum Ratings

e Temperature	−65°C to +150°C
erature (Ambient) Under Bias	−55°C to +125°C
y Voltage to Ground Potential	−0.5 V to +6.3 V
oltage Applied to Outputs for Output State	−0.5 V to +V_{CC} max
put Voltage	−0.5 V to +5.5 V
utput Current, into Outputs	30 mA
put Current	−30 mA to +5.0 mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM2901A DC, PC	0°C to +70°C	4.75 V to 5.25 V
IDM2901A DM, FM	−55°C to +125°C	4.50 V to 5.50 V

ndard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level DC, PC	Level DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

ctrical Characteristics Over Operating Range

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA; C_{n+4}	2.4			
			I_{OH} = −800 µA; OVR/P	2.4			
			I_{OH} = −600 µA; F_3	2.4			
			I_{OH} = −600 µA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

Electrical Characteristics (cont'd.)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$			0.5	V
				I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$			0.5	
				I_{OL} = 16 mA; G/F = 0			0.5	
				I_{OL} = 10 mA; C_{n+4}			0.5	
				I_{OL} = 10 mA; OVR/$\overline{P}$			0.5	
				I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max; V_{IN} = 0.5 V		Clock/$\overline{OE}$/C_n			−0.36	mA
				$A_0/A_1/A_2/A_3$			−0.36	
				$B_0/B_1/B_2/B_3$			−0.36	
				$D_0/D_1/D_2/D_3$			−0.36	
				$I_0/I_1/I_2/I_6$			−0.36	
				$I_3/I_4/I_5$			−0.36	
				I_7/I_8			−0.72	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V		Clock/OE			20	μA
				$A_0/A_1/A_2/A_3$			20	
				$B_0/B_1/B_2/B_3$			20	
				$D_0/D_1/D_2/D_3$			20	
				$I_0/I_1/I_2/I_6/I_8$			20	
				$I_3/I_4/I_5/I_7$			20	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			100	
				C_n			20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V, V_O = 0.5 V	$Y_0/Y_1/Y_2/Y_3/G$		−30		−85	mA
			C_{n+4}		−30		−85	
			OVR/$\overline{P}$		−30		−85	
			F_3		−30		−85	
			$RAM_{0,3}/Q_{0,3}$		−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max	T_A = 25°C			180	250	mA
			DC	T_A = 0°C to +70°C		180	265	
				T_A = +70°C		180	230	
			DM	T_C = −55°C to +125°C		180	280	
				T_C = +125°C		180	190	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25°C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

Note 5: "Mil" = IDM2901A DM, FM; "Com'l" = IDM2901A DC, PC.

Note 6: Worst case I_{CC} is at minimum temperature.

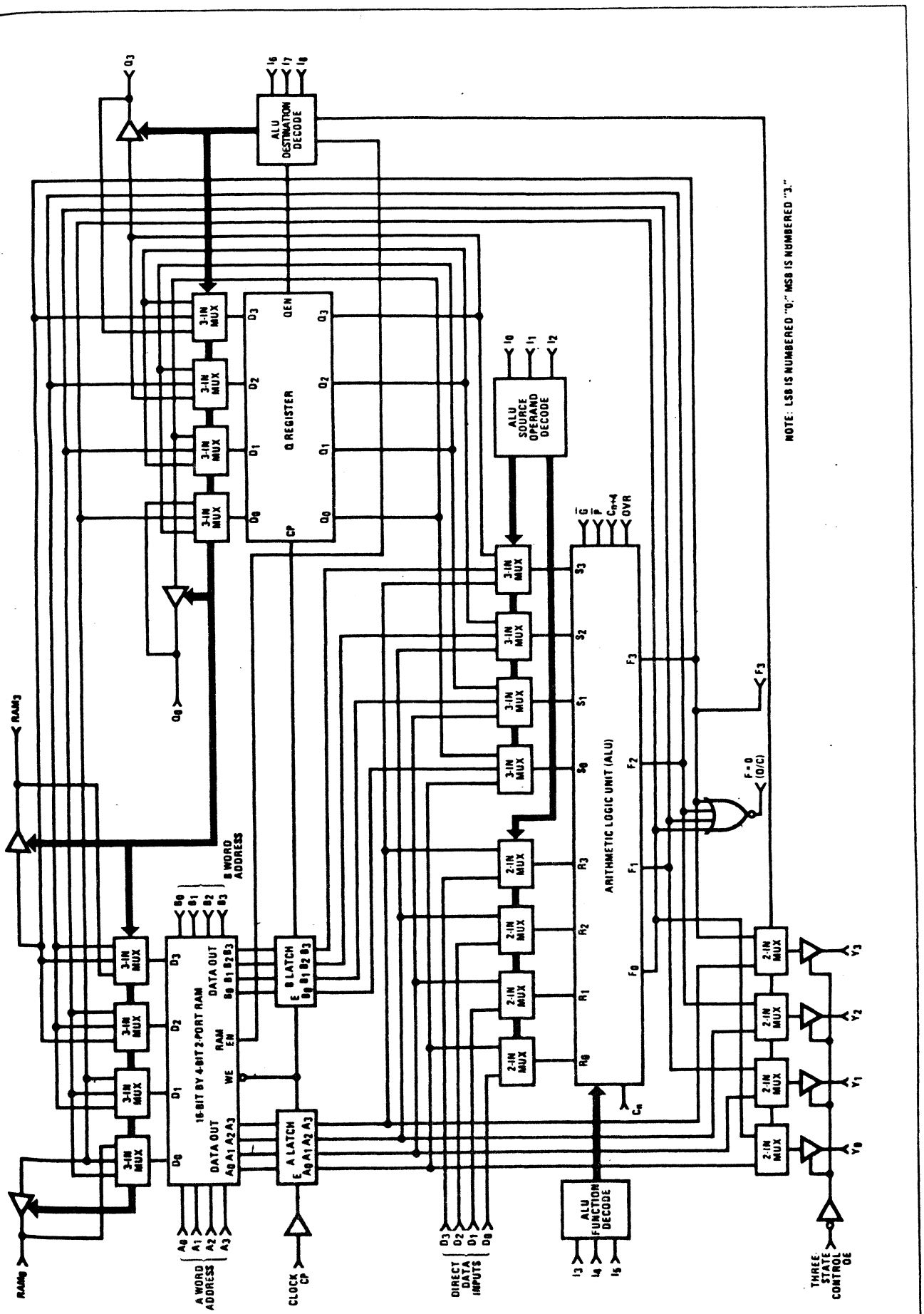


Figure 1. IDM2901A Microprocessor, Detailed Block Diagram

Figure 1 shows a detailed block diagram of the IDM2901A. Observe that all data paths are 4 bits wide; however, the 4-bit slice can be cascaded to the number of bits required for a particular application. Although all parts of the bipolar device are important, the two key elements are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Any one of the 16 words in RAM can be read from the A-port (A_3 - A_0) or the B-port (B_3 - B_0); the selected word for the A-port is determined by the 4-bit A-address field, whereas the B-address field controls the output of the B-port. If the two address codes are identical, the same file data appears simultaneously at both output ports (A and B).

When enabled by RAM EN, new data is written into the file "word" defined by the B-address field; the write function is implemented when the clock input is low.

Each bit of data to be written is input via a 3-input multiplexer; this scheme permits shifting up one bit position (from LSB towards MSB), shifting down one bit position (from MSB towards LSB), or not shifting at all. A similar scheme is used when data is written into the "Q" register.

Each of the A and B data ports drives an associated 4-bit latch. These latches hold the RAM data while the clock input is low; consequently, any possibility of race conditions when writing new data is eliminated.

The high-speed ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words (R_3 - R_0 and S_3 - S_0). The R-input field is driven from a 2-input multiplexer, whereas the S-input field is driven by a 3-input multiplexer. Both the R- and S-multiplexers have an inhibit capability, where no data is passed is equivalent to a "zero" source operand. Refer figure 1, observe that the A-port output of the RA the 4-bit direct-data inputs (D_3 - D_0) are connec the R-input multiplexers; the S-input multiplex three inputs – one from the A-port of RAM, on the B-port of RAM, and one from the Q-register.

With the foregoing input-multiplexer scheme, the (A, B, D, Q, and "Zero"), when taken in pairs, p any one of ten source operands for the ALU – A AQ, A0, BD, BQ, B0, DQ, D0, and Q0. When the B address fields for RAM are identical, it is cle certain combinations (AD/BD, AQ/BQ, and A0/B redundant; that is, the identical function is implem for either operand. Only seven of the combinatio completely nonredundant. Eight of the ten co tions (source operands) are implemented by IDM2901A microprocessor. The ALU source ope are selected by three microinstruction inputs – I_0 and I_2. These inputs are defined in figure 2. Each preceding D and Q operands provides an eas function. The D input (direct-data) is used to loa working registers inside the 2901 device; also, this source can be used to modify data files within the A The Q-register is an internal 4-bit data source th well suited for a multiply/divide operation; however, some applications, it can be used as a data-hol register or as an accumulator.

The ALU is a high-speed arithmetic/logic operator th capable of performing three binary arithmetic funct and five logic functions. Three microinstruction inp (I_3, I_4, and I_5) are used to select one of the e functions; these inputs, along with their octal codes, defined in figure 3.

Micro Code				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Micro Code				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ∨ S
H	H	H	7	R EX-NOR S	$\overline{R \vee S}$

Figure 3. ALU Function Control

Normally, the look-ahead carry mode is used when cascading the ALUs of several microprocessor devices. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) outputs are suitable for use in a carry-look-ahead generator. A carry-out (C_{n+4}) is also generated and is available for use as the carry flag in a status register or as a ripple-carry output. Both carry-in (C_n) and carry-out (C_{n+4}) are active-high signals. Three other status-oriented outputs are available from the ALU; these are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU, and, without enabling the TRI-STATE outputs, it can be used to determine positive or negative results. When enabled, the logic level of F_3 is identical to that of sign bit Y_3. The F = 0 output is used for zero detect; F = 0 is high when all F outputs are low. The F = 0 output is of the open-collector type and can be wire ORed between microprocessor slices. The overflow (OVR) output is used to flag arithmetic operations that exceed the available twos-complement number range. When an overflow exists (C_{n+3} and C_{n+4} are of opposite polarity), the OVR output is high.

Outputs from the ALU can be stored in the register file or the Q register, or can be transmitted to the outside world. Eight possible destination codes are defined by microinstruction inputs I_6, I_7, and I_8; the various destination control codes are shown in figure 4. The 4-bit data field (Y_3-Y_0) is a TRI-STATE output that can be directly bus organized. The Y outputs are enabled by $\overline{OE}$; when this control signal is high, the Y-outputs are TRI-STATEd. A 2-input multiplexer is also used at the Y-output port to select either the A port of RAM or the F output of the ALU; this selection is controlled by the previously described microinstruction inputs (I_6, I_7, and I_8).

As previously described, the RAM inputs (register file) are driven by a 3-input multiplexer. Thus, outputs from the ALU can be entered nonshifted, shifted up (towards MSB) one position (x 2), or shifted down (towards LSB) one position (÷ 2). The shifter is equipped with two ports — RAM_0 and RAM_3; both ports consist of a TRI-STATE buffer-driver, each of which supplies one input to the foregoing multiplexer. In the shift-up (x 2) mode, the RAM_3 output driver and the RAM_0 multiplexer input are enabled, whereas in the shift-down (÷ 2) mode, the RAM_0 output driver and RAM_3 multiplexer input are enabled; in the no-shift mode, both drivers are TRI-STATE and neither multiplexer input is enabled. The shifter is controlled by the I_6, I_7, and I_8 microinstruction inputs.

The Q register likewise is driven from a 3-input multiplexer and the Q shifter is equipped with two input/output ports — Q_0 and Q_3. Operation of these two ports is similar to that of the RAM shifter, and the ports are controlled by I_6, I_7, and I_8. In the shift-up or shift-down modes, the Q register is shifted in a specified direction with the input/output terminals of the register being an input (for a shift-up) or an output (for a shift-down). In the no-shift mode, the multiplexer may enter the ALU data into the Q register; in this case, input/output lines of the register are TRI-STATE.

The clock input shown in figure 1 controls the RAM, the A and B latches, and the Q register. When the clock input is high, the A and B latches are open and data from the RAM outputs is allowed to pass through to the ALU or "Y" outputs. When the clock input is low, both latches are closed and the last data entered is retained. When the clock input is low and if the input control code (I_6, I_7, and I_8) has enabled a file-write operation, new data, as defined by the 4-bit B-address field, is written into the RAM file. When enabled, data is clocked into the Q register on the low-to-high transition of the clock pulse.

Source Operands and ALU Functions

Any one of eight source operand pairs can be selected by instruction inputs I_0, I_1, and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU — five logic and three arithmetic functions. In the arithmetic mode, the carry input (C_n) also affects the ALU functions; the carry input has no effect on the "F" result in the logic mode. These control parameters (I_6-I_0 and C_n) are summarized in figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input will affect the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states ($C_n = 0/C_n = 1$) are defined in the function matrices.

Figure 4. ALU Destination Control

Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 5. Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$	$I_{2,1,0}$ Octal / ALU Source / ALU Function	0	1	2	3	4	5	6	7
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	A ∀ Q	A ∀ B	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; V = OR, ∧ = AND; ∀ = EX-OR.

Figure 6. ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}/I_{2,1,0}$	Group	Function
40 41 45 46	AND	A ∧ Q A ∧ B D ∧ A D ∧ Q
30 31 35 36	OR	A V Q A V B D V A D V Q
60 61 65 66	EX-OR	A ∀ Q A ∀ B D ∀ A D ∀ Q
70 71 75 76	EX-NOR	$\overline{A \forall Q}$ $\overline{A \forall B}$ $\overline{D \forall A}$ $\overline{D \forall Q}$
72 73 74 77	INVERT	$\overline{Q}$ $\overline{B}$ $\overline{A}$ $\overline{D}$
62 63 64 67	PASS	Q B A D
32 33 34 37	PASS	Q B A D
42 43 44 47	"ZERO"	0 0 0 0
50 51 55 56	MASK	$\overline{A}$ ∧ Q $\overline{A}$ ∧ B $\overline{D}$ ∧ A $\overline{D}$ ∧ Q

Figure 7. ALU Arithmetic Mode Functions

Octal $I_{5,4,3}/I_{2,1,0}$	C_n = 0 (Low)		C_n = 1 (High)	
	Group	Function	Group	Function
00 01 05 06	ADD	A + Q A + B D + A D + Q	ADD plus one	A + Q + 1 A + B + 1 D + A + 1 D + Q + 1
02 03 04 07	PASS	Q B A D	Increment	Q + 1 B + 1 A + 1 D + 1
12 13 14 27	Decrement	Q − 1 B − 1 A − 1 D − 1	PASS	Q B A D
22 23 24 17	1s Comp	− Q − 1 − B − 1 − A − 1 − D − 1	2s Comp (Negate)	− Q − B − A − D
10 11 15 16 20 21 25 26	Subtract (1s Comp)	Q − A − 1 B − A − 1 A − D − 1 Q − D − 1 A − Q − 1 A − B − 1 D − A − 1 D − Q − 1	Subtract (2s Comp)	Q − A B − A A − D Q − D A − Q A − B D − A D − Q

ogic Functions for G, P, Cn+4, nd OVR

n the IDM2901A is in the add or the subtract mode, signals (G, P, C_{n+4}, and OVR) are available to dicate carry and overflow conditions. Based on the ht ALU functions, logic equations for these signals as follows. (Note: The "R" and "S" inputs are ected according to figure 2.)

Definitions (+ = OR):

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$= G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

nout Descriptions of IDM 2901A

functions for the IDM2901A 4-bit slice microproces- are as follows:

-A_0 4-bit address field used to select one of the file registers whose contents are displayed through the A port of RAM.

-B_0 4-bit address field used to select one of the file registers whose contents are displayed through the B port of RAM. When the clock is low, new data can be written into the selected B-port register.

-I_0 Nine instruction-control lines — $I_0/I_1/I_2$ determine data sources of ALU, $I_3/I_4/I_5$ select ALU function, and $I_6/I_7/I_8$ select data inputs for the Q register or the register file.

$_3$/RAM_3 Serves as shift data input/output lines for the most significant bit (MSB) of Q register (Q_3) and the register stack (RAM_3). These lines are TRI-STATE outputs that connect to TTL inputs within the IDM2901A device. When the destination code, as defined by $I_6/I_7/I_8$, indicates an up-shift (octal 6 or 7), the TRI-STATE outputs are enabled; accordingly, the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, these output lines are TRI-STATE or serve as LS-TTL inputs. When a down-shift is indicated by the destination code, the Q_3 and RAM_3 pins are used as data inputs to the MSB of the Q register or RAM.

Q_0/RAM_0 These shift lines are similar to Q_3 and RAM_3, except they operate on the least significant bit (LSB) of the Q register and RAM. To transfer data for up- and down-shifts of the Q register and the ALU, the Q_0 and RAM_0 pins are connected, respectively, to the next less-significant device (Q_n and RAM_n) in the cascaded chain.

$D_3 - D_0$ A 4-bit data field that can be selected as a source of external data for ALU — D_0 is the least significant bit.

$Y_3 - Y_0$ 4-bit output data of IDM2901A. These lines are TRI-STATE; when enabled, they provide either the ALU output or data from the A port of the register file — the selected source is determined by the destination code, as defined by I_6, I_7, and I_8.

$\overline{OE}$ When the Output Enable ($\overline{OE}$) signal is high, the Y outputs are inactive; when the signal is active-low, the active high or low outputs are enabled.

$\overline{P}/\overline{G}$ Carry generate and propagate outputs — see figure 8 for logic equations.

OVR The overflow flag corresponds to the exclusive-OR of the carry-in and carry-out of the MSB of the ALU. When set high, it indicates that the result of an arithmetic twos-complement operation has overflowed into the sign bit — see figure 8 for the logic equation.

F = 0 An open-collector output that goes high if all data lines ($F_3 - F_0$) are low, that is, the result of an ALU operation is zero.

C_n Carry-in to ALU.

C_{n+4} Carry-out of ALU — see figure 8 for logic equations.

CP Clock input. Outputs of Q register and file are clocked on low-to-high transition; the low interval of the clock input corresponds to the "write enable" period of the 16-by-4 RAM, that is, the "master" latches of the register file. When the clock is low, the output latches store the data previously held at the RAM outputs; thus, synchronous master-slave operation of the register file is permitted.

F_3 Most significant (sign) bit output of the ALU.

$I_{5,4,3}$	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions.			
2	R − S	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions.			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions.		
6	R ∀ S		Same as R ∀ S equations, but substitute $\overline{R_i}$ for R_i in definitions.		
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	See Note 1	See Note 2

Note 1: $G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})$ Note 2: $(\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n) \forall (\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n)$

Figure 8. Logic Equations for Flag Outputs

Guaranteed Operating Conditions Over Temperature and Voltage

When operated in a system, the timing requirements for the IDM2901A are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A	
	DC, PC	DM, FM
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	20 MHz	16 MHz
Minimum Clock Low Time	25 ns	30 ns
Minimum Clock High Time	25 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

To Output / From Input	Commercial IDM2901A DC, PC (0°C to +70°C; 5 V ± 5%)								Military IDM2901A DM, FM (−55°C to +125°C; 5 V ± 10%)							
	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	70	65	65	60	70	65	70	–	85	80	80	75	85	80	85	–
D (arithmetic mode)	45	45	45	45	55	45	50	–	55	55	55	55	70	55	60	–
D (I = X37)	45	45	–	–	55	–	50	–	55	55	–	–	70	–	60	–
C_n	32	32	20	–	40	30	35	–	40	40	25	–	50	35	45	–
$I_{2,1,0}$	55	50	50	45	60	50	60	–	70	60	60	55	75	60	75	–
$I_{5,4,3}$	50	50	50	45	55	50	50	–	60	60	60	55	70	60	60	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	30	–	–	–	–	–	40	40
$\overline{OE}$ Enable/Disable	30/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	60	60	60	50	60	55	60	35	75	75	75	65	75	70	75	45

Table 3. Setup and Hold Times (all in ns) — Note 1

From Input	Notes	Commercial IDM2901A DC, PC (0°C to +70°C, 5 V ± 5%) Setup Time	Commercial IDM2901A DC, PC (0°C to +70°C, 5 V ± 5%) Hold Time	Military IDM2901A DM, FM (−55°C to +125°C, 5 V ± 10%) Setup Time	Military IDM2901A DM, FM (−55°C to +125°C, 5 V ± 10%) Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		25	0	30	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		20	0	25	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

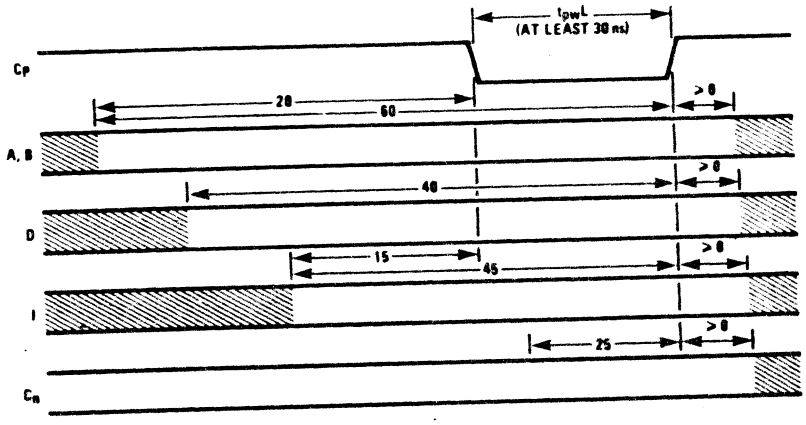
Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

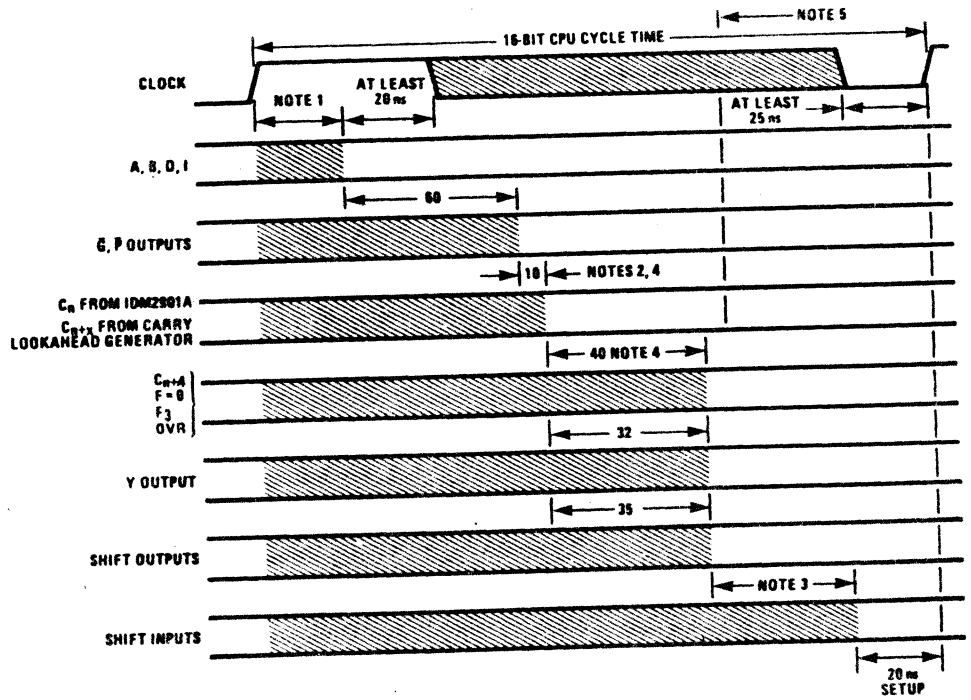
Set-Up and Hold Times (mimimum cycles from each input)

-up and hold times are defined relative to the low-to- transition of the clock pulse. At all times, inputs st be stable from the setup time prior to the clock until the hold time after the clock – observe that all hold times are "zero." The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into the correct register.



Note: Numbers shown are minimum data-stable times in nanoseconds for commercial product – see table 3 for detailed information.

Figure 9. Setup Times for Input Parameters of IDM2901A



Notes:

1. This delay is the max t_{pd} of the register containing A, B, D, and I.
2. 10 ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 60 ns.
3. This is the delay associated with the multiplexer between the shift outputs and the shift inputs on the IDM2901A.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 10. Switching Waveforms for 16-Bit System Assuming A, B, D, and I are Driven from Registers with the Same Propagation Delay and Clocked by the IDM2901A. (These are maximum times in nanoseconds using commercial-product specifications.)

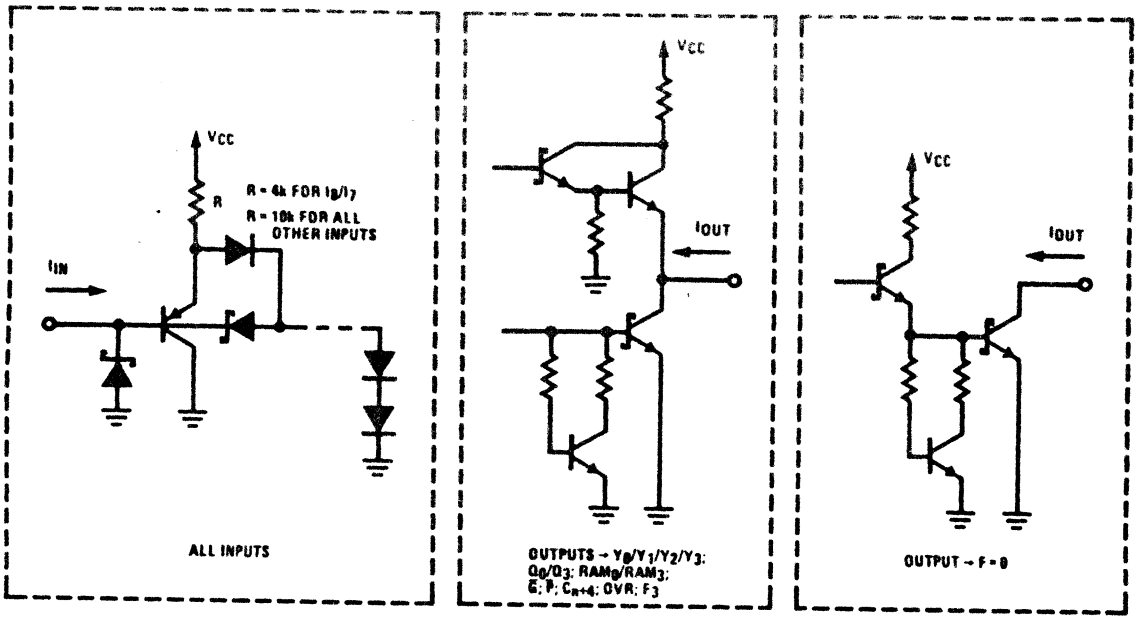


Figure 11. Input/Output Current Interface Conditions for IDM2901A

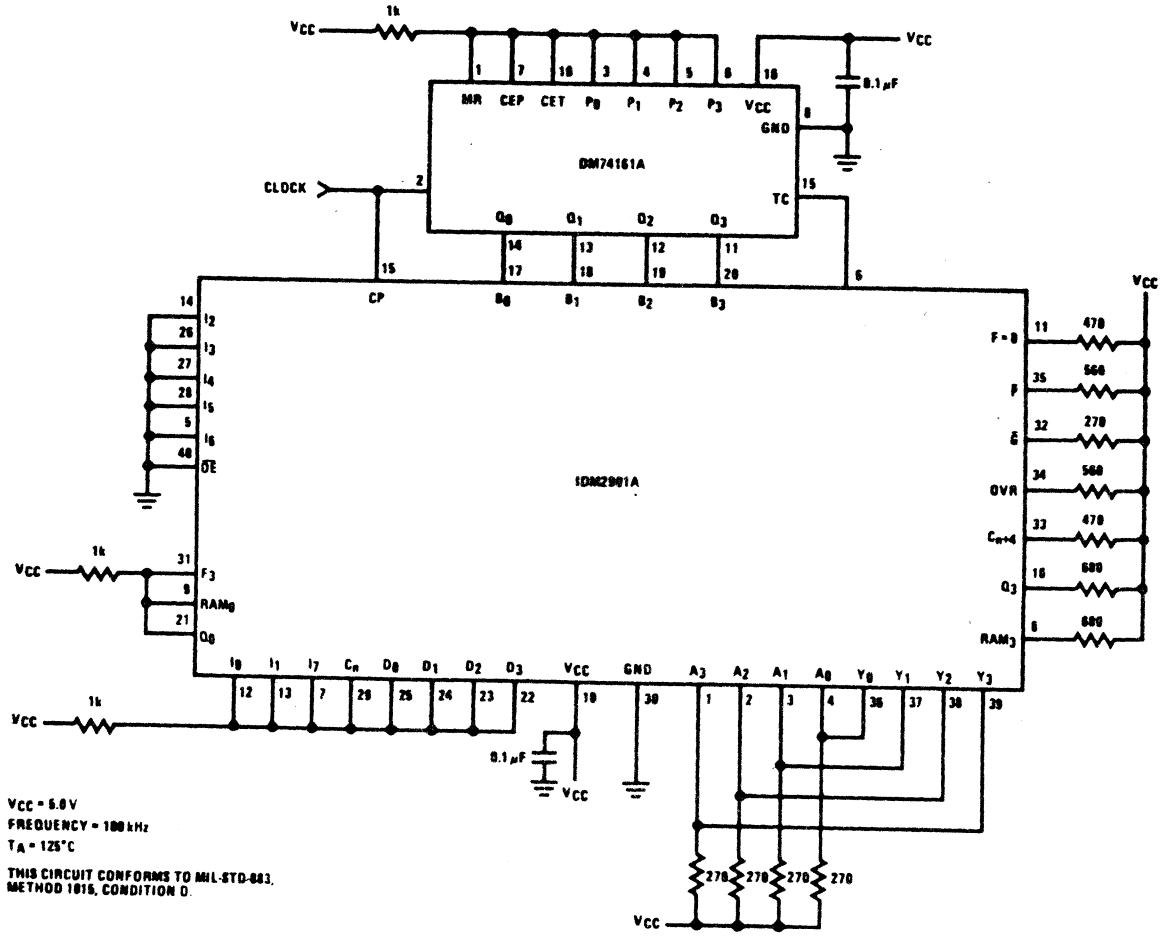
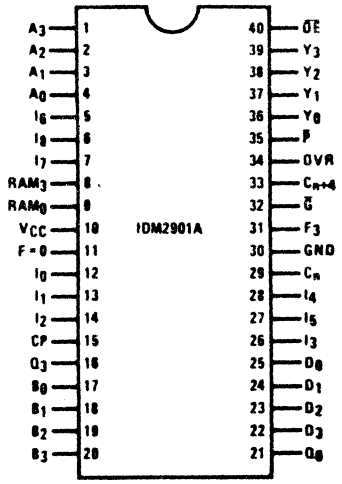


Figure 12. Burn-In Circuit for IDM2901A

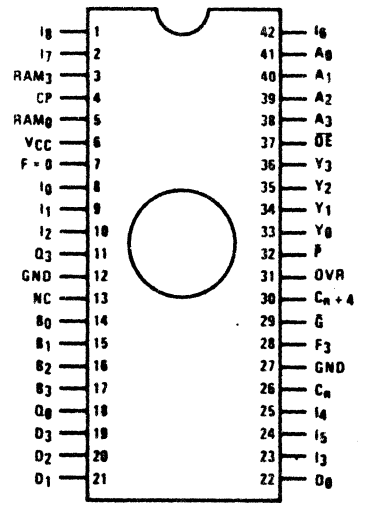
Connection Diagrams

DIP (Top View)



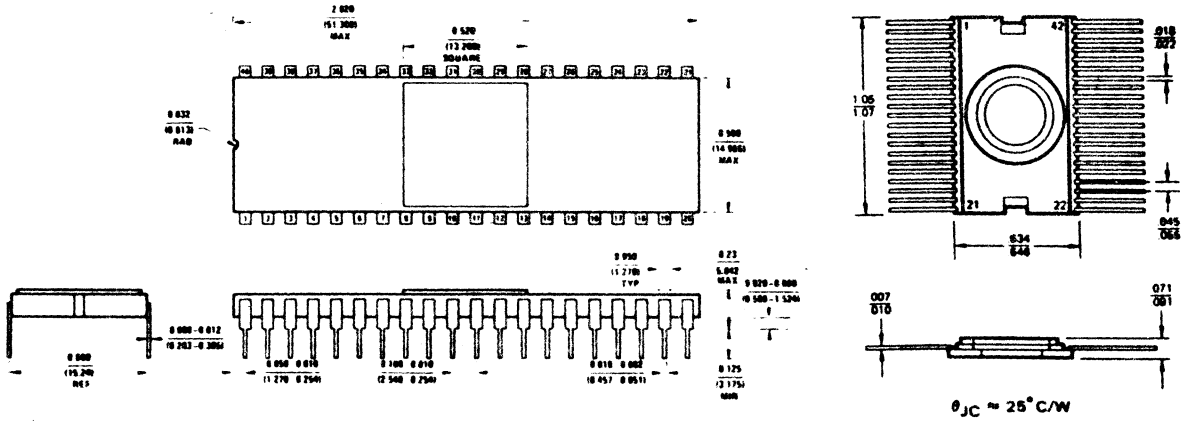
NOTE: PIN 1 IS MARKED FOR ORIENTATION.

Flat Pack (Top View)



NOTE: BOTH GROUNDS (PINS 12 and 27) MUST BE CONNECTED.

Physical Dimensions



$\theta_{JC} \approx 25^{\circ}C/W$

Ordering Information

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	IDM2901APC
Hermetic DIP	0°C to +70°C	IDM2901ADC
Hermetic DIP	−55°C to +125°C	IDM2901ADM
Hermetic Flat Pack	−55°C to +125°C	IDM2901AFM
Dice	0°C to +70°C	IDM2901AXC

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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Larkfield Industrial Estate, Greenock, Scotland, Tele. (0475) 33251/Telex 778-632

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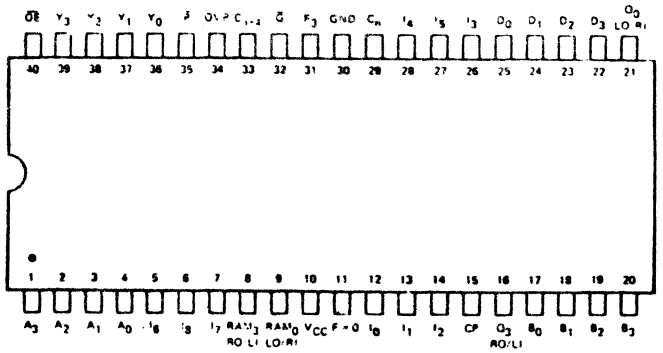
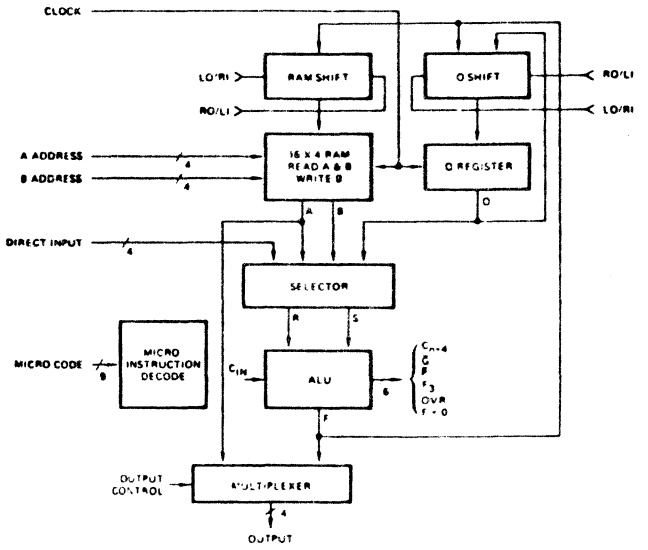
Four-Bit Bipolar Microprocessor Slice

PIN CONFIGURATION



Note: Pin 1 is marked for orientation.

MICROPROCESSOR SLICE BLOCK DIAGRAM



ALU LOGIC MODE FUNCTIONS

$I_5 I_4 I_3 I_2 I_1 I_0$	Octal I_{543} I_{210}	Group	Function
1 0 0 0 0 0	40	AND	A∧Q
0 0 1	41		A∧B
1 0 1	45		D∧A
1 1 0	46		D∧Q
0 1 1 0 0 0	30	OR	A∨Q
0 0 1	31		A∨B
1 0 1	35		D∨A
1 1 0	36		D∨Q
1 1 0 0 0 0	60	EX-OR	A∨Q
0 0 1	61		A∨B
1 0 1	65		D∨A
1 1 0	66		D∨Q
1 1 1 0 0 0	70	EX NOR	$\overline{A \vee Q}$
0 0 1	71		$\overline{A \vee B}$
1 0 1	75		$\overline{D \vee A}$
1 1 0	76		$\overline{D \vee Q}$
1 1 1 0 1 0	72	INVERT	$\overline{Q}$
0 1 1	73		$\overline{B}$
1 0 0	74		$\overline{A}$
1 1 1	77		$\overline{D}$
1 1 0 0 1 0	62	PASS	Q
0 1 1	63		B
1 0 0	64		A
1 1 1	67		D
0 1 1 0 1 0	32	PASS	Q
0 1 1	33		B
1 0 0	34		A
1 1 1	37		D
1 0 0 0 1 0	42	ZERO	0
0 1 1	43		0
1 0 0	44		0
1 1 1	47		0
1 0 1 0 0 0	50	MASK	A∧Q
0 0 1	51		A∧B
1 0 1	55		D∧A
1 1 0	56		D∧Q

ALU ARITHMETIC MODE FUNCTIONS

	Octal	$C_n = 0$		$C_n = 1$	
$I_5 I_4 I_3 I_2 I_1 I_0$	I_{543} I_{210}	Group	Function	Group	Function
0 0 0 0 0 0	0 0	ADD	A+Q	ADD plus one	A+Q+1
0 0 1	0 1		A+B		A+B+1
1 0 1	0 5		D+A		D+A+1
1 1 0	0 6		D+Q		D+Q+1
0 0 0 0 1 0	0 2	PASS	Q	Increment	Q+1
0 1 1	0 3		B		B+1
1 0 0	0 4		A		A+1
1 1 1	0 7		D		D+1
0 0 1 0 1 0	1 2	Decrement	Q-1	PASS	Q
0 1 1	1 3		B-1		B
1 0 0	1 4		A-1		A
0 1 0 1 1 1	2 7		D-1		D
0 1 0 0 1 0	2 2	1's Comp.	-Q-1	2's Comp.	-Q
0 1 1	2 3		-B-1		-B
1 0 0	2 4		-A-1		-A
0 0 1 1 1 1	1 7		-D-1		-D
0 0 1 0 0 0	1 0	Subtract (1's Comp)	Q-A-1	Subtract (2's Comp)	Q-A
0 0 1	1 1		B-A-1		B-A
1 0 1	1 5		A-D-1		A-D
1 1 0	1 6		Q-D-1		Q-D
0 1 0 0 0 0	2 0		A-Q-1		A-Q
0 0 1	2 1		A-B-1		A-B
1 0 1	2 5		D-A-1		D-A
1 1 0	2 6		D-Q-1		D-Q

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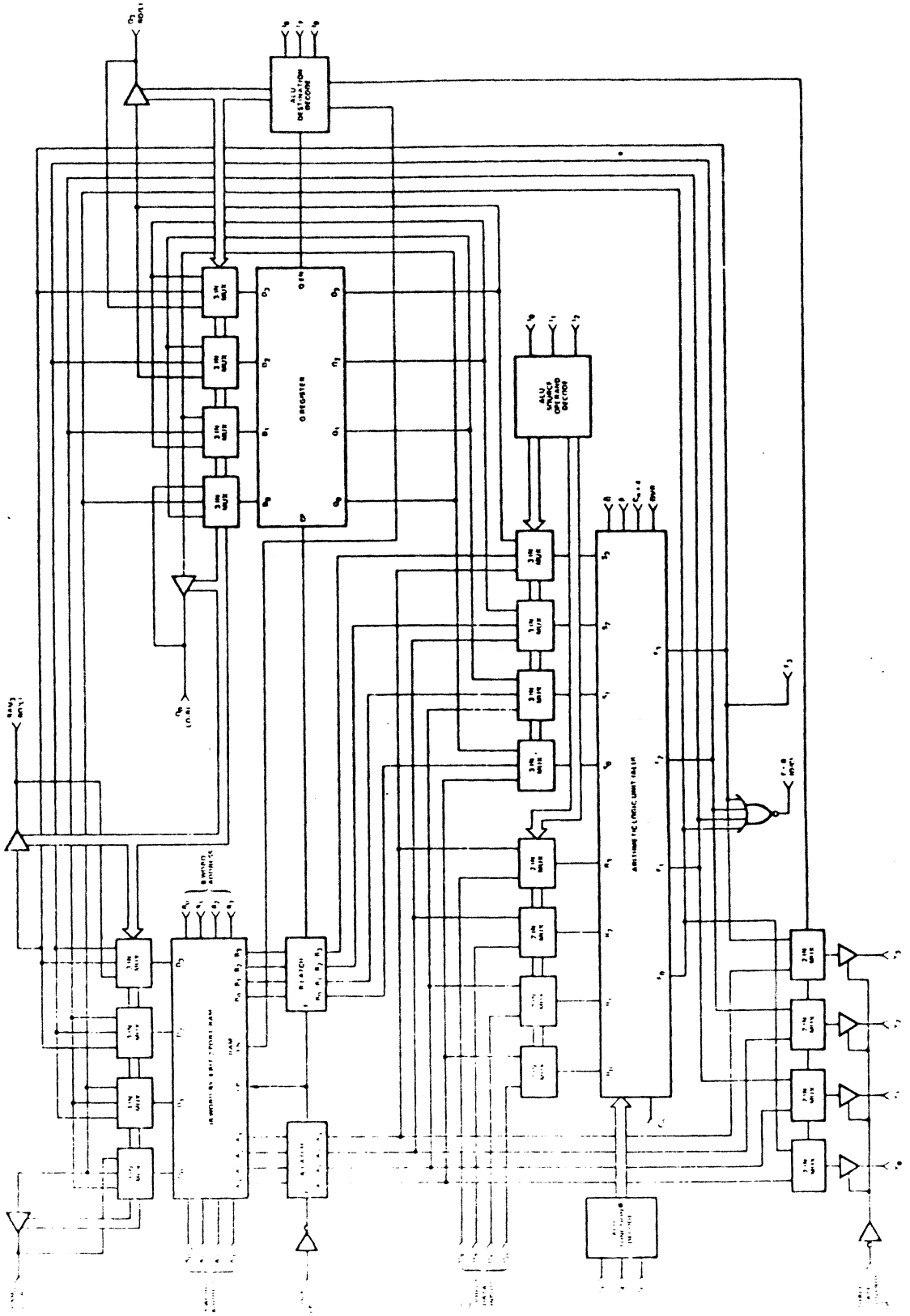
MICROPROCESSOR BLOCK DIAGRAM



100001073
(Continued)

The Q register is also driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports: Q0-LO/RI and Q3-RO/LI. These ports operate in the same way as the RAM shifter and are controlled by I6, I7, and I8.

The RAM, the Q register, and the A and B data latches are controlled by the clock input. When enabled, data is clocked into the Q register on the low-to-high clock transition. When the clock input is high, the A and B latches are open and pass the data present at the RAM outputs. When the clock input is low, the latches are closed and retain the last data entered. If the RAM-EN is enabled, new data is written into the RAM file (word) which is specified by the B address field when the clock input is low.

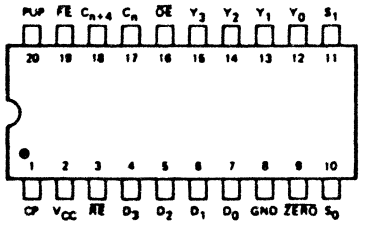
The 100001073 has tri-state outputs.

NOTE *The 100001073 is a low power Schottky device.*

100001074

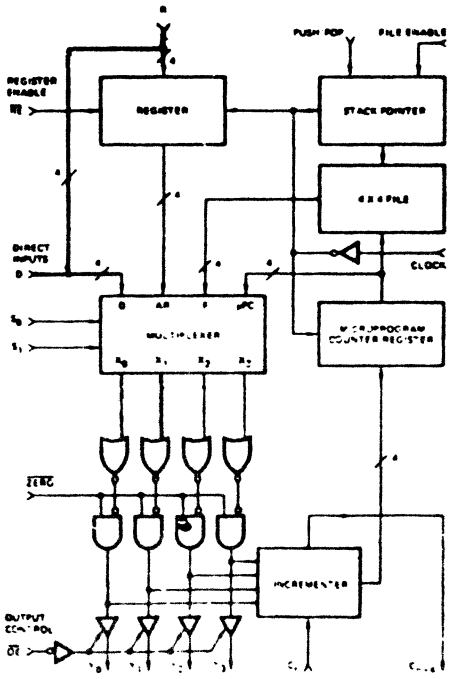
Microprogram Sequencer

PIN CONFIGURATION



Note: Pin 1 is marked for orientation.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



DEFINITION OF TERMS

C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External

A*	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

Inputs

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs

Y_i	Address outputs. (Address inputs to control memory.)

100001074
(Continued)

ADDRESS SELECTION

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

OUTPUT CONTROL

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

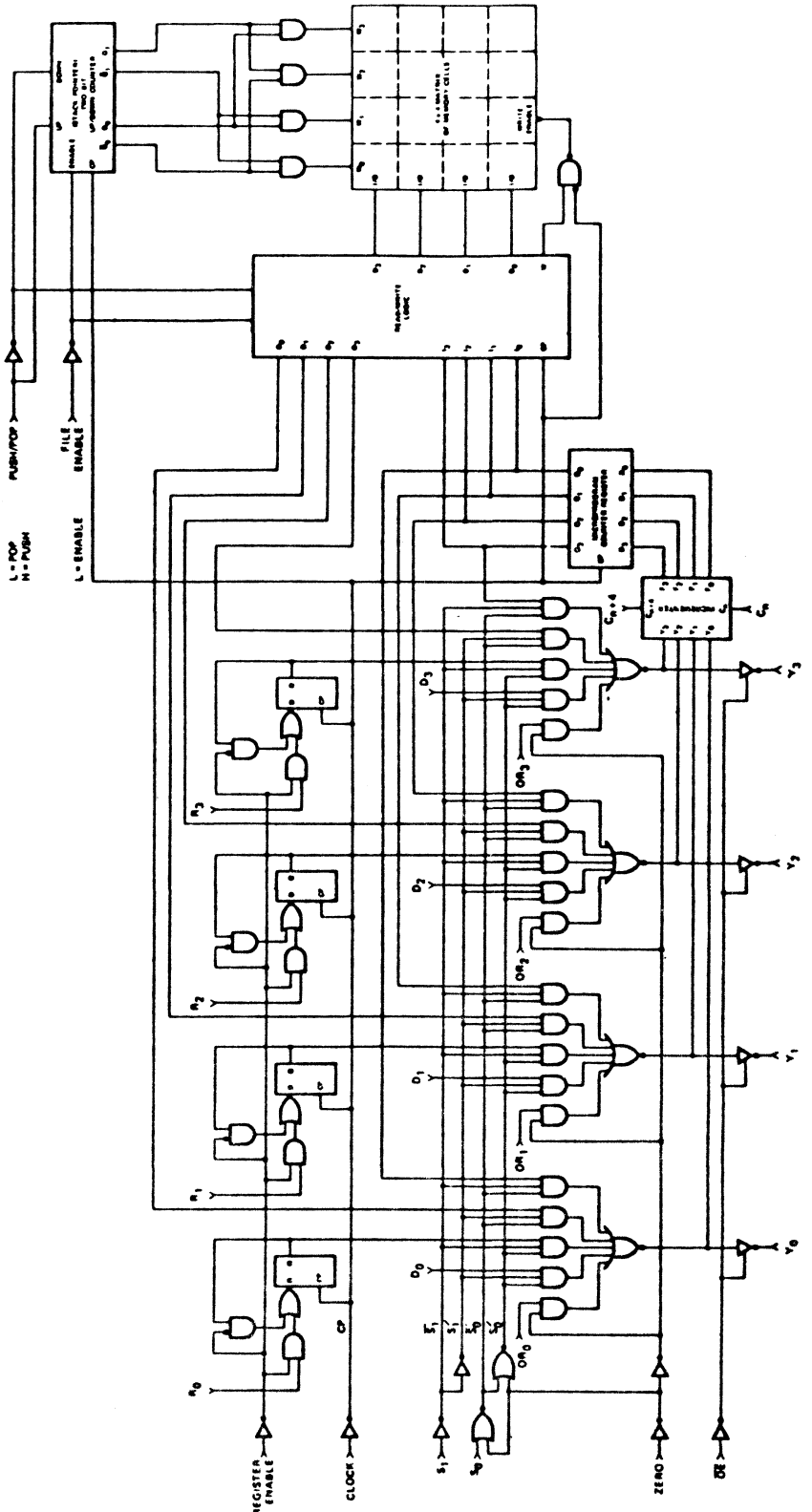
OUTPUT AND INTERNAL NEXT-CYCLE REGISTER STATES

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer

100001074
(Continued)

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



Note: R_i and D_i connected together and OR_i removed.

100001074
(Continued)

The 100001074 is a bipolar microprogram sequencer consisting of a 4-bit cascadable slice. Two 100001074s can address up to 256 words of microprogram and three devices can address up to 4K words of microprogram.

A four-input multiplexer is used select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. The S0 and S1 inputs control this multiplexer.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is low, data enters the register on the low-to-high transition of the clock. The 4-bit direct data inputs are also used as inputs to the register to permit an N-way branch where N is any word in the microcode.

The microprogram counter (uPC) consists of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (Cn) and carry-out (Cn+4). When the least significant carry-in to the incrementer is high, the current Y output word plus one is loaded into the microprogram register on the next clock cycle. In this way, sequential microinstructions can be executed. When the least-significant Cn is low, the incrementer passes the Y unmodified and this same word is loaded into the microprogram register on the next clock cycle. In this way, the same microinstruction can be executed any number of times by using the least-significant Cn as the control.

The file is a 4 x 4 stack which provides the return address linkage when executing microsubroutines. It contains a stack pointer (SP) which points to the last file word written. This permits stack reference operations to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. The Push operation is enabled when the file enable is low and the push/pop input is high. When this happens the stack pointer increments and the file is written with the appropriate return linkage (the next microinstruction address after the subroutine jump which initiated the Push). A Pop operation is enabled when the file enable is low and the push/pop input is low. The stack pointer decrements on the next low-to-high clock transition. When the file enable is high, no action is taken by the stack pointer regardless of any other input.

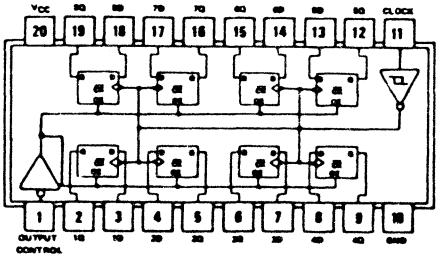
When the Zero input is low, all Y outputs are low regardless of any other inputs (except $\overline{OE}$). Each Y output bit has an independent OR input so a conditional logic one can be forced at each Y output to allow jumping to different microinstructions on programmed conditions.

The 100001074 has tri-state outputs.

100001075

Octal D-Type Edge-Triggered Flip-Flops

PIN CONFIGURATION

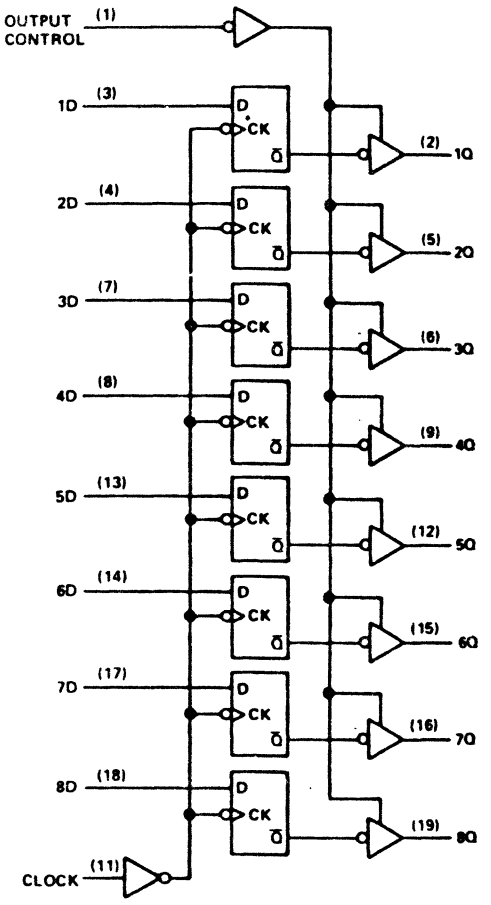


logic: see function table

FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

BLOCK DIAGRAM

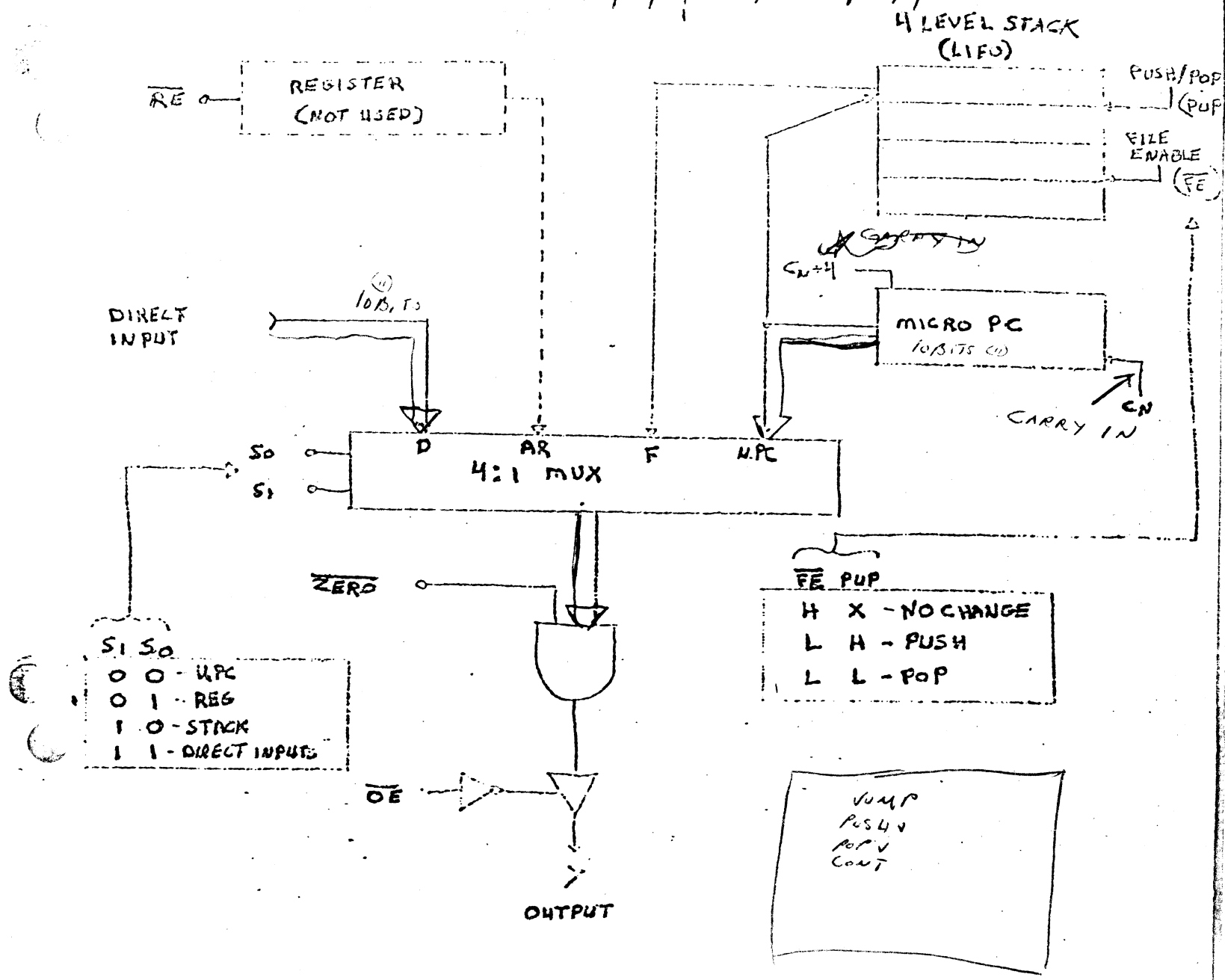


The 100001075 is an 8-bit register containing edge triggered D-type flip-flops with totem-pole tri-state outputs. The D inputs are applied to the Q outputs on the positive transition of the clock.

The buffered output control will place the outputs in a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs can neither load nor drive the bus lines. Data can be retained or new data entered even when the outputs are off.

NOTE *The 100001075 is a low power Schottky device.*

2711 100-1014



1ST ADDR GOES TO M.P.C. (10 BITS

ALLOWS SUB ROUTINES IN MICRO CODE

SIMPLIFIED BLOCK DIAG

Am2909 • Am2911

Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines.
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only).
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package

GENERAL DESCRIPTION

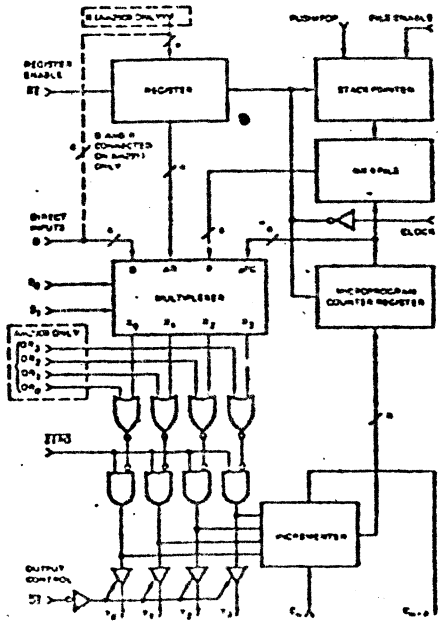
The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package.

TABLE OF CONTENTS

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

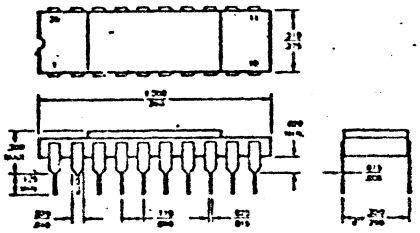
The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

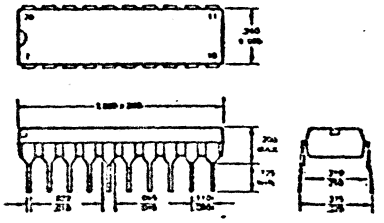
The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

PHYSICAL DIMENSIONS

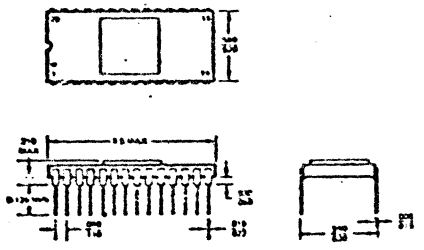
20-Pin Side Brazed



20-Pin Molded



28-Pin Side Brazed



28-Pin Flat Package

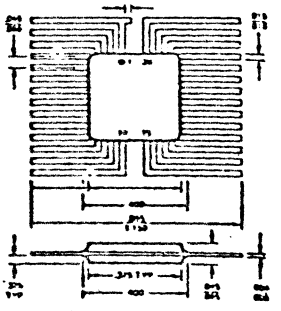
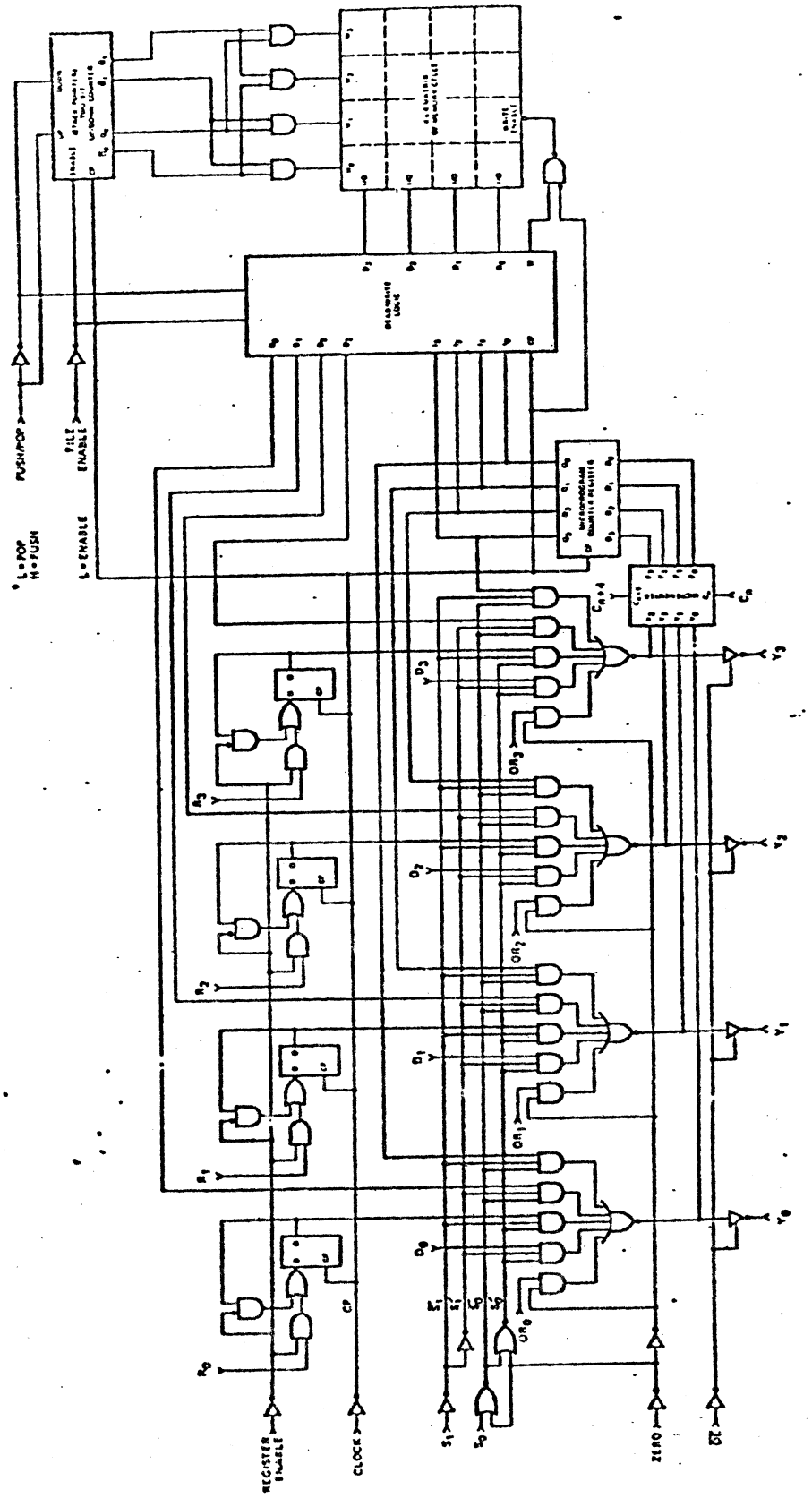


Figure 1.



Note: A_i and D_i connected together on Am2911 and OR_i removed.

Figure 2. Microprogram Sequencer Block Diagram.

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)

Internal Signals

μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

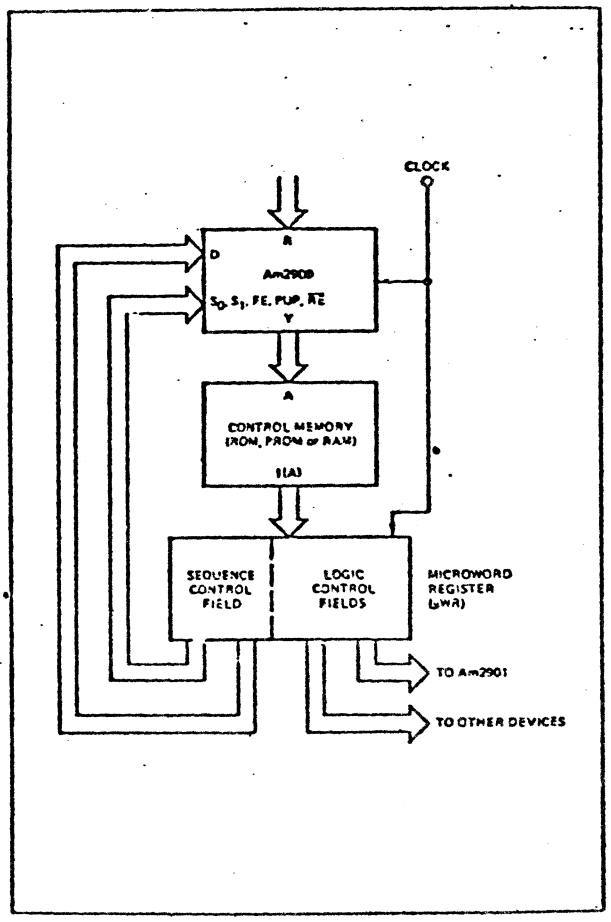


Figure 3. Microprogram Sequencer Control.

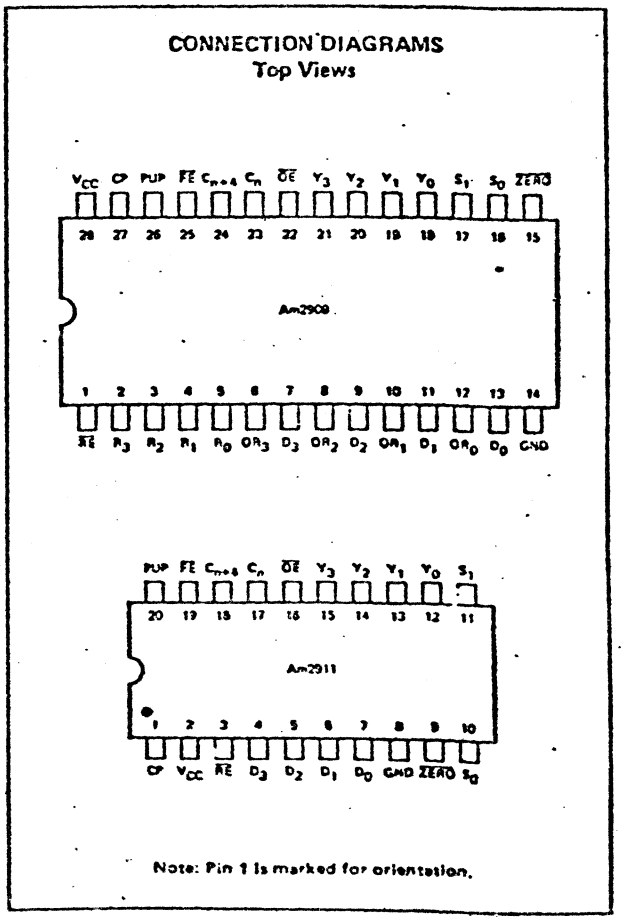


Figure 4.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	µPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	µPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 —	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J —	Pop Stack	End Loop
N N+1	0 0 0 1 —	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J —	Push µPC	Set-up Loop
N N+1	0 0 1 X —	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J —	Continue	Continue
N N+1	0 1 0 0 —	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K —	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 —	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K —	Push µPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X —	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K —	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 —	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra —	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 —	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra —	Jump to Address in STK0; Push µPC	
N N+1	1 0 1 X —	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra —	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 —	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D —	Pop-Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 —	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D —	Jump to Address on D; Push µPC	JSR D
N N+1	1 1 1 X —	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D —	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2909/2911DC, PC	0°C to +70°C	4.75V to 5.25V
Am2909/2911DM, FM	−55°C to +125°C	4.50V to 5.50V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2909/Am2911PC, DC	Am2909/Am2911DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100%	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm³	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2909PC or Am2911PC.

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level
			Am2909/Am2911DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

ORDERING INFORMATION

Package Type	Temperature Range	Am2909 Order Number	Am2911 Order Number
Molded DIP	0°C to +70°C	AM2909PC	AM2911PC
Hermetic DIP	0°C to +70°C	AM2909DC	AM2911DC
Hermetic DIP	−55°C to +125°C	AM2909DM	AM2911DM
Hermetic Flat Pak	−55°C to +125°C	Am2909FM	—
Dice	0°C to +70°C	Am2909XC	—

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

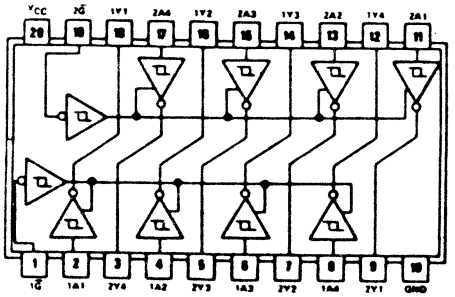
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA (Note 5)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{CE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	µA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)				80	130	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	µA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

100001080

Octal Buffer And Line Driver With 3-State Outputs

PIN CONFIGURATION



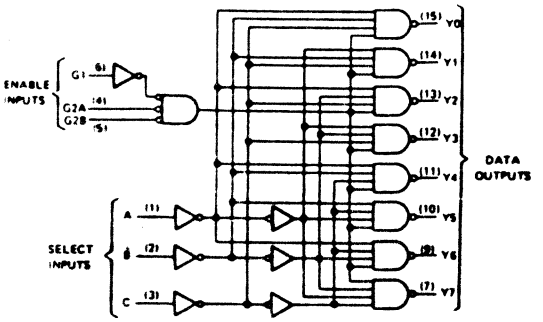
This device features three-state outputs, selectable combinations of inverting and noninverting outputs, symmetrical G'(active-low output control) inputs, and complementary G and G'inputs.

NOTE *The 100001080 is a low power Schottky device.*

100001081

Decoder/Demultiplexer

BLOCK DIAGRAM



NOTE *The 100001081 is a low power Schottky device.*

instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine" to save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J–1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

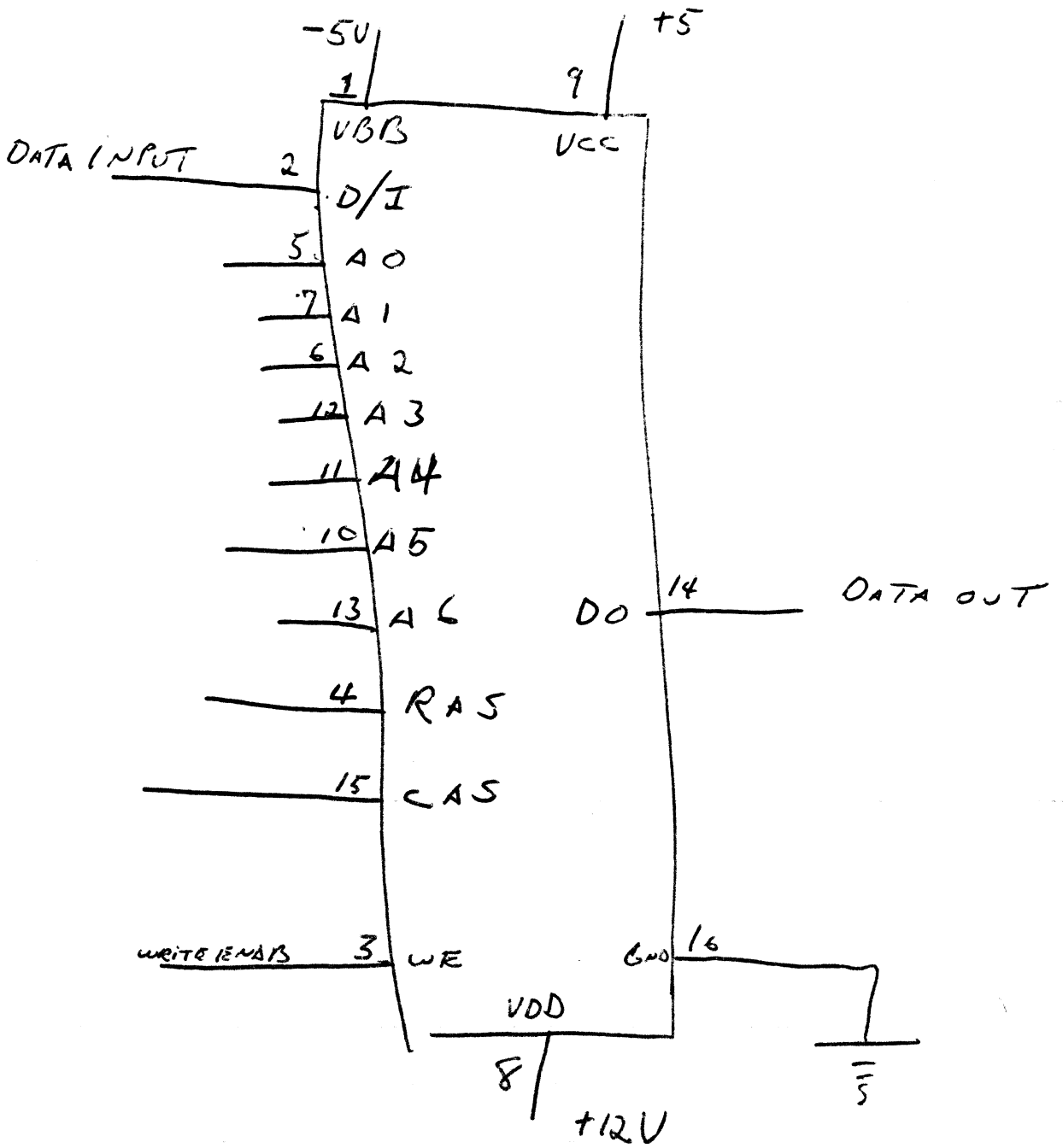
Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J–1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T_5	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

DQ1100

MK4116P-3



μPD416
μPD416-1
μPD416-2
μPD416-3

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

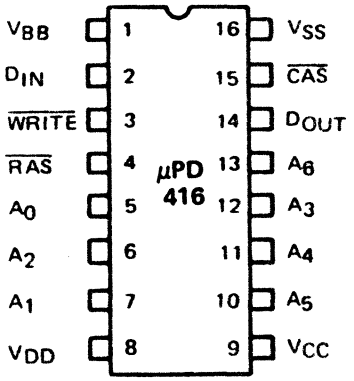
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 4 Performance Ranges:

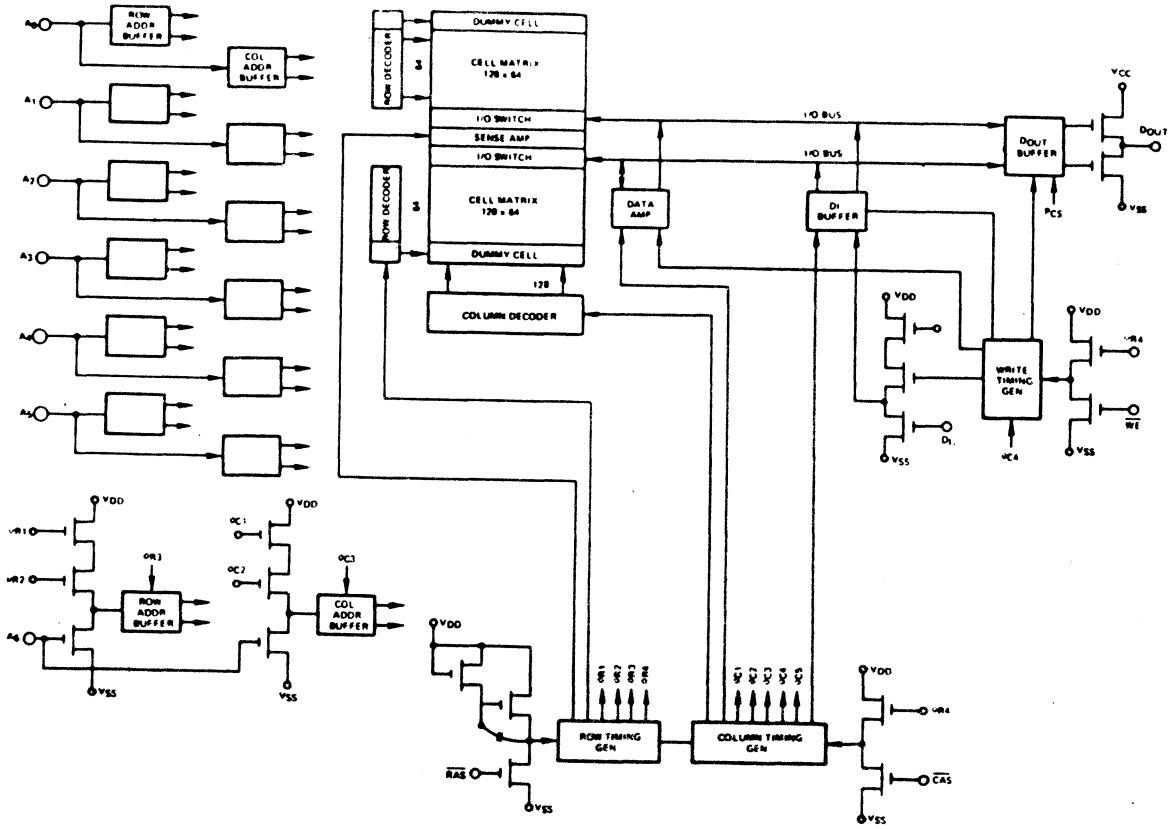
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	510 ns
μPD416-1	250 ns	430 ns	430 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns

PIN CONFIGURATION



PIN NAMES

A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

CHARACTERISTICS

T_a = 0°C to +70°C (1), V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	-4.5	-5.0	-5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns (5)
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	-10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	-10		10	μA	V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	-10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = -5 mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: (1) T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

DERATING CURVES

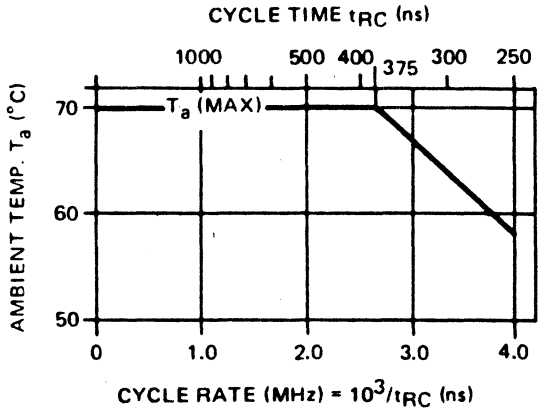


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 - 9.0 x (cycle rate [MHz] -2.66).

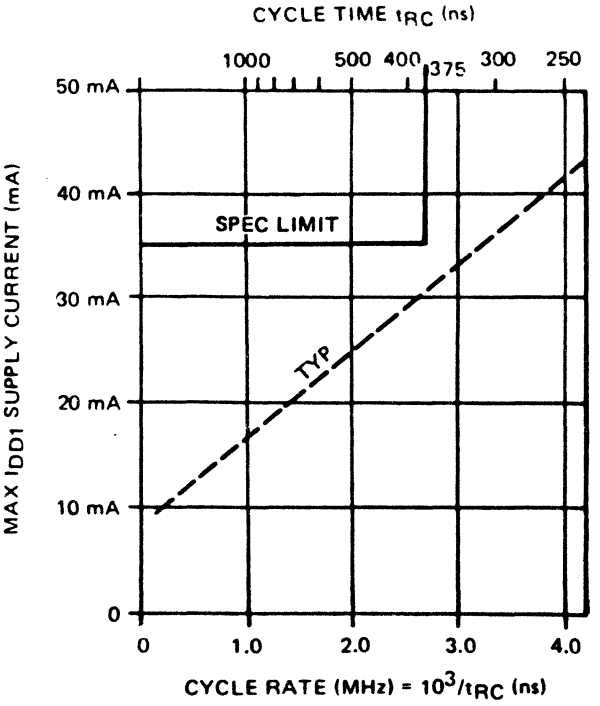


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

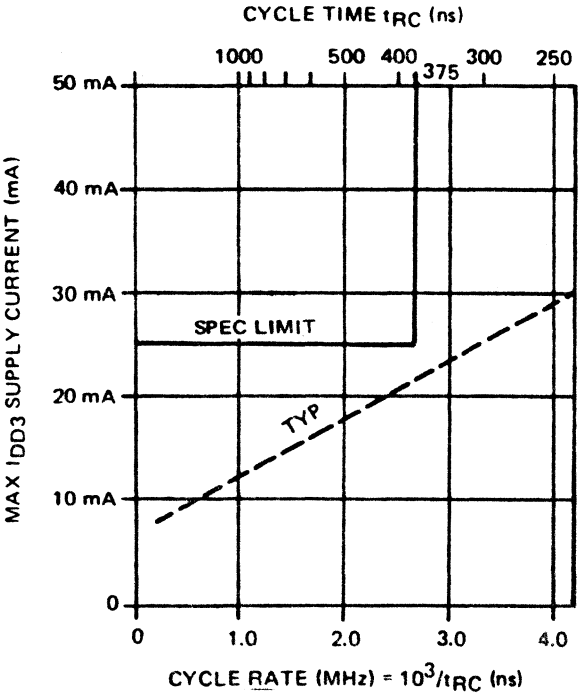


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

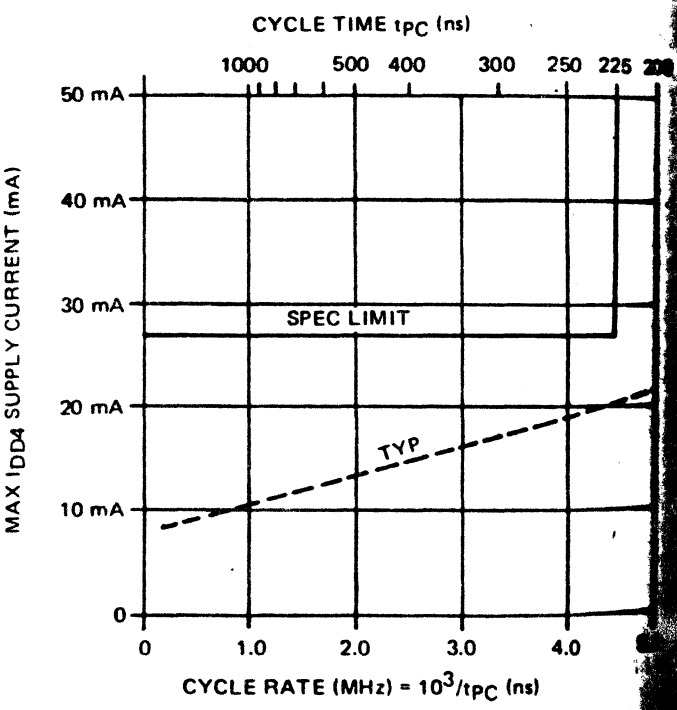


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS								UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		430		375		375		ns	③
Read-write cycle time	t_{RWC}	510		430		375		375		ns	③
Page mode cycle time	t_{PC}	330		280		225		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		170		135		100	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	70	0	50	0	40	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		170		120		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	32,000	250	32,000	200	32,000	150	32,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		170		135		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	170	10,000	135	10,000	100	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row Address hold time	t_{RAH}	40		35		25		20		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		ns	
Write command pulse width	t_{WP}	90		75		55		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		ns	
$\overline{CAS}$ precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		ns	
Refresh period	t_{REF}		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−10		−10		−10		−10		ns	
CAS to $\overline{WRITE}$ delay	t_{CWD}	140		120		95		70		ns	
RAS to $\overline{WRITE}$ delay	t_{RWD}	210		175		160		120		ns	

Notes:

(1) AC measurements assume t_T = 5 ns.

(2) V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

(3) The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

(4) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

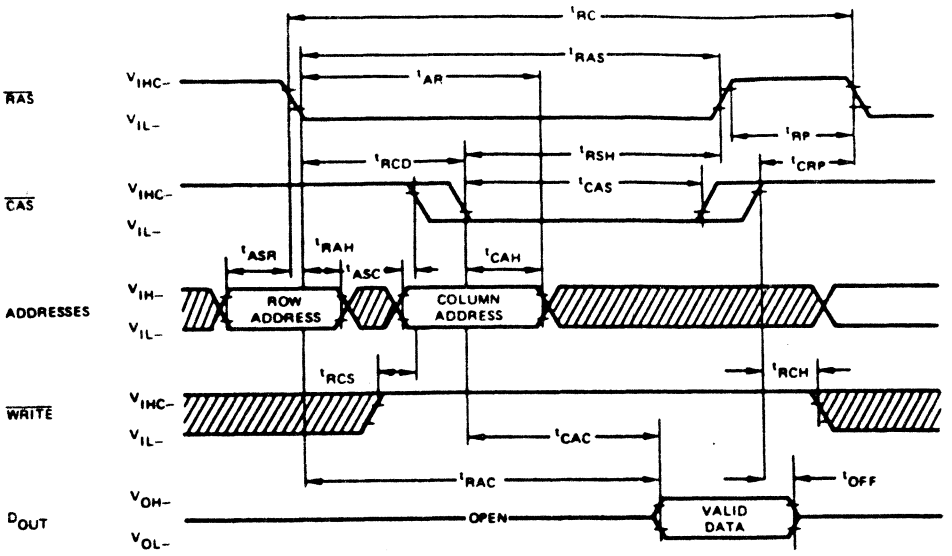
(6) Measured with a load equivalent to 2 TTL loads and 100 pF.

(7) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

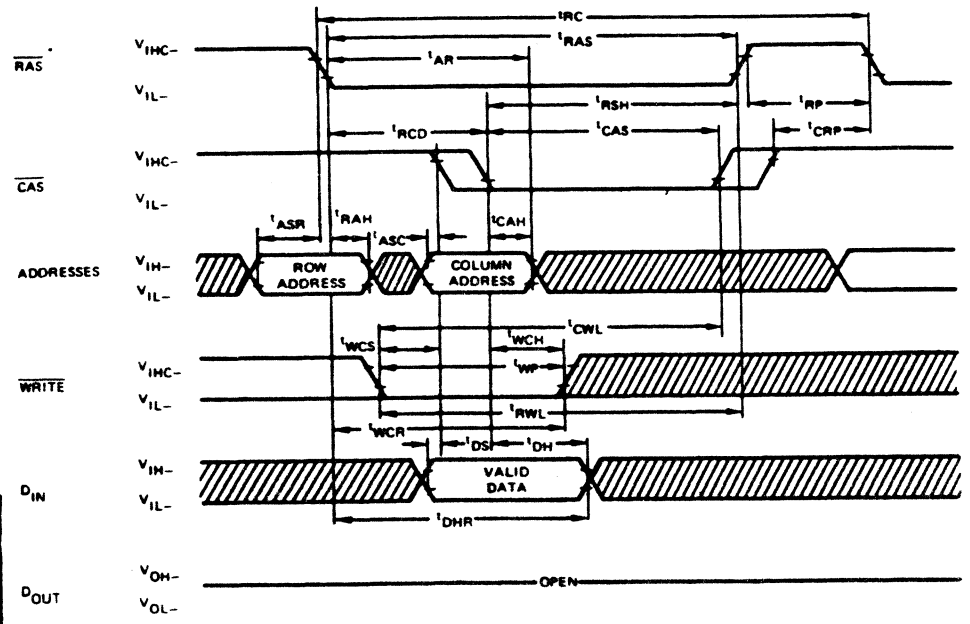
(8) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(9) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

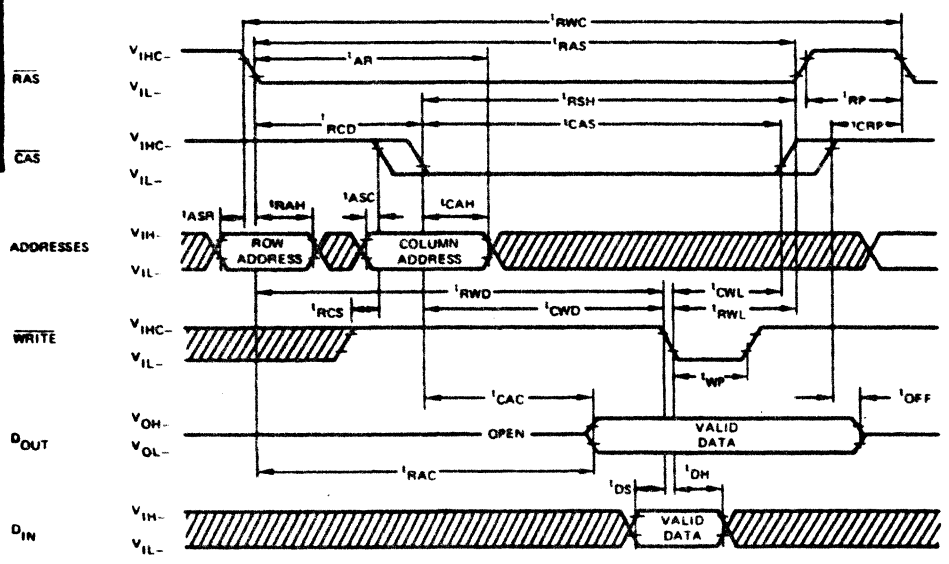
READ CYCLE



WRITE CYCLE

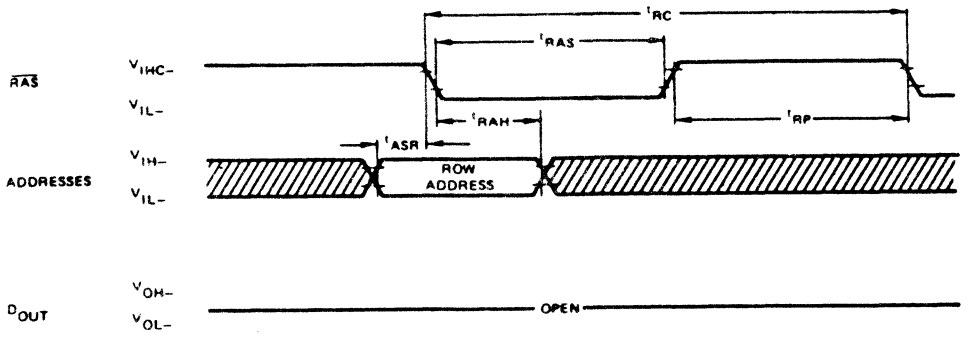


READ-WRITE/READ-MODIFY-WRITE CYCLE



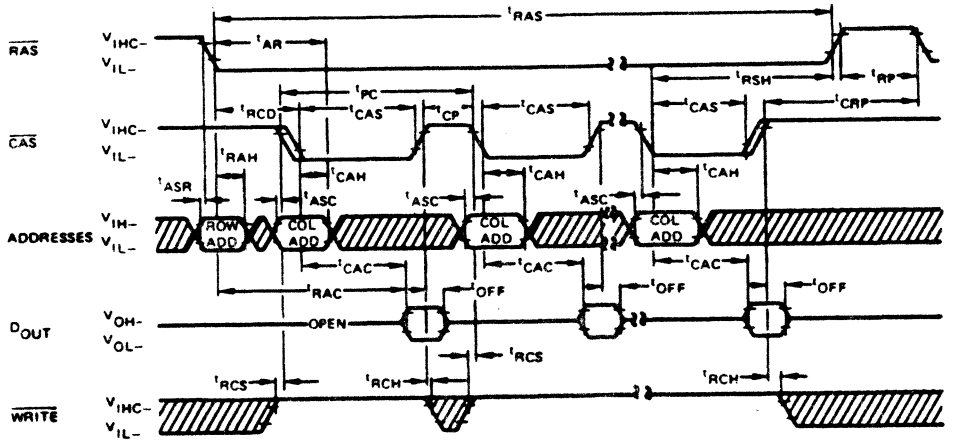
TIMING WAVEFORMS (CONT.)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

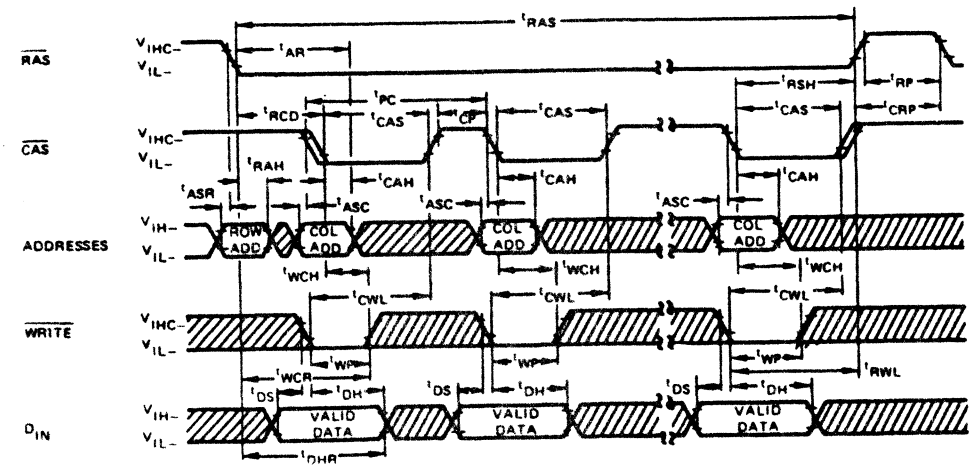


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

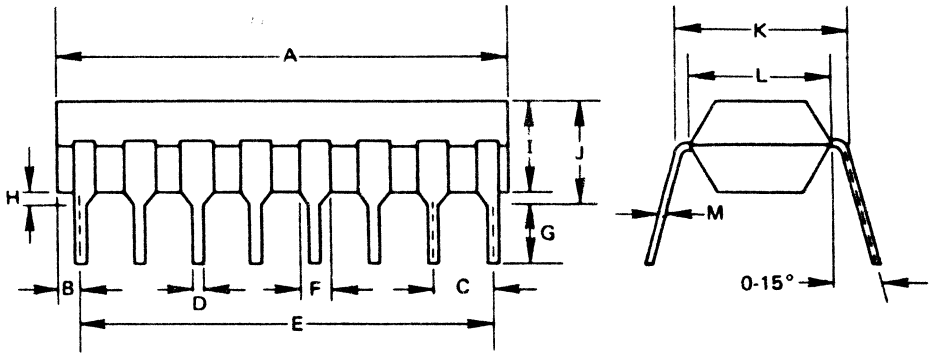
REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

CHIP SELECTION

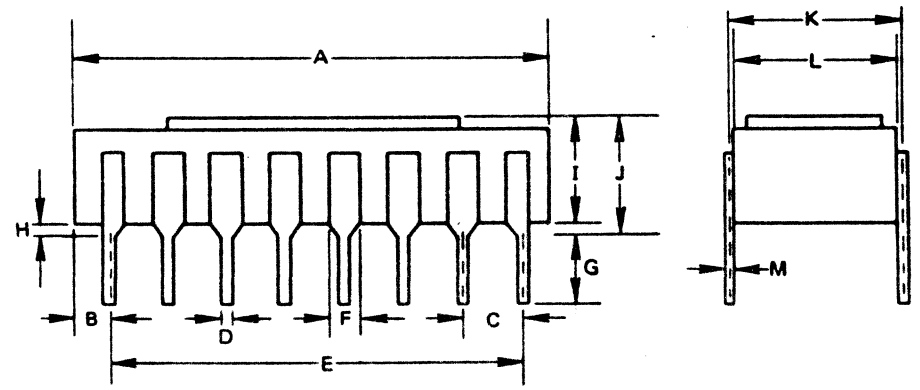
Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



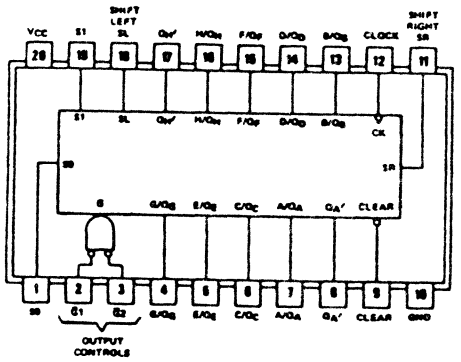
μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

100001150

8-Bit Universal Shift/Storage Register

PIN CONFIGURATION



FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

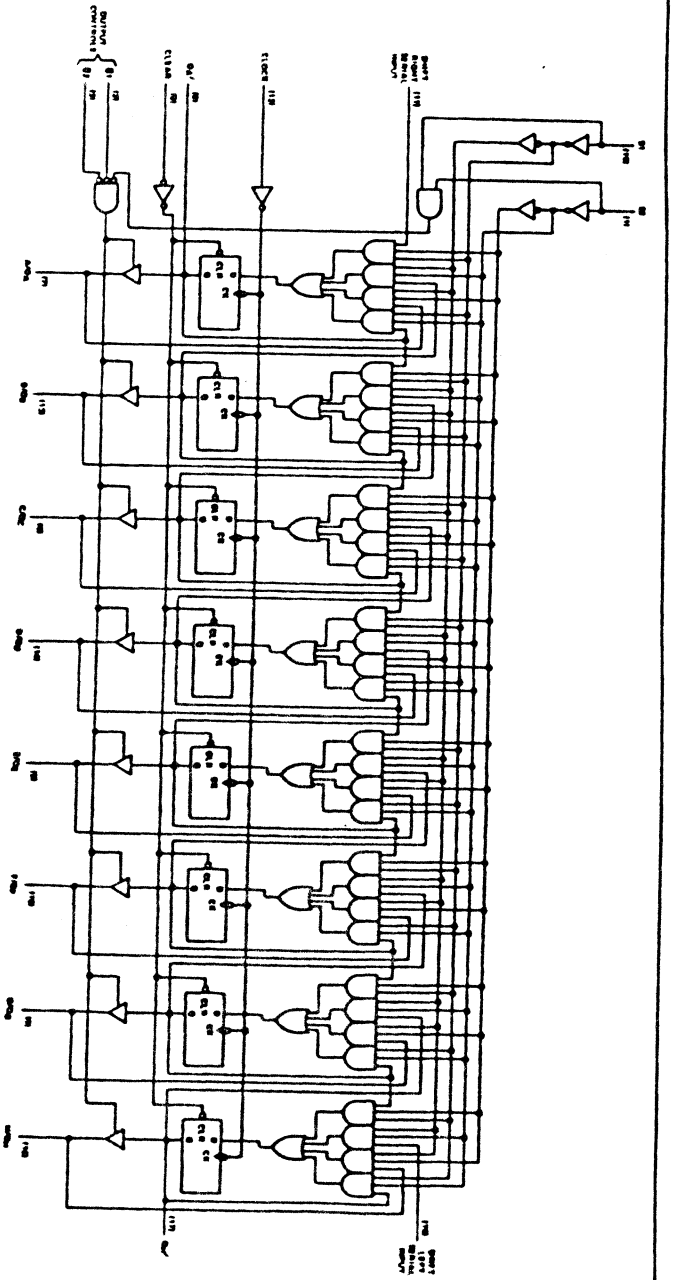
a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

The 100001150 is controlled by two function select inputs and two output control outputs which select the four operating modes listed in the function table.

In load mode, the tri-state outputs are in a high-impedance state to permit data to be clocked into the register. Data can be read when the outputs are enabled in any mode. The register can be cleared at any time using the clear input.

NOTE *The 100001150 is a low power Schottky device.*

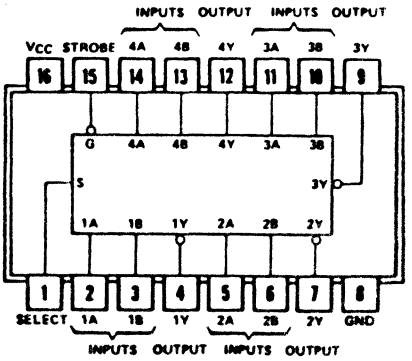
BLOCK DIAGRAM



100001211

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



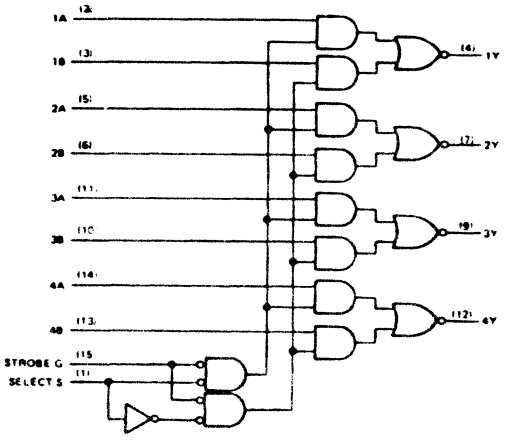
positive logic:
Low level at S selects A inputs
High level at S selects B inputs

FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



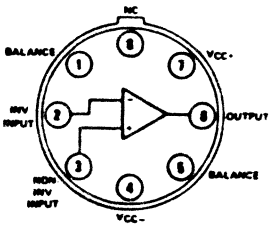
The 100001211 is a selector/multiplexor with inverters and drivers to supply on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The device presents inverted data.

NOTE *The 100001211 is a low power Schottky device.*

100001212

JFET-Input Operational Amplifier

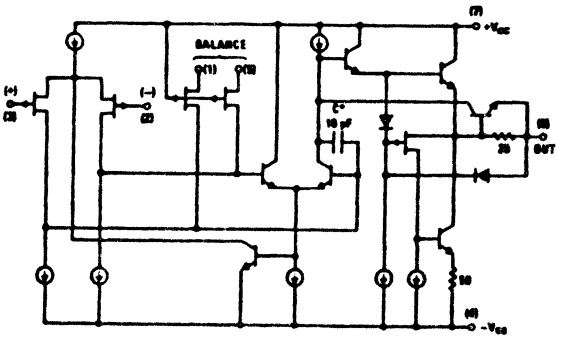
PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

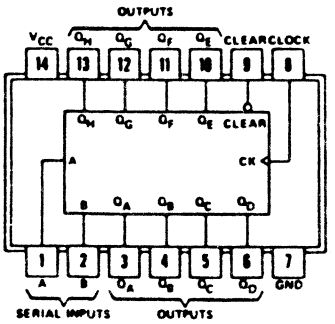
LOGIC DIAGRAM



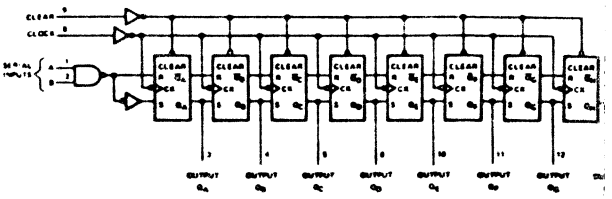
100001231

8-Bit Parallel-Out Serial Shift Register

PIN CONFIGURATION



BLOCK DIAGRAM

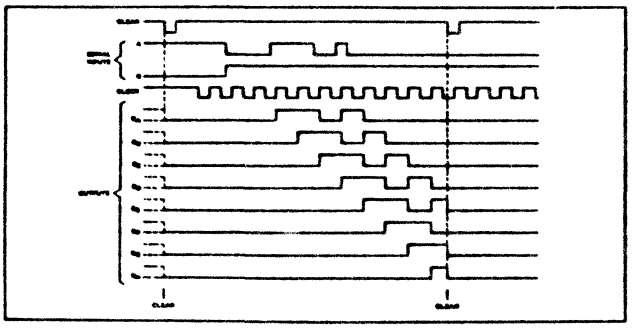


TRUTH TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



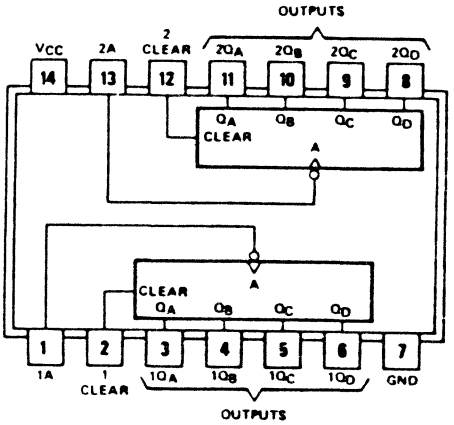
The 100001231 is a 8-bit shift register which featu
gated serial inputs, asynchronous clear,
totem-pole outputs. A low on either (both) of
serial gated inputs (A,B) inhibits the entry of
data and resets the first flip-flop to low on the
clock pulse. A high input enables the other in
which will determine the state of the first flip-
Clocking occurs on the low-to-high transition of
clock.

NOTE *The 100001231 is a low power Scho
device.*

100001232

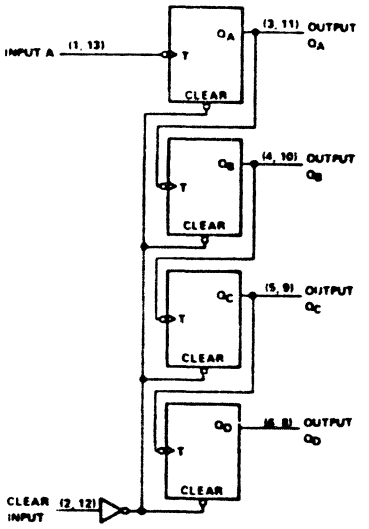
Dual 4-Bit Binary Counter

PIN CONFIGURATION



positive logic: High input to clear resets all four outputs low

BLOCK DIAGRAM



TRUTH TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

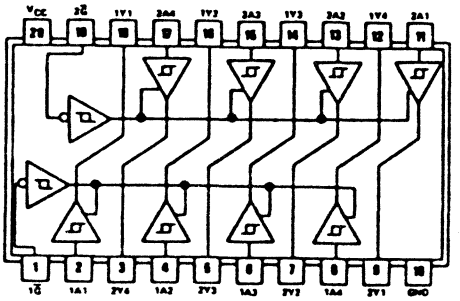
The 100001232 consists of eight master-slave flip-flops and additional gating to implement two independent 4-bit counter. Each counter has a direct clear and a clock input.

NOTE *The 100001231 is a low power Schottky device.*

100001253

Octal Buffer And Line Driver With 3-State Outputs

PIN CONFIGURATION



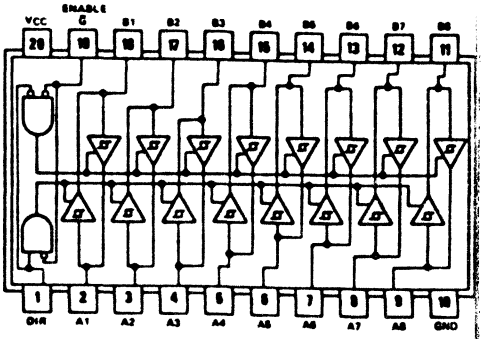
This device has 3-state outputs to drive bus lines or buffer memory address registers. It features selectable combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

NOTE *The 100001253 is a low power Schottky device.*

100001254

Octal Bus Transceiver With 3-State Outputs

PIN CONFIGURATION



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

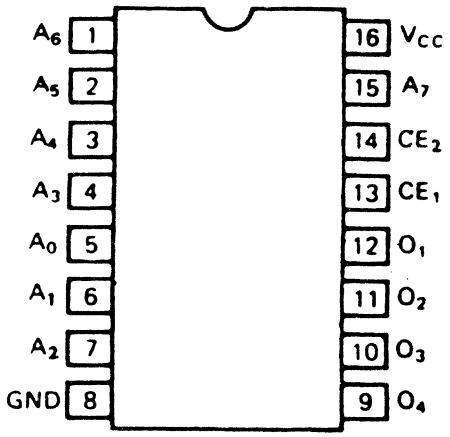
This device allows data transmission from the A to the B bus or from the B bus to the A bus depe upon the logic level at the direction control input. The enable input ($\overline{G}$) can be used to disab device so that the buses are effectively isolated.

NOTE *The 100001254 is a low power Sch device.*

100001264

1024-Bit Bipolar PROM

PIN CONFIGURATION



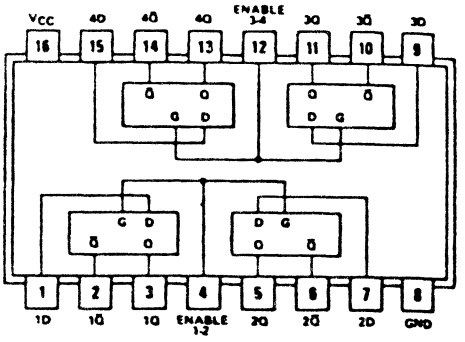
This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001264 is a Schottky device.*

100001265

4-Bit Bistable Latch

PIN CONFIGURATION

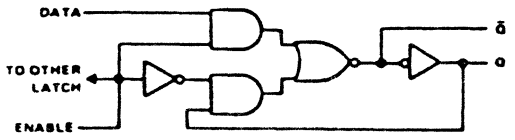


FUNCTION TABLE
(EACH LATCH)

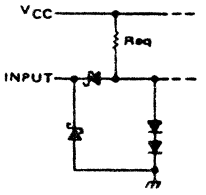
INPUTS		OUTPUTS	
D	G	Q	Q̄
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G.

BLOCK DIAGRAM
(each latch)

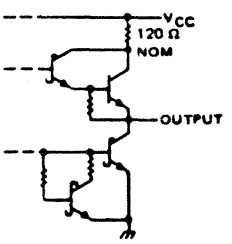


EQUIVALENT OF EACH INPUT



Data: Req = 17 kΩ
Enable: Req = 4.2 kΩ

TYPICAL OF ALL OUTPUTS



Information present at a data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

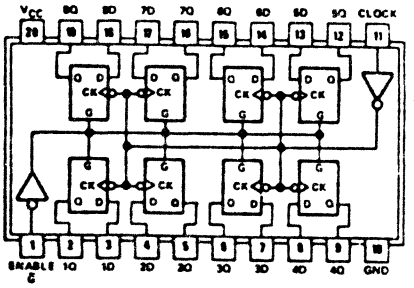
NOTE *The 100001265 is a low power Schottky device.*

100001266

74LS377

Octal D-Type Flip-Flops With Enable

PIN CONFIGURATION

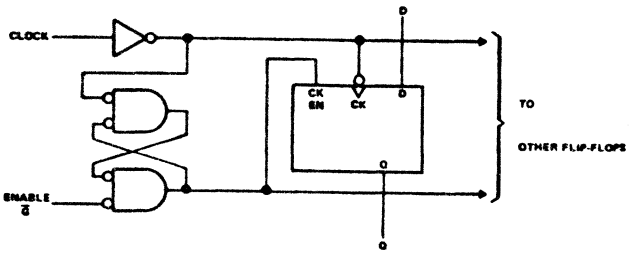


FUNCTION TABLE

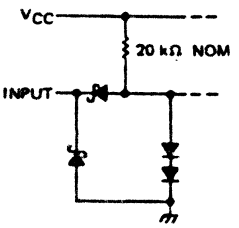
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

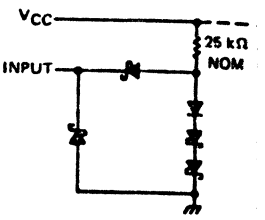
BLOCK DIAGRAM



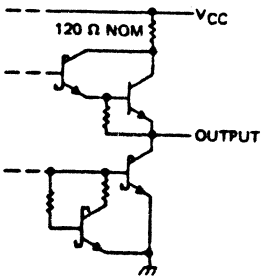
EQUIVALENT OF CLOCK OR ENABLE INPUT



EQUIVALENT OF DATA INPUT



TYPICAL OF ALL OUTPUTS



The 100001266 consists of eight edge-triggered D-typ flip-flops with a common enable input.

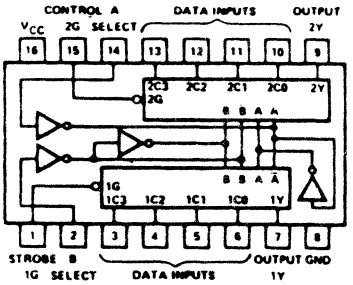
Information at the D inputs meeting the setup tim requirements is transferred to the Q outputs on th positive going edge of the clock pulse if the enabl input $\overline{G}$ is low. Clock triggering occurs at a particula voltage level and is not directly related to th transition time of the positive-going pulse. When th clock input is at either the high or low level, the I input signal has no effect at the output.

NOTE *The 100001266 is a low power Schottk device.*

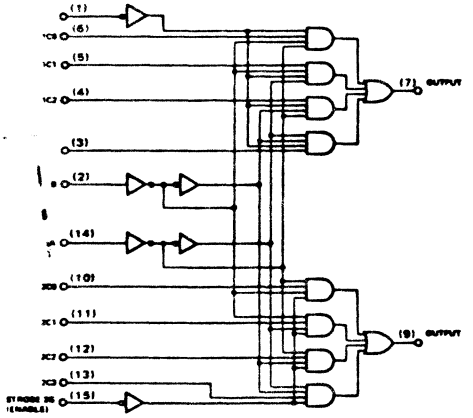
100001355

Dual 4-Line To 1-Line Data Selector/Multiplexer

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

The 100001355 data selector/multiplexor contains inverters and drivers which supply complementary, decoding data selection to its AND-OR gates. There are independent control inputs for each of the two 4-line sections.

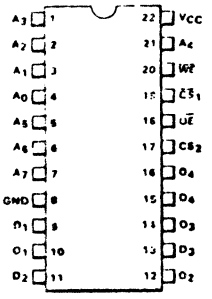
The tri-states outputs allow the 100001355 to drive the data lines of bus-oriented systems. When all of the common outputs but one are disabled (in a high impedance state), the remaining output is enabled (in low impedance state) to drive the bus line high or low.

NOTE *The 100001355 is a Schottky device.*

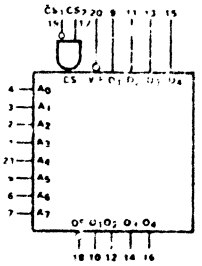
100001497

1024-Bit RAM

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 22
GND Pin 8

The 100001497 is a fully decoded 1024-bit random access memory organized as 256 words by 4 bits. It features three-state outputs and two chip select inputs. A word is addressed by the 8-bit address A0 through A7.

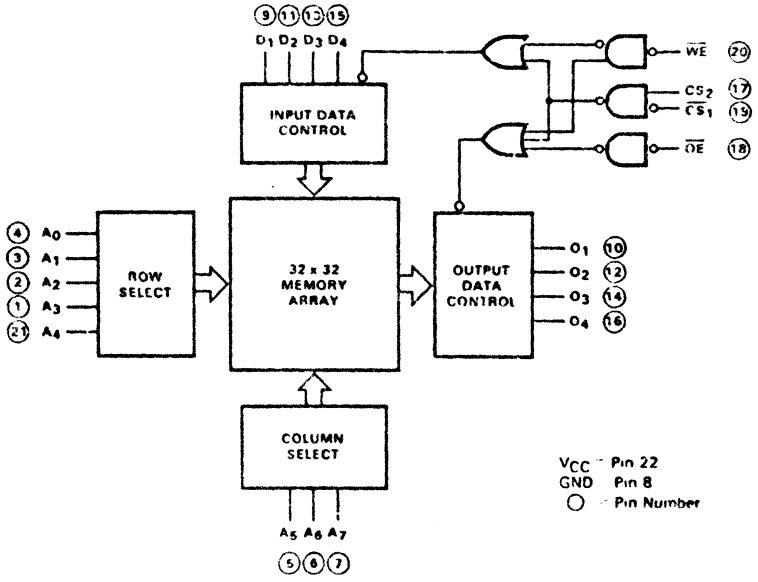
The read and write operations are controlled by the state of the active low Write Enable (WE). When WE is low and the chip is selected, the data at Din is written into the addressed location. When WE is high and the chip is selected, the data in the addressed location is read out at Dout.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS_1}$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11, 13, 15	93422 3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW), HIGH Z = High Impedance.

LOGIC DIAGRAM

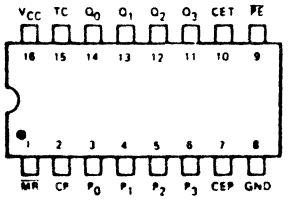


V_{CC} = Pin 22
GND Pin 8
○ = Pin Number

100001524

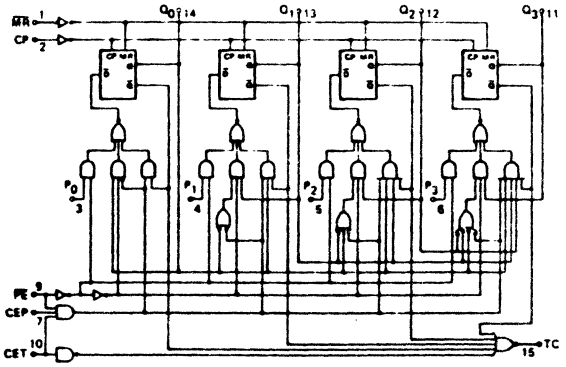
Four-Bit Binary Counter

PIN CONFIGURATION

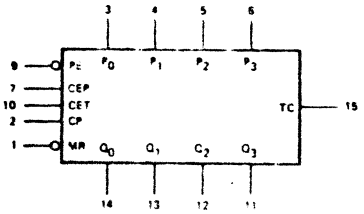


Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS									OUTPUTS			
CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
X	L	X	X	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	H	X	X	X	X	COUNT			

H = HIGH
L = LOW
X = Don't Care
NC = No Change
D_i may be either HIGH or LOW
↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

CET	Q_0	Q_1	Q_2	Q_3	TC
H	H	H	H	H	H
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L

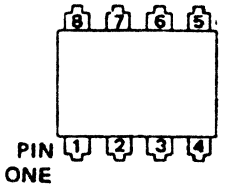
The 100001524 is a synchronous 4-bit binary counter. When the parallel enable ($\overline{PE}$) is low, the data on the P0-P3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is high and both count enables (CEP,CET) are also high, counting occurs on the positive transition of the clock. The terminal count output (TC) is high when CET is high and the counter is in its terminal count state. The counter also has a master reset input ($\overline{MR}$), which, when low, forces the Q outputs low independently of all other inputs.

NOTE *The 100001524 is a Schottky device.*

100001528

High Speed Optically Coupled Isolators

PIN CONFIGURATION

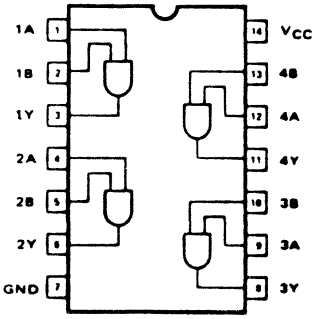


This device uses GaAsP light emitting diodes optically coupled to a photo-sensitive circuit. It provides 3000 Vdc isolation between the input and the output.

100001529

Quad 2-Input AND Gate w/Open Collector Outputs

PIN CONFIGURATION



NOTE *The 100001529 is a Schottky device.*