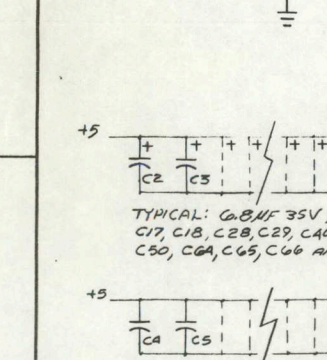
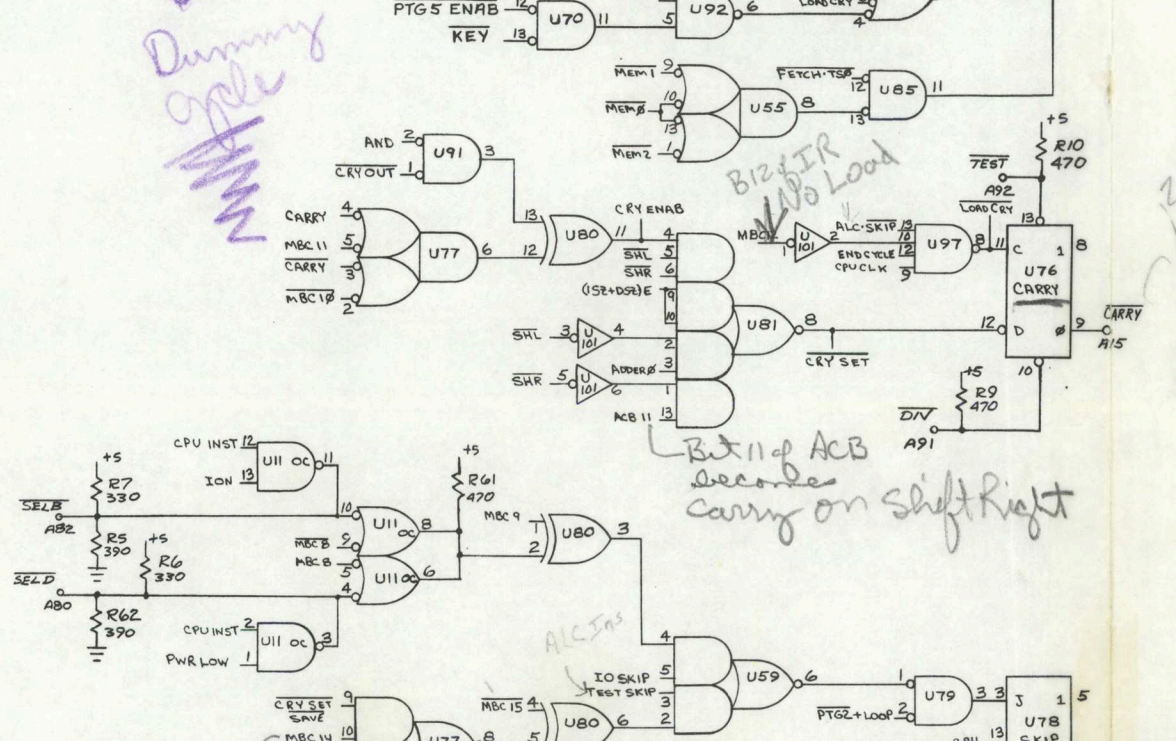
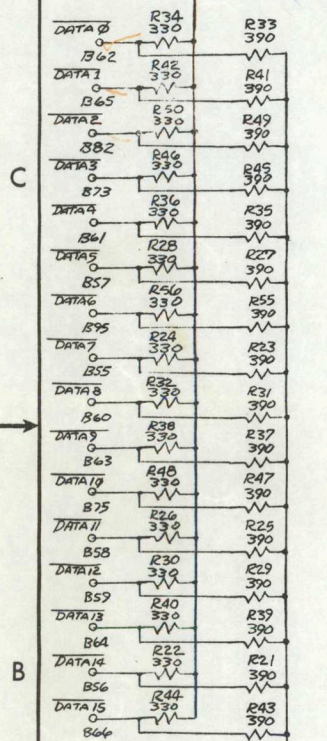
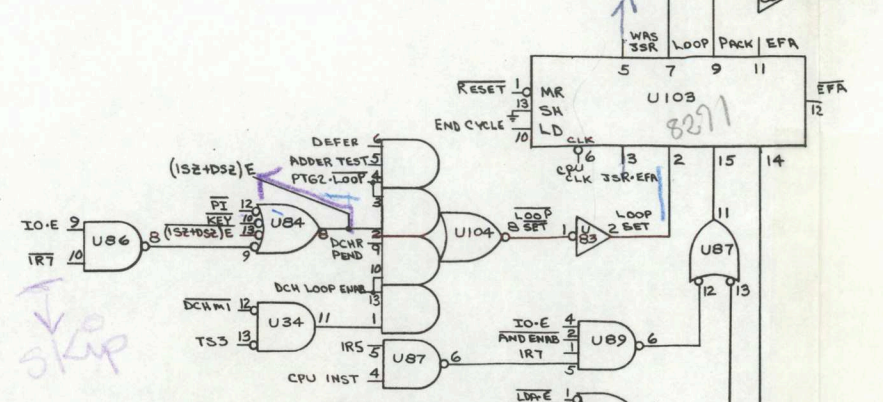
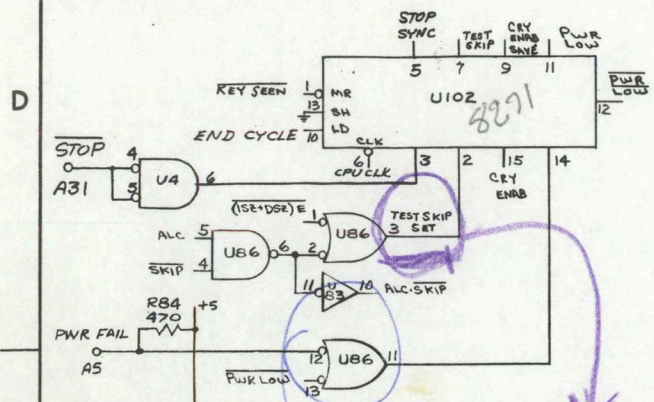
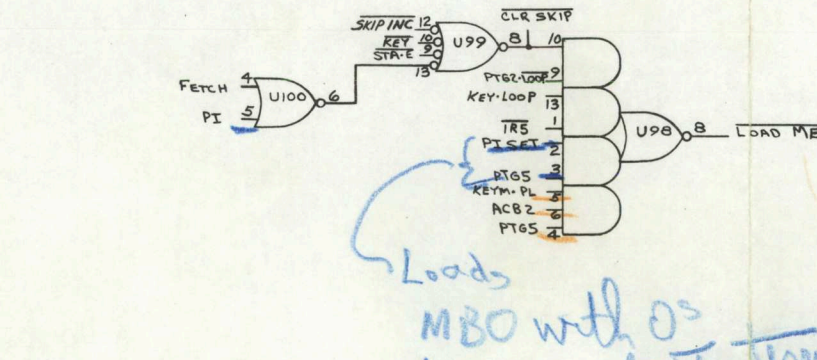
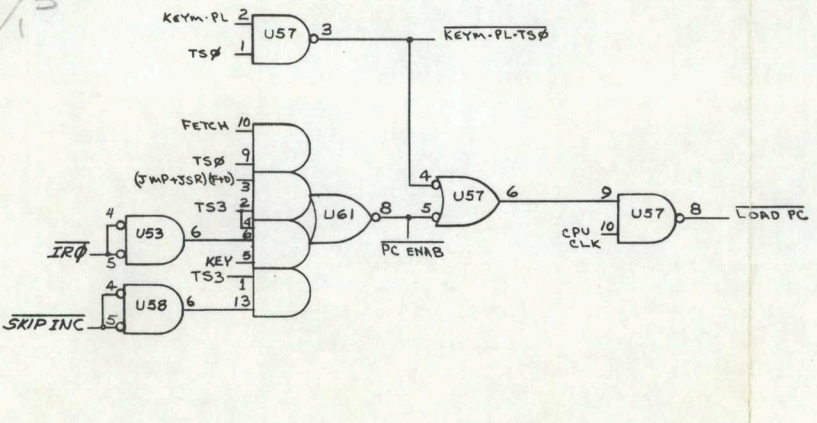
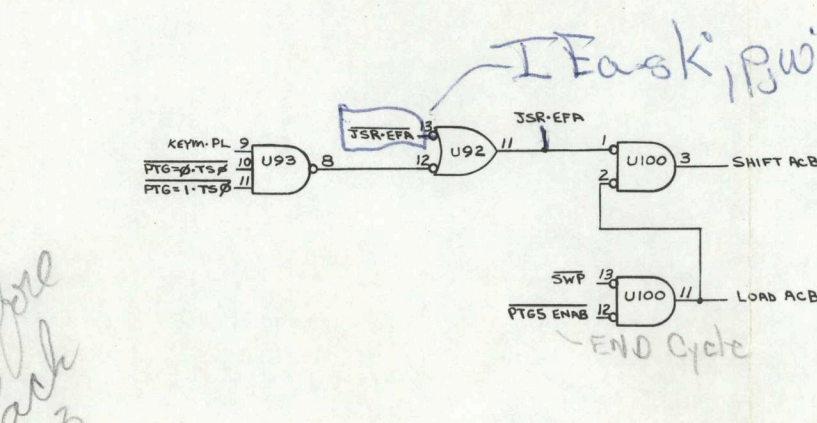
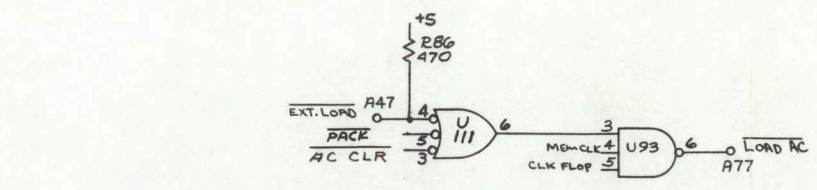


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REVISIONS				
REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
01	REVISED PER MKD PRINT	RHS		11/17/70
02	REVISED PER ECO 117	RHS		12/14/70
03	REV PER ECO 138 SHEET 1	RHS		12/21/70
04	REV PER ECO 148	RHS		1/4/71
05	REV PER ECO# 194,209	RHS		2/17/71
06	ADD REF. DESIG. PER ECO# 364	RHS		4/15/71
14	REV PER ECO# 992	RHS		5/15/72



TYPICAL: .05 CAPACITORS
 CA - C13, C19 - C27, C30 - C39, C42 - C48, C51 - C63, C67 - C72, (55 REQ)



Dummy cycle

skip

Bit 11 of ACB

*Bit 11 of ACB
 second carry on shift right*

Looking at Result

*decided after
 at TEO of next state*

*checking for
 hex 20-37*

first 2 nibbles

check for 1 and 15 after nibble xfer

*Before Pack
 153*

see if you got hex 20-37

*I think, (w/ill) not cause this, will
 not shift ACB*

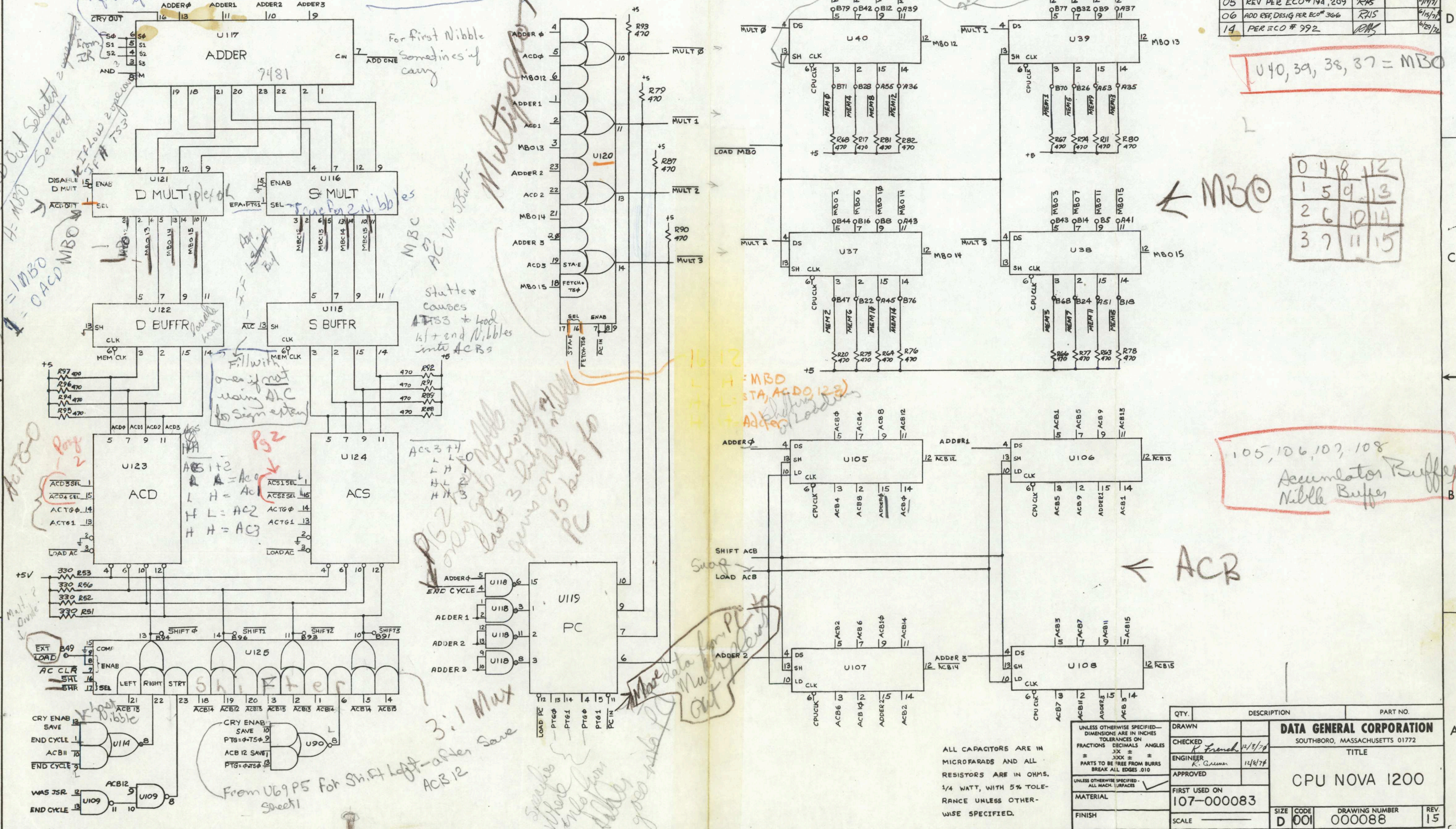
*Loads MBO with 00
 at F comm for interrupt*

*loads old
 during PL after
 Rom is read in
 mem*

QTY.	DESCRIPTION	PART NO.
	DRAWN	
	CHECKED	
	ENGINEER	
	APPROVED	
	FIRST USED ON	
	107-000083	
	MATERIAL	
	FINISH	

DATA GENERAL CORPORATION			
SOUTHBORO, MASSACHUSETTS 01772			
TITLE			
CPU NOVA 1200			
SIZE	CODE	DRAWING NUMBER	REV
D	001	000088	15

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Top + ACB
hold + S BUFR
Subtracting of locations 203
IF Low No Combining
I-H = Combine through S BUFR
what comes

If hard had high of storage high multiplexer
4-12 parallel
sh-13
sh-13

ACD = MBO
H = MBO
ACD = 0
1 = MBO
2 = 0 ACD MBO
Fill with ones if not using ACD for sign exten
ACB 1 + 2
A = AC0
L H = AC1
H L = AC2
H H = AC3
3:1 Max
From U69 P5 for Shift Left after save

Multiplex
For first Nibble Sometimes if carry
stutter causes ATSS to load left end nibbles into ACBs
Ac3 + 4
L L = 0
L H = 1
H L = 2
H H = 3
only gate through
least 3 bits only
15 bits
PC

REV.	DESCRIPTION	DRFTG.	APP. BY	DATE
01	REVISED PER MID PRINT	RHS		11/9/70
02	REV PER ECO #17 SHEET 3	RHS		12/4/70
03	REV PER ECO #138 SHEET 1	RHS		12/24/70
04	REV PER ECO #148	RHS		1/4/71
05	REV PER ECO #194, 209	RHS		2/19/71
06	ADD REF. DESIG PER ECO #366	RHS		6/15/71
14	PER ECO #992	RHS		6/29/72

U40, 39, 38, 37 = MBO

0	4	8	12
1	5	9	13
2	6	10	14
3	7	11	15

MBO

105, 106, 107, 108
Accumulator Buffer
Nibble Buffer

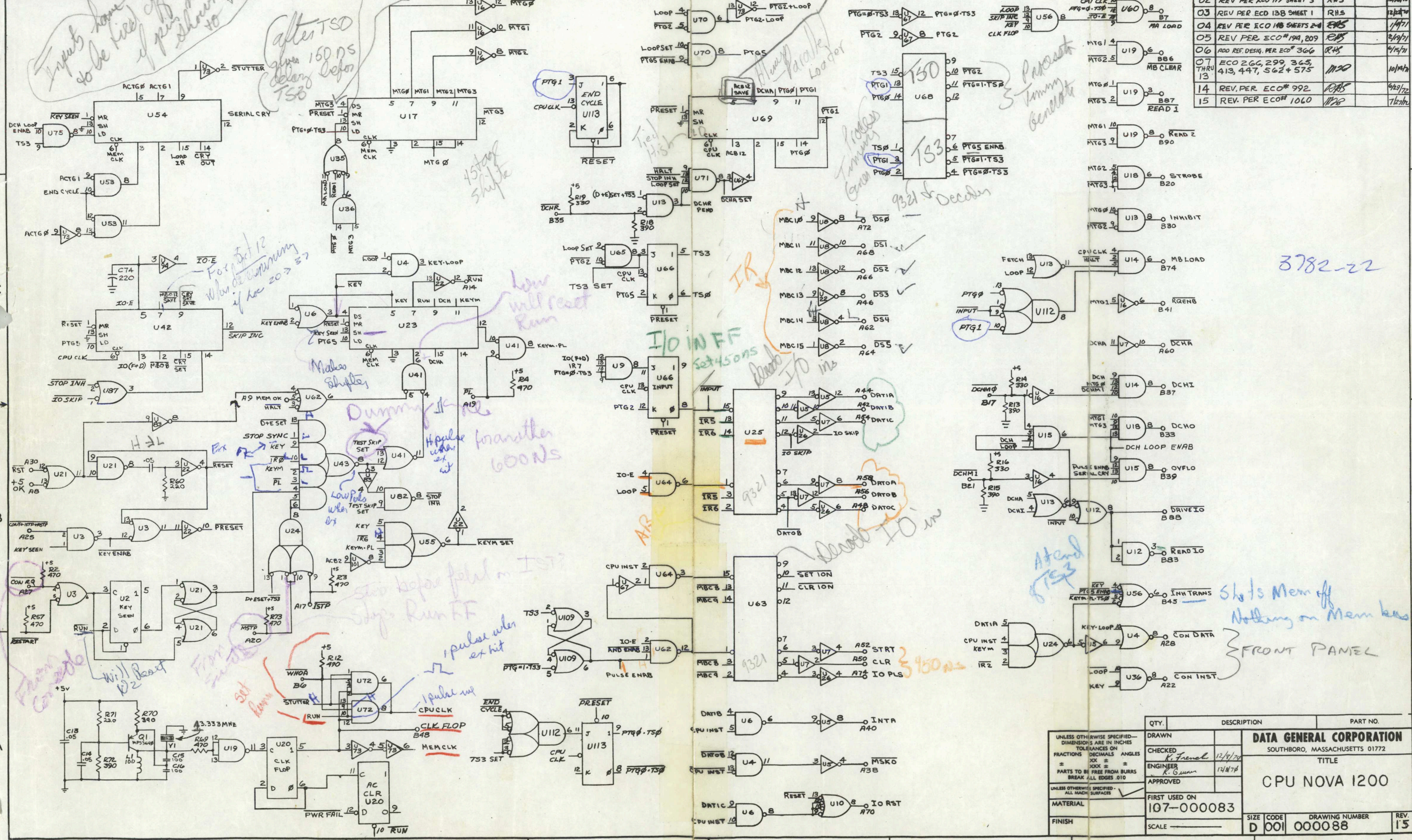
ACB

QTY.	DESCRIPTION	PART NO.

<small>UNLESS OTHERWISE SPECIFIED—</small> <small>DIMENSIONS ARE IN INCHES</small> <small>FRACTIONS DECIMALS ANGLES</small> <small>TOLERANCES ON</small> <small>JXX ±</small> <small>PARTS TO BE FREE FROM BURRS</small> <small>BREAK ALL EDGES .010</small>	<small>DRAWN</small> <small>CHECKED</small> <small>ENGINEER</small> <small>APPROVED</small>	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 <hr/> CPU NOVA 1200
<small>UNLESS OTHERWISE SPECIFIED—</small> <small>ALL MACH. SURFACES</small>	<small>FIRST USED ON</small> 107-000083	<small>DRAWING NUMBER</small> 000088
<small>MATERIAL</small> <small>FINISH</small>	<small>SCALE</small>	<small>REV.</small> 15

ALL CAPACITORS ARE IN MICROFARADS AND ALL RESISTORS ARE IN OHMS. 1/4 WATT, WITH 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.

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REVISIONS				
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03	REV PER ECO 138 SHEET 1	RHS		12/17/70
04	REV PER ECO 146 SHEETS 2-4	RHS		1/17/71
05	REV PER ECO 194, 209	RHS		2/19/71
06	ADD REF. DESIG. PER ECO 306	RHS		4/15/71
07	ECO 266, 299, 365, 413, 447, 562+575	MZG		10/17/71
14	REV. PER ECO 992	RHS		4/2/72
15	REV. PER ECO 1060	MZG		7/27/72

UNLESS OTHERWISE SPECIFIED— DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES X.XX ± .01 X.X ± .02 PARTS TO BE FREE FROM BURRS BREAK ALL EDGES .010	QTY.	DESCRIPTION	PART NO.
	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772		
	TITLE CPU NOVA I200		
	DRAWN CHECKED <i>K. French</i> 12/9/70 ENGINEER <i>K. Green</i> 12/17/70 APPROVED		
MATERIAL	FIRST USED ON	DRAWING NUMBER	
FINISH	107-000083	000088	
SCALE		SIZE	REV.
		D 001	15

3782-22

Shots Mem off
Nothing on Mem bus
FRONT PANEL

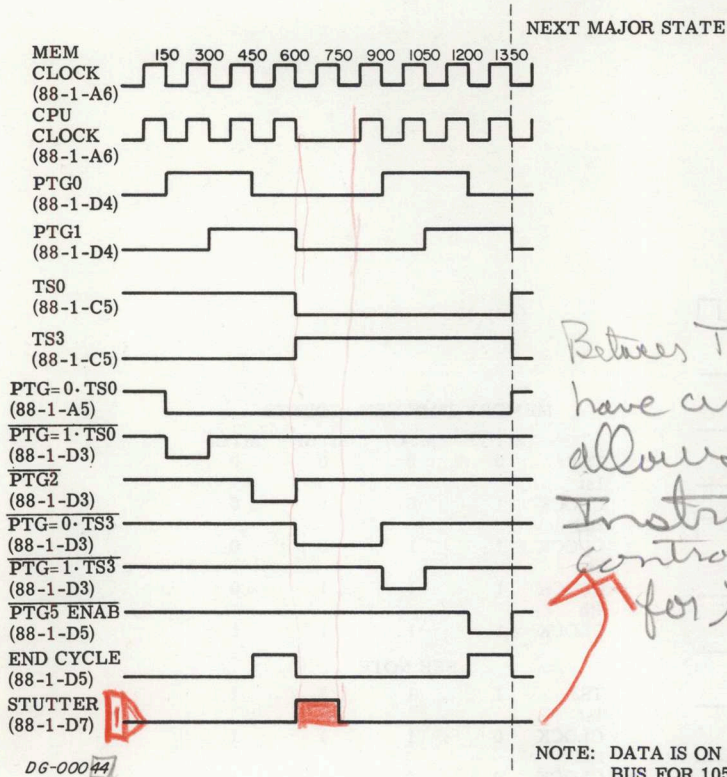


Figure C-2 Timing For The Processor Timing Generator During Fetch or Key

Between TS0 + TS3 have an extra 150Ns allows time to decode instruction and set up controls for next that are necessary for instruction 1

*Process Time
 Accumulator Timing
 Memory Timing Gen*

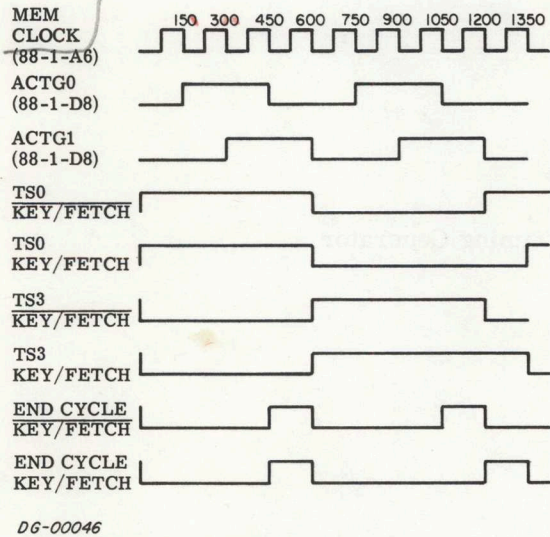
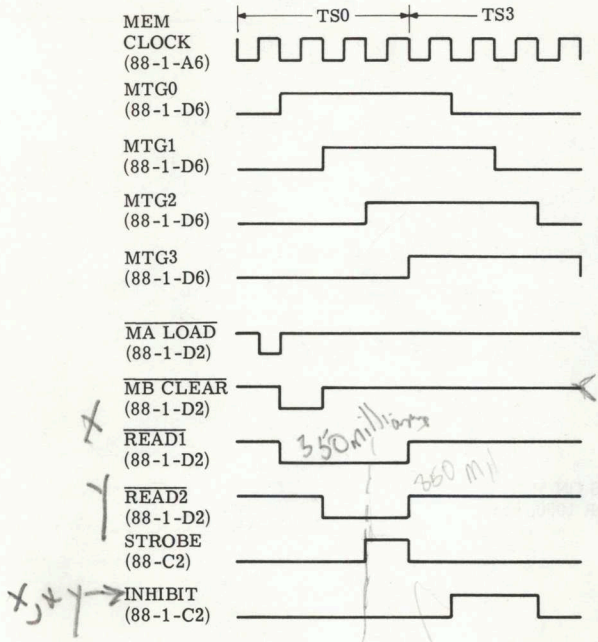


Figure C-3 Timing For The Accumulator Timing Generator

ACCUMULATOR TRUTH TABLE (88-4-B6 & B7 U124 & U123)

ACTG0	ACTG1	
0	0	BITS 12-15
1	0	BITS 8-11
1	1	BITS 4-7
0	1	BITS 0-3

12/10
1820
 Current rating of power supply
 17 Amps



MEMORY TIME GEN. COUNTS

	MTG0	MTG1	MTG2	MTG3
TS0	0	0	0	0
1st CLOCK	1	0	0	0
2nd CLOCK	1	1	0	0
3rd CLOCK	1	1	1	0
4th CLOCK	1	1	1	1
	SEE NOTE			
TS3	1	1	1	1
1st CLOCK	0	1	1	1
2nd CLOCK	0	0	1	1
3rd CLOCK	0	0	0	1
4th CLOCK	0	0	0	0

NOTE - IF LOOPING TS0, CLOCK FREEZES WITH ALL ONES UNTIL FIRST CLOCK IN TS3.

DG-00047

780 millisecs

100
45 ON
DATA NO READ
output 9mm

Figure C-4 Timing For The Memory Timing Generator