Data General

Technical
Manual

COMPONENTS GUIDE

015-000028-07

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Rev. 07, December, 1980

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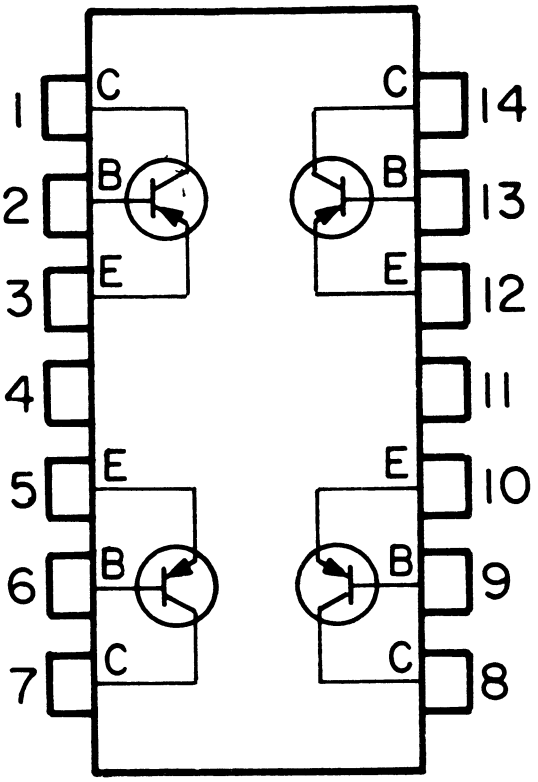
100000001

PNP Quad Core Driver

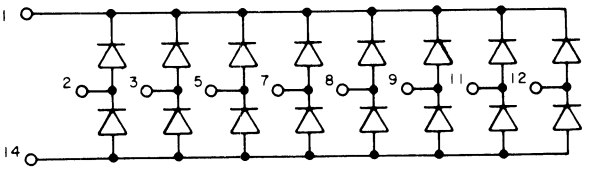
PIN CONFIGURATION



100000002

16 Diode Array

LOGIC DIAGRAM



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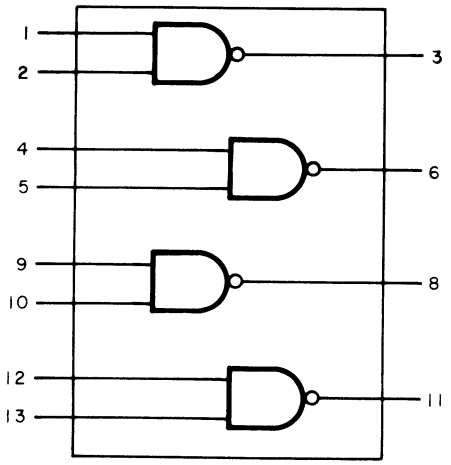
100000003

Quad 2-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

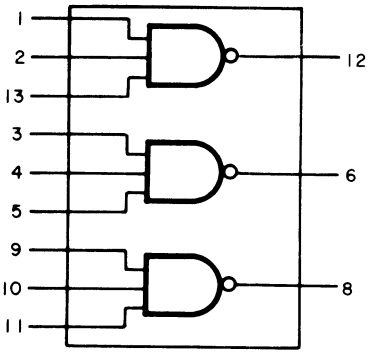
All Inputs High = Low Out
Any Input Low = High Out

$Y = \overline{AB}$

100000004

Triple 3-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

All Inputs High = Low Out
Any Input Low = High Out

$Y = \overline{ABC}$

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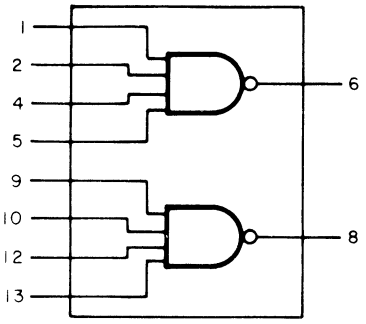
100000005

Dual 4-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

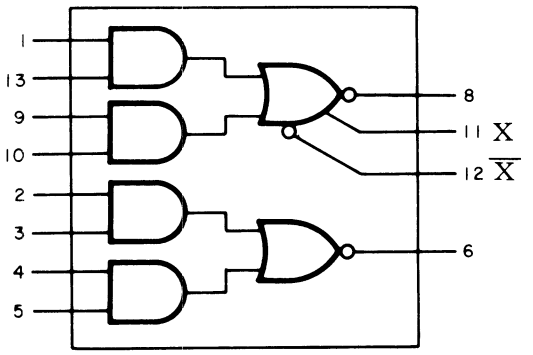
TRUTH TABLE

All Inputs High = Low Out
Any Input Low = High Out
$Y=\overline{ABCD}$

100000006

Dual Extendable AND-OR-INVERT Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

$(2\cdot3)+(4\cdot5) = 6$
$(\overline{2} + \overline{3}) + (\overline{4} + \overline{5}) = 6$

Four extenders may be tied to these terminals.

$Y_8=\overline{AB+CD+X}$
$Y_6=\overline{AB+CD}$
X = Output of DGC 10000039

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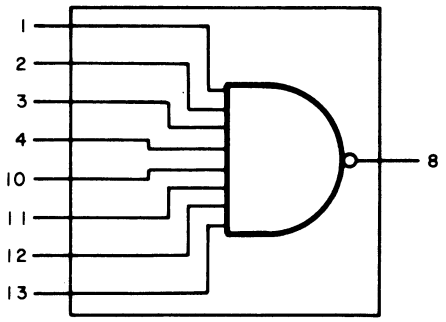
100000007

8-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

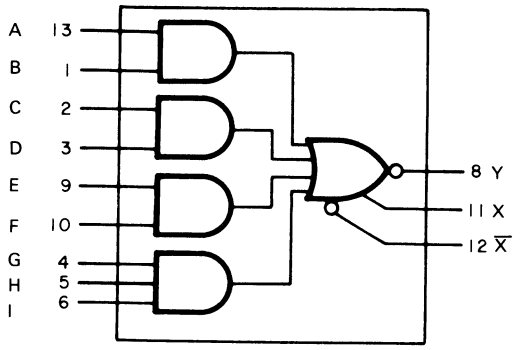
TRUTH TABLE

All Inputs High = Low Out
Any Input Low = High Out

100000008

Single Extendable AND-OR-INVERT Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

$8 = \overline{(1\cdot13)+(2\cdot3)+(9\cdot10)+(4\cdot5\cdot6)+11+\overline{12}}$
$Y = \overline{AB+CD+EF+GHI+X}$

Four extenders (100000039) may be tied to these terminals.

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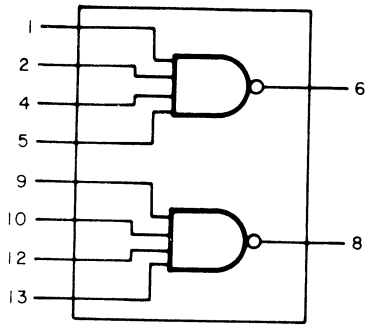
100000009

Dual 4-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

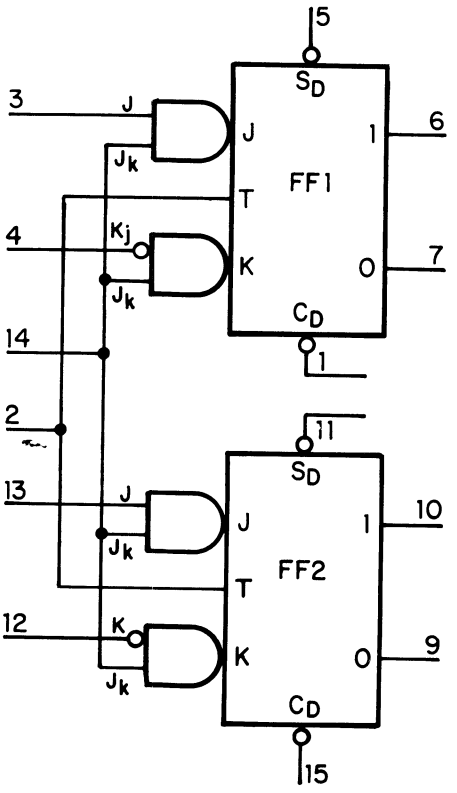
All Inputs High = Low Out
Any Input Low = High Out

$Y = \overline{ABCD}$

100000011

Dual J-K Flip-Flop

BLOCK DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

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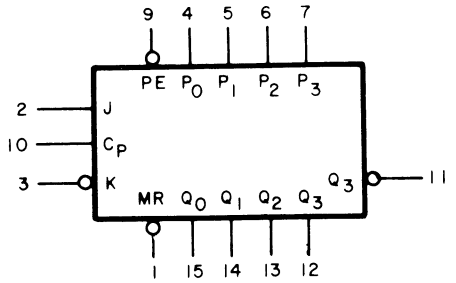
100000012

4-Bit Shift Register

PIN CONFIGURATION



V_{CC} = Pin 16

Gnd = Pin 8

PIN NOMENCLATURE

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active High) Input
$\overline{K}$	First Stage K (Active Low) Input
Cp	Clock Active High Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q_3}$	Complementary Last Stage Output

TRUTH TABLE FOR SERIAL ENTRY

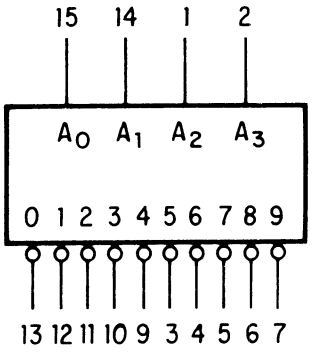
J	$\overline{K}$	Q_o at $t_{(n+1)}$
L	L	L
L	H	Q_o at t_n (no change)
H	L	$\overline{Q}_o$ at t_n (toggles)
H	H	H

$\overline{PE}$ = High, $\overline{MR}$ = High, (n+1) indicates state after next clock.

100000013

One-Of-Ten Decoder

PIN CONFIGURATION



V_{CC} = Pin 16

Gnd = Pin 8

PIN NAMES

A_0, A_1, A_2, A_3 = Addressed Inputs

$\overline{0}$ to $\overline{9}$ = Outputs, Active LOW

The 100000013 is a multipurpose decoder designed to accept four active HIGH BCD inputs and to provide ten mutually exclusive active LOW outputs, as shown by the logic symbol.

The logic design ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the device is used as a one-of-eight decoder.

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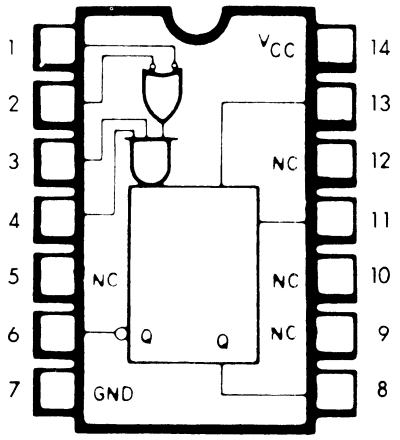
100000015

Retriggerable Monostable Multivibrator

PIN CONFIGURATION



TRUTH TABLE

Pin Numbers				
1	2	3	4	Operation
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

$T\ (\text{trigger}) = (\overline{1} + \overline{2}) \cdot 3 \cdot 4$

Change of T from FALSE to TRUE causes trigger.

H = HIGH voltage level $\geqslant V_{IH}$

L = LOW voltage $\leqslant V_{IL}$

L→H = transition from LOW to HIGH voltage level

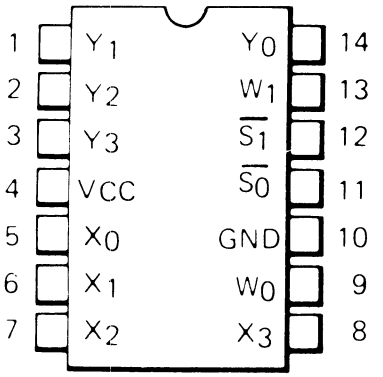
H→L = transition from HIGH to LOW voltage level

X = Don't care (either HIGH or LOW voltage level)

100000016

16-Bit Coincident Select Read-Write Memory

PIN CONFIGURATION



X,Y – Address
W – Write Input
S – Sense Output

This device is comprised of 16-bit, bit-oriented, non-destructive readout memory cells. These memory cells, organized as 16 words by one bit, are designed for high speed scratch-pad memory applications.

The memory cell consists of 16 RS flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.4 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the $\overline{S_1}$ output will be LOW and the $\overline{S_0}$ output will be HIGH. If the addressed bit location contains a "0", the $\overline{S_1}$ output will be HIGH and the $\overline{S_0}$ output will be LOW.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a HIGH level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a HIGH level.

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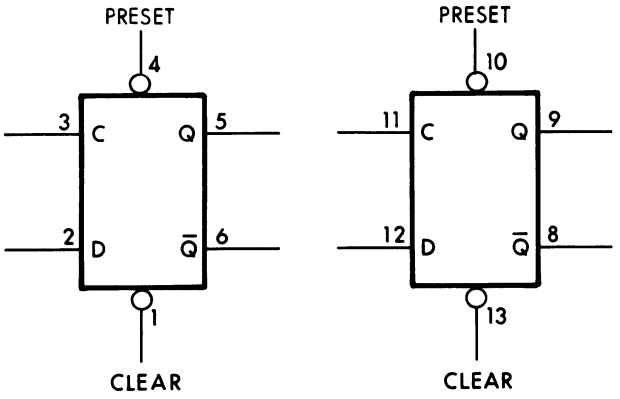
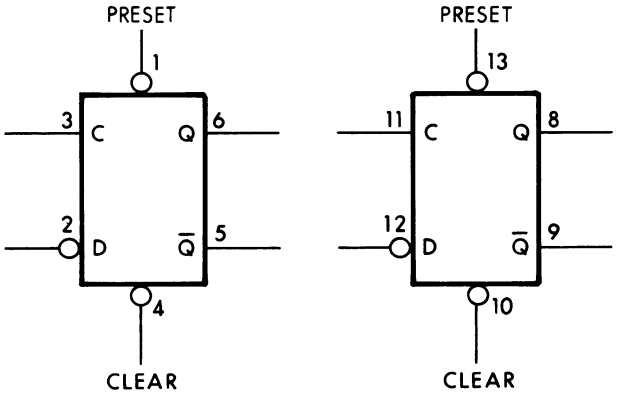
100000017

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



Alternate Pin Connections



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

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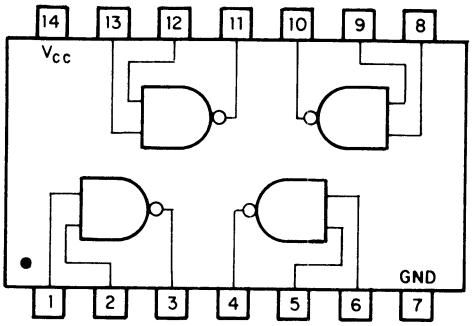
100000019

Quad 2-Input NAND Interface Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

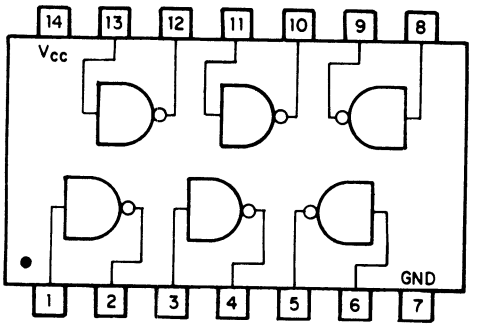
V_{IN}	V_{IN}	V_{OUT}
L	L	H
L	H	H
H	L	H
H	H	L

$Y = \overline{AB}$

100000020

Hex Inverter

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

$Y = \overline{A}$

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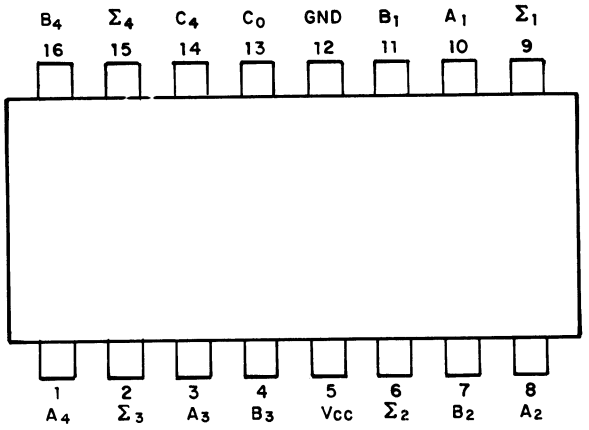
100000021

4-Bit Binary Full Adder (Look Ahead Carry)

PIN CONFIGURATION



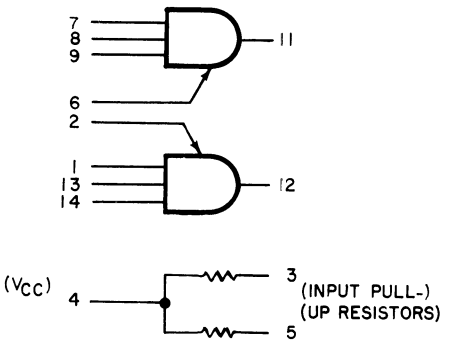
TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

100000023

Dual Pulse Shaper-Delay AND Gate

LOGIC DIAGRAM



$Y = ABCD$

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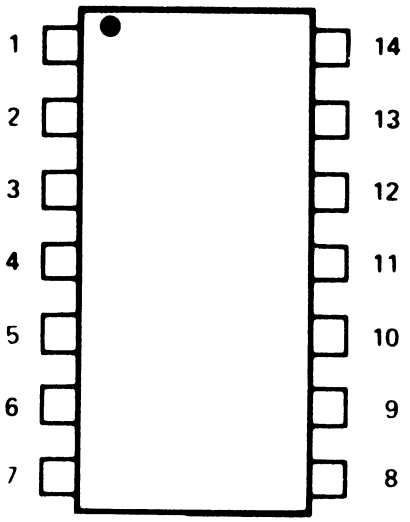
100000024

Dual Differential Amplifier

PIN CONFIGURATION



PIN DESIGNATIONS

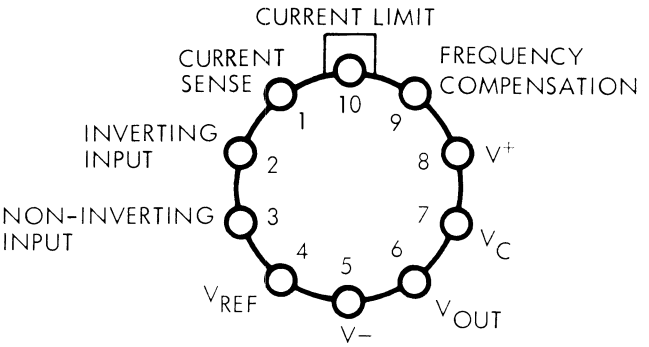
1.	Output B	8.	Source 2
2.	Output A	9.	Bias
3.	Input A	10.	Input D
4.	Input B	11.	Input C
5.	Reference	12.	Output C
6.	Source 1	13.	Output D
7.	Ground	14.	V^+

The 100000024 is a dual high-frequency differential amplifier with associated constant current sources and biasing elements contained within a silicon monolithic epitaxial substrate. This device is intended for RF-IF amplifier service to beyond 100mHz. Circuit layout provides for connection as either a high-gain, common-emitter, common-base, cascade amplifier or a common-collector, common-base, differential amplifier. Automatic gain control may be applied to either circuit.

100000026

Precision Voltage Regulator

PIN CONFIGURATION



Note: pin 5 is connected to case

The 100000026 is a monolithic voltage regulator consisting of a temperature-compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

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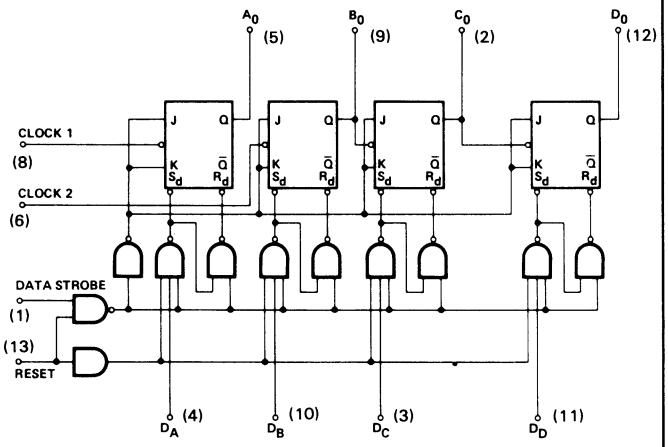
100000028

4-Bit Binary Counter/Storage Element

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 7

The Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level.

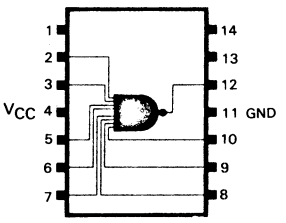
Both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse; however, there is no restriction on the transition time since the individual binaries are level-sensitive.

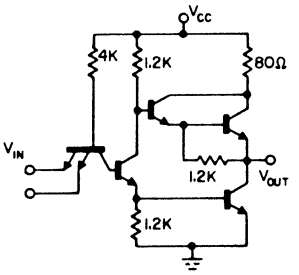
100000033

8-Input NAND Gate

PIN CONFIGURATION



LOGIC DIAGRAM



NOTE: Component values are typical.

The 100000033 performs the NAND function for positive logic and the NOR function for negative logic. It features a totem-pole arrangement using a Darlington Pair for active pullup. It provides very low output impedance for the high output state.

$$Y = \overline{ABCDEFGH}$$

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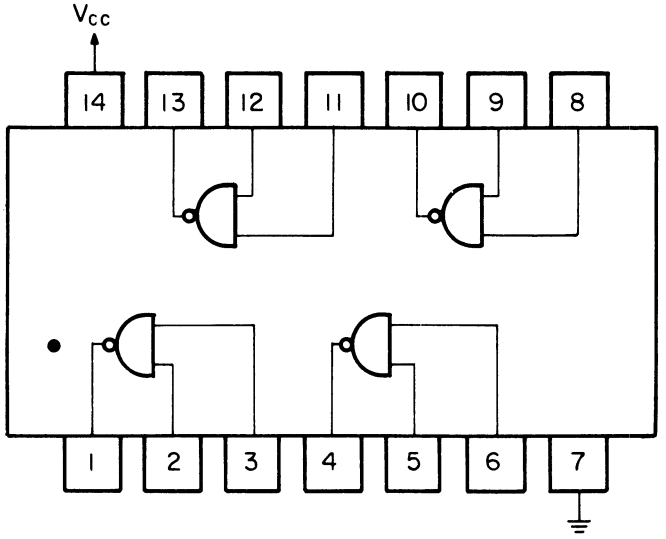
100000036

Quad 2-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14

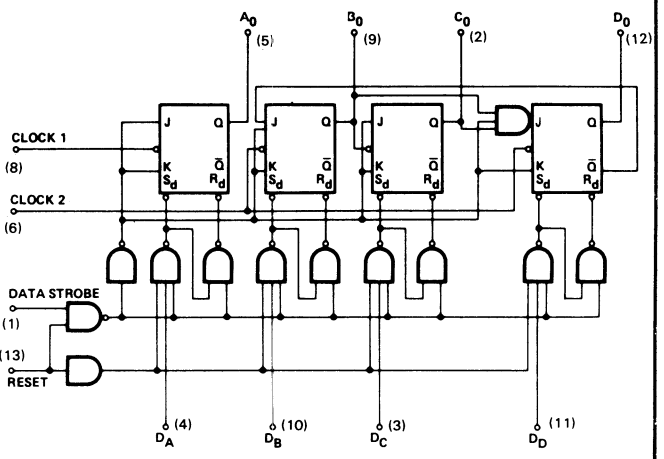
Gnd = Pin 7

$Y = \overline{AB}$

100000038

BCD Decade Counter/Storage Element

LOGIC DIAGRAM



The Decade Counter can be connected in the BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level.

Both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse; however, there is no restriction on the transition time since the individual binaries are level-sensitive.

V_{CC} = Pin 14

Gnd = Pin 7

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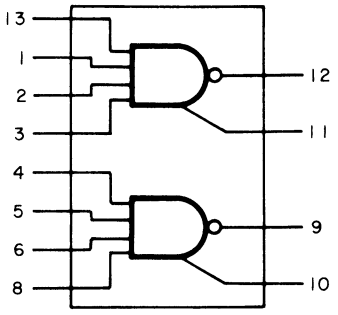
100000039

Dual Extender AND-OR-INVERT Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

$4 \cdot 5 \cdot 6 \cdot 8 = \overline{9}$

$\overline{4} + \overline{5} + \overline{6} + \overline{8} = 9$

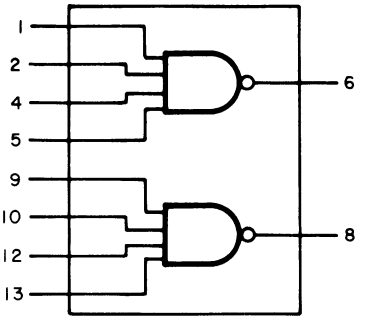
Extender for use with 100000006 and 100000008.

Y = ABCD when connected to x and $\bar{x}$ inputs of DGC 100000006; 100000376; or 10000

100000040

Dual 4-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

All Inputs High = Low Out
Any Input Low = High Out

$Y = \overline{ABCD}$

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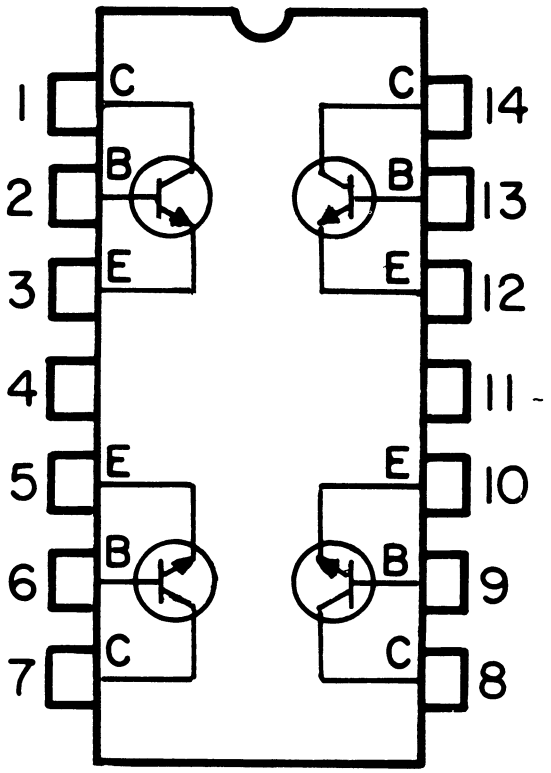
100000041

NPN Quad Core Driver

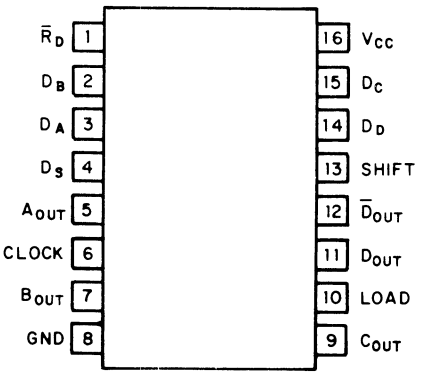
PIN CONFIGURATION

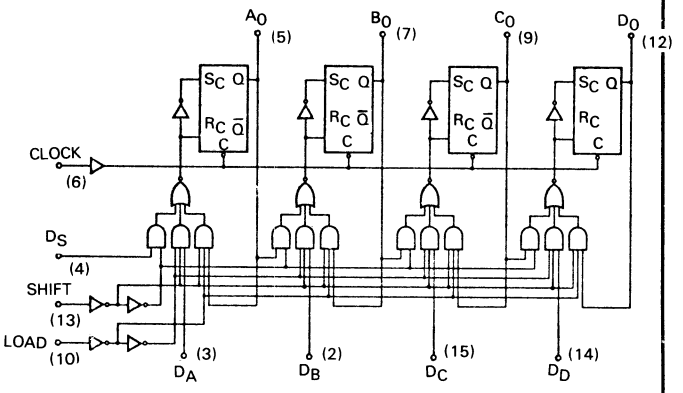


100000042

4-Bit Shift Register

PIN CONFIGURATION





V_{CC} = (16)
GND = (7)
( ) = denotes pin numbers

TRUTH TABLE

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

This 4-bit shift register has both a serial and a parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

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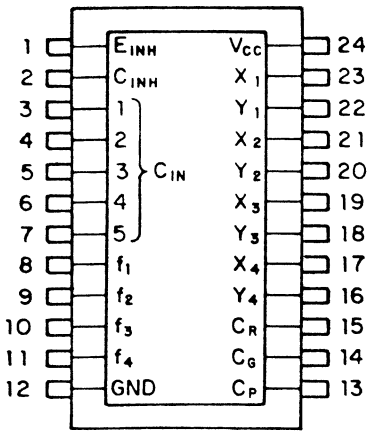
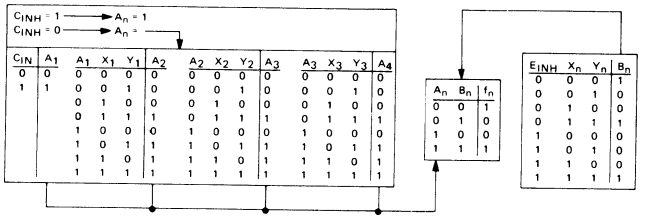
100000043

Arithmetic Logic Element

PIN CONFIGURATION



TRUTH TABLE



C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

This arithmetic logic element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder, this device permits high speed parallel addition of four sets of data and has both simultaneous addition on a character to character and on a bit to bit basis.

When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G), Propagated (C_p) and Ripple (C_R).

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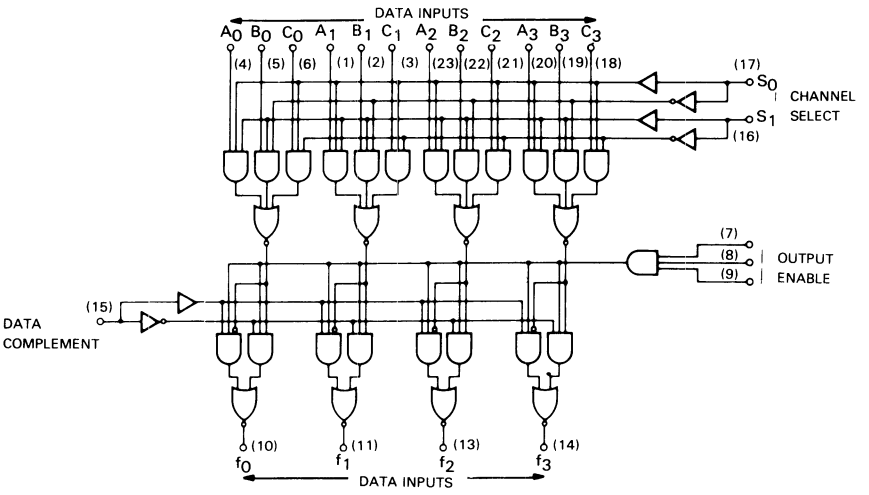
100000044

3-Input, 4-Bit Digital Multiplexer

LOGIC DIAGRAM

(Open Collector)



TRUTH TABLE

Data Input A_n	B_n	C_n	Channel Select S_0	S_1	Data Complement	Output Enable '044	Data Outputs
A_n	x	x	1	1	0	1	A_n
x	B_n	x	0	1	0	1	B_n
x	x	C_n	1	0	0	1	C_n
x	x	x	0	0	0	1	0
A_n	x	x	1	1	1	1	$\overline{A}_n$
x	B_n	x	0	1	1	1	$\overline{B}_n$
x	x	C_n	1	0	1	1	$\overline{C}_n$
x	x	x	0	0	1	1	1
x	x	x	x	x	x	0	1

X = Either state.

The 3-input, 4-bit multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The data complement input controls the conditional complement circuit at the multiplexer output to effect either inverting or non-inverting data flow.

Gnd = Pin 12 V_{CC} = Pin 24

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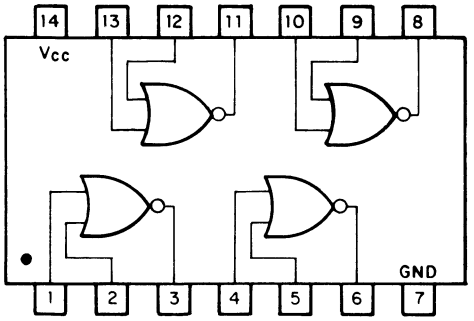
100000045

Quad 2-Input NOR Gate

PIN CONFIGURATION



TRUTH TABLE

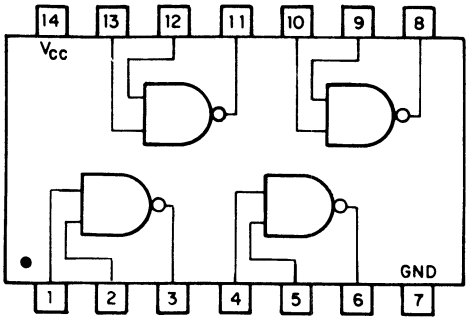
V_{IN}	V_{IN}	V_{OUT}
H	H	L
H	L	L
L	H	L
L	L	H

$Y = \overline{A+B}$

100000046

Quad 2-Input NAND Gate

PIN CONFIGURATION



$Y = \overline{AB}$

NOTE *The 100000046 is a high speed TTL device.*

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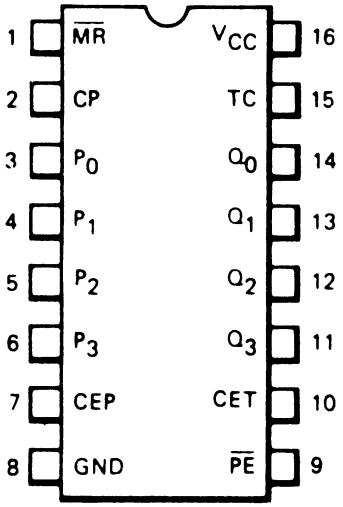
100000047

4-Bit Binary Counter

PIN CONFIGURATION



PIN NAMES

$\overline{PE}$ ..... Parallel Enable (Active LOW) Input

P_0, P_1, P_2, P_3 .. Parallel Inputs

CEP ..... Count Enable Parallel Input

CET ..... Count Enable Trickle Input

CP ..... Clock (Active HIGH Going Edge) Input

$\overline{MR}$ ..... Master Reset (Active LOW) Input

Q_0, Q_1, Q_2, Q_3 .. Parallel Outputs

TC ..... Terminal Count Outputs

MODE SELECTION

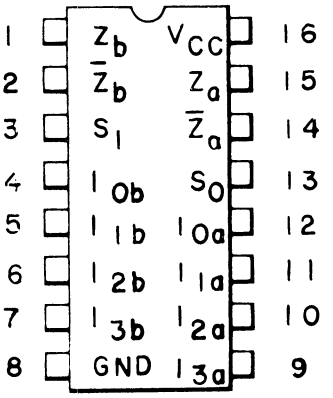
$\overline{PE}$	CEP	CET	Mode
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH) $TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

100000048

Dual 4-Input Multiplexer

PIN CONFIGURATION



PIN NAMES

S_0, S_1 ..... Common Select Inputs

Multiplexer A

I_{0a}, I_{1a}, I_{2a}, I_{3a} .. Multiplexer Inputs

Z_a ..... Multiplexer Output

$\overline{Z}_a$ ..... Complementary Multiplexer Output

Multiplexer B

I_{0b}, I_{1b}, I_{2b}, I_{3b} ... Multiplexer Inputs

Z_b ..... Multiplexer Output

$\overline{Z}_b$ ..... Complementary Multiplexer Output

TRUTH TABLE

Select Inputs		Inputs				Outputs	
S_0	S_1	I_0	I_1	I_2	I_3	Z	$\overline{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

The 100000048 is a monolithic, high speed, Dual Four-Input Multiplexer circuit, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. This device can generate any two functions of three variables. It may be cascaded to multiple levels so that any number of lines can be multiplexed on to a single output bus.

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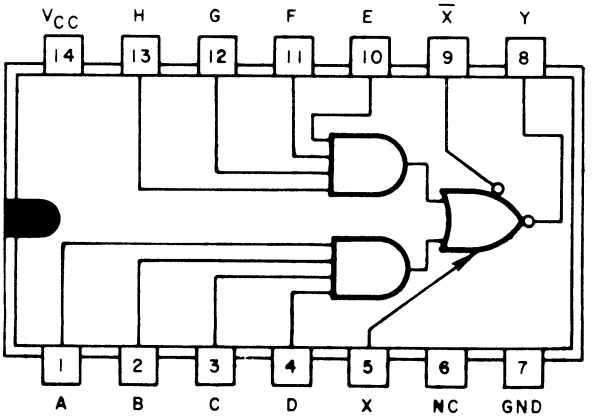
100000049

Expandable 4-Input AND-OR-INVERT Gate

PIN CONFIGURATION

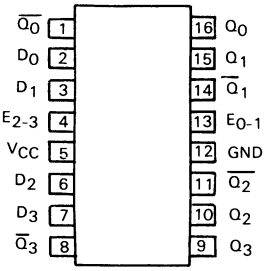


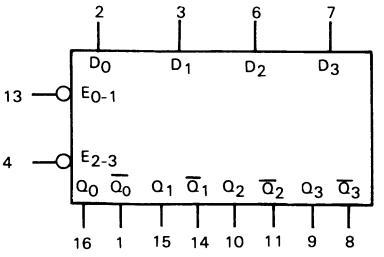
NOTE *The 100000049 is a high speed TTL device.*

100000050

4-Bit Bistable Latch

PIN CONFIGURATION





V_{CC} = Pin 5
GND = Pin 12

TRUTH TABLE

Inputs		Ouputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level; L = low level; X = irrelevant.
Q_0 = the level of Q before the high-to-low transition of G.

These latches are suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

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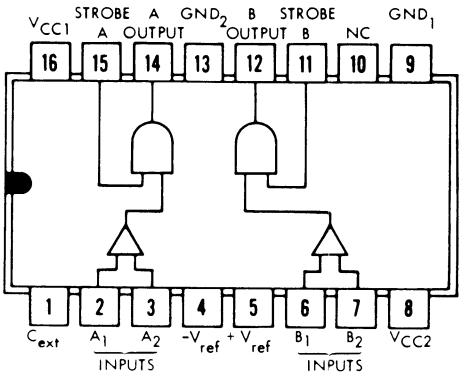
100000052

Dual Sense Amplifier

PIN CONFIGURATION



V_{CC1} = Pin 16
V_{CC2} = Pin 8
Gnd 1 = Pin 9
Gnd 2 = Pin 13

TRUTH TABLE

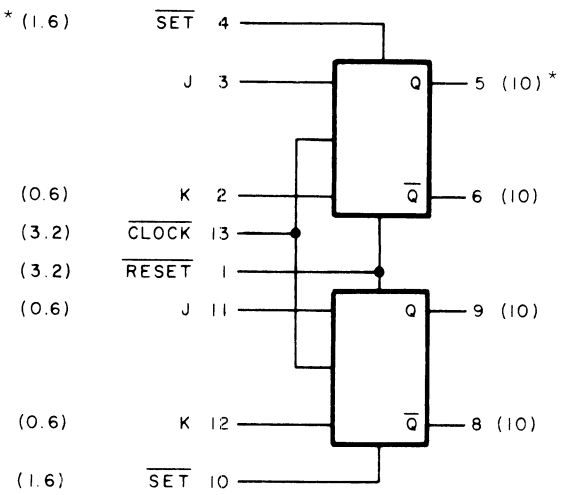
$IN_A \cdot$ STROBE A = OUT A
$\overline{IN}_A \cdot$ STROBE A = $\overline{\text{OUT A}}$
$IN_B \cdot$ STROBE B = OUT B
$\overline{IN}_B \cdot$ STROBE B = $\overline{\text{OUT B}}$

$Y = AS$

100000053

Dual J-K Flip-Flop

LOGIC DIAGRAM



*Loading Max. Shown in Parenthesis

V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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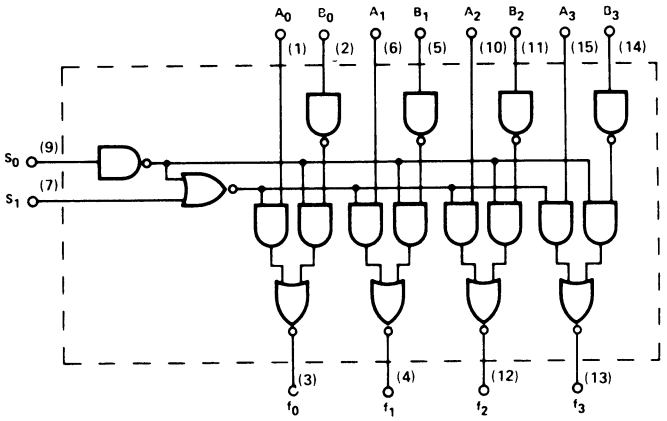
100000057

2-Input, 4-Bit Digital Multiplexer

PIN CONFIGURATION



V_{CC} = Pin 16
Gnd = Pin 8

$$Y = \overline{(\overline{S_0} + S_1)}\,(A_n) + \overline{S_0}\,B_n$$

TRUTH TABLE

Select Lines		Outputs
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

The 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing TTL circuit structures. The 100000108 features a bare-collector output to allow expansion with other devices.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3); B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform Addition/Subtraction. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

NOTE *The 100000057 has open collector outputs.*

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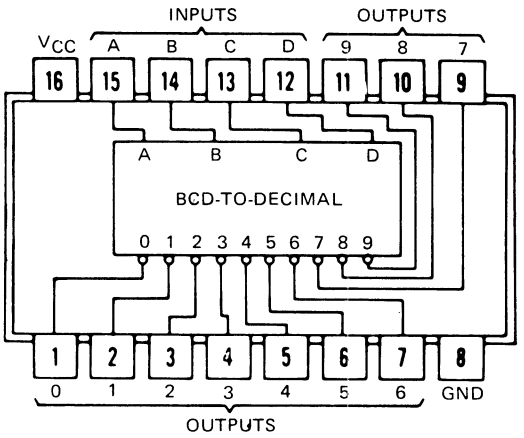
100000058

BCD-To-Decimal Decoder-Driver

PIN CONFIGURATION



FUNCTION TABLE

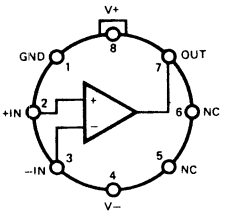
	Inputs				Outputs									
No.	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off); L = low level (on).

100000059

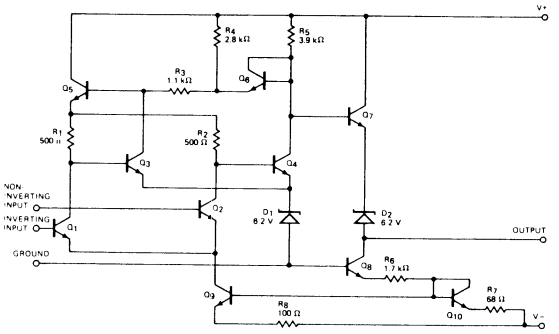
High Speed Differential Voltage Comparator

PIN CONFIGURATION



NOTE: Pin 4 connected to case.

EQUIVALENT CIRCUIT



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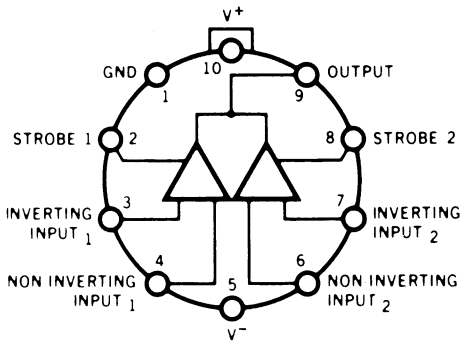
100000060

Dual Comparator

PIN CONFIGURATION



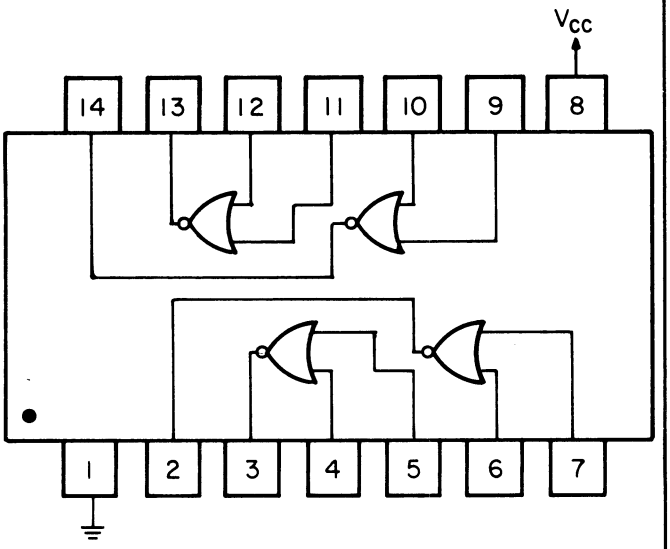
This device is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided.

100000061

Quad 2-Input NOR Gate

PIN CONFIGURATION



$Y = \overline{A + B}$

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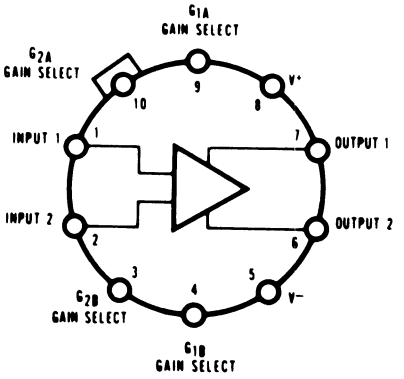
100000062

Differential Video Amplifier

PIN CONFIGURATION

Top View

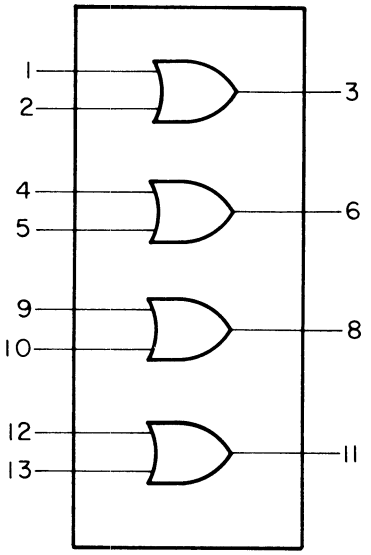


This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

100000063

Quad 2-Input OR Gate

PIN CONFIGURATION



V_{CC} = Pin 14

Gnd = Pin 7

3 = 1 + 2

Y = A + B

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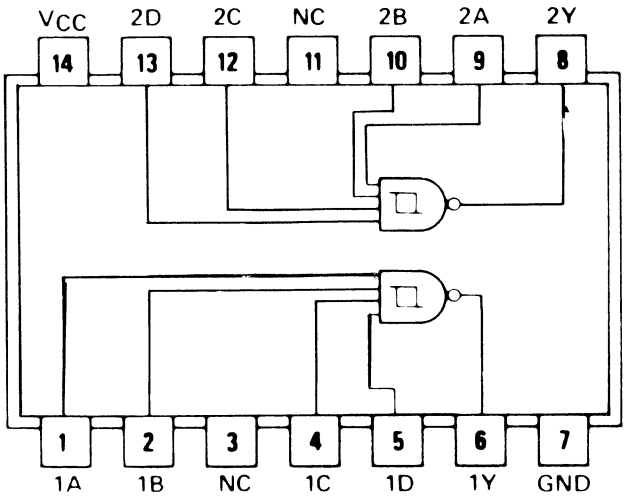
100000066

Dual 4-Input Positive-NAND Schmitt Trigger

PIN CONFIGURATION



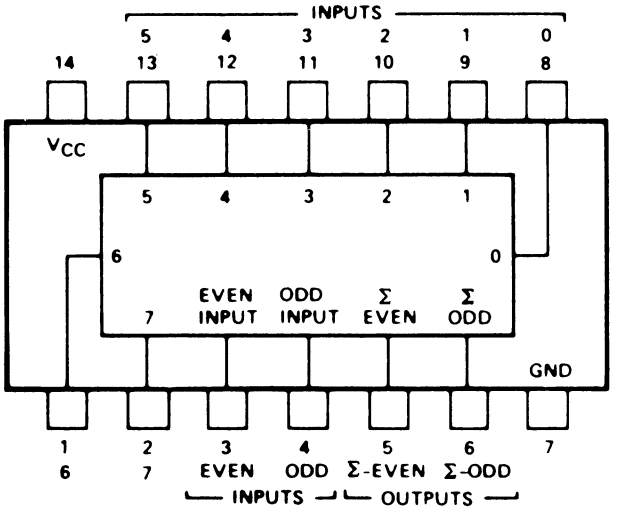
V_{CC} = Pin 14
Gnd = Pin 7
NC = No internal connection

Positive logic: $Y = \overline{ABCD}$

100000067

8-Bit Odd/Even Parity Generator/Checker

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

Inputs			Outputs	
Σof 1's at 0 thru 7	Even	Odd	Σ Even	Σ Odd
Even	1	0	1	0
Odd	1	0	0	1
Even	0	1	0	1
Odd	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant.

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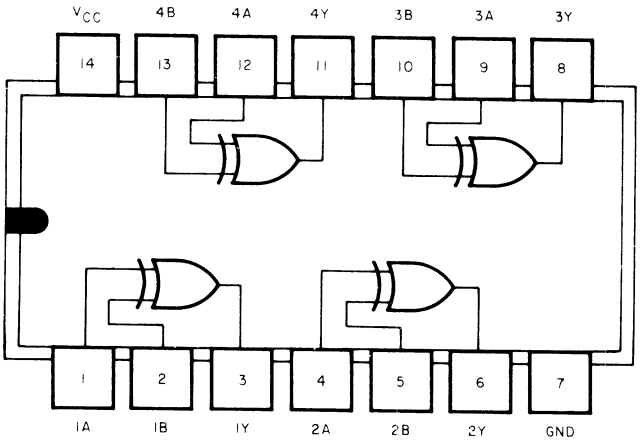
100000068

Quad 2-Input Exculsive-OR Gate

PIN CONFIGURATION



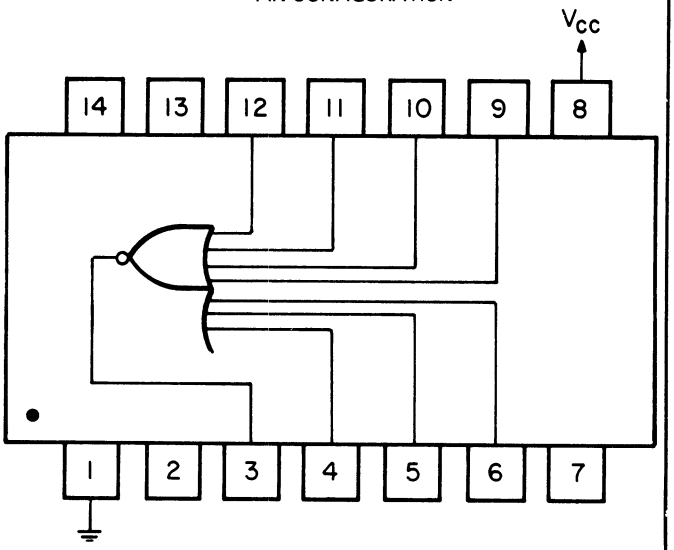
Positive logic: $Y = A \oplus B$

or $\overline{A}B + A\overline{B}$

100000069

Single 7-Input NOR Gate

PIN CONFIGURATION



$Y = \overline{A + B + C + D + E + F + G}$

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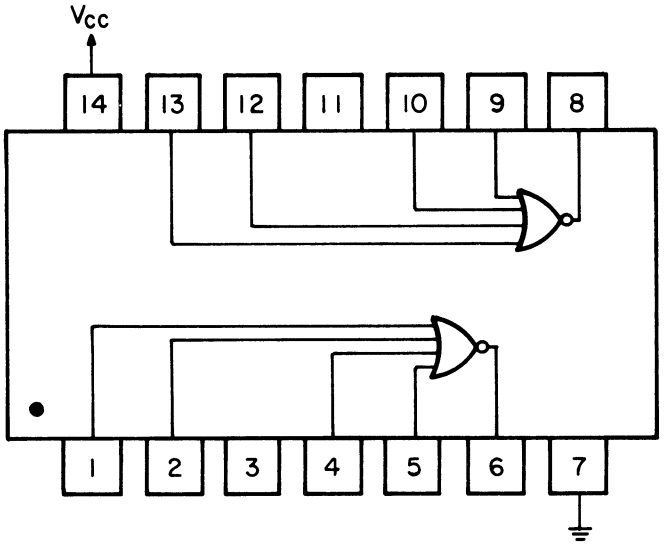
100000070

Dual 4-Input NOR Gate

PIN CONFIGURATION

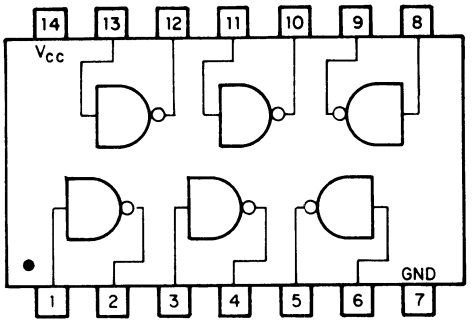


$$Y = \overline{A + B + C + D}$$

100000071

Hex Inverter

PIN CONFIGURATION



$$Y = \overline{A}$$

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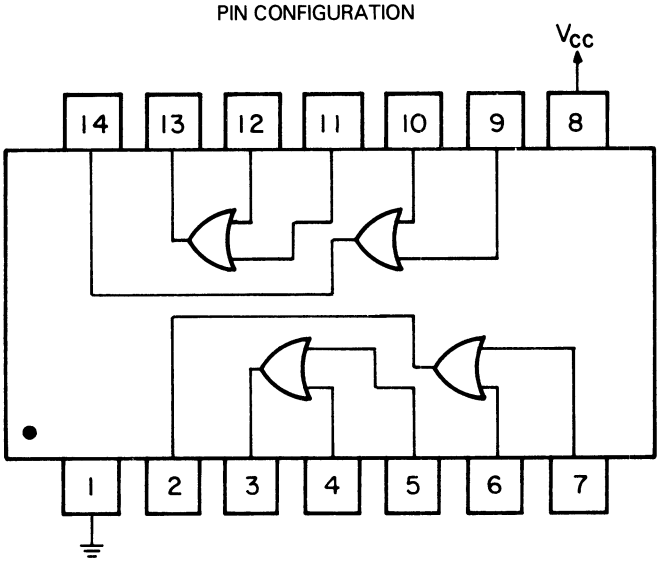
100000072

Quad 2-Input OR Gate

PIN CONFIGURATION

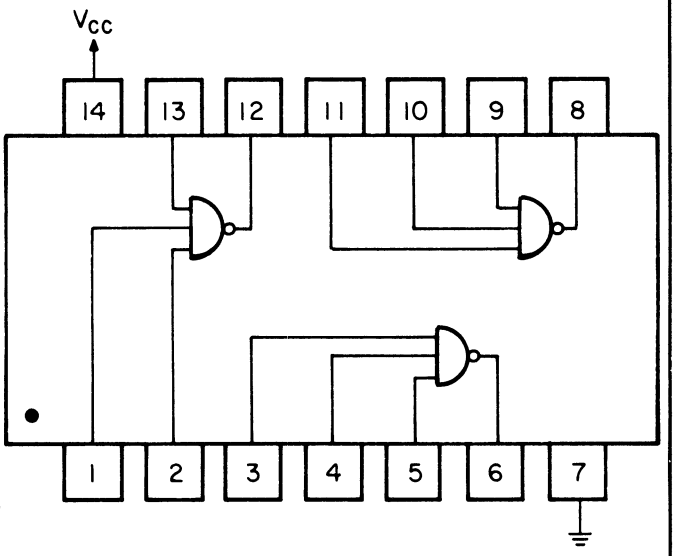


$Y = A + B$

100000073

Triple 3-Input NAND Gate

PIN CONFIGURATION



$Y = \overline{ABC}$

NOTE *The 100000073 is a high speed TTL device.*

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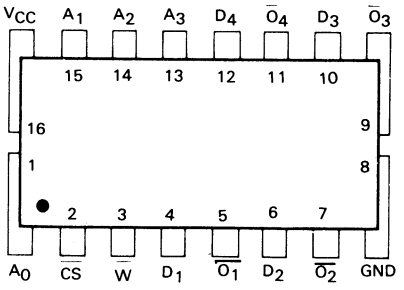
100000074

64-Bit RAM

PIN CONFIGURATION



NOTE: PIN 1 is marked for orientation.

TRUTH TABLE

Inputs			Outputs	Mode	
$\overline{CS}$	$\overline{W}$	D_i	$\overline{O}_i$		
H	L	L	H	No Selection)	Note
H	L	H	L	No Selection)	
H	H	X	H	No Selection	
L	L	L	H	Write "0"	
L	L	H	L	Write "1"	
L	H	X	$\overline{D}_i(t_{n-x})$	Read	

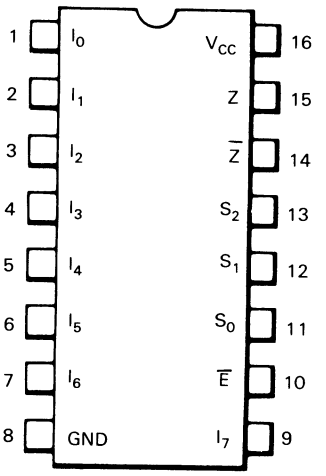
H = HIGH Voltage Level
L = LOW Voltage Level

Note: When the chip select $\overline{CS}$ input is HIGH and the Write Enable $\overline{W}$ is LOW data is not written into the memory. However, the data outputs do follow the data inputs inverted.

100000075

Eight-Input Multiplexer

PIN CONFIGURATION



Pin Names

S_0, S_1, S_2 ... Select Inputs
$\overline{E}$..... Enable (Active LOW) Input
I_0 to I_7 ..... Multiplexer Inputs
Z..... Multiplexer Output
$\overline{Z}$..... Complementary Multiplexer Output

The 100000075 is a monolithic, high speed, eight-input digital multiplexer circuit. It can be used as a universal function generator to generate any logic function of four variables. It is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select Inputs, S_0, S_1 and S_2. Both assertion and negation outputs are provided. The Enable Input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs.

The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

This device provides the ability, in one package, to select from eight sources of data or control information. Proper manipulation of the inputs can provide any logic function of four variables and its negation.

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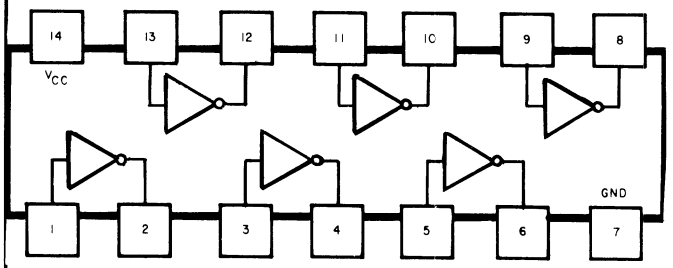
100000076

Hex Inverter

PIN CONFIGURATION



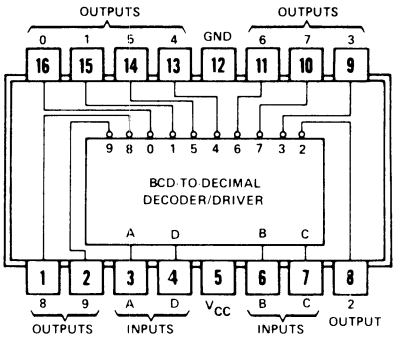
NOTE *The 100000076 is a high speed TTL device.*

$$Y = \overline{A}$$

100000077

BCD-To-Decimal Decoder-Driver

PIN CONFIGURATION



FUNCTION TABLE

Input				Output
D	C	B	A	On*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

H = high level; L = low level.
* All other outputs are off.

The 100000077 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore, this device, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing edge zeroes in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

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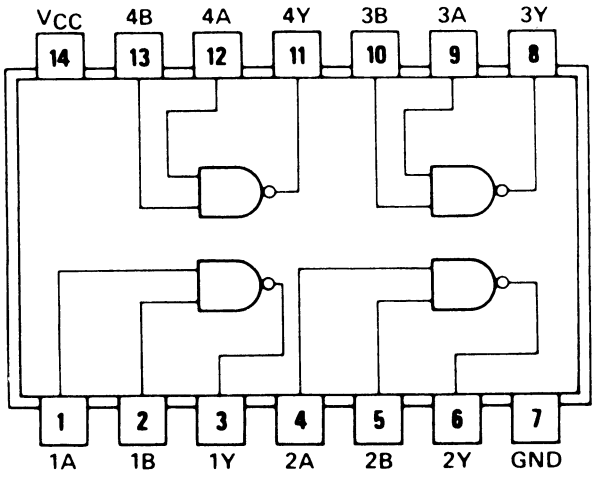
100000078

Quad 2-Input Positive-NAND Buffer with Open-Collector Outputs

PIN CONFIGURATION

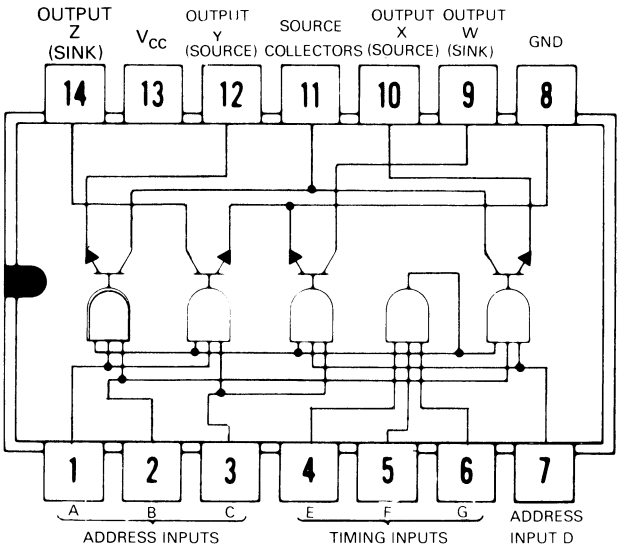


Positive logic: $Y = \overline{AB}$

100000079

Memory Driver with Decode Inputs

PIN CONFIGURATION



TRUTH TABLE

Inputs							Outputs			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	On	Off	Off	Off
0	1	0	1	1	1	1	Off	On	Off	Off
1	1	0	0	1	1	1	Off	Off	On	Off
1	0	1	0	1	1	1	Off	Off	Off	On
X	X	X	X	0	X	X	Off	Off	Off	Off
X	X	X	X	X	0	X	Off	Off	Off	Off
X	X	X	X	X	X	0	Off	Off	Off	Off

Notes:

X = Logical 1 or logical 0.

Not more than one output is allowed to be On at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

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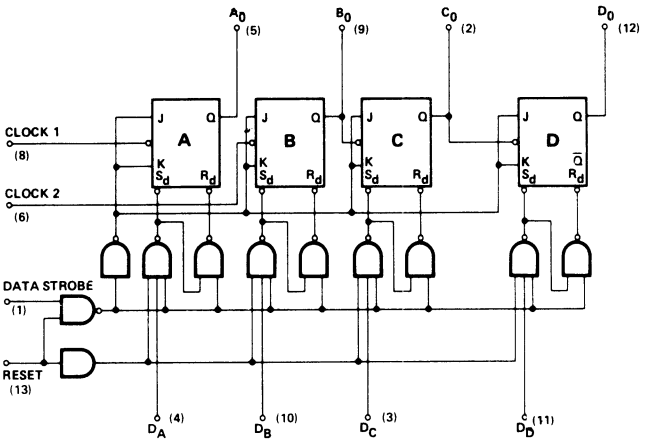
100000080

Presettable High Speed Binary Counter

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers for DIP packages.

TRUTH TABLE

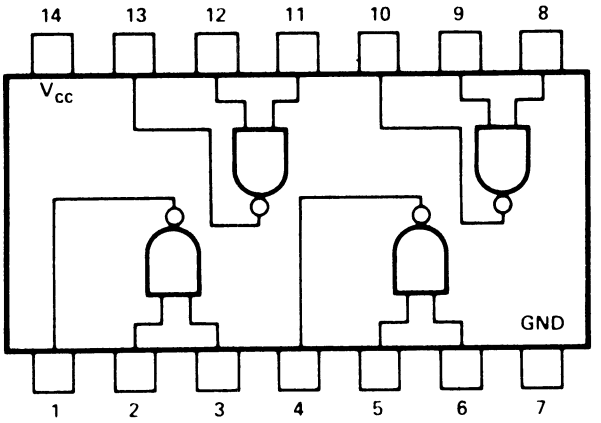
Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

The 100000080 Presettable High Speed Binary Counter may be connected as a divide-by-two, four, eight or sixteen counter.

100000081

Quad 2-Input Positive-NAND Buffer

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

The 100000081 is a NAND Gate with an open-collector output for "WIRE-AND" applications.

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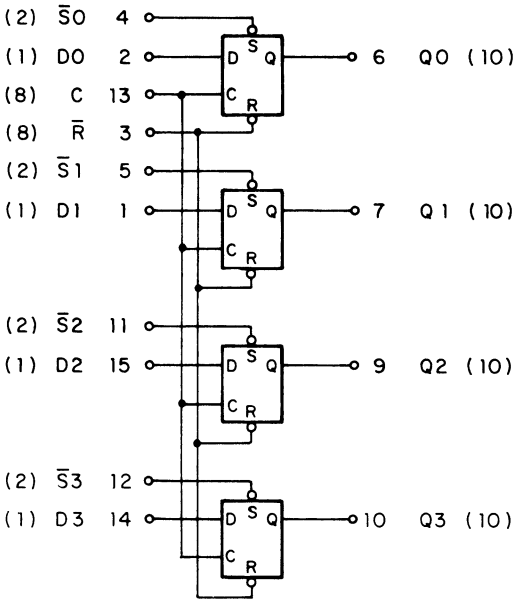
100000082

Quad D Type Flip-Flop

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE

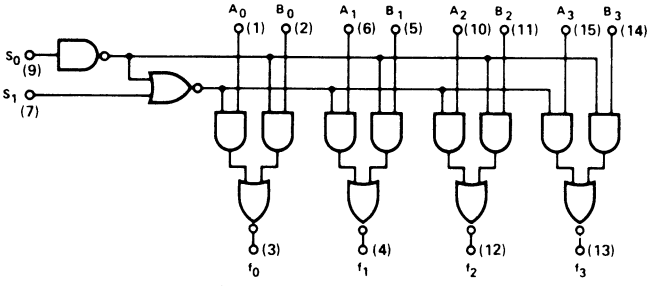
D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = Time period prior to clock pulse
Q_n = Time period following clock pulse

100000083

2-Input, 4-Bit Digital Multiplexer

LOGIC DIAGRAM



$Y = \overline{(\overline{S_0} + S_1)}\,(A_n) + \overline{S_0}\,\overline{B_n}$

V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE

S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

This multiplexer has inverting data paths. It has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty of these devices in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

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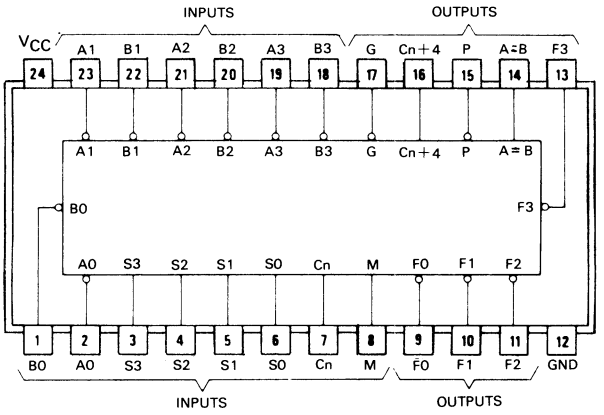
100000084

Arithmetic Logic Unit/Function Generator

PIN CONFIGURATION



Pin Designations

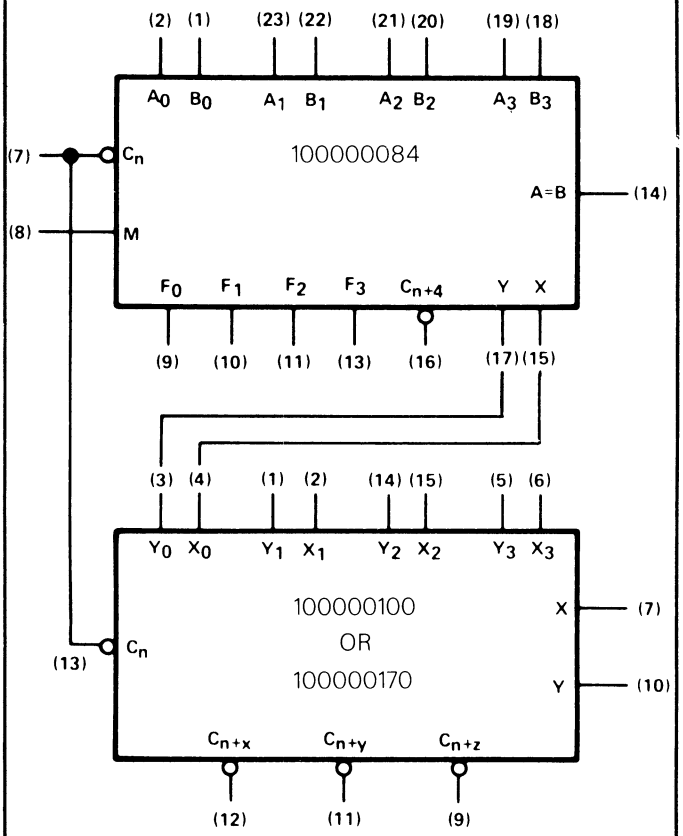
Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

Figure 1



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100000084 (Continued)

Figure 2

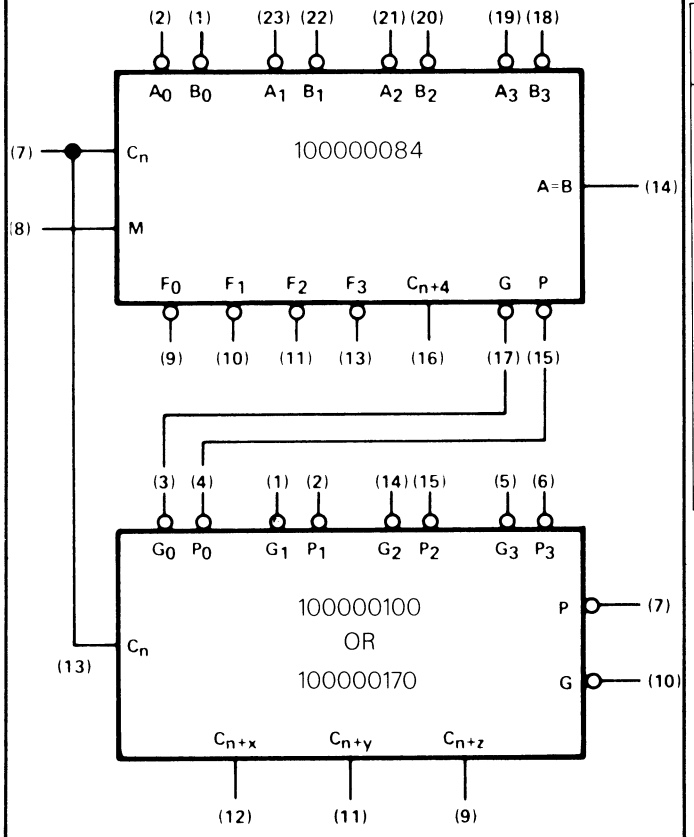

Table 1

Selection S3 S2 S1 S0	M = H Logic Functions	Active-High Data M = L: Arithmetic Operations	
		C_n = H (no carry)	Cn = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A Plus 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L H L H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L H H L	F = A⊙B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H L L H	F = $\overline{A⊙B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

Table 2

Selection S3 S2 S1 S0	M = H Logic Functions	Active-Low Data M = L: Arithmetic Operations	
		C_n = L (no carry)	C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A Minus 1	F = A
L L L H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L H L H	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L H H L	F = $\overline{A⊙B}$	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H L L L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	F = A⊙B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = $\overline{AB}$	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

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100000084 (Continued)

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	A $\leqslant$ B	A $\geqslant$ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A $\geqslant$ B	A $\leqslant$ B

These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

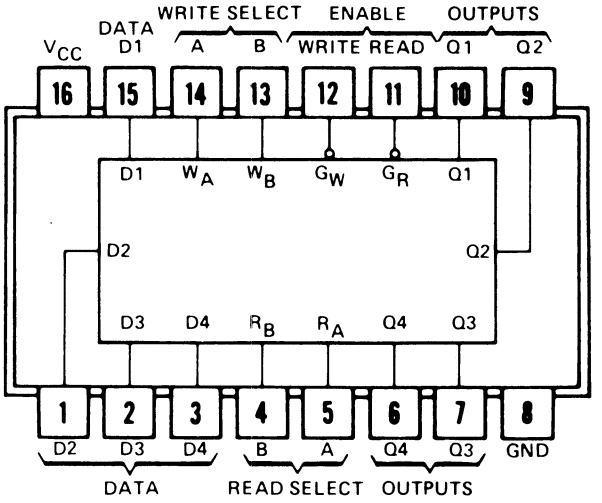
ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

100000085

4-By-4 Register File

PIN CONFIGURATION



The 100000085 16-bit TTL register file is organized as 4 words of 4 bits each. Separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data; this permits simultaneous writing into one location and reading from another word location. The register file has a nondestructive readout in that data is not lost when addressed.

Four data inputs are available which are used to supply 4-bit words to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form; that is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

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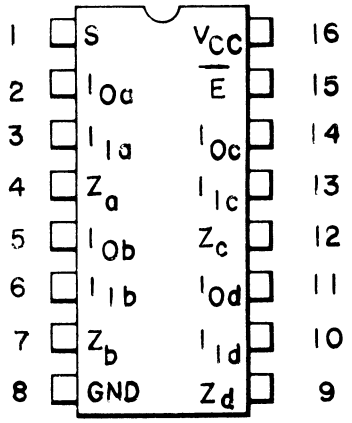
100000086

Quad 2-Input Multiplexer

PIN CONFIGURATION



Pin Names

S	Common Selected Input
$\overline{E}$	Enable (Active LOW)Inputs
I_{0a}, I_{1a}, I_{0b}, I_{1b}) I_{0c}, I_{1c}, I_{0d}, I_{1d})	Multiplexer Inputs
Z_a, Z_b, Z_c, Z_d	Multiplexer Output

The 100000086 Quad Two-Input Multiplexer consists of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output. The Enable input ($\overline{E}$) is active LOW. When not activated, all outputs (Z) are LOW regardless of other inputs.

TRUTH TABLE

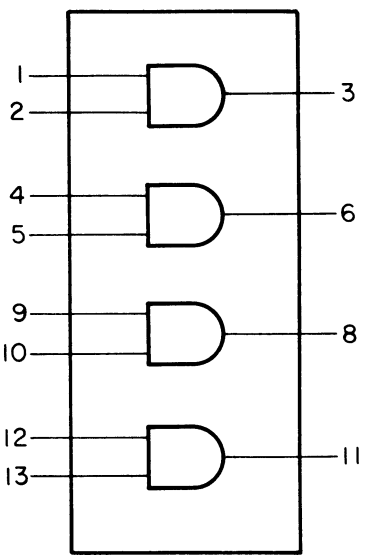
Enable	Select Input	Inputs		Output
$\overline{E}$	S	I_{0X}	I_{IX}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

100000089

Quad 2-Input AND Gate

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7
3 = 1 · 2

Y = AB

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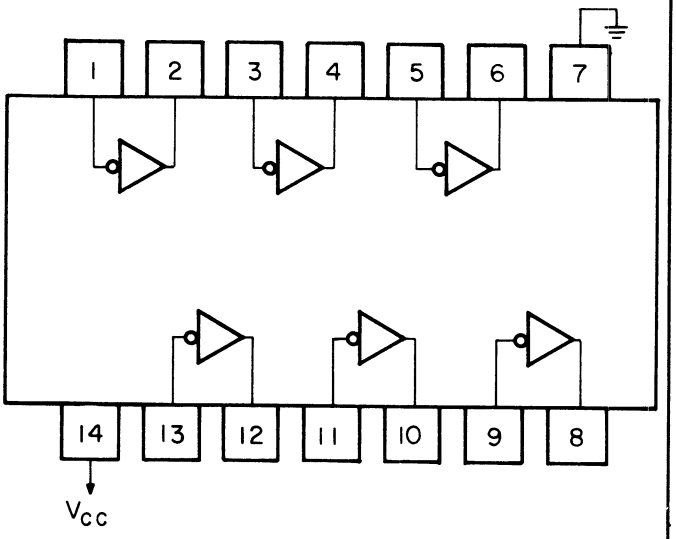
100000090

Hex Inverter

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

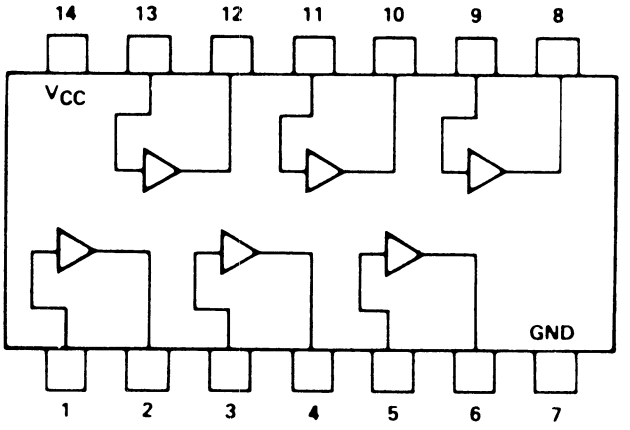
Positive logic: $Y = \overline{A}$

NOTE *The 100000090 is a low power TTL device.*

100000091

Hex Buffer/Driver with Open Collector High Voltage Outputs

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: Y = A

The 100000091 has standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays.

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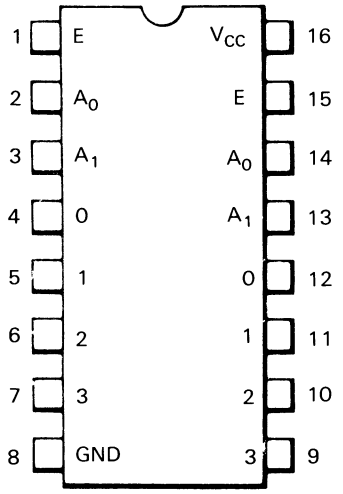
100000092

Dual One-of-Four Decoder

PIN CONFIGURATION



Pin Names

Decoder 1 and 2

$\overline{E}$ ..... Enable (Active LOW) Input

A_0, A_1 ..... Address Inputs

$\overline{0}, \overline{1}, \overline{2}, \overline{3}$ ..... (Active LOW) Outputs

TRUTH TABLE
Decoder 1 & 2

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

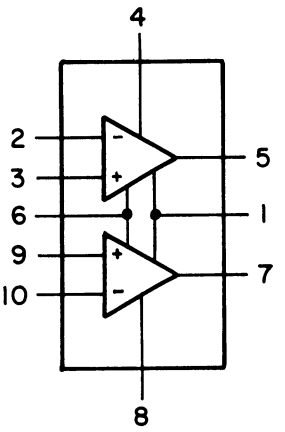
H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

The 100000092 consists of two independent multipurpose decoders, each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

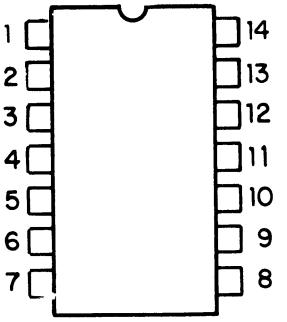
100000093

Monolithic Dual Operational Amplifier

PIN CONFIGURATION



CASE



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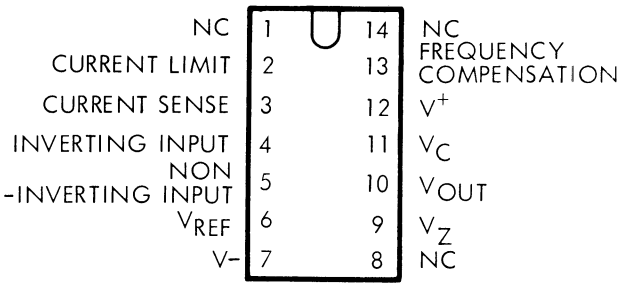
100000094

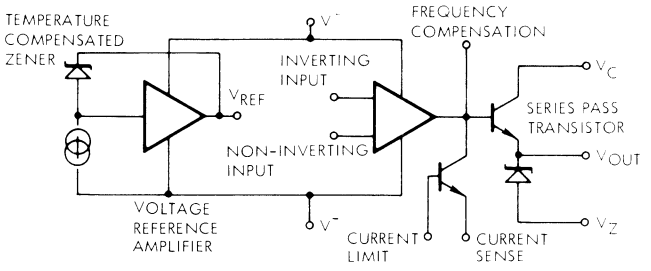
ADJ + 2 - 37V, 150mA
Precision Voltage Regulator

PIN CONFIGURATION



The 1000000094 is a precision voltage regulator consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

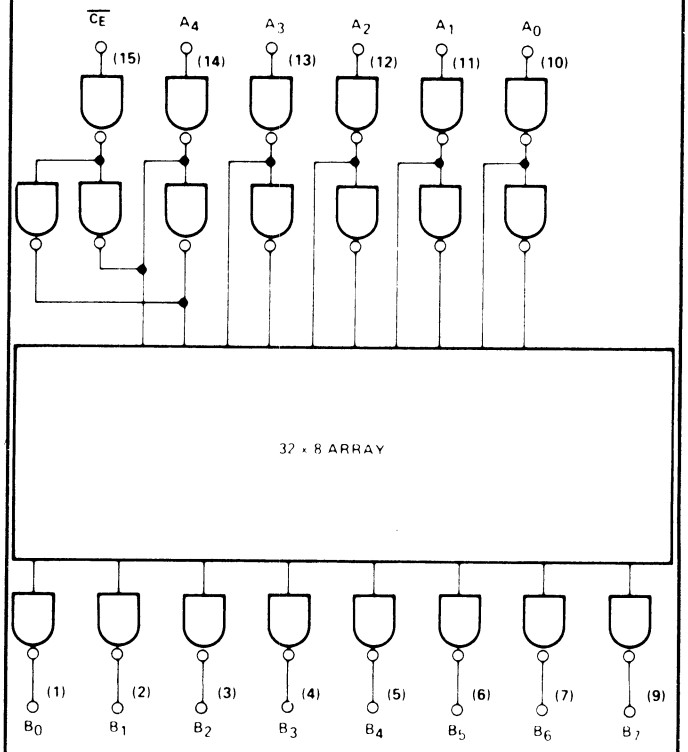
Equivalent Circuit



100000095 and 100000096

256-Bit Bipolar ROM

LOGIC DIAGRAM



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

These TTL 256-bit read only memories are organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Enable input is taken high.

The 100000095 and 100000096 are fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-AND operation with the outputs of other TTL or DTL devices.

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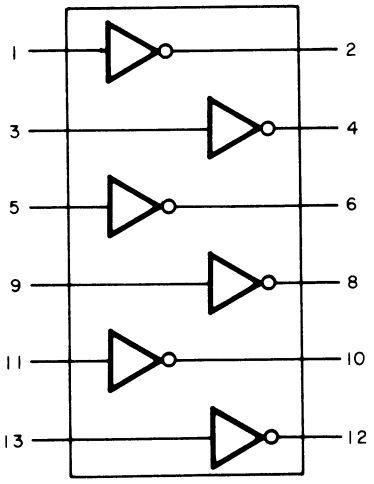
100000098

Hex Inverter

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

$Y = \overline{A}$

TRUTH TABLE

Any Input Low = High Out
Any Input High = Low Out

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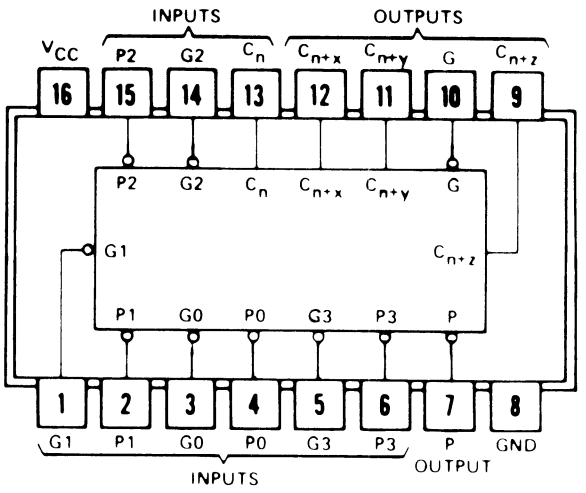
100000100

Look-Ahead Carry Generator

PIN CONFIGURATION



PIN DESIGNATIONS

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
Gnd	8	Ground

Positive Logic:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$

$$C_{n+y} = \overline{G}_1 + \overline{P}_1\overline{G}_0 + \overline{P}_1\overline{P}_0 C_n$$

$$C_{n+z} = \overline{G}_2 + \overline{P}_2\overline{G}_1 + \overline{P}_2\overline{P}_1\overline{G}_0 + \overline{P}_2\overline{P}_1\overline{P}_0 C_n$$

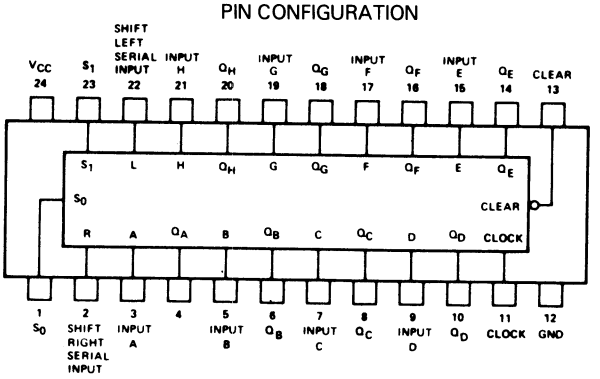
$$\overline{G} = \overline{G}_3(\overline{P}_3+\overline{G}_2)(\overline{P}_3+\overline{P}_2+\overline{G}_1)(\overline{P}_3+\overline{P}_2+\overline{P}_1+\overline{G}_0)$$

$$\overline{P} = \overline{P}_3\overline{P}_2\overline{P}_1\overline{P}_0$$

100000101

8-Bit Shift Register

PIN CONFIGURATION



TRUTH TABLE

Operation of Mode Control		
Inputs		
S_1	S_0	Mode
L	L	Inhibit Clock
H	L	Shift Left
L	H	Shift Right
H	H	Parallel Load

This 8-bit shift register contains 87 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load

Shift Right (in the direction Q_A toward Q_H)

Shift Left (in the direction Q_H toward Q_A)

Inhibit Clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

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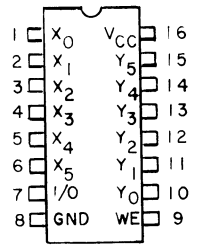
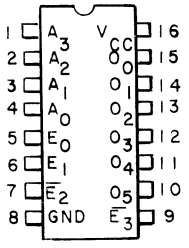
100000102 and 100000103

256-Bit RAM and Decoder/Driver

PIN CONFIGURATION



100000102



100000103

TRUTH TABLE

Binary Input To 100000103				3 of 6 Code Output of 100000103 Input to 100000102 (L = O or X or Y)						100000102 Internal X or Y Address
A3	A2	A1	A0	L0	L1	L2	L3	L4	L5	Row or Column
L	L	L	L	H	H	L	L	L	H	0
L	L	L	H	H	L	H	L	L	H	1
L	L	H	L	H	L	L	H	L	H	2
L	L	H	H	H	L	L	L	H	H	3
L	H	L	L	H	H	H	L	L	L	4
L	H	L	H	H	L	H	L	H	L	5
L	H	H	L	H	H	L	H	L	L	6
L	H	H	H	H	L	L	H	H	L	7
H	L	L	L	L	H	L	H	L	H	8
H	L	L	H	L	H	H	L	L	H	9
H	L	H	L	L	L	L	H	H	H	10
H	L	H	H	L	L	H	L	H	H	11
H	H	L	L	L	H	H	H	L	L	12
H	H	L	H	L	H	H	L	H	L	13
H	H	H	L	L	H	L	H	H	L	14
H	H	H	H	L	L	H	H	H	L	15

Note: Enables on 100000103 must be LLHH. Any other state on the enable inputs causes the Decoder/Driver outputs to go LOW, and addresses no internal row or column in the 100000102 memory matrix.

The 100000102 256-Bit Read/Write Memory and the 100000103 Decoder/Driver are components for use in high speed memory systems.

The 100000102 contains 256 bipolar storage cells arranged in a 16 by 16 format. Any one of the 256 cells may be accessed by supplying an address code on the X address inputs and the Y address inputs. Internal decoders decode the X and Y addresses into one of 16 rows and one of 16 columns in the matrix of storage cells. Data may be written into or read out from the cell lying at the intersection of the selected row and column.

The X and Y addresses supplied to the memory are partially decoded in a "3 of 6" code. Of the six X address lines and the six Y address lines there are always three lines HIGH and three lines LOW. There are 20 such combinations, 16 are decoded by the internal row and column decoders. The four unused combinations of 3 of 6 will not select any row or column. If there are more than three lines HIGH in either the X or Y address, then multiple row or column selection will occur. The sixteen 3 of 6 codes used by the 100000102 memory are generated by the 100000103 decoder/driver.

Data enters and leaves the memory on a single input/output (I/O) line (pin 7). The I/O line is an open collector output, so many 100000102 I/O lines can be connected together in a wired-OR configuration. Input data must be applied to the I/O lines through an open collector gate. Each I/O line requires a pull-up resistor to V_{CC}. The magnitude of the pull-up resistor is determined by the number of memory I/O lines tied together. The I/O of the memory which is not addressed will be HIGH.

Read/Write selection is determined by the state of pin 9, the active HIGH write enable. When WE is HIGH, the data on the I/O line will be written into the selected address in the 100000102. When the Write Enable line is LOW, data will be read out of the addressed location.

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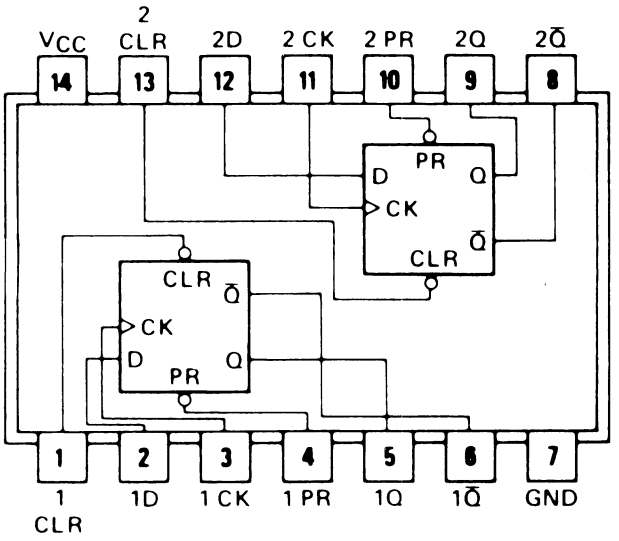
100000104

Dual D-Type Positive-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

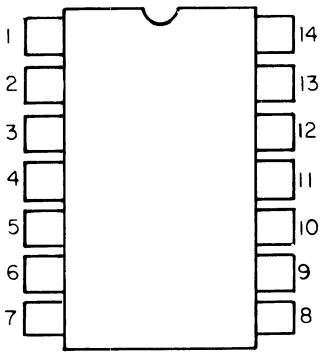
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000104 is a high speed TTL device.*

100000105

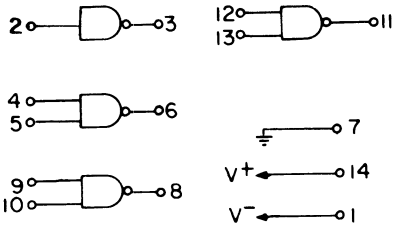
Quad MDTL Line Driver

PIN CONFIGURATION



$Y = \overline{AB}$

LOGIC DIAGRAM



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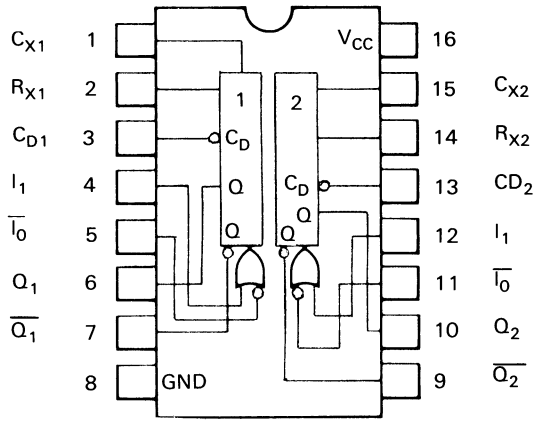
100000106

Dual Retriggerable Resettable Monostable Multivibrator

PIN CONFIGURATION



TRUTH TABLE

Pin Numbers			
5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geqslant V_{IH}$

L = LOW Voltage Level $\leqslant V_{IL}$

X = Don't Care

H→L = HIGH to LOW Voltage Level transition

L→H = LOW to HIGH Voltage Level transition

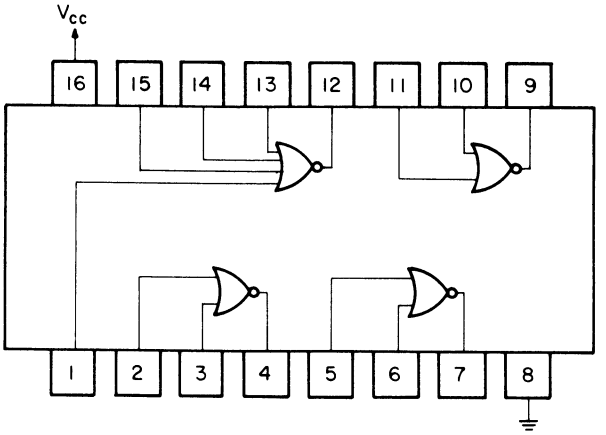
The Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components.

This device has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the device and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW.

100000107

Quad NOR Gate

PIN CONFIGURATION



The 100000107 consists of three 2-input and one 4-input NOR gates. The NOR gate produces a Low output if any of the inputs are High.

$$Y_4 = \overline{A + B}$$
$$Y_7 = \overline{A + B}$$
$$Y_9 = \overline{A + B}$$
$$Y_{12} = \overline{A + B + C + D}$$

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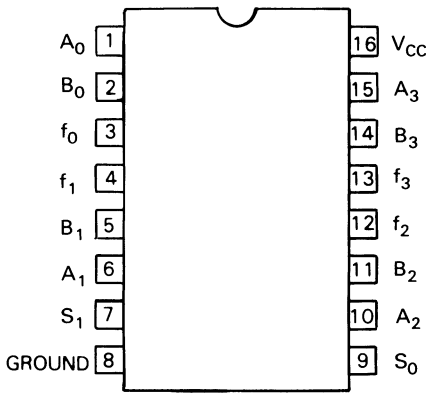
100000108

2-Input, 4-Bit Digital Multiplexer

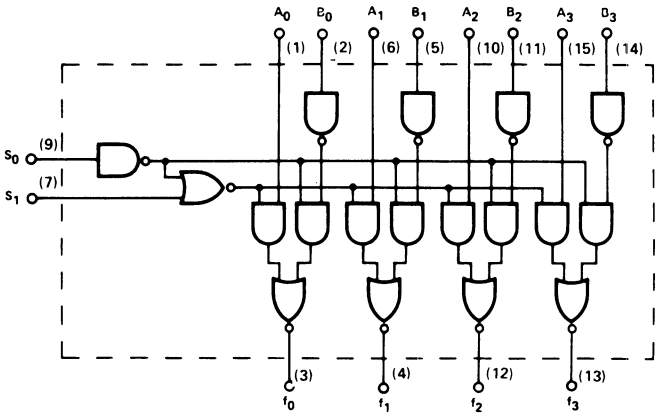
PIN CONFIGURATION



V_{CC} = PIN 16
GND = PIN 8

$$Y = \overline{(\overline{S_0} + S_1)(A_n) + S_0 B_n}$$

LOGIC DIAGRAM



TRUTH TABLE

Select Lines		Outputs
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

The 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing TTL circuit structures. The 100000108 features a bare-collector output to allow expansion with other devices.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3); B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform Addition/Subtraction. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

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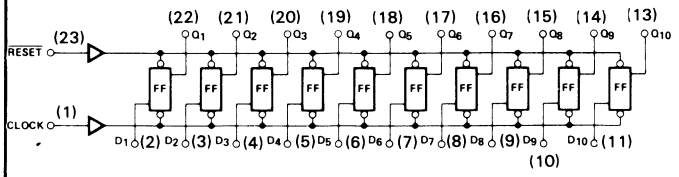
100000109

Buffer Register

LOGIC DIAGRAM



TRUTH TABLE

10-Bit Buffer Register No. 100000109

D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

Notes:

$\overline{RESET} = 0 \Rightarrow Q = 0$ (overrides clock).
n is time prior to clock.
n+1 is time following clock.

V_{CC} = Pin 24
Gnd = Pin 12

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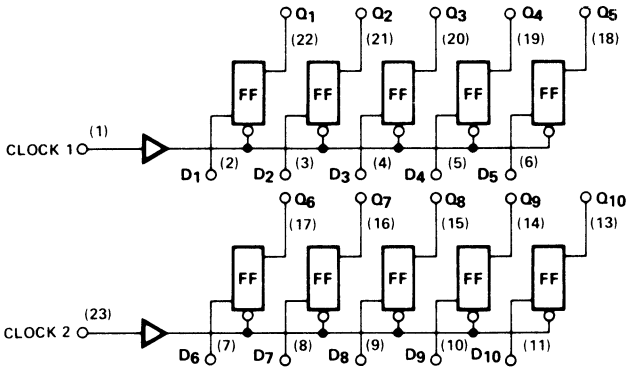
100000111

Buffer Registers

LOGIC DIAGRAM



TRUTH TABLE

D_n	Q_{n+1}
1	1
0	0

Notes:

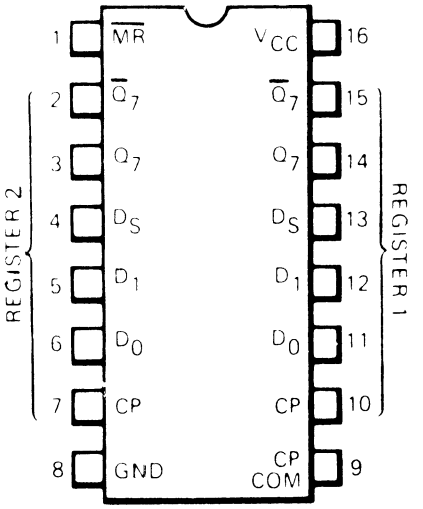
n is time prior to clock.
n+1 is time following clock.

V_{CC} = Pin 24
Gnd = Pin 12

100000112

Dual 8-Bit Shift Register

PIN CONFIGURATION



PIN NAMES

D_S . . . . . Data Select Input
D_0, D_1 . . . . Data Inputs
CP . . . . . Clock (Active HIGH) Going Edge Input
Common (Pin 9)
Separate (Pins 7 and 10)
$\overline{MR}$ . . . . . Master Reset (Active LOW) Input
Q_7 . . . . . Last Stage Output
$\overline{Q_7}$ . . . . . Complementary Output

TRUTH TABLE
Shift Selection

D_S	D_0	D_1	Q_7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = Indicates state after eight clock pulse.
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

This device is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers that will shift at greater than 20 MHz rates.

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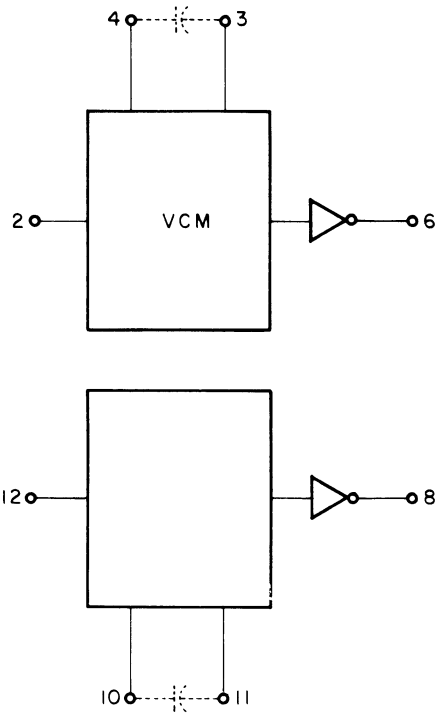
100000114

Dual Voltage Controlled Multivibrator

BLOCK DIAGRAM



Pin Designations

V_{cc}: VCM = 1, 3
Output Buffer = 14

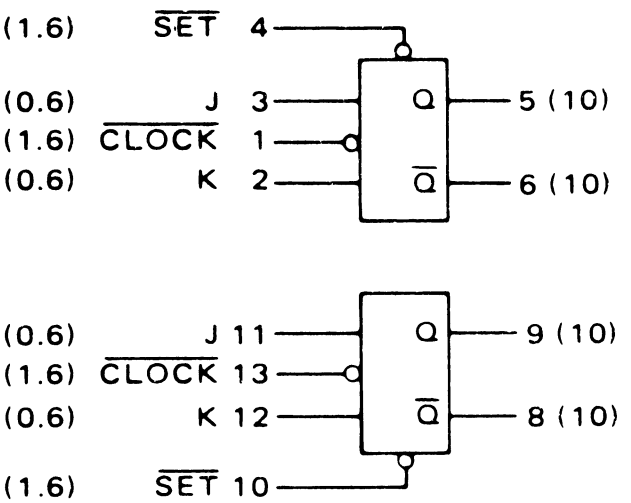
Gnd: VCM = 5, 9
Output Buffer = 7

External capacitor for frequency range determination.

100000115

Dual J-K Flip-Flop

LOGIC DIAGRAM



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

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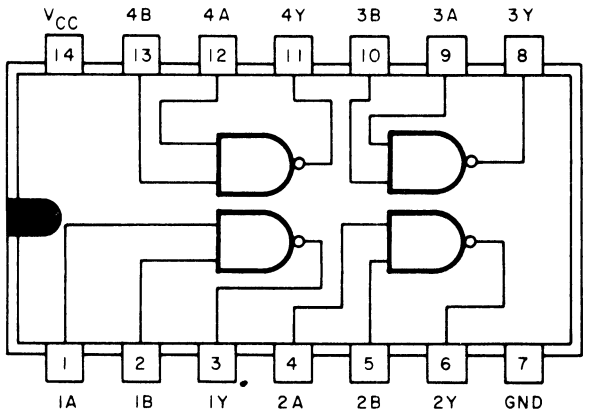
100000116

Quad 2-Input Positive-NAND Buffer

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14

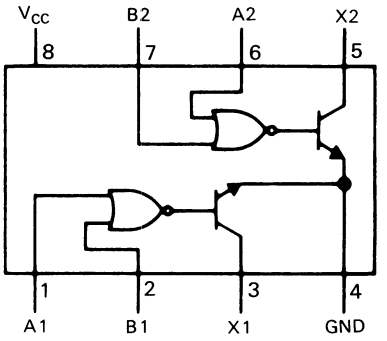
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

100000117

Dual Peripheral Driver

PIN CONFIGURATION



Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

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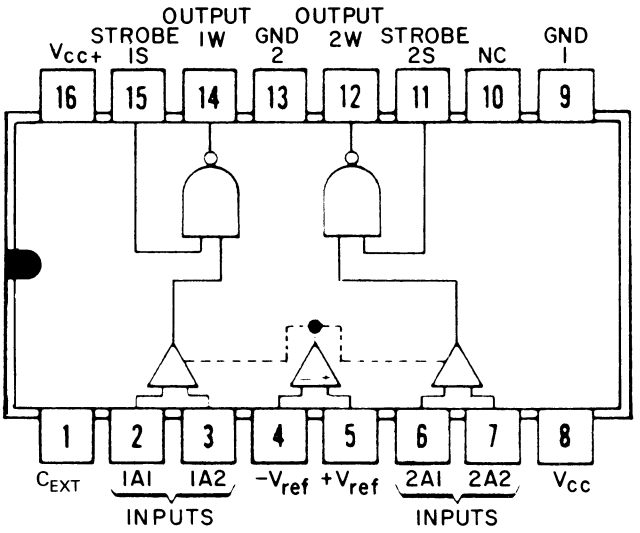
100000118

Dual Sense Amplifier

PIN CONFIGURATION



Positive logic: $W = \overline{AS}$

TRUTH TABLE

Inputs		Output**
A	S	W
H	H	L
L	X	H
X	L	H

Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geq V_{Tmax}$	$V_{ID} \leq V_{Tmin}$	Irrelevant
S	$V_I \geq V_{IHmin}$	$V_I < V_{ILmax}$	Irrelevant

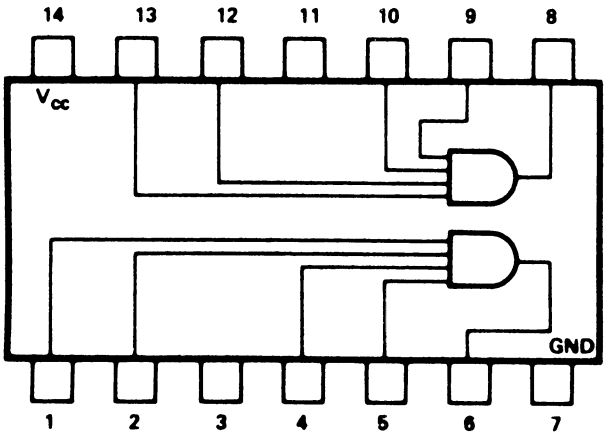
* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

**Open Collector

100000119

Dual 4-Input Positive-AND Gate

PIN CONFIGURATION



Positive logic: $Y = ABCD$

NOTE *The 100000119 is a high speed TTL device.*

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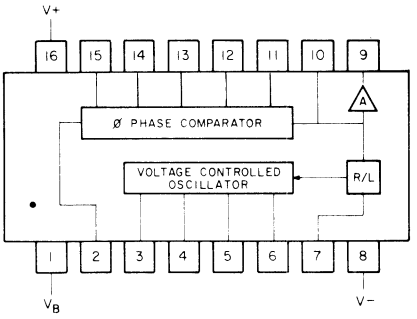
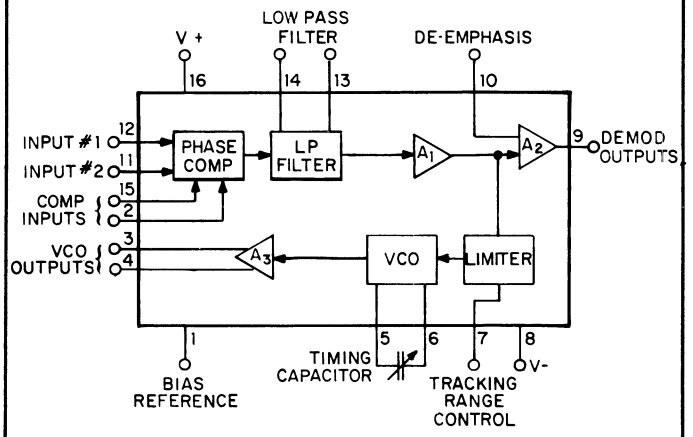
100000120

Phase Locked Loop

PIN CONFIGURATION



BLOCK DIAGRAM



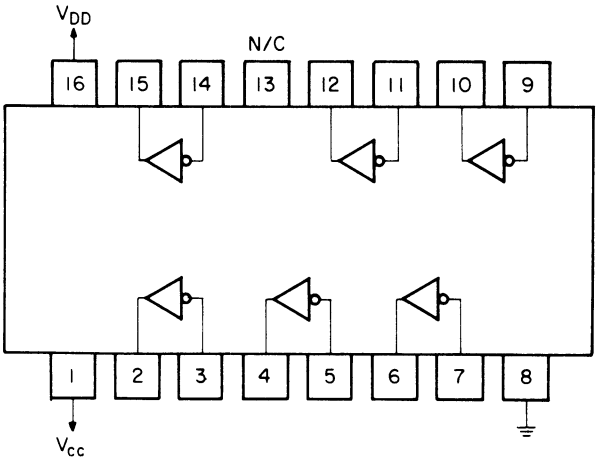
The 100000120 Phase Locked Loop is a monolithic signal conditioner and demodulator system, comprising a VCO, phase comparator, amplifier and low pass filter.

The center frequency of the Phase Locked Loop is determined by the free running frequency of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by two capacitors and two resistors at the phase comparator output. This Phase Locked Loop has two sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits.

100000121

CMOS Hex Inverter

PIN CONFIGURATION



$Y = \bar{A}$

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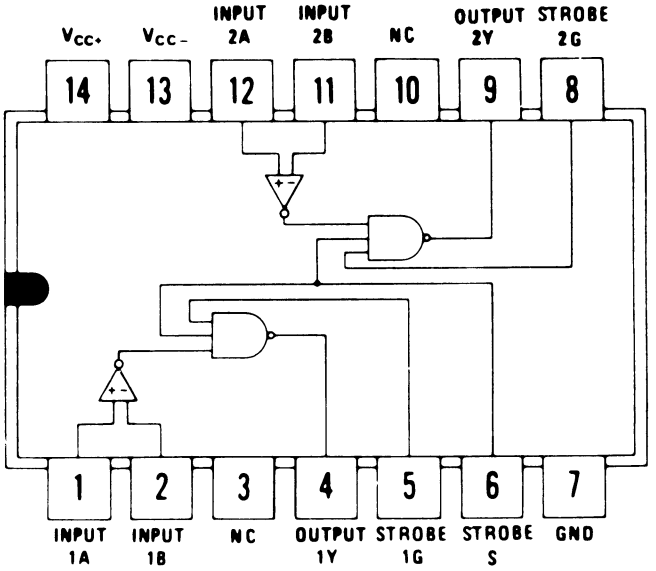
100000122

Dual Line Receiver

PIN CONFIGURATION



$Y = \overline{(AB)\ (GS)}$

Logic Diagram/Pin Designations

V_{CC+} = Pin 14

V_{CC-} = Pin 13

Gnd = Pin 7

NC = No internal connection

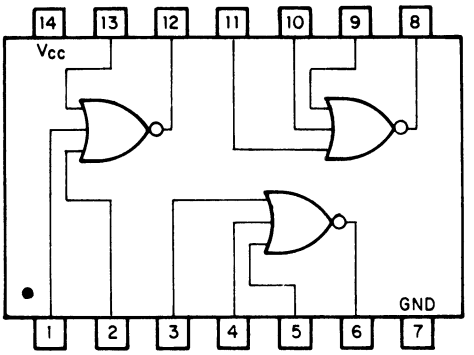
TRUTH TABLE

Differential Inputs A-B	Strobes G	Strobes S	Output Y
$V_{ID} \geq 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
	H	H	Indeterminate
$V_{ID} \leq -25mV$	L or H	L	H
	L	L or H	H
	H	H	L

100000123

Triple 3-Input NOR Gate

PIN CONFIGURATION



$Y = \overline{A + B + C}$

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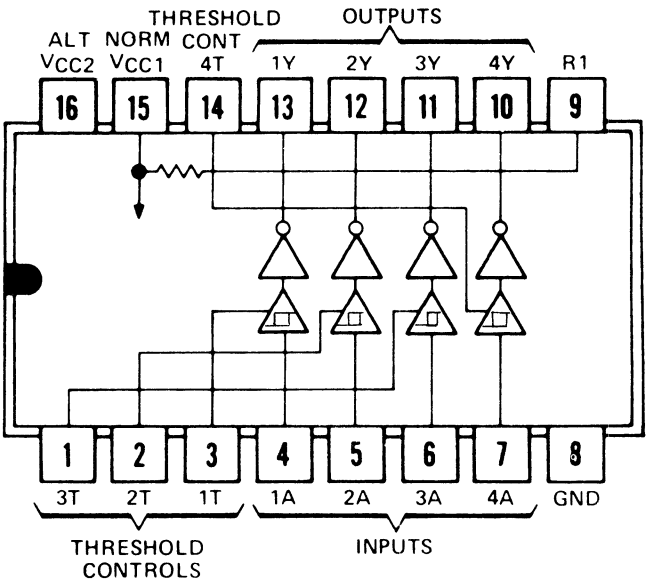
100000124

Quad Line Receiver

PIN CONFIGURATION



Logic Diagram/Pin Designations

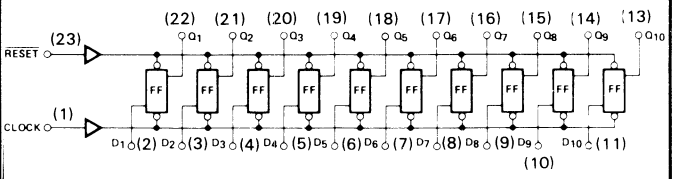
V_{CC1} = Pin 15
V_{CC2} = Pin 16
Gnd = Pin 8

Logic: $Y = \overline{A}$

100000125

Buffer Registers

LOGIC DIAGRAM



TRUTH TABLE

10-Bit Buffer Register-Inverted Inputs

D_n	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

Notes:

$\overline{RESET} = 0 \Rightarrow Q = 0$ (overrides clock).
n is time prior to clock.
n+1 is time following clock.

V_{CC} = Pin 24
Gnd = Pin 12

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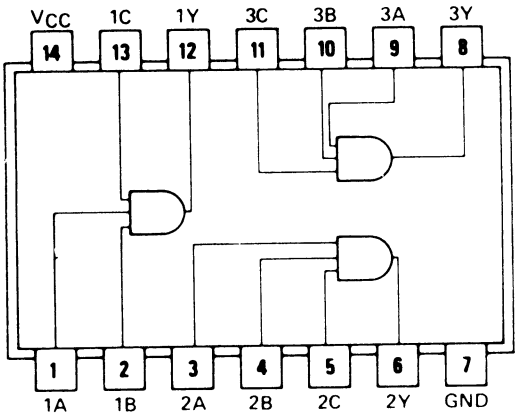
100000126

Triple 3-Input AND Gate

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

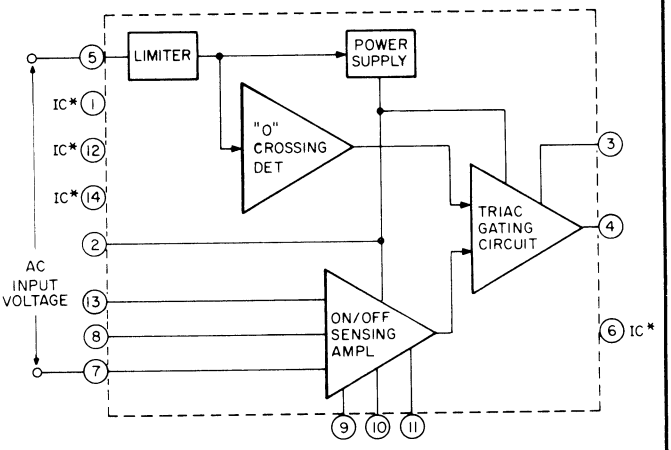
Positive logic: Y = ABC

NOTE *The 100000126 is a high speed TTL device.*

100000127

Zero Voltage Switch

BLOCK DIAGRAM



IC* = INTERNAL CONNECTION
DO NOT USE

The 100000127 zero voltage switch is a monolithic integrated circuit designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V and 277V at 50/60 and 400Hz. This switch incorporates four functional blocks:

1. Limiter-Power Supply -- permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier -- tests the condition of external sensors or command signals.
3. Zero-Crossing Detector -- synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point.
4. Triac Gating Circuit -- Provides high-current pulses to the gate of the power controlling thyristor.

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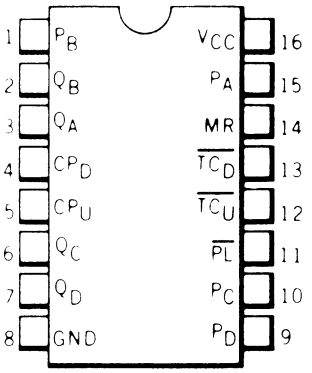
100000128

Up/Down Binary Counter

PIN CONFIGURATION



MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

All these counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous over-riding master reset.

These counters can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table.

Counting is synchronous, with the outputs changing state after the Low to High transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is High. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are Low simultaneously.)

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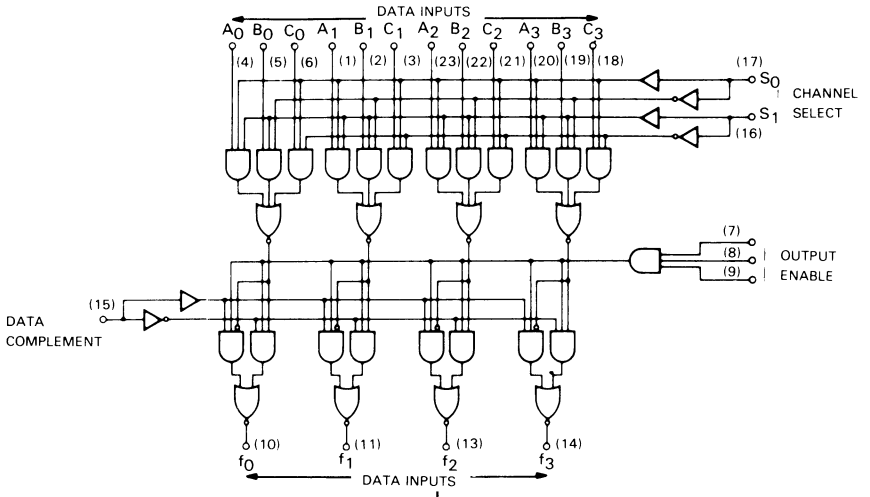
100000129

3-Input, 4-Bit Digital Multiplexer

LOGIC DIAGRAM
(Open Collector)



TRUTH TABLE

Data Input A_n	B_n	C_n	Channel Select S_0	S_1	Data Complement	Data Outputs
A_n	x	x	1	1	0	A_n
x	B_n	x	0	1	0	B_n
x	x	C_n	1	0	0	C_n
x	x	x	0	0	0	0
A_n	x	x	1	1	1	$\overline{A}_n$
x	B_n	x	0	1	1	$\overline{B}_n$
x	x	C_n	1	0	1	$\overline{C}_n$
x	x	x	0	0	1	1

X = Either state.

V_{CC} = Pin 24
Gnd = Pin 12

The 3-input, 4-bit multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

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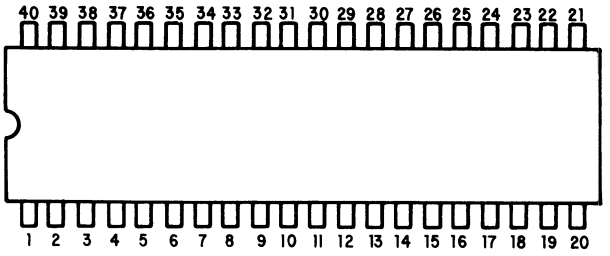
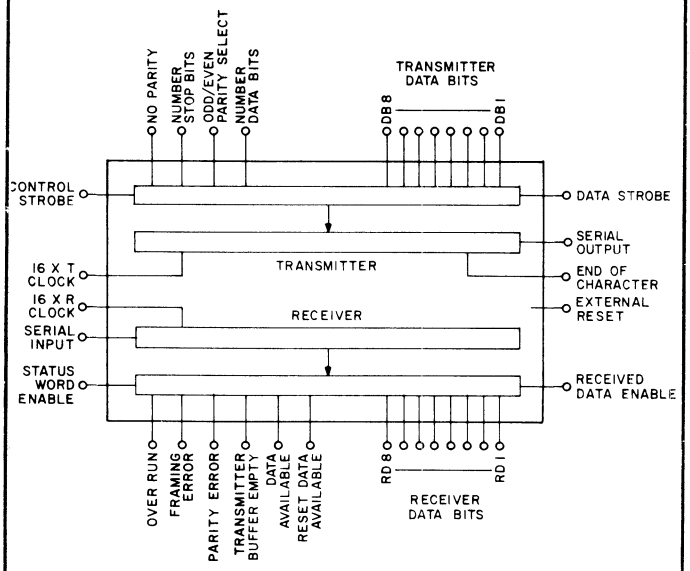
100000130

Asynchronous Receiver/Transmitter

PIN CONFIGURATION



BLOCK DIAGRAM



The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{gr}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.

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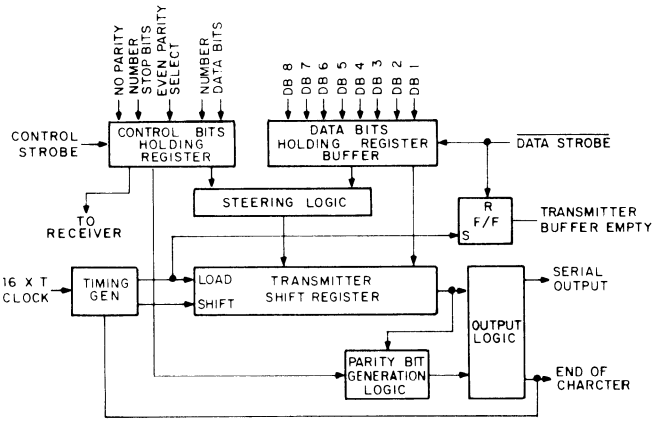
100000130 (Continued)

DESCRIPTION OF PIN FUNCTIONS (CONTINUED)

Pin No.	Name	Symbol	Function
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character. NB1 NB2 Bits Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER BLOCK DIAGRAM



Transmitter Operation

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously mentioned.

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100000130 (Continued)

Receiver Operation

Initializing

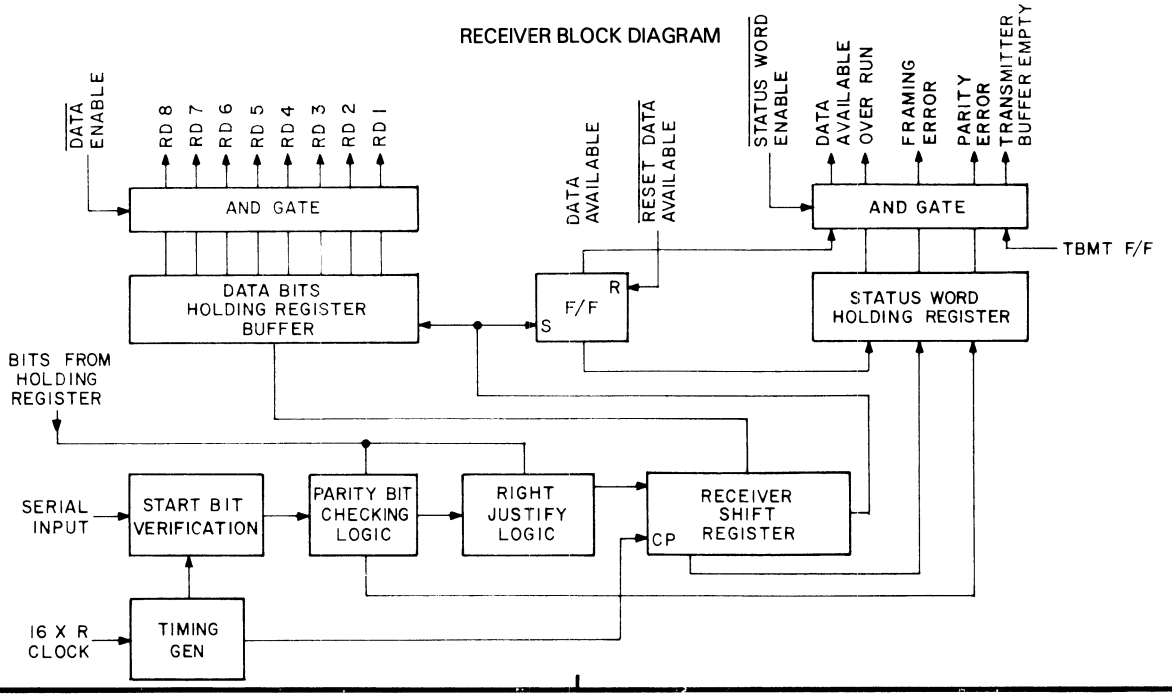
Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16X clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditioning set to a logic "0".

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

RECEIVER BLOCK DIAGRAM



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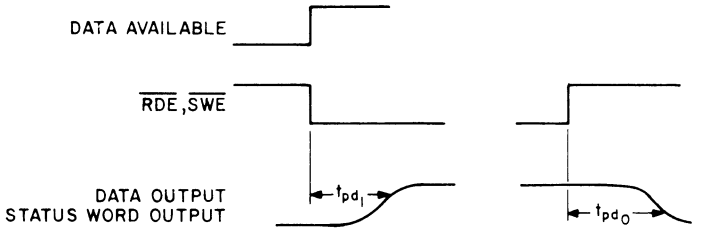
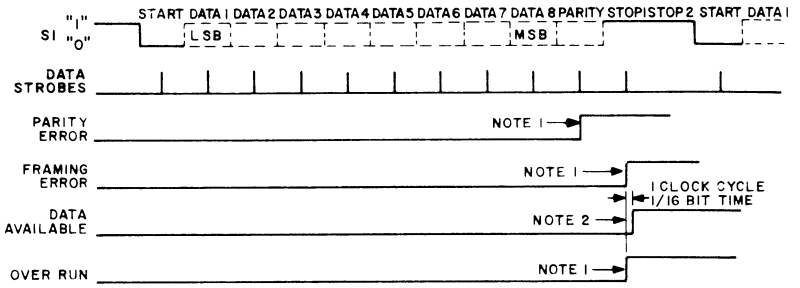
100000130 (Continued)

RECEIVER PROPAGATION DELAY TIMING DIAGRAM

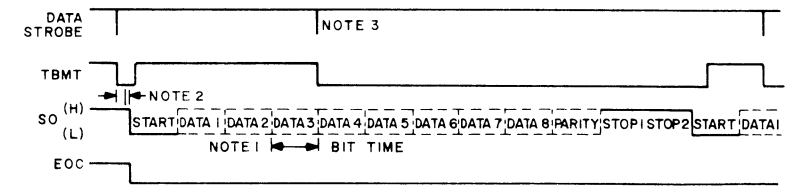


RECEIVER TIMING DIAGRAM



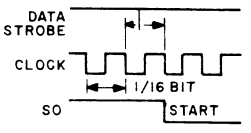
NOTES:
1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGH JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

TRANSMITTER TIMING DIAGRAM



NOTE: TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.
1: BIT TIME = 16 CLOCK CYCLES.
2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.
3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1.

DETAIL:



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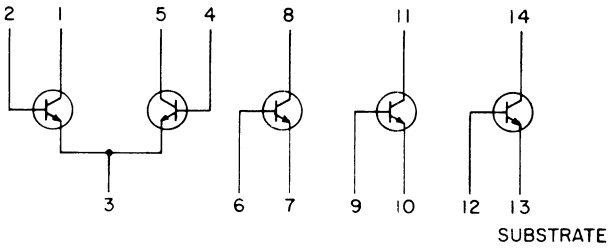
100000131

General Purpose Transistor Array

LOGIC DIAGRAM

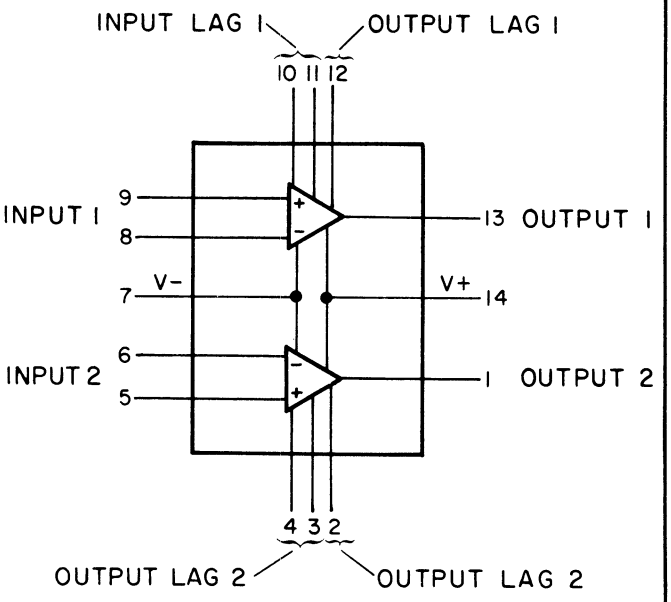


NOTE: *The collector of each transistor is isolated from the substrate by an integral diode. The substrate terminal (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

100000132

Dual Stereo Preamplifier

PIN CONFIGURATION



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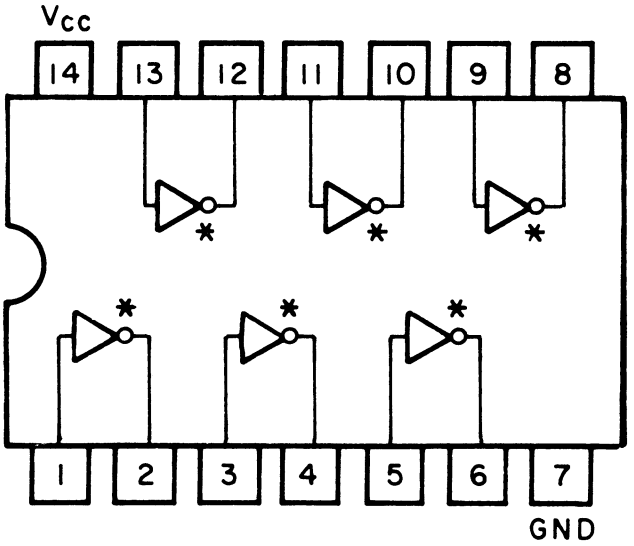
100000133

Hex Inverter Buffer/Driver With High Voltage Outputs

PIN CONFIGURATION



DIP (TOP VIEW)

*Open collector

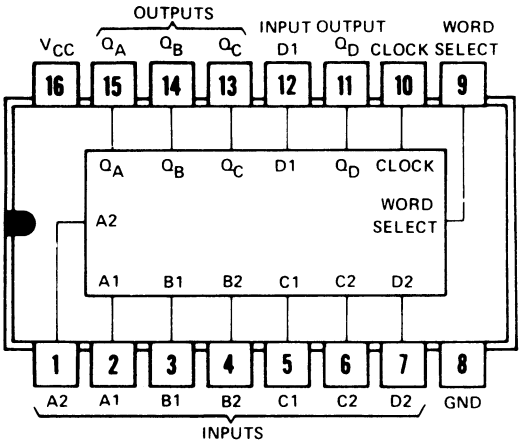
V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: $Y = \overline{A}$

100000134

4-Bit Data Selector/Storage Register

PIN CONFIGURATION



V_{CC} = Pin 16
Gnd = Pin 8

Positive logic: word select low for word 1, word select high for word 2.

This monolithic data selector/storage register is composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

NOTE *The 100000134 is a low power TTL device.*

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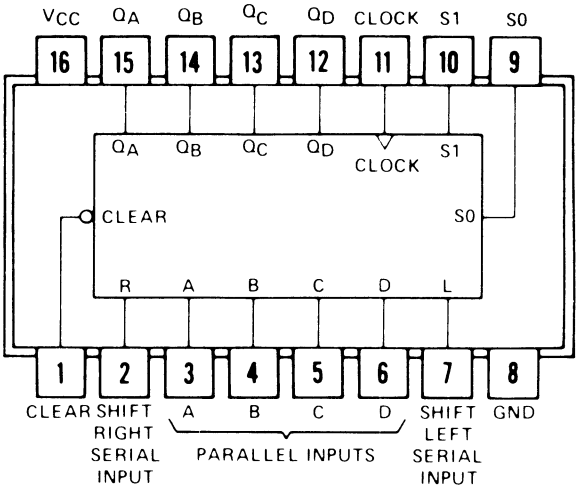
100000135

4-Bit Bidirectional Universal Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

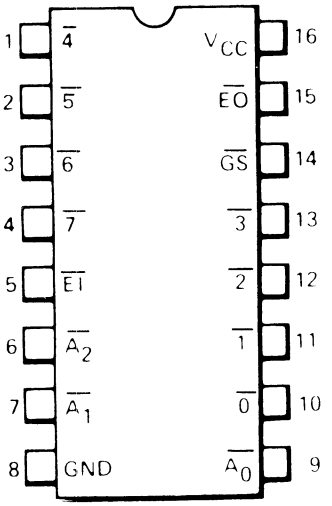
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

100000136

8-Input Priority Encoder

PIN CONFIGURATION



V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

$\overline{0}$..... Priority (Active LOW) Input
$\overline{1}$ to $\overline{7}$..... Priority (Active LOW) Inputs
$\overline{EI}$..... Enable (Active LOW) Input
$\overline{EO}$ ..... Enable (Active LOW) Output
$\overline{GS}$ ..... Group Select (Active LOW) Output
$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$. Address (Active LOW) Outputs

TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

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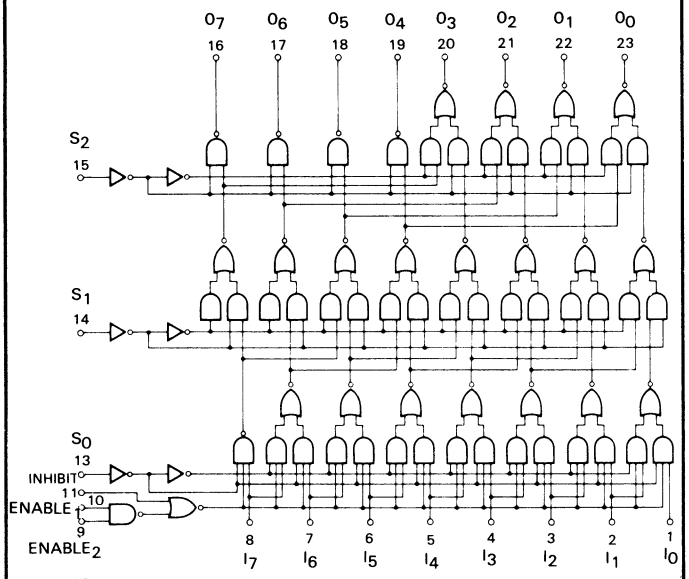
100000137

8-Bit Position Scaler

LOGIC DIAGRAM



NOTE: All inputs have diode clamps.

TRUTH TABLE

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	$\bar{I}_0$	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$
0	1	1	0	0	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1
0	1	0	1	0	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1
0	1	1	1	0	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1
0	1	0	0	1	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1
0	1	1	0	1	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1
0	1	0	1	1	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\bar{I}_7$	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

X indicates either logic "1" or logic "0" may be present.

V_{CC} = Pin 24

Gnd = Pin 12

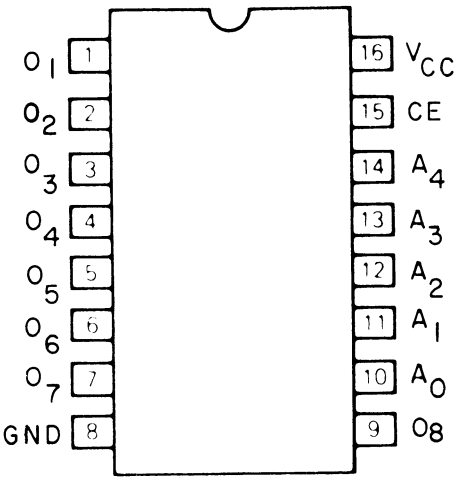
The 8-bit position scaler is an MSI array of approximately 70 gate complexity. The primary function of this device is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

100000140 through 100000142

256-Bit Bipolar ROM

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

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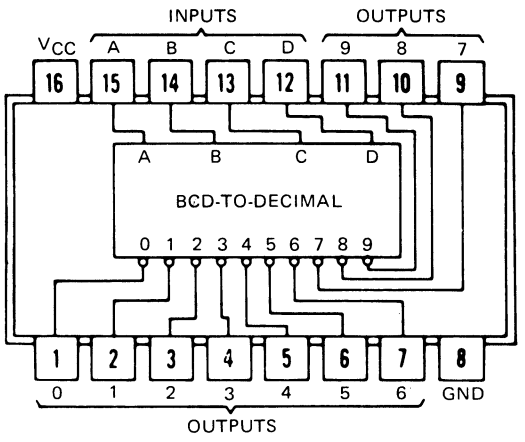
100000143

BCD-To-Decimal Decoder/Driver

PIN CONFIGURATION



FUNCTION TABLE

No.	Inputs D	C	B	A	Outputs 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

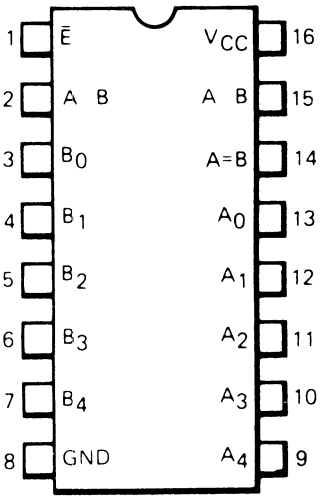
H = high level (off); L = low level (on).

This monolithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions.

100000144

5-Bit Comparator

PIN CONFIGURATION



Pin Names

$\overline{E}$ ..... Enable (Active LOW) Input

A_0, A_1, A_2, A_3, A_4 .... Word A Parallel Inputs

B_0, B_1, B_2, B_3, B_4 .... Word B Parallel Inputs

A < B ..... A Less Than B Output

A > B ..... A Greater Than B Output

A = B ..... A Equal to B Output

TRUTH TABLE

$\overline{E}$	Ay	By	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A =	Word B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B >	Word A	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

The 100000144 is a high speed expandable comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

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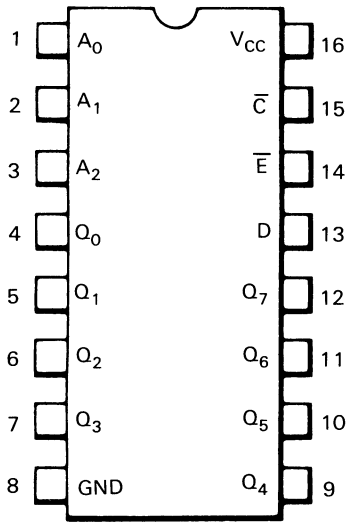
100000145

8-Bit Addressable Latch

PIN CONFIGURATION



Pin Names

A0, A1, A2..... Address Inputs
D..... Data Input
$\overline{E}$..... Enable (Active LOW) Input
$\overline{C}$..... Clear (Active LOW) Input
Q0 to Q7..... Parallel Latch Outputs

TRUTH TABLE

Present Ouput States

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Mode
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						Latch
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1} L		
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1} H		

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

The 100000145 is a high speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches as well as an active level LOW enable.

This latch has four modes of operation, which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating this device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

MODE SELECTION

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

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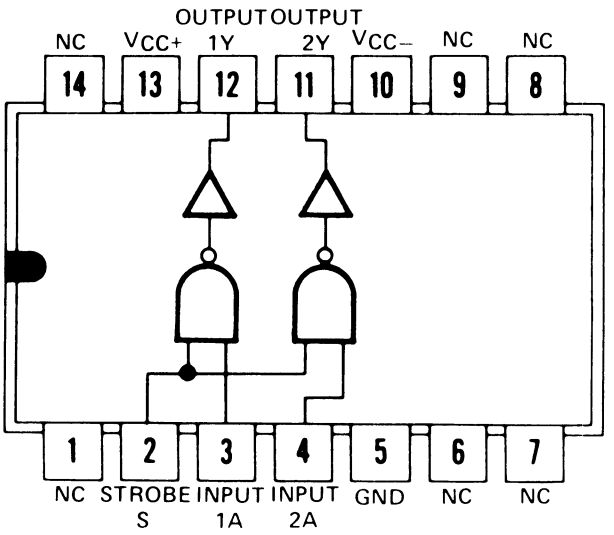
100000146

Dual Line Driver

PIN CONFIGURATION



V_{CC+} = Pin 13
V_{CC-} = Pin 10
Gnd = Pin 5
NC = No Internal Connection

Positive logic: $Y = \overline{AS}$

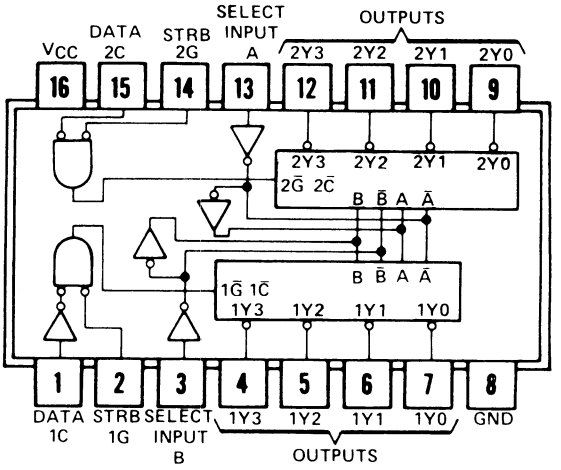
This device is a monolithic dual line driver which satisfies the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C.

A rate of 20, 000 bits per second can be transmitted with a full 2500pF load.

100000147

Dual 2-Line-To-4-Line Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs			
Select		Strobe	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

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100000147 (Continued)

FUNCTION TABLE

Inputs		Outputs							
Select	Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C* B A	G**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X X X	H	H	H	H	H	H	H	H	H
L L L	L	L	H	H	H	H	H	H	H
L L H	L	H	L	H	H	H	H	H	H
L H L	L	H	H	L	H	H	H	H	H
L H H	L	H	H	H	L	H	H	H	H
H L L	L	H	H	H	H	L	H	H	H
H L H	L	H	H	H	H	H	L	H	H
H H L	L	H	H	H	H	H	H	L	H
H H H	L	H	H	H	H	H	H	H	L

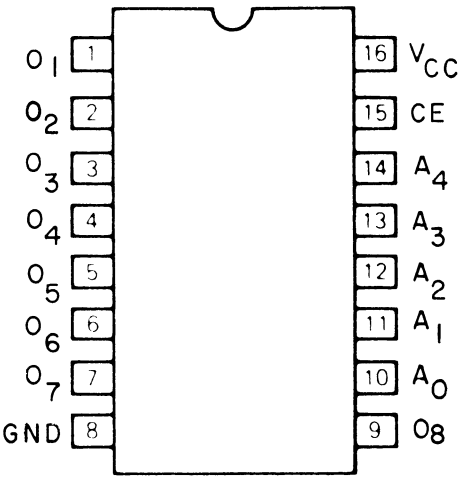
Notes: *C = inputs 1C and 2C connected together.
**G = inputs 1G and 2G connected together.
H = high level, L = low level,
X = irrelevant.

The 100000147 monolithic TTL circuit features dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided to minimize transmission-line effects and simplify system design.

100000148 and 100000149

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

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100000150

High Speed 64 X 7 X 5 Character Generator

PIN DESIGNATIONS

1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

CHARACTER FORMAT

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

CHARACTER ADDRESS

	A_4	A_5	A_6	A_7	A_8	A_9
ASCII Character	1	1	0	0	1	0

The 100000150 is a high speed 2560-bit static ROM. The 64x7x5 character organization is formed on a 64x8x5 field.

The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and tri-state outputs.

FUNCTION TABLE

CE	OUTPUT
0	DATA
1	OPEN

100000151

Hex 40-Bit Static Shift Register

PIN DESIGNATIONS

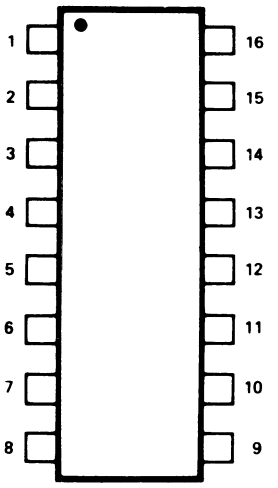
1.	IN_4	16.	VCC
2.	IN_5	15.	IN_3
3.	IN_6	14.	IN_2
4.	Recirculate	13.	IN_1
5.	V_{GG}	12.	OUT_1
6.	Clock	11.	OUT_2
7.	OUT_6	10.	OUT_3
8.	OUT_5	9.	OUT_4

FUNCTION TABLE

Recirculate	Input	Function
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

The Hex 40-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for interfacing capability.

PIN CONFIGURATION



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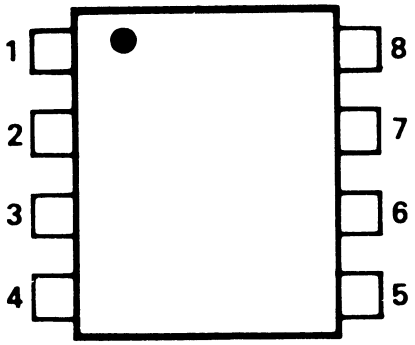
100000152

1024 x 1-Bit Recirculating Dynamic Shift Register

PIN CONFIGURATION



PIN DESIGNATIONS

1. 0_2 Input clock
2. Output
3. Read
4. V_{DD}
8. V_{CC}
7. 0_1 Output clock
6. Input
5. Write

TRUTH TABLE

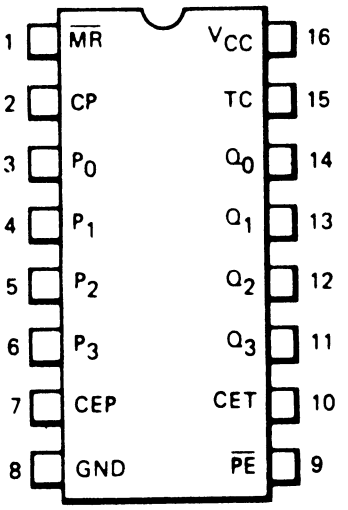
Write	Read	Function
0	0	Recirculate, Output is "0"
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is "0"
1	1	Read Mode, Output is Data

The 1024 bit recirculating dynamic shift register consists of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

100000153

BCD Decade Counter

PIN CONFIGURATION



PIN NAMES

$\overline{PE}$ ..... Parallel Enable (Active LOW) Input

P_0, P_1, P_2, P_3 .. Parallel Inputs

CEP ..... Count Enable Parallel Input

CET ..... Count Enable Trickle Input

CP ..... Clock (Active HIGH Going Edge) Input

$\overline{MR}$ ..... Master Reset (Active LOW) Input

Q_0, Q_1, Q_2, Q_3 .. Parallel Outputs

TC ..... Terminal Count Outputs

MODE SELECTION

$\overline{PE}$	CEP	CET	Mode
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

$TC = CET \cdot Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$

Preset = $\overline{PE}$ · CP + (rising clock edge)

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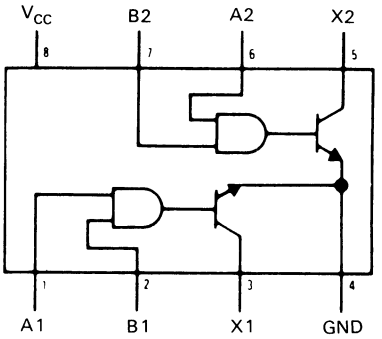
100000154

Dual Peripheral Driver

PIN CONFIGURATION



FUNCTION TABLE

Positive logic: $X = \overline{AB}$

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

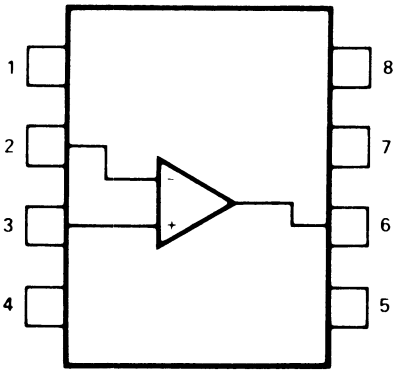
*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000156

High Performance Operational Amplifier

PIN CONFIGURATION



PIN DESIGNATIONS

1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

This device is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and temperature stability.

The device is short-circuit protected and allows for nulling of offset voltage.

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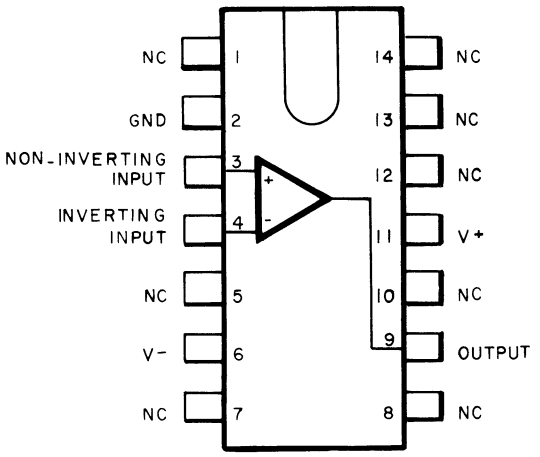
100000157

High Speed Differential Comparator

PIN CONFIGURATION

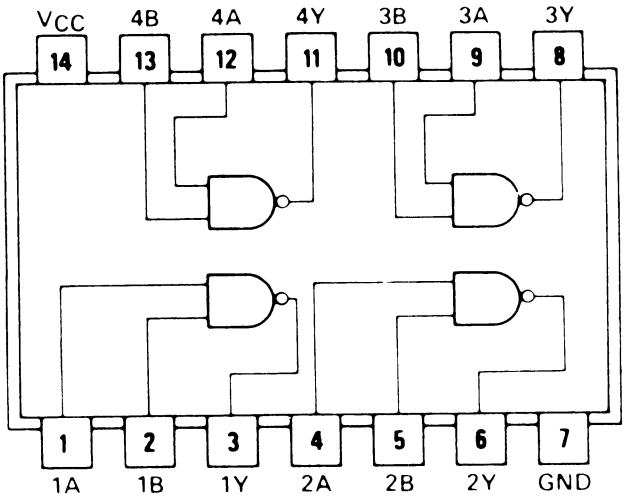


The 100000157 is a differential voltage comparator intended for applications requiring high accuracy fast response times. Constructed on a single silicon chip, the device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier, or a high-noise immunity line receiver.

100000158

Quad 2-Input Positive-NAND Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

NOTE *The 100000158 is a Schottky device.*

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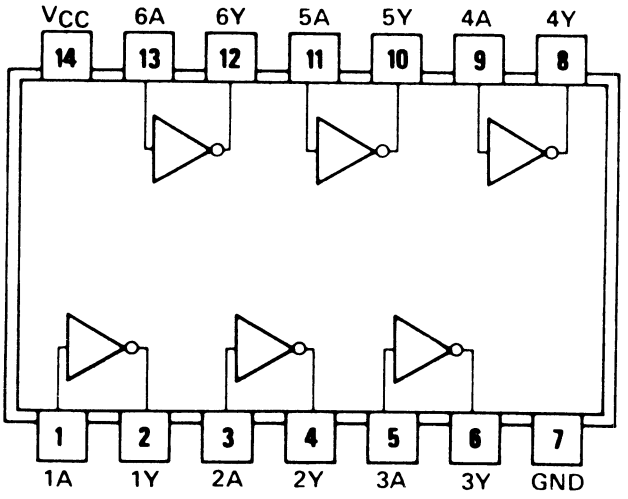
100000159

Hex Inverter

PIN CONFIGURATION



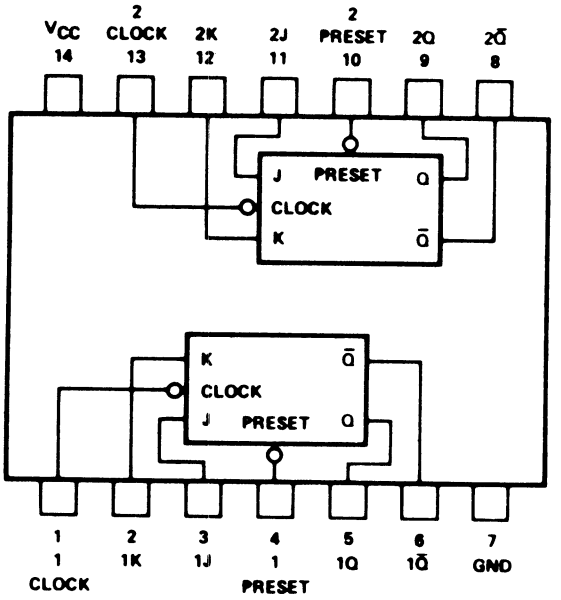
Positive logic: $Y = \overline{A}$

The 100000159 is a Schottky device.

100000160

Dual J-K Edge-Triggered Flip-Flop

PIN CONFIGURATION



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes:

t_n = bit time before clock pulse.

t_{n+1} = bit time after clock pulse.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bi-stable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

NOTE *The 100000160 is a Schottky device.*

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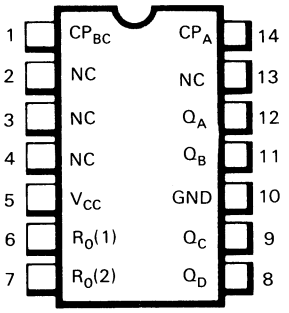
100000161

Divide-By-12 Counter (Divide-By-2 and Divide-By-6)

PIN CONFIGURATION



PIN NAMES

R_0 ..... Reset-Zero Inputs
$\overline{CP}_A$ ..... Clock Input
$\overline{CP}_{BC}$ ..... Clock Input
Q_A, Q_B, Q_C, Q_D .... Count Outputs

TRUTH TABLE

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

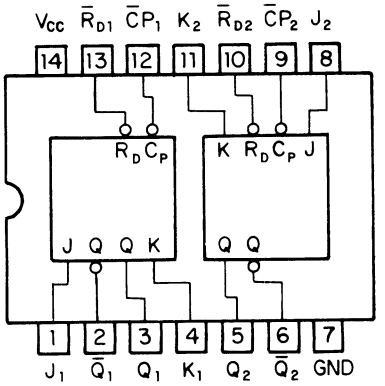
Notes:

1. Output Q_A connected to input $\overline{CP}_{BC}$.
2. To reset all outputs to Low level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at High level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a Low level to count.

100000162

Dual J-K Master/Slave Flip-Flop with Separate Clears and Clocks

PIN CONFIGURATION



LOW input to clear sets Q to LOW level. Clear is independent of clock.

TRUTH TABLE

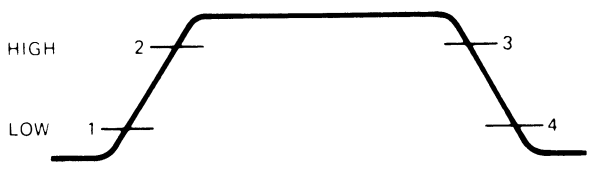
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.

These Dual JK Master/Slave flip-flops have a separate clear and a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; and 4) transfer information from master to slave.

CLOCK WAVEFORM



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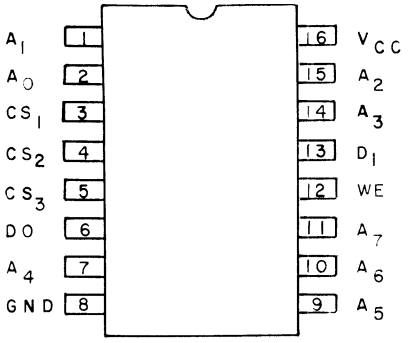
100000164

256 x 1-Bit Bipolar RAM

PIN CONFIGURATION



FUNCTION TABLE

Chip Selects	Write Enable	Operation	Output
All "0"	"0"	Write	Logical "1" State
All "0"	"1"	Read	Complement of data written in memory
One or More "1"	X	Hold	Logical "1" State

The 100000164 integrated circuit is a high speed, fully decoded, static bipolar 256-bit random access memory in a 256 x 1 organization. This device provides uncommitted collector output and three chip selects.

Operation

Read

The memory is addressed through the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by placing all chip selects (CS) to logic "0". If any or all CS inputs are logic "1", then the device will be disabled. If the write enable (WE) is at logic "1" the stored bit is read out of DO.

Write

The memory is addressed through the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by placing all the CS inputs to logic "0". If the WE input is at logic "0", the data on terminal DI is written into the addressed word.

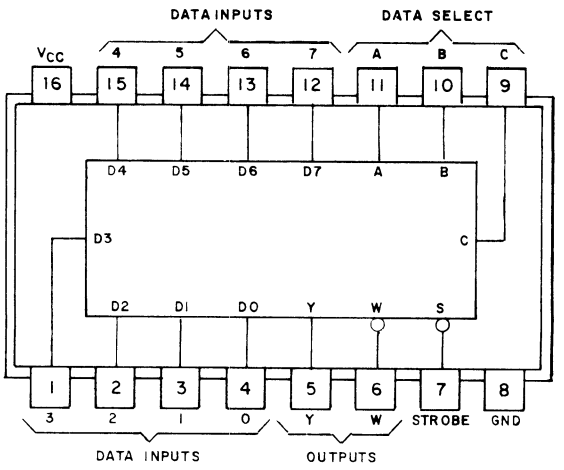
When WE returns to logic "1", the information that was written in is now read out; however, each word read out is the complement of what was written in.

NOTE *The 100000164 is a low power Schottky device.*

100000165

Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off).
D0, D1 ....D7 = the level of the respective D input.

The device has tri-state output.

NOTE *The 100000165 is a Schottky device.*

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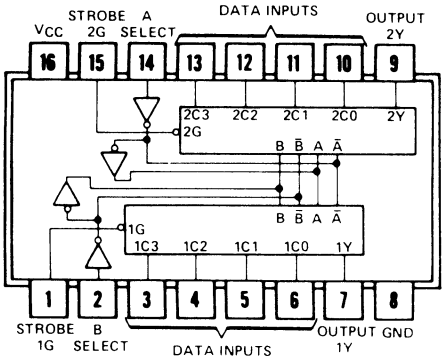
100000166

Dual 4-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select Inputs A and B are common to both sections.

H = high level; L = low level; X = irrelevant.

This monolithic, data selector-multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates.

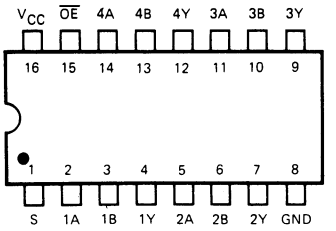
Separate strobe inputs are provided for each of the two four-line sections.

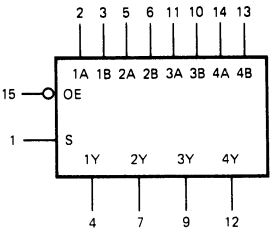
NOTE *The 100000166 is a Schottky device.*

100000167

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



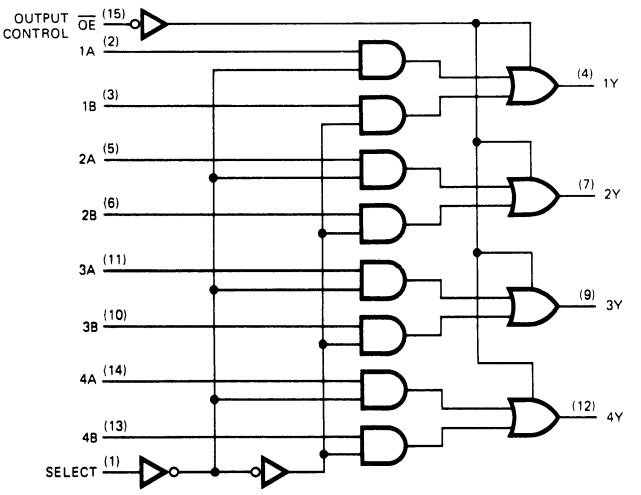


INPUTS				OUTPUTS
Output Control	Select	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

LOGIC DIAGRAM



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100000167 (cont.)

Quad 2-Line-To-1-Line Data Selector/Multiplexor

The 2-line to 1-line data multiplexor has tri-state outputs which interface directly with bus organized systems. With the output control ($\overline{OE}$) high, the four outputs of the data selector are in the high impedance state. With output control low, the selected four bits (A or B inputs) are bussed onto the four data lines.

To keep the two outputs from trying to drive the common bus to opposite logic levels, the output enabling circuitry is designed so that the output disable times are shorter than the output enable times.

The device is TTL compatible and inverting. The typical propagation delay time from data input to output average 4 ns.

NOTE: *This is a Schottky device.*

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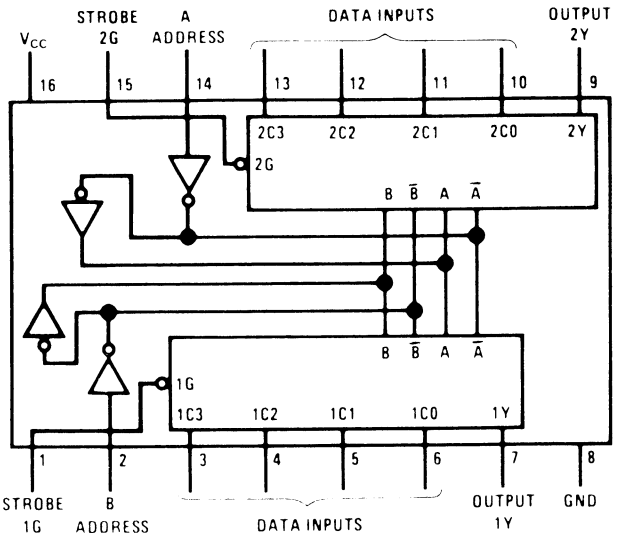
100000168

Dual 4-Line-To-1-Line Multiplexer

PIN CONFIGURATION



TRUTH TABLE

Address Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	Hi-Z
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

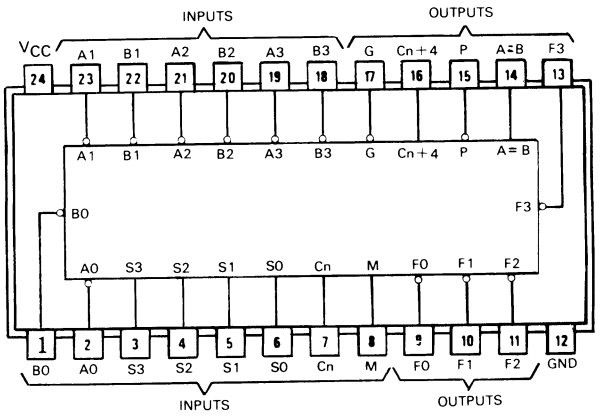
X = Don't care.

This device acts as a double-pole four-throw switch. One data line is selected from each of two four-line inputs. Two select lines determine which of the four inputs is chosen; however, the same input of both four-line selections will be selected. The logic allows outputs of the device to be tied to outputs of similar devices and connected to a common bus-line.

100000169

Arithmetic Logic Unit/Function Generator

PIN CONFIGURATION



PIN DESIGNATIONS

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

NOTE *The 100000169 is a Schottky device. The A=B output is an open collector.*

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100000169 (Continued)

These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

Figure 1

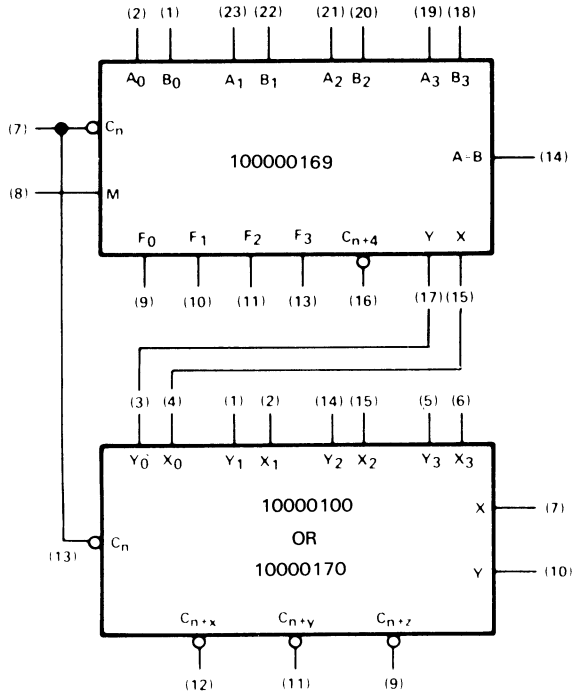

Figure 2

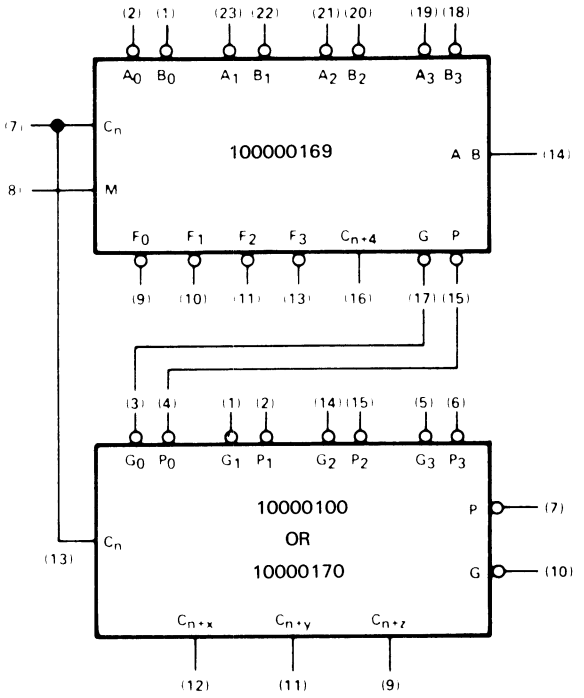

Table 1

Selection S3 S2 S1 S0	M=H Logic Functions	Active-High Data M=L: Arithmetic Operations	
		C_n=H (no carry)	C_n=L (with carry)
L L L L	F = A	F = A	F = A Plus 1
L L L H	F = A + B	F = A + B	F = (A + B) Plus 1
L L H L	F = AB	F = A + B	F = (A + B) Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	F = AB	F = A Plus AB	F = A Plus AB Plus 1
L H L H	F = B	F = (A + B) Plus AB	F = (A + B) Plus AB Plus 1
L H H L	F = A + B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = AB	F = AB Minus 1	F = AB
H L L L	F = A + B	F = A Plus AB	F = A Plus AB Plus 1
H L L H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = (A + B) Plus AB	F = (A + B) Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A	F = A Plus A Plus 1
H H L H	F = A + B	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

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100000169
(Continued)

Selection S3 S2 S1 S0	Functions	Active-Low Data	
		C_n = L (no carry)	C_n = H (with carry)
L L L L	F = A	F = A Minus 1	F = A
L L L H	F = AB	F = AB Minus 1	F = AB
L L H L	F = A + B	F = AB Minus 1	F = AB
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	F = A + B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
L H L H	F = B	F = AB Plus (A + B)	F = AB Plus (A + B) Plus 1
L H H L	F = A + B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A + B	F = A + B	F = (A + B) Plus 1
H L L L	F = AB	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = AB Plus (A + B)	F = AB Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = AB	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	F = AB Plus A	F = AB Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	$A \leqslant B$	$A \geqslant B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geqslant B$	$A \leqslant B$

These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

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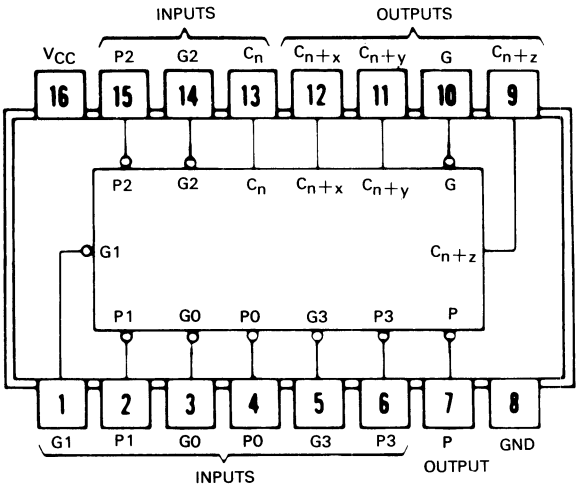
100000170

Look-Ahead Carry Generator

PIN CONFIGURATION



Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
Gnd	8	Ground

Positive Logic:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$

$$C_{n+y} = \overline{G}_1 + \overline{P}_1\overline{G}_0 + \overline{P}_1\overline{P}_0 C_n$$

$$C_{n+z} = \overline{G}_2 + \overline{P}_2\overline{G}_1 + \overline{P}_2\overline{P}_1\overline{G}_0 + \overline{P}_2\overline{P}_1\overline{P}_0 C_n$$

$$\overline{G} = \overline{G}_3(\overline{P}_3+\overline{G}_2)(\overline{P}_3+\overline{P}_2+\overline{G}_1)(\overline{P}_3+\overline{P}_2+\overline{P}_1+\overline{G}_0)$$

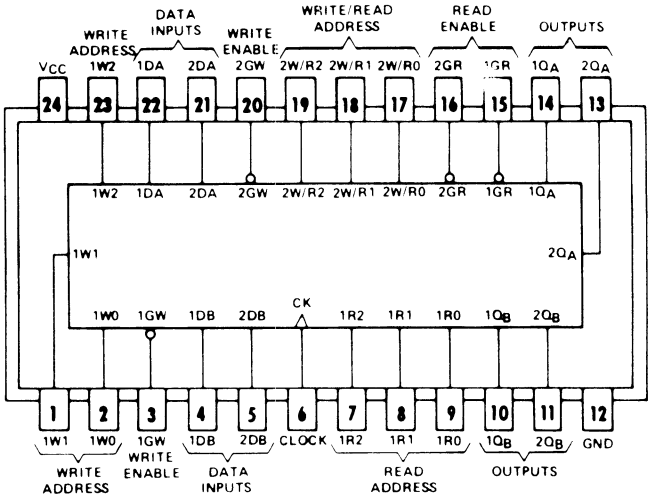
$$\overline{P} = \overline{P}_3\overline{P}_2\overline{P}_1\overline{P}_0$$

NOTE *The 100000170 is a Schottky device.*

100000171

16-Bit Multiple-Port Register File with 3-State Outputs

PIN CONFIGURATION



The 100000171 is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits.
2) Reading from two bits.
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

Functions of the inputs and outputs are as shown in the following table:

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100000171
(Continued)

Function	Section 1	Section 2	Description
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA $\neq$ 2DA and/or 1DB $\neq$ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

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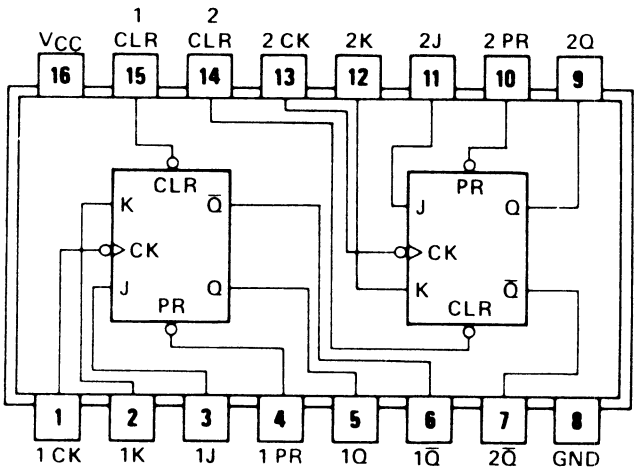
100000172

Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes:

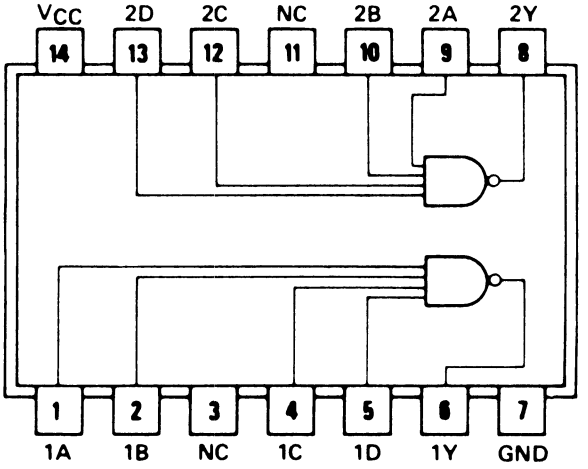
H = high level (steady state).
L = low level (steady state).
X = irrelevant.
↓ = transition from high to low level.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000172 is a Schottky device.*

100000173

Dual 4-Input Positive-NAND 50 Ohm Line Driver

PIN CONFIGURATION



Positive logic: $Y = \overline{ABCD}$

NOTE *The 100000173 is a Schottky device*

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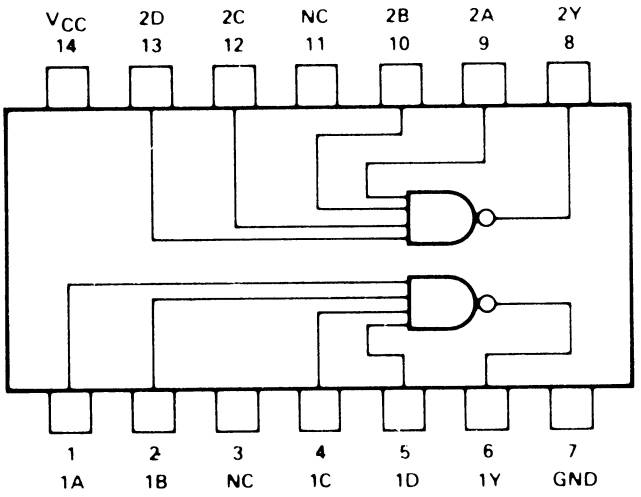
100000174

Dual 4-Input Positive-NAND Gate with Open-Collector Outputs

PIN CONFIGURATION



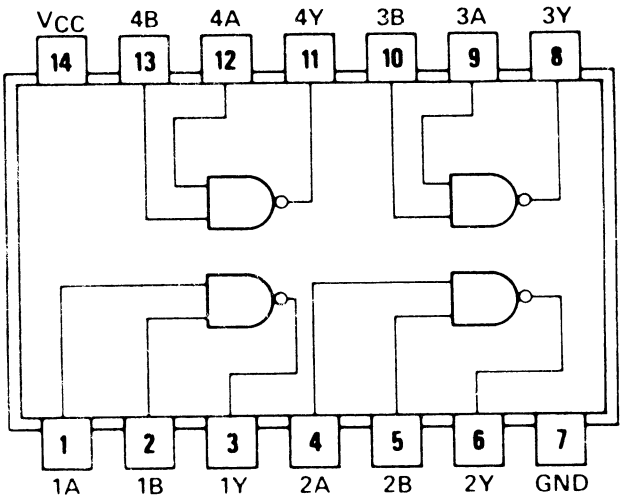
$Y = \overline{ABCD}$

NOTE *The 100000174 is a Schottky device.*

100000175

Quad 2-Input Positive-NAND Gate with Open-Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

NOTE *The 100000175 is a Schottky device.*

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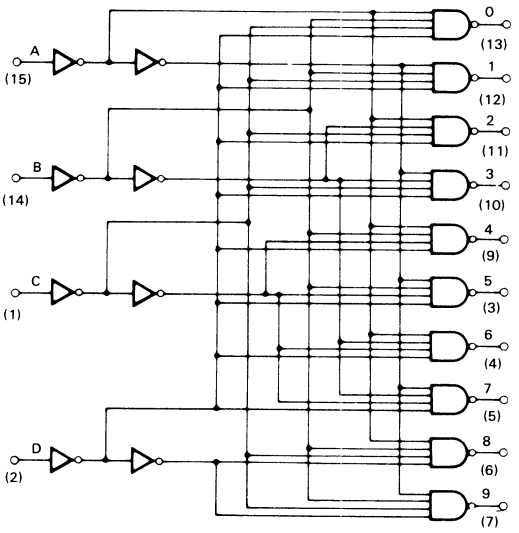
100000178

BCD-To-Decimal Decoder

LOGIC DIAGRAM



V_{CC} = Pin 16

Gnd = Pin 8

TRUTH TABLE

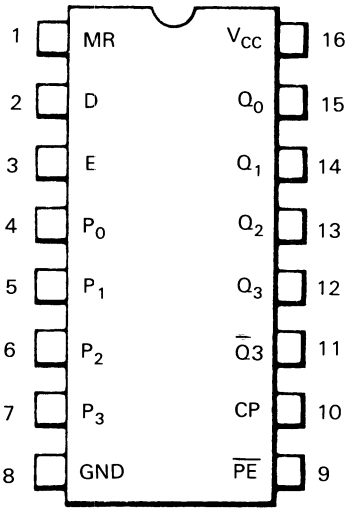
Input State				Output States									
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

The 100000178 is a Schottky device.

100000180

High Speed 4-Bit Shift Register with Enable

PIN CONFIGURATION



PIN NAMES

$\overline{E}$ ..... Active LOW Enable Input
$\overline{PE}$ ..... Active LOW Parallel Enable Input
P_0, P_1, P_2, P_3.. Parallel Data Inputs
$\overline{CP}$ ..... Clock Input
$\overline{MR}$ ..... Active LOW Master Reset Input
Q_0 to Q_3 ..... Parallel Outputs
$\overline{Q_3}$ ..... Last Stage Complementary Output
D..... Serial Data Input

MODE SELECTION

Mode		$\overline{MR}$	$\overline{E}$	$\overline{PE}$	P_0 P_1 P_2 P_3	D
Synchronous	Parallel Load	H	L	L	Parallel Data Entry	X
	Serial Shift	H	L	H	X X X X	Serial Data Entry
	Hold	H	H	L	X X X X	X
	Hold	H	H	H	X X X X	X
Asynchronous	Reset	L	X	X	All Outputs set LOW	

PARALLEL DATA ENTRY

P_0, P_1, P_2 or P_3 Input at t_n	Q at t_{n+1}
L	L
H	H

SERIAL DATA ENTRY

D Input at t_n	Q_0 at t_{n+1}
L	L
H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
t_n = Present State
t_n+1 = State after Next Clock

NOTE *The 100000180 is a high speed TTL device.*

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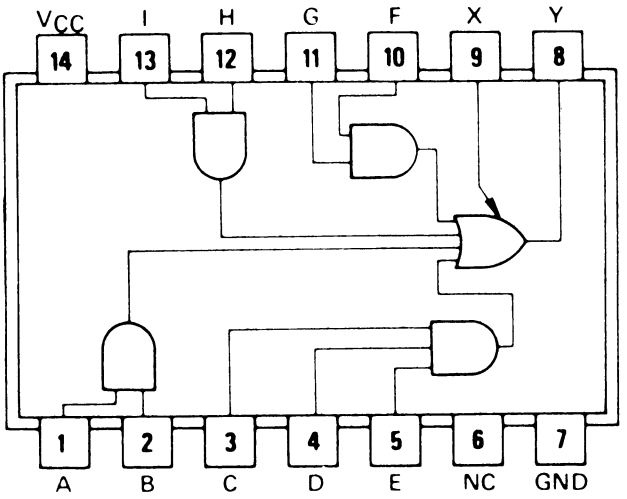
100000181

Expandable 4-Wide AND-OR Gate

PIN CONFIGURATION



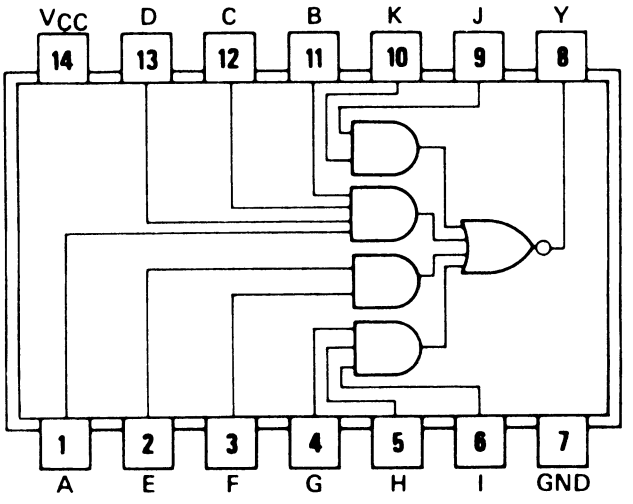
Positive logic: Y = AB+CDE+FG+HI+X

NOTE: *This is a high speed TTL device.*

100000182

4-2-3-2-Input AND-OR-INVERT Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

NOTE *The 100000182 is a Schottky device.*

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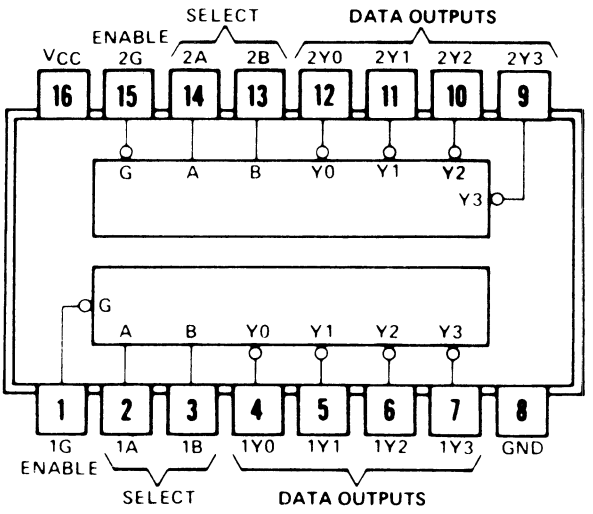
100000185

Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

(Each Decoder/Demultiplexer)

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level; L = low level; X = irrelevant

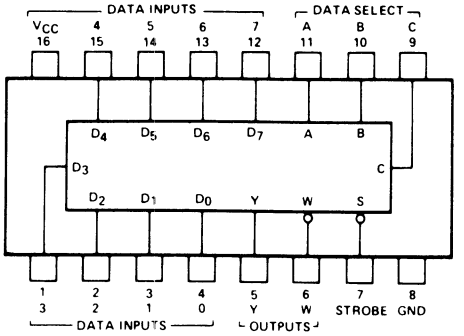
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

NOTE *The 100000185 is a Schottky device.*

100000186

8-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



TRUTH TABLE

Inputs										Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

Note: When used to indicate an input, X = irrelevant.

The 100000186 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

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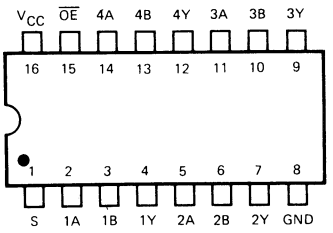
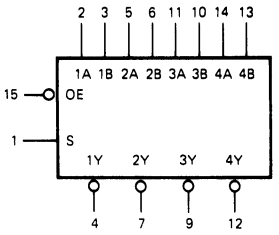
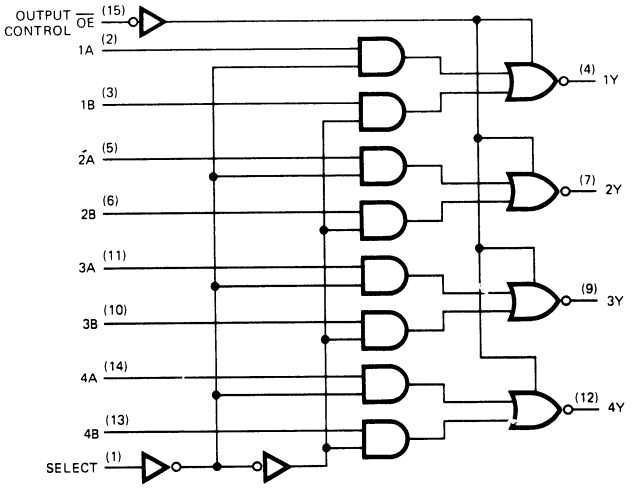
100000187

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION







The 2-line to 1-line data multiplexor has tri-state outputs which interface directly with bus organized systems. With the output control ($\overline{OE}$) high, the four outputs of the data selector are in the high impedance state. With output control low, the selected four bits (A or B inputs) are bussed onto the four data lines.

To keep the two outputs from trying to drive the common bus to opposite logic levels, the output enable circuitry is designed so that the output disable times are shorter than the output enable times.

The device is TTL compatible and non-inverting. The typical propagation delay time from data input to output averages 4.8 ns.

NOTE: *This is a Schottky device.*

INPUTS				OUTPUTS
Output Control	Select	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

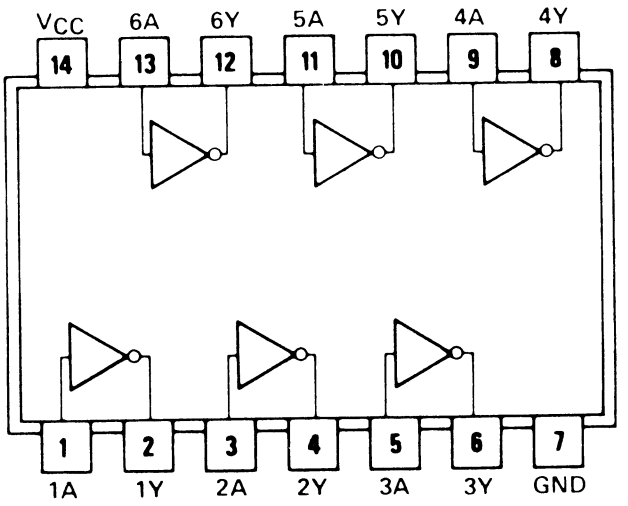
H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

100000188

Hex Inverter with Open-Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{A}$

NOTE *The 100000188 is a Schottky device.*

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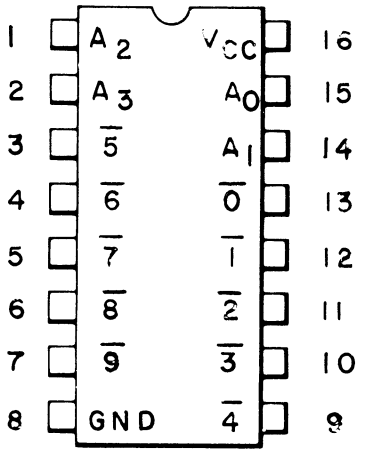
100000189

1-Of-10 Decoder with Open Collector Output

PIN CONFIGURATION



PIN NAMES

A_0, A_1, A_2, A_3 = Address Inputs
$\overline{0}$ to $\overline{9}$ = Outputs, Active LOW*

* An external pull-up resistor is needed to provide HIGH level drive capability.

TRUTH TABLE

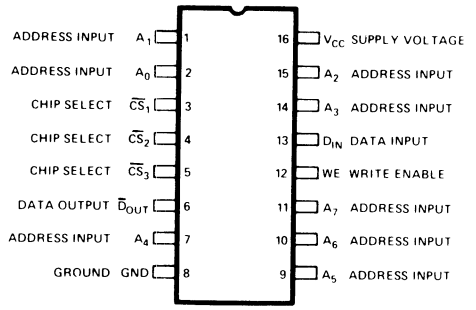
A0	A1	A2	A3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

100000190

High Speed Fully Decoded 256-Bit RAM

PIN CONFIGURATION



TRUTH TABLE

Chip Select	Write Enable	Operation	Output
All Low	Low	Write	Complement of data input
All Low	High	Read	Complement of written data
One or more High	Don't Care	Hold	High Impedance State

The 100000190 is a high speed, fully decoded, 256 bit read/write random access memory. The device features three chip-select inputs and a three-state output.

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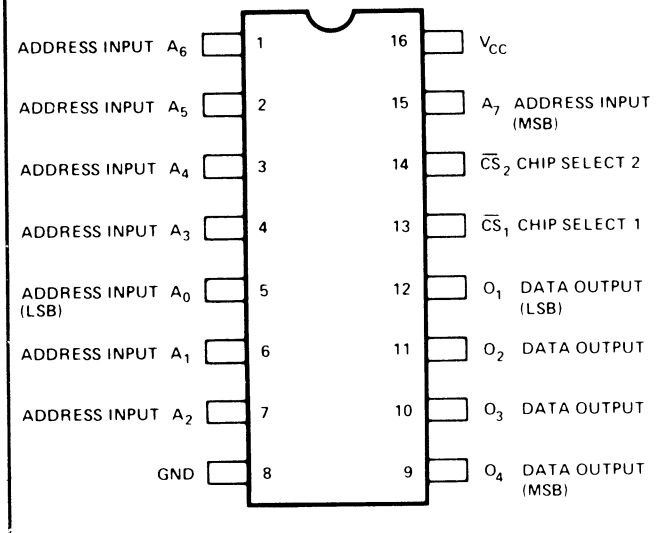
100000191

High Speed Fully Decoded 1024-Bit ROM

PIN CONFIGURATION

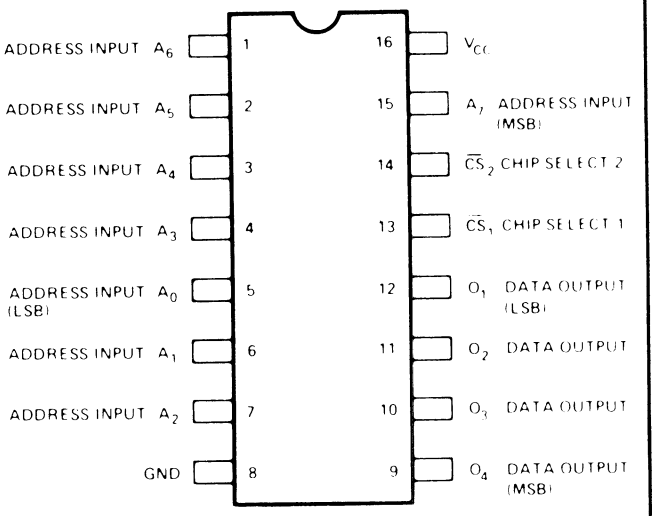


The 100000191 is a fully decoded 1024-bit read only memory organized as 256 words by 4 bits.

100000192

High Speed Electrically Programmable 1024-Bit ROM

PIN CONFIGURATION



The 100000192 is a 1024-bit (256 word by 4 bit) electrically programmable ROM. All outputs are low; logic output high levels can be electrically programmed in selected bit locations.

The same address inputs are used for both programming and reading.

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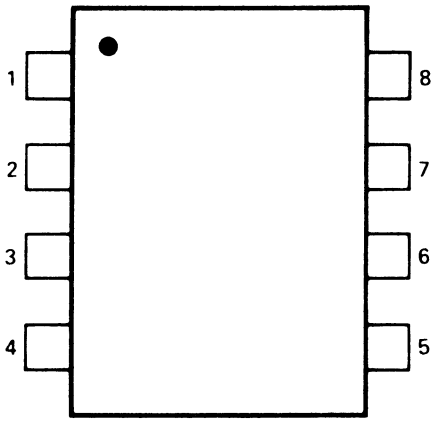
100000193

Timer

PIN CONFIGURATION



PIN DESIGNATIONS

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

The 100000193 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting, if desired.

In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. For a stable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

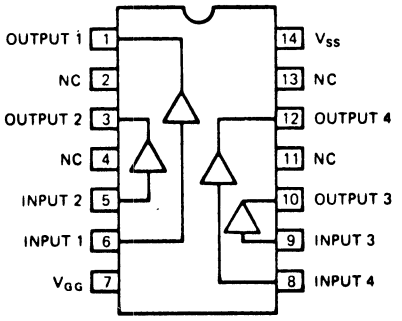
The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

NOTE *The 100000194 is a Schottky device.*

100000194

Quad MOS Clock Driver

PIN CONFIGURATION



The 100000194 is a monolithic quad driver designed primarily for use as a ı MOS clock driver. It can be driven by high current TTL buffers or drivers, either directly or through input coupling capacitors, if level shifting is required.

NOTE: *This is a MOS device.*

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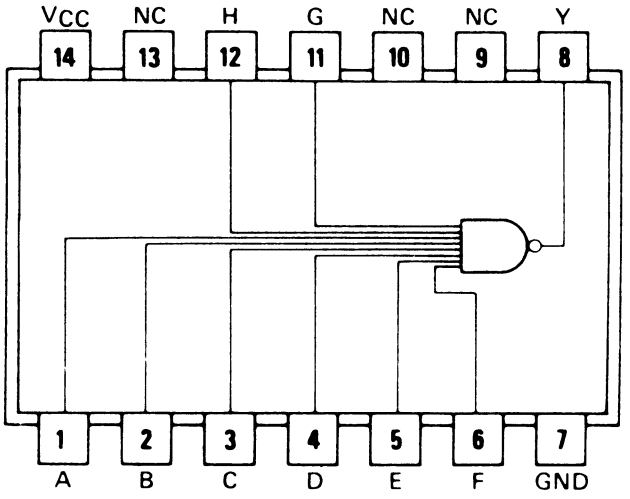
100000195

8-Input Positive-NAND Gate

PIN CONFIGURATION

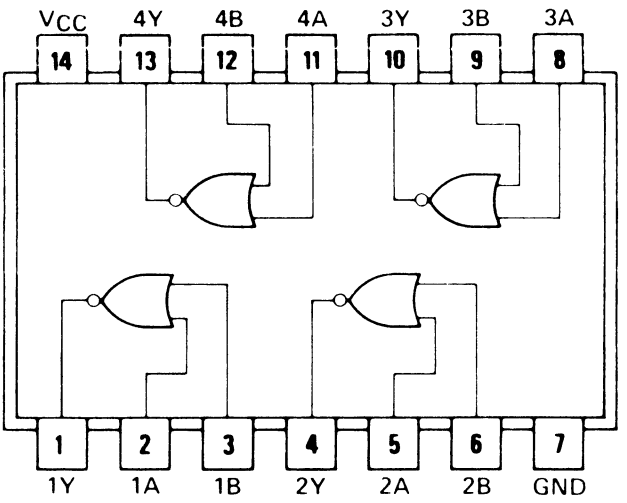


Positive logic: $Y = \overline{ABCDEFGH}$

100000196

Quad 2-Input Positive-NOR Buffer with Open-Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B}$

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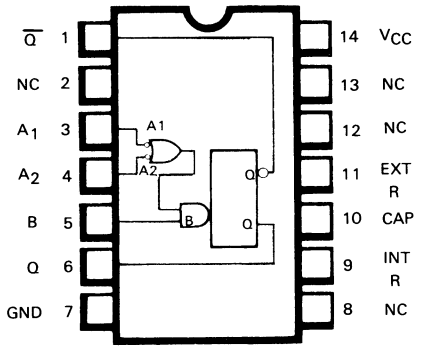
100000197

Monostable Multivibrator

PIN CONFIGURATION



TRUTH TABLE

t_n Input			t_{n+1} Input			Output
A_1	A_2	B	A_1	A_2	B	
H	H	L	H	H	H	Inhibit
L	X	H	L	X	L	Inhibit
X	L	H	X	L	L	Inhibit
L	X	L	L	X	H	One Shot
X	L	L	X	L	H	One Shot
H	H	H	X	L	H	One Shot
H	H	H	L	X	H	One Shot
X	L	L	X	H	L	Inhibit
L	X	L	H	X	L	Inhibit
X	L	H	H	H	H	Inhibit
L	X	H	H	H	H	Inhibit
H	H	L	X	L	L	Inhibit
H	H	L	L	X	L	Inhibit

H = $V_{IH} \geq 2V$
L = $V_{IL} \leq 0.8V$

Notes:

1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a High or Low may be present.
4. NC = No internal connection.
5. A_1 and A_2 are negative edge triggered-logic inputs and will trigger the one shot when either or both go to Low level with B at High level.
6. B is a positive Schmitt-trigger input for slow edges or level detection and will trigger the one shot when B goes to High level with either A_1 or A_2 at Low level. (See Truth Table.)

The 100000197 is a TTL Monostable Multivibrator with dc triggering from positive or gated negative going inputs and with inhibit facility. Both positive and negative going output pulses are provided with full fan out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1.0 V/s, providing the circuit with noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40ns to 40s by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pins 10, 11 open) an output pulse of typically 30ns is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$. Duty cycles as high as 90% are achieved when using R_T = 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

7. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30ns is obtained.
8. To use the internal timing resistor (2kΩ nominal), connect pin 9 to pin 14.
9. To obtain variable pulse width, connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
10. For accurate repeatable pulse widths, connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit.

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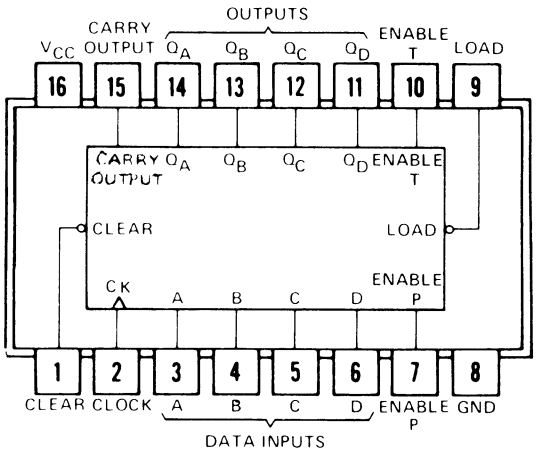
100000198

Synchronous 4-Bit Counter

PIN CONFIGURATION



This synchronous, presettable 4-bit binary counter features an internal carry look-ahead for application in high-speed counting schemes.

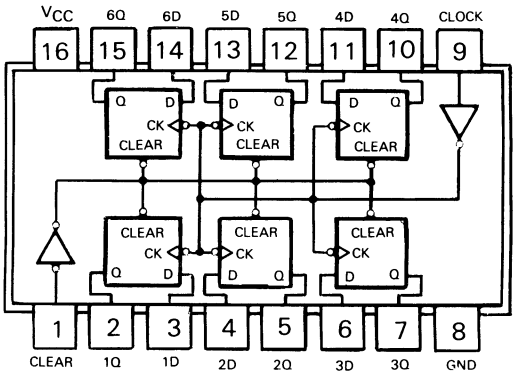
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000(LLLL).

100000199

Hex D-Type Flip-Flop with Clear

PIN CONFIGURATION



FUNCTION TABLE

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
* = Type 100000200 and 100000205 only.

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the Quadruple devices feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

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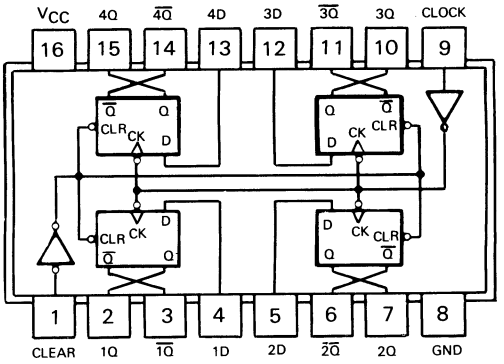
100000200

Quad D-Type Flip-Flop with Clear

PIN CONFIGURATION



FUNCTION TABLE
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

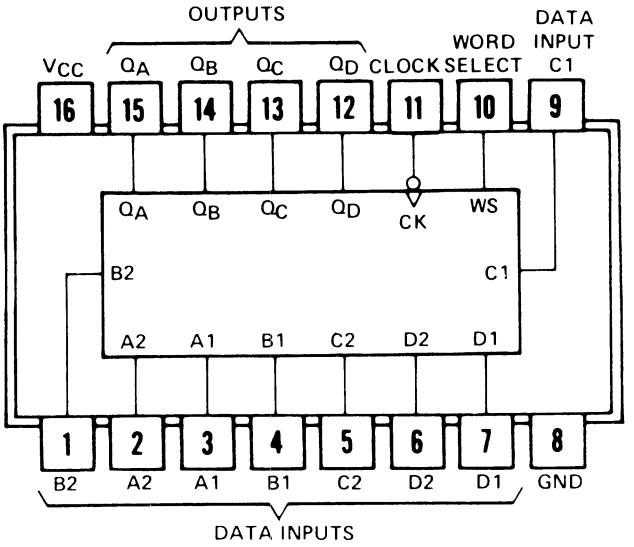
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the Quadruple devices feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

100000201

Quad 2-Input Multiplexer with Storage

PIN CONFIGURATION



FUNCTION TABLE

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Notes:

H = high level (steady state).
L = low level (steady state).
X = irrelevant (any input, including transitions).
↓ = transition from high to low level.
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., entered on the most recent ↓ transition of the clock input.

This monolithic quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (100000240 and 100000200) in a single 16-pin package.

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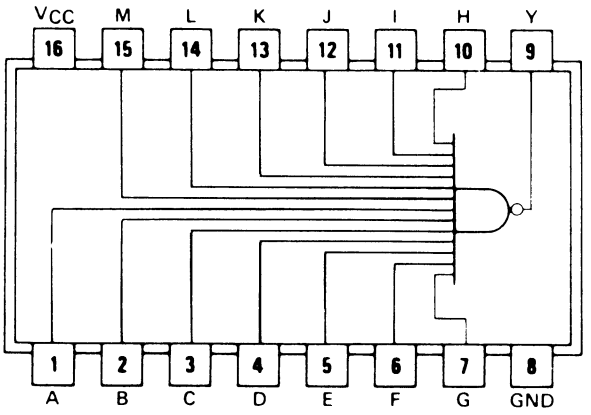
100000203

13-Input Positive-NAND Gate

PIN CONFIGURATION



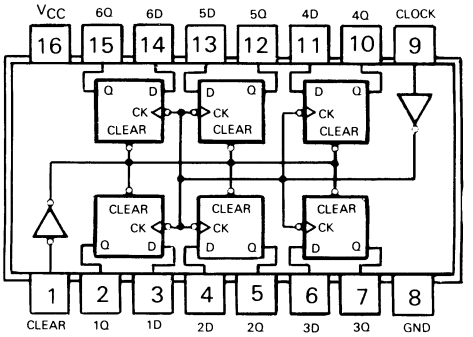
Positive logic: $Y = \overline{ABCDEFGHIJKLM}$

NOTE *The 100000203 is a Schottky device.*

100000204

Hex D-Type Flip-Flop with Clear

PIN CONFIGURATION



FUNCTION TABLE

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

NOTE *The 100000204 is a Schottky device.*

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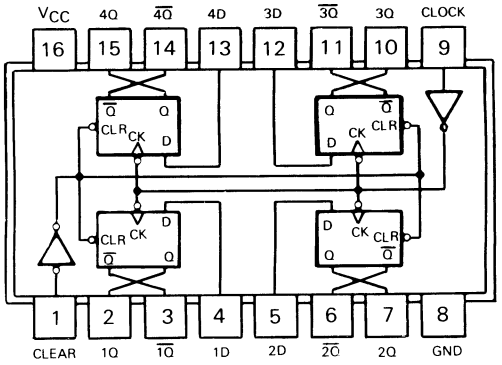
100000205

Quad D-Type Flip-Flop with Clear

PIN CONFIGURATION



FUNCTION TABLE

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and complementary outputs from each flip-flop.

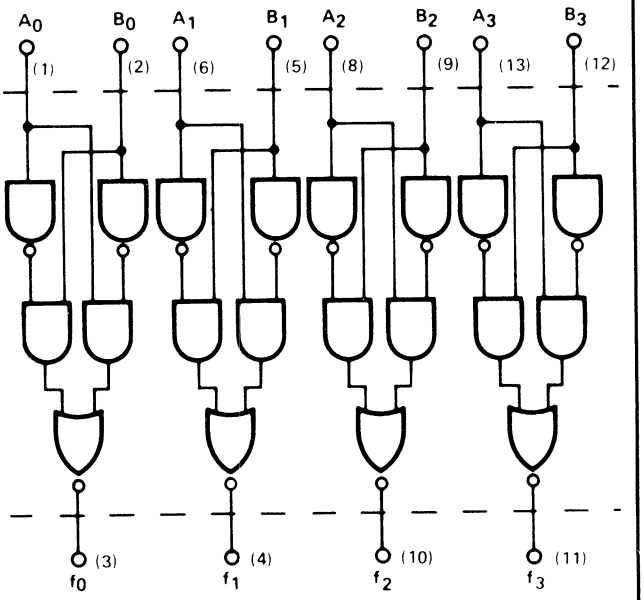
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

NOTE *The 100000205 is a Schottky device.*

100000206

Quad 4-Bit Exclusive-NOR Gate

LOGIC DIAGRAM



V_{CC} = Pin 14
Gnd = Pin 7
$Y = \overline{A} \cdot \overline{B} + A \cdot B$

TRUTH TABLE

A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

The 100000206 contains four independent Exclusive NOR gates which may be used to implement digital comparison functions. The device outputs are open collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

NOTE *The 100000206 is a Schottky device*

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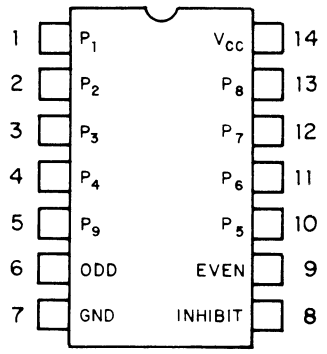
100000207

9-Bit Parity Generator and Checker

PIN CONFIGURATION



Logic Equations:

$$\text{Odd} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

$$\text{Even} = \overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

The 100000207 9-Input Parity Generator/Parity Checker is an ultra high speed Schottky MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided. An INHIBIT input is provided to disable both outputs of the device. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 100000207 supplies a parity bit which is transmitted together with the data word.

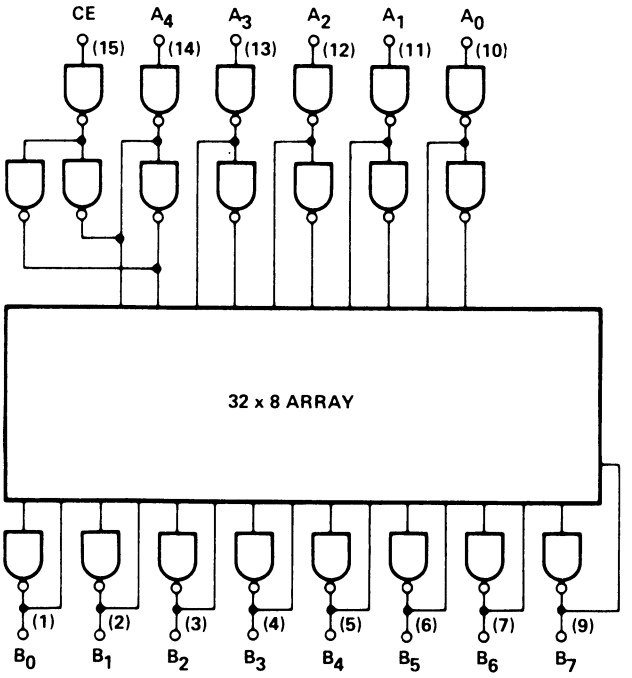
At the receiving end, the device acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

NOTE *The 100000207 is a Schottky device.*

100000208

32 x 8-Bit Bipolar ROM

LOGIC DIAGRAM



The 100000208 is a Bipolar 256-Bit Read Only Memory organized as 32 words by 8 bits per word. A chip enable line is provided, and the outputs are Tristate to allow for memory expansion capability.

NOTE *The 100000208 is a Schottky device.*

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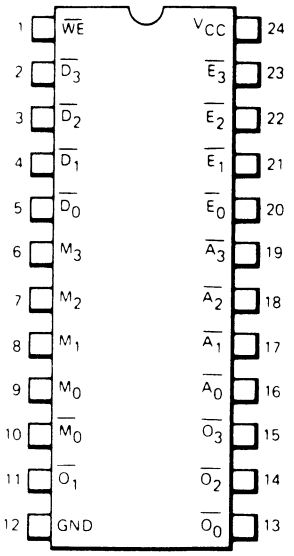
100000211

4 x 4-Bit Associative-Content Addressable Memory

PIN CONFIGURATION



The 100000211 is a high speed 16-bit associative random access memory. It is a linear select 4-word by 4-bit array which performs the equality search on all bits in parallel.

With the bit enable lines ($\overline{E}_0$ - $\overline{E}_3$) LOW, the outputs (M_0 - M_3) go HIGH if associated stored data matches the descriptor bits ($\overline{D}_0$ - $\overline{D}_3$). If a bit enable line is held HIGH, a match is forced on the corresponding bit in all the words regardless of the state of the descriptor bit ($\overline{D}_0$ - $\overline{D}_3$). An inverter is connected to the match output M_0 to give its negation $\overline{M}_0$.

A word is addressed by having an active LOW on the appropriate address line ($\overline{A}_0$ - $\overline{A}_3$). Any number of words may be addressed simultaneously.

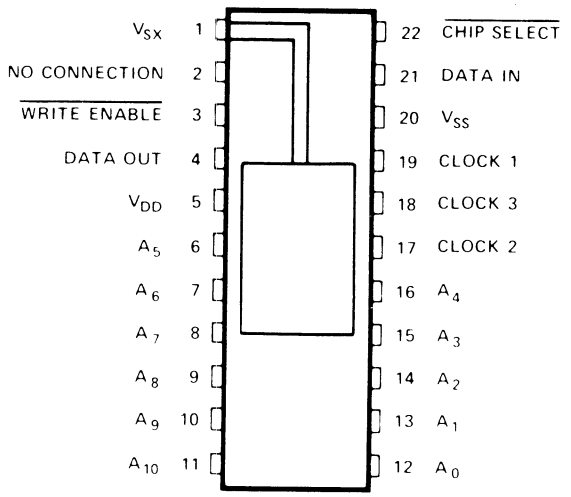
Data can be written into the memory through the data inputs ($\overline{D}_0$ - $\overline{D}_3$) under control of the address inputs and the appropriate bit enable ($\overline{E}_0$ - $\overline{E}_3$) when the write enable ($\overline{WE}$) is LOW.

Reading can occur either during an equality search or a write operation. If a single word is addressed that word will appear at the data outputs ($\overline{O}_0$ - $\overline{O}_3$). If multiple addressing is used, the word appearing at the data output is the AND (positive logic) or the OR (negative logic) of the addressed words.

100000214

2048 - Bit MOS LSI RAM

PIN CONFIGURATION



The 100000214 is a dynamic MOS random access memory device which utilizes the gate capacitance of a MOS device as a storage medium. The storage cell consists of the storage device T_1, the read select device T_2 and the write select device T_3.

The cycle begins with the negative transition of clock 1. During this time precharge is taking place. In addition, the address inputs, which must be stable during the last 65ns of clock 1 are inverted and amplified. At the end of clock 1 the internal address lines become stable. One of 64 row decoders and one of 32 column decoders are activated during t_{12}, the clock 1 to clock 2 delay time.

Clock 2, the read clock, is channeled by the decoders to the addressed column where T_2, the read select device, is turned on. The condition of the storage device T_1, (on or off) can now be sensed by the bit sense line. The addressed bit sense line is multiplexed to the I/O control circuit which then generates the Data Out. Data In, which must be valid 50ns before clock 3, is conditioned and amplified in the I/O control circuit. During clock 3, the write driver transmits the input data through the multiplexer to the addressed bit sense line.

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100000214
(Continued)

Clock 3, the write clock, is channeled by the decoders to the addressed column where T_3, the write select device, is turned on. Any information on the bit sense line is, therefore, transferred to the C_S, the gate capacitance of the storage device.

The refresh cycle consists of clock 1, clock 2 and clock 3. Clock 1 precharges the bit sense line. Clock 2 senses the status of the storage device T_1, which is operating in the inverter mode, and places the inverted state of the storage device on the bit sense line. Clock 3, by turning on T_3, transfers the information from the bit sense line to the storage device. Note, each refresh cycle will result in the inversion of the stored data. To refresh all 2048 cells, each of the 32 columns must be selected for a refresh cycle by exercising all 32 combinations of the low order addresses (A_0 - A_4).

The read cycle may consist only of clock 1 and clock 2. Since each refresh cycle inverts the data in the storage cells in an accessed column, a control circuit, the Data Control Register, is used. The Data Control Register, which is basically another set of memory cells, is slaved to the memory array. The state of the Data Control Register will provide information as to whether a column of storage cells is in a non-inverting or inverting state.

Clock 1 of the read cycle precharges the device. Clock 2 is transmitted by the column decoders to the addressed column. At this time, data from both the storage cell and the Data Control Register is sensed. The row multiplexer transfers the data from the addressed row to the I/O Control circuit. In the I/O Control circuit, an exclusive-OR function of the data from the memory array and the Data Control Register is performed. The output of the exclusive-OR is then amplified and presented to the Data Out pin. The output data is held in a register until the initiation of the next memory cycle. A new memory cycle may begin 20ns after clock 2 has returned to a positive state. The 100000214 is a non-inverting device; i. e., TTL "high" Data-In will result in an output high current.

The write cycle consists of clock 1, clock 2 and clock 3. During clock 1 the precharge operation takes place. During clock 2 the Data Control Register is read to determine whether the accessed column is in a true or inverted state. At the beginning of clock 3 the exclusive-OR function of Data-In and the content of the Data Control Register is performed in the I/O Control circuit. The output of the input exclusive-OR is then amplified and transmitted to the addressed cell by the write-driver. A new memory cycle may begin 20ns after clock 3 has returned to the positive state.

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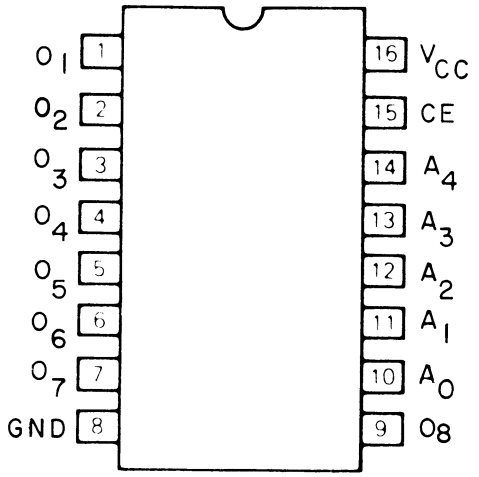
100000215 through 100000219

32 x 8-Bit ROM

PIN CONFIGURATION



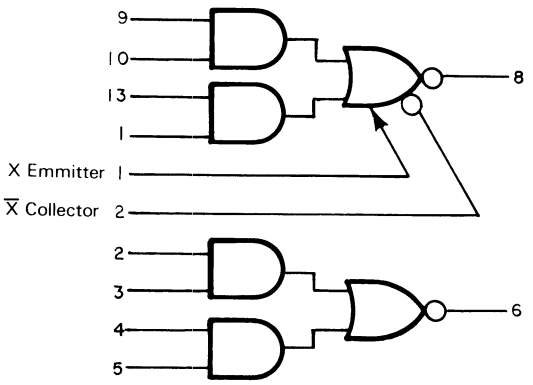
These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

100000221

Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate

LOGIC DIAGRAM



V_{CC} = Pin 14

Gnd = Pin 7

Positive Logic: $Y = \overline{AB + CD + X}$

$\overline{8 = (9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$

Negative Logic:

$\overline{8 = (9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})}$

X = Output of 100000039

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion.

NOTE *The 100000221 is a high speed TTL device.*

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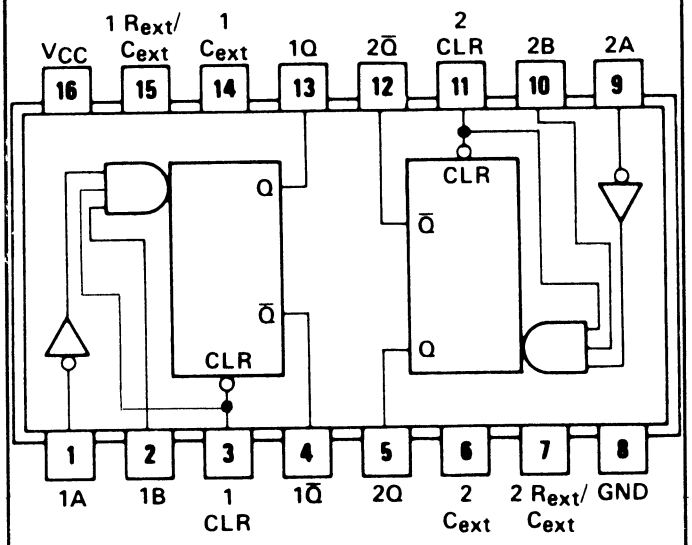
100000222

Dual Retriggerable Monostable Multivibrator with Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Notes:

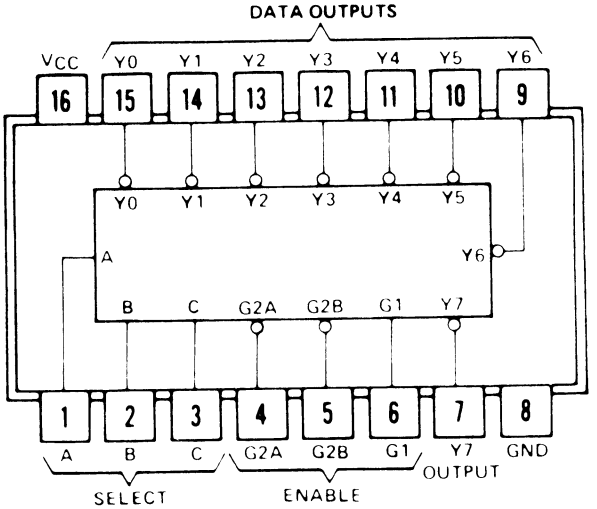
H = high level (steady state).
L = low level (steady state).
↑ = transition from low to high level.
↓ = transition from high to low level.
⎍ = one high-level pulse.
⎎ = one low-level pulse.
X = irrelevant (any input, including transitions).

An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

100000223

Decoder/Demultiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level; L = low level; X = irrelevant

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

NOTE *The 100000223 is a Schottky device.*

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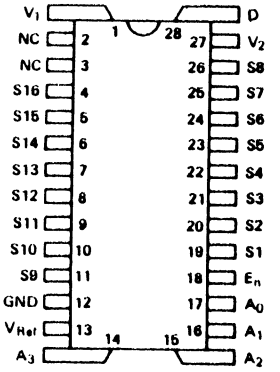
100000224

16-Channel Analog Multiplexer Complementary MOS (CMOS)

PIN CONFIGURATION



V_1 COMMON TO SUBSTRATE

TRUTH TABLE

A3	A2	A1	A0	En	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

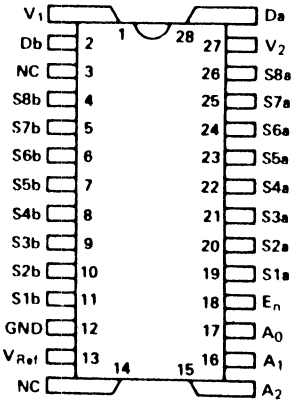
Logic "1" = $V_{AH} > 2.4V$

Logic "0" = $V_{AL} < 0.8V$

100000225

8-Channel Differential Analog Multiplexer Complementary MOS (CMOS)

PIN CONFIGURATION



V_1 COMMON TO SUBSTRATE

TRUTH TABLE

A2	A1	A0	En	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} > 2.4V$

Logic "0" = $V_{AL} < 0.8V$

The 100000225 is a double-pole 8-position (plus OFF) electronic switch array which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction; in the OFF condition each switch will block voltages up to 30V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input.

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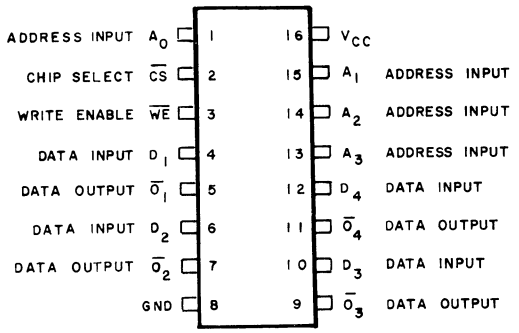
100000226

High Speed Fully Decoded 64-Bit Memory

PIN CONFIGURATION



PIN NAMES

D_1-D_4	Data Inputs
A_0-A_3	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select Input
$\overline{O_1}$-$\overline{O_4}$	Data Outputs
V_{CC}	Power (+5V)

The 100000226 is a high speed, fully decoded 64-bit random access memory, using Schottky barrier diode clamped transistors. Organization is 16 words by 4 bits.

An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

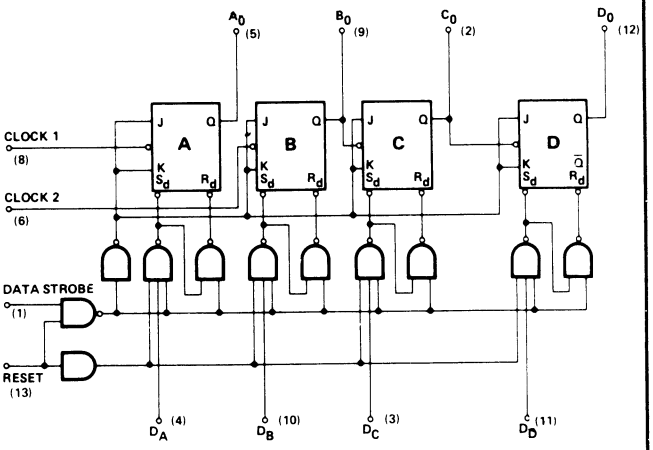
The storage cells are addressed through an on-chip 1 of 16 binary decoder using four input address leads.

A separate Chip Select lead allows selection of an individual package when outputs are OR-tied. In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

100000227

Presettable High Speed Binary Counter

PIN CONFIGURATION



The 100000227 Presettable High Speed Binary Counter may be connected as a divide-by-two, four, eight or sixteen counter.

This device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. This unit is provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

NOTE *The 100000227 is a Schottky device.*

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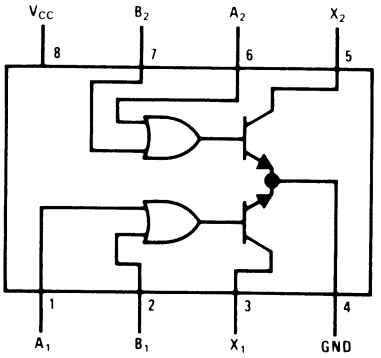
100000228

Dual Peripheral Driver

PIN CONFIGURATION



$$X = \overline{A + B}$$

TRUTH TABLE

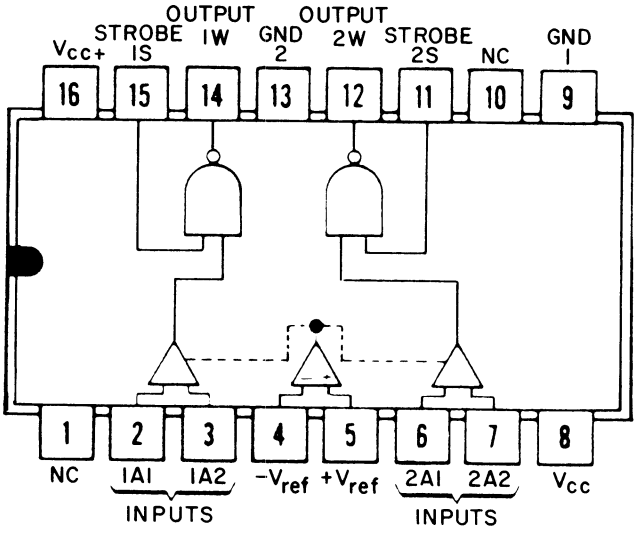
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000229

Dual Sense Amplifier

PIN CONFIGURATION



Positive logic: $W = \overline{AS}$

TRUTH TABLE

Inputs		Output**
A	S	W
H	H	L
L	X	H
X	L	H

Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geq V_{Tmax}$	$V_{ID} \leq V_{Tmin}$	Irrelevant
S	$V_I \geq V_{IHmin}$	$V_I < V_{ILmax}$	Irrelevant

* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

**Internal pull-up resistors

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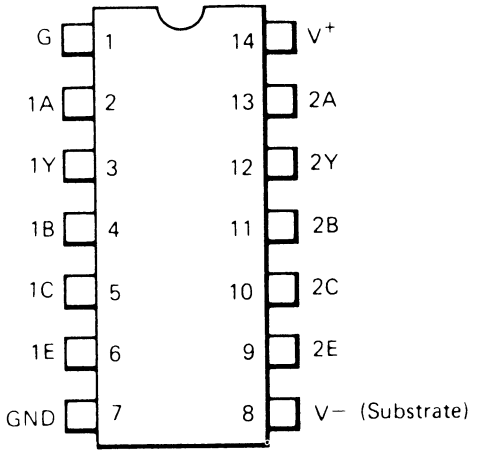
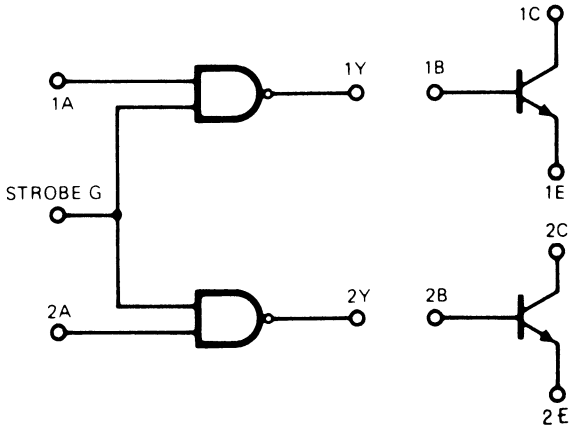
100000231

Dual Peripheral Driver

PIN CONFIGURATION



BLOCK DIAGRAM

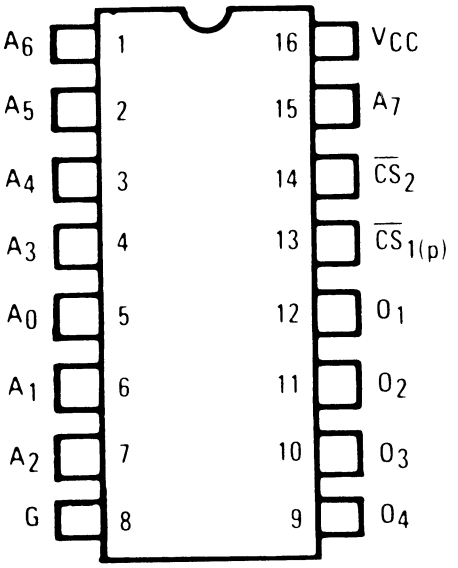


$Y = \overline{AG}$

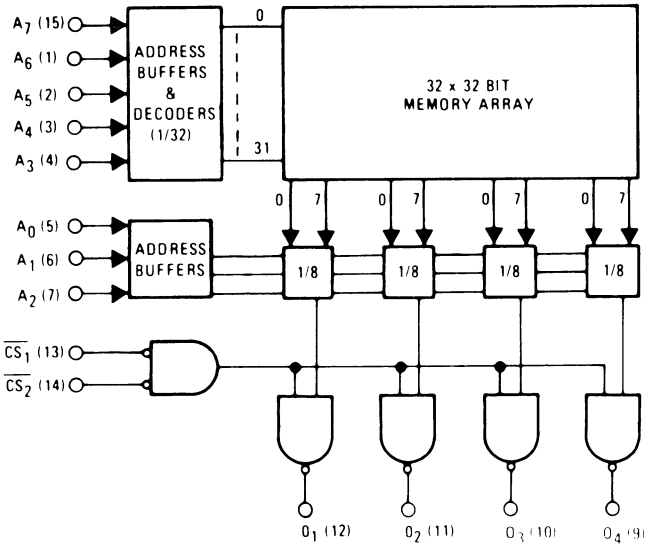
100000232

256 x 4-Bit Field Programmable Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



The 100000232 is a fully decoded, high speed, 1024-bit, field programmable ROM, organized as 256 words by 4 bits per word. The device has an open collector output.

This PROM is supplied with all bits storing a logical "1" (output high) and can be selectively programmed for a logical "0" (output low). The addressing scheme for programming and reading the information in the system is the same.

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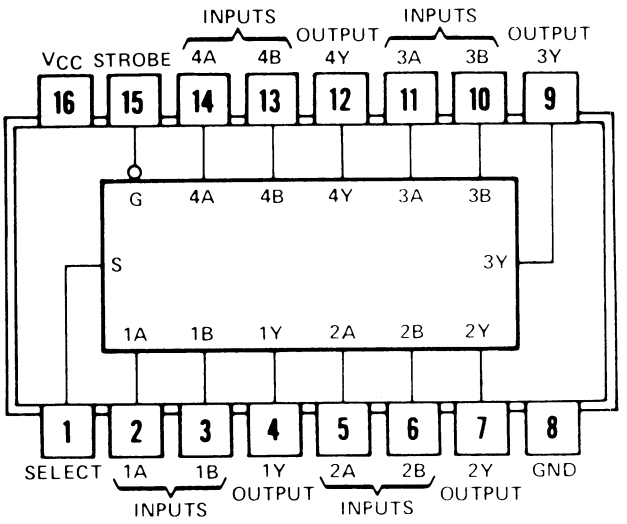
100000233

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



Positive logic:

Low logic level at S selects A inputs.

High logic level at S selects B inputs.

FUNCTION TABLE

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Notes:

H = high level; L = low level; X = irrelevant.

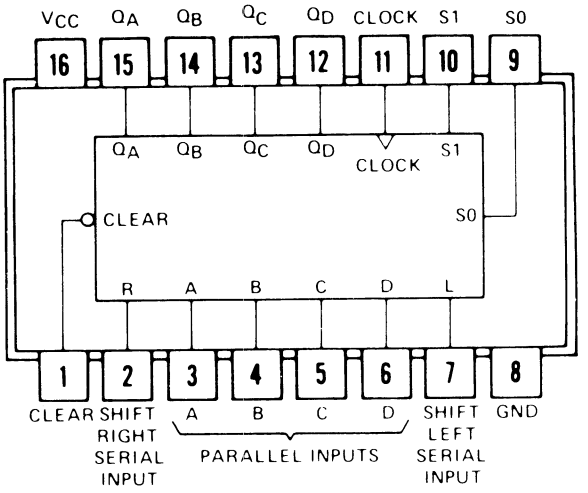
These monolithic data selectors/multiplexors contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. These devices present true data.

NOTE *The 100000233 is a Schottky device.*

100000234

4-Bit Bidirectional Universal Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS									OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL						
	S_1	S_0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

The 100000234 is a Schottky device.

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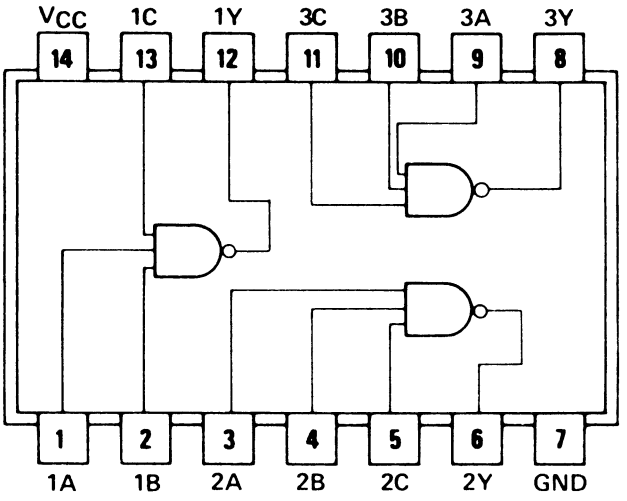
100000235

Triple 3-Input Positive-NAND Gate

PIN CONFIGURATION



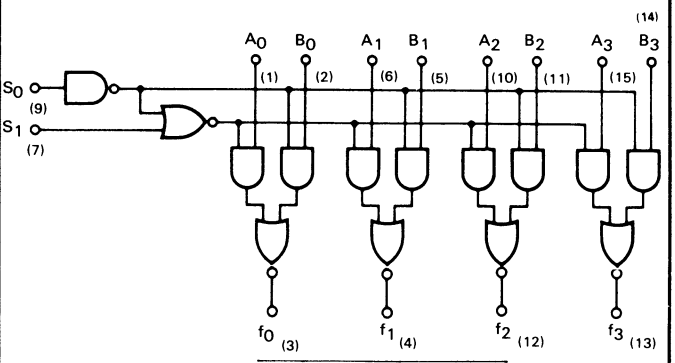
Positive logic: $Y = \overline{ABC}$

NOTE *The 100000235 is a Schottky device.*

100000236

2-Input, 4-Bit Digital Multiplexer

LOGIC DIAGRAM



$$Y = \overline{(\overline{S}_0 + S_1)}\,(A_n) + \overline{S}_0\,\overline{B}_n$$

V_{CC} = Pin 16

Gnd = Pin 8

TRUTH TABLE

S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

This 2-Input, 4-Bit Digital Multiplexer features inverting data paths.

The 100000236 has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as forty four-bit words can be multiplexed by using twenty of these devices in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

NOTE *The 100000236 is a Schottky device.*

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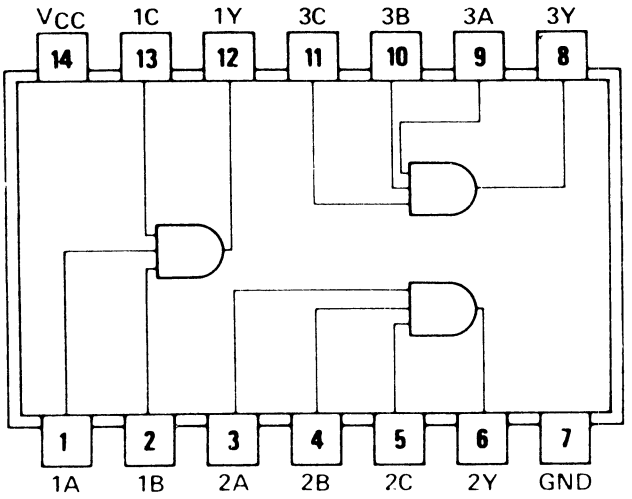
100000237

Triple 3-Input Positive-AND Gate

PIN CONFIGURATION



V_{CC} = Pin 14

Gnd = Pin 7

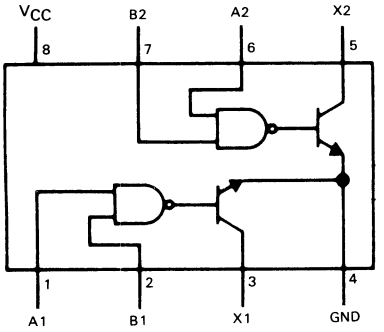
Positive logic: Y = ABC

NOTE *The 100000237 is a Schottky device.*

100000238

Dual Peripheral Driver

PIN CONFIGURATION



TRUTH TABLE

Positive logic: X = AB

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

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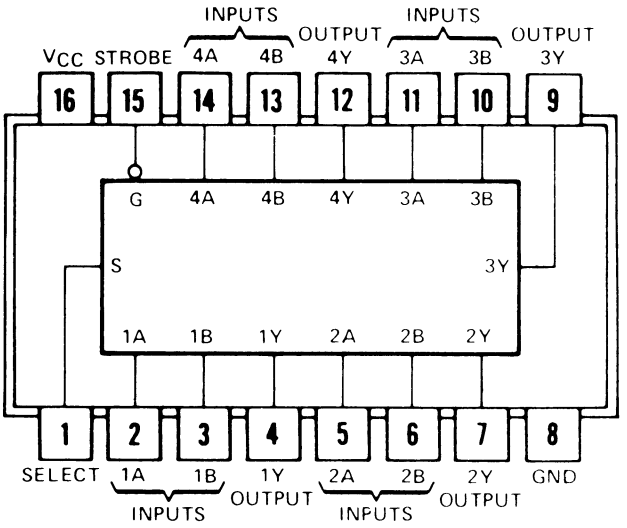
100000240

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



Positive logic:

Low logic level at S selects A inputs.

High logic level at S selects B inputs.

TRUTH TABLE

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Notes:

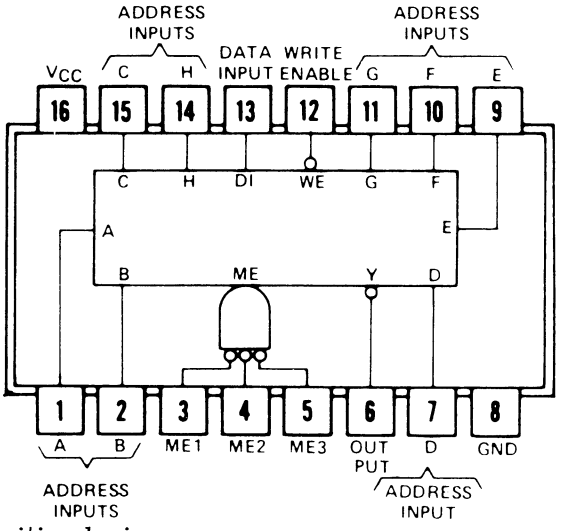
H = high level; L = low level; X = irrelevant.

These monolithic data selectors/multiplexors contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. These devices present true data.

100000241

256 x 1-Bit RAM with 3-State Outputs

PIN CONFIGURATION



Positive logic:

Data out is complement of data which was applied at data input.

TRUTH TABLE

Function	Inputs		Output
	Memory Enable*	Write Enable	
Write (Store complement of data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level
L = low level
X = irrelevant
* For memory enable:

L = all ME inputs low
H = one or more ME inputs high

This 256-bit active-element memory is a monolithic TTL array organized as 256 words of one bit each. It is fully decoded and has three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

NOTE *The 100000241 is a Schottky device.*

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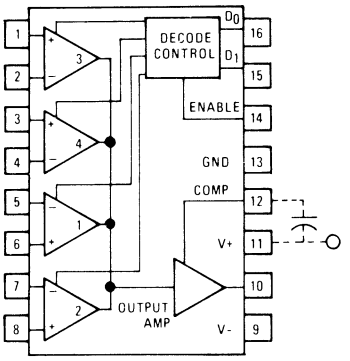
100000242

4-Channel Programmable Amplifier

PIN CONFIGURATION



TRUTH TABLE

D_1	D_0	EN	Selected Channel
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

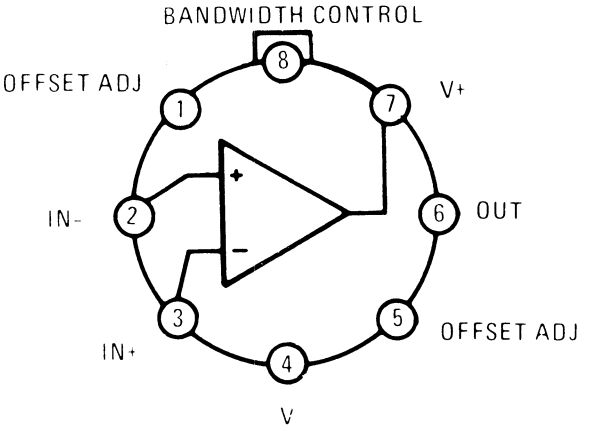
This operational amplifier has four identical input stages, any one (or none) of which may be electronically connected to the single output stage. The "ON" channel is selected through DTL/TTL compatible address inputs. The unselected amplifier inputs are effectively "floating".

This device can be used as an analog signal selector, sampler or multiplexer with built in buffering or signal conditioning. By connecting different feedback networks from the output to each input pair, it can be used as a single or multiple channel amplifier with programmable feedback characteristics.

100000243

Wide Band, High Impedance Operational Amplifier

PIN CONFIGURATION



This operational amplifier has very low input bias current and is intended for use as a high impedance comparator and a wide band amplifier. The device provides very high gain, very high slew rate and output short circuit protection.

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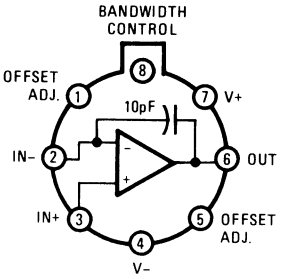
100000244

High Slew Rate F.E.T. Input Operational Amplifier

PIN CONFIGURATION



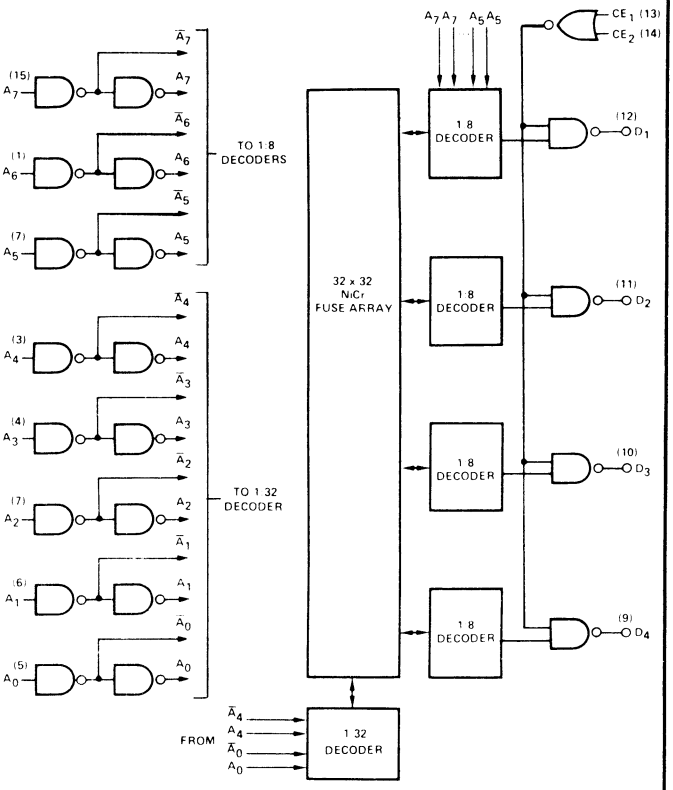
This operational amplifier combines very high slew rate and wide bandwidth with ultra-low input current and high input resistance.

The device may be operated inverting or non-inverting. External compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

100000245

256 x 4-Bit Bipolar PROM

BLOCK DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

The 100000245 is a Bipolar 1024 Bit Read Only Memory organized as 256 words by 4 bits per word, with open collector outputs. This device is field-programmable.

Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

NOTE *The 100000245 is a Schottky device.*

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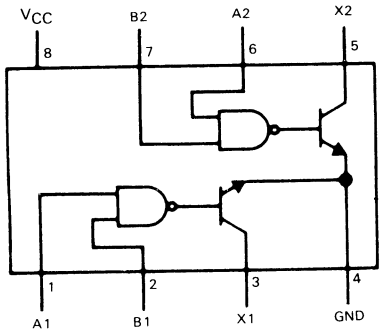
100000247

Dual Peripheral Driver

PIN CONFIGURATION



TRUTH TABLE

Positive logic: X = AB

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

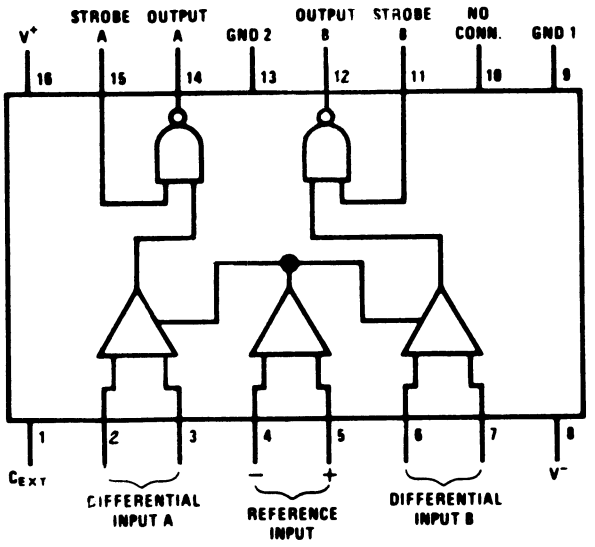
*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000248

Sense Amplifier

PIN CONFIGURATION



PIN DESIGNATIONS

V+ = Pin 16
V- = Pin 8
Gnd 1 = Pin 9
Gnd 2 = Pin 13

These dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible.

$$Y = \overline{(AB)\ (REF)\ (S)}$$

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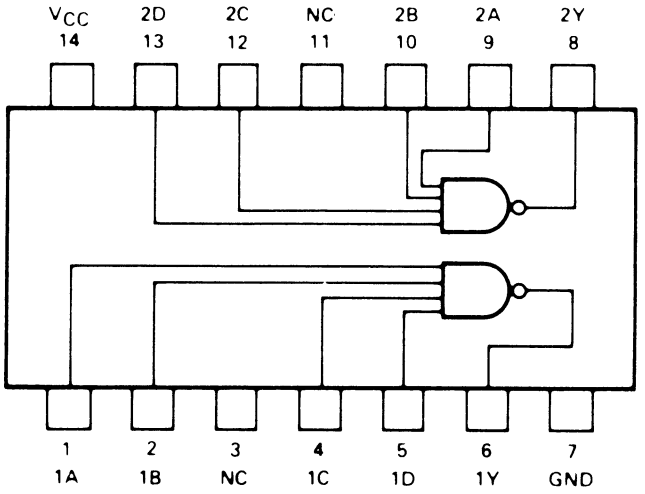
100000249

Dual 4 Input Positive-NAND Gate

PIN CONFIGURATION



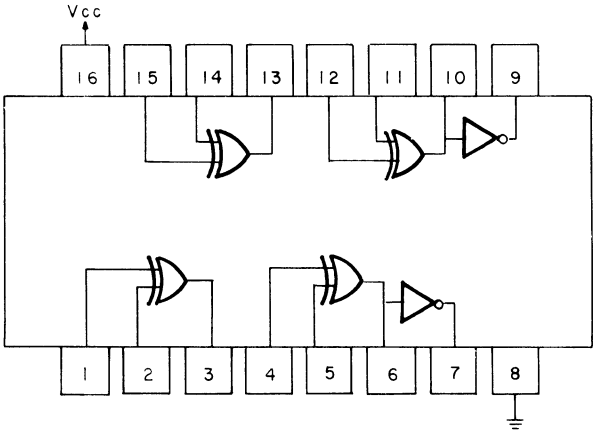
$Y = \overline{ABCD}$

NOTE: *This is a Schottky device*

100000250

Quad Exclusive-OR Gate

PIN CONFIGURATION



TRUTH TABLE

A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = High Voltage Level
L = Low Voltage Level

The exclusive OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expressions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{AB}$.

NOTE The 100000249 is a Schottky device.

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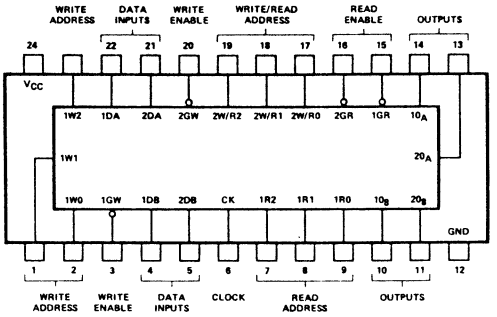
100000251

8 x 2 - Bit Multiple Port Register File

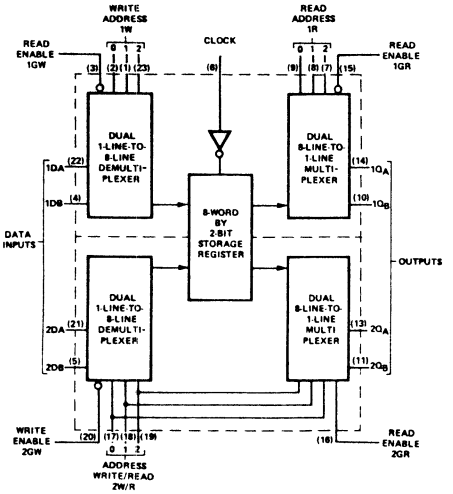
PIN CONFIGURATION



FUNCTION TABLE

FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA≠2DA and/or 1DB≠2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1O_A$, $1O_B$	$2O_A$, $2O_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

BLOCK DIAGRAM



The 100000251 is a 16-bit register file organized as eight words by 2 bits. The file consists of two sections (see block diagram) which function independently of each other.

Section 1 uses independent write and read address inputs so that read and write operations can be performed simultaneously on two word locations.

Section 2 is similar to section 1 except that it uses common write and read address inputs. This section has three modes of operation: write, read, and read-modify-write.

The register file has tri-state outputs which are controlled by the read/write circuitry. They function as standard TTL totem-pole outputs when the read enable is low or they are placed in a high impedance state when the read enable is high.

NOTE *The 100000251 is a Schottky device.*

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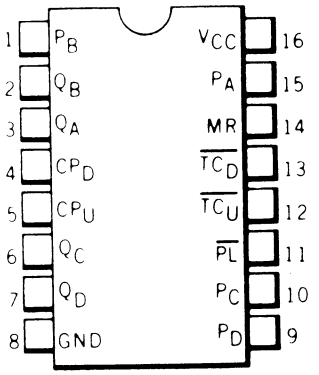
100000252

Up/Down Decade Counter

PIN CONFIGURATION



MODE SELECTION

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

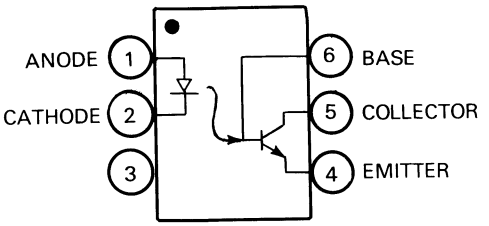
The 100000252 is a synchronous Up/Down BCD Decade Counter. It has separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset.

It can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table.

100000253

Phototransistor Opto-Isolator

PIN CONFIGURATION



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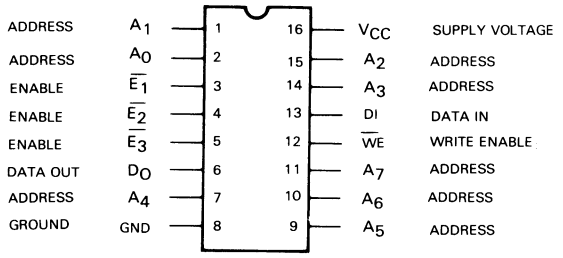
100000255

256 x 1-Bit Bipolar RAM

PIN CONFIGURATION



TRUTH TABLE

Chip Select	Write Enable	Operation	Output
All Low	Low	Write	Complement of data input
All Low	High	Read	Complement of written data
One or More High	Don't Care	Hold	High

The 100000255 is a fully decoded static bipolar random access memory organized 256 words by 1 bit, with open-collector outputs. The open-collector parts have 3 chip enables for easy expansion to larger size memories.

Memory Operation

Read

The memory is addressed with the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by making all chip enables low. If any or all chip enables are high the chip is disabled. If the write enable is high and the chip is enabled the stored data is read out on the data out pin. The data read out is the complement of the data written in during the write cycle.

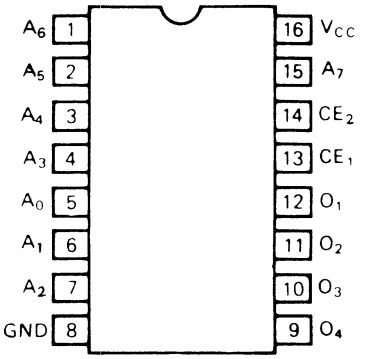
Write

The memory is addressed with the A_0-A_7 inputs which select one of the 256 words. The chip is enabled as in the read cycle. If the write enable is low the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle.

100000256

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

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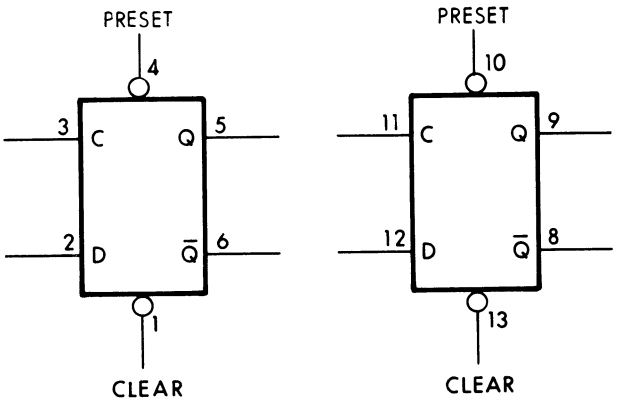
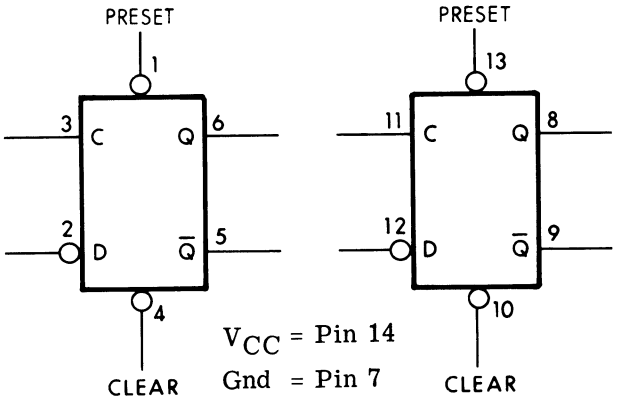
100000257

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



ALTERNATE PIN CONNECTIONS



V_{CC} = Pin 14
Gnd = Pin 7

FUNCTION TABLE

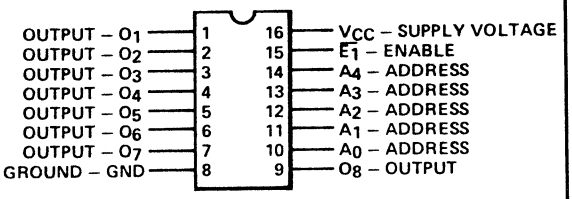
Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

100000258

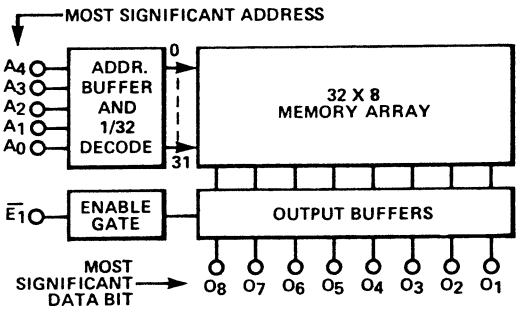
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



V_{CC} = 16
GND = 8

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE: *The 100000258 is a Schottky device.*

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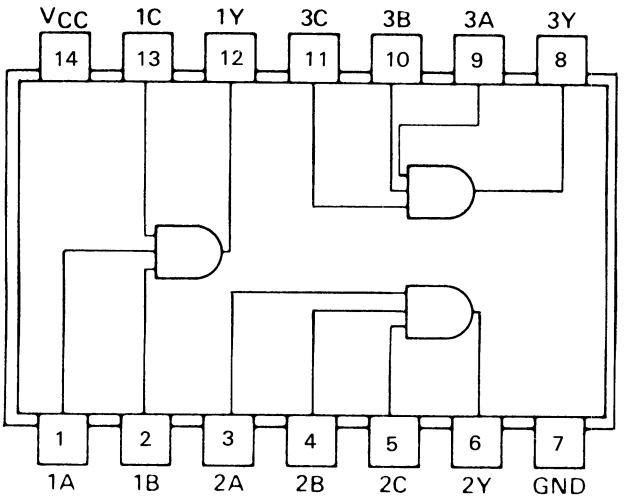
100000259

Triple 3-Input Positive-AND Gate with Open-Collector Outputs

PIN CONFIGURATION



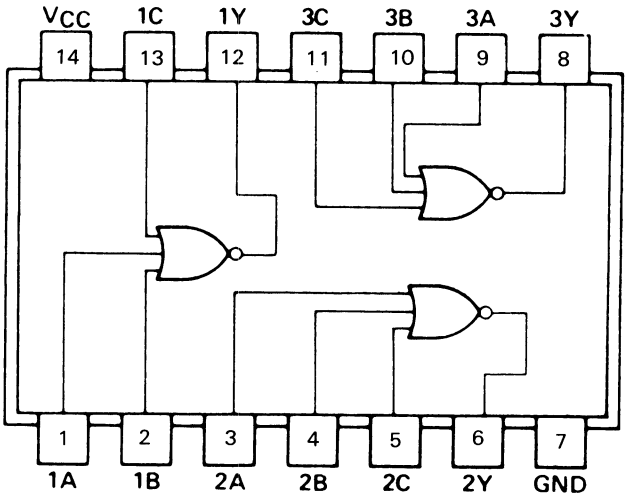
Positive logic: $Y = ABC$

NOTE *The 100000259 is a Schottky device.*

100000260

Triple 3-Input Positive-NOR Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B+C}$

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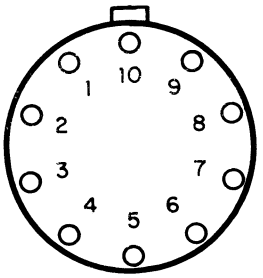
100000261

Phase Locked Loop

PIN CONFIGURATION



PIN DESIGNATIONS

1. V^-
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V^+

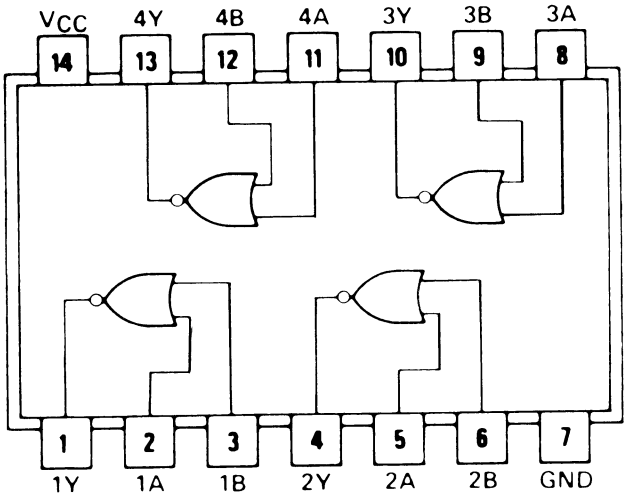
This Phase Locked Loop is a self-contained, adaptable filter and demodulator for the frequency range 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator, a phase comparator, an amplifier and a low-pass filter.

The center frequency of the device is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

100000262

Quad 2-Input Positive-NOR Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B}$

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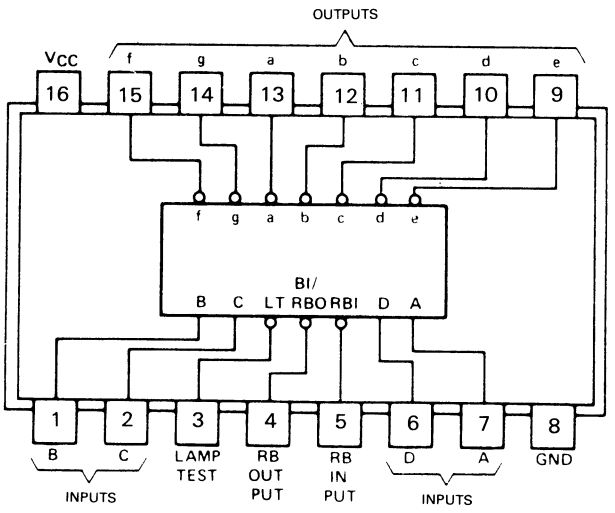
100000263

BCD-To-7-Segment Decoder/Driver with Open Collector Outputs (a through g)

PIN CONFIGURATION



FUNCTION TABLE

Decimal or Function	Inputs						BI/RBO*	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	On	On	On	On	On	On	Off	1
1	H	X	L	L	L	H	H	Off	On	On	Off	Off	Off	Off	1
2	H	X	L	L	H	L	H	On	On	Off	On	On	Off	On	
3	H	X	L	L	H	H	H	On	On	On	On	Off	Off	On	
4	H	X	L	H	L	L	H	Off	On	On	Off	Off	On	On	
5	H	X	L	H	L	H	H	On	Off	On	On	Off	On	On	
6	H	X	L	H	H	L	H	Off	Off	On	On	On	On	On	
7	H	X	L	H	H	H	H	On	On	On	Off	Off	Off	Off	
8	H	X	H	L	L	L	H	On	On	On	On	On	On	On	
9	H	X	H	L	L	H	H	On	On	On	Off	Off	On	On	
10	H	X	H	L	H	L	H	Off	Off	Off	On	On	Off	On	
11	H	X	H	L	H	H	H	Off	Off	On	On	Off	Off	On	
12	H	X	H	H	L	L	H	Off	On	Off	Off	Off	On	On	
13	H	X	H	H	L	H	H	On	Off	Off	On	Off	On	On	
14	H	X	H	H	H	L	H	Off	Off	Off	On	On	On	On	
15	H	X	H	H	H	H	H	Off	Off	Off	Off	Off	Off	Off	
BI	X	X	X	X	X	X	L	Off	Off	Off	Off	Off	Off	Off	2
RBI	H	L	L	L	L	L	L	Off	Off	Off	Off	Off	Off	Off	3
LT	L	X	X	X	X	X	H	On	On	On	On	On	On	On	4

H = High level; L = Low level; X = irrelevant.

Notes:

1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

* BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

This circuit has full ripple-blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

Automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated in this device. A lamp test (LT) may be performed at any time when the BI/RBO is at a high level. An overriding blanking input (BI) can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are compatible for use with TTL or DTL logic outputs.

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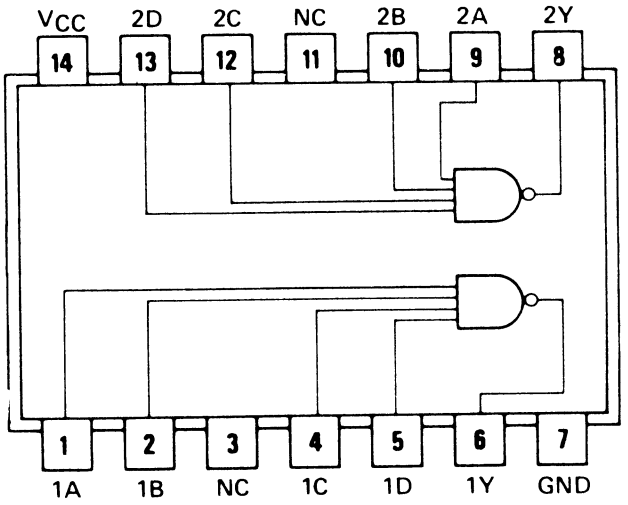
100000264

Dual 4-Input Positive-NAND Buffer

PIN CONFIGURATION



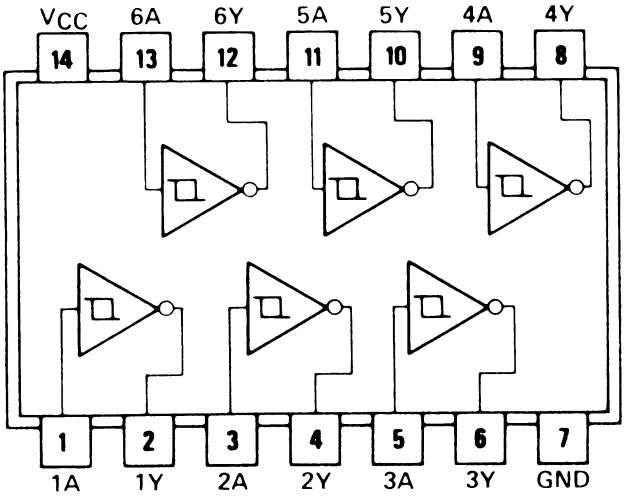
Positive logic: $Y = \overline{ABCD}$

NOTE *The 100000264 is a Schottky device.*

100000265

Hex Schmitt-Trigger Inverter

PIN CONFIGURATION



Positive logic: $Y = \overline{A}$

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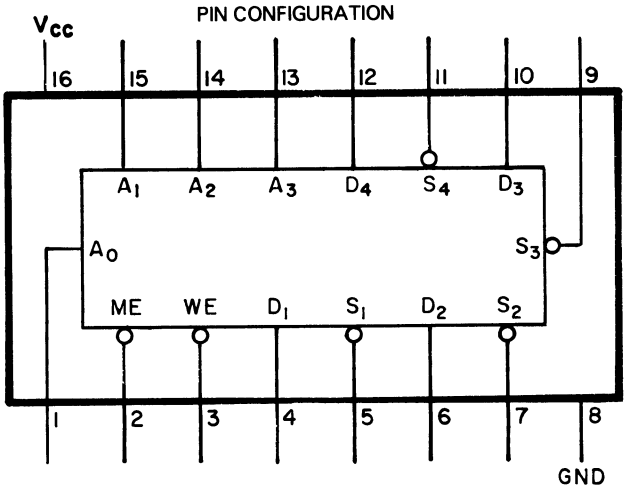
100000266

16 x 4-Bit RAM

PIN CONFIGURATION



TRUTH TABLE

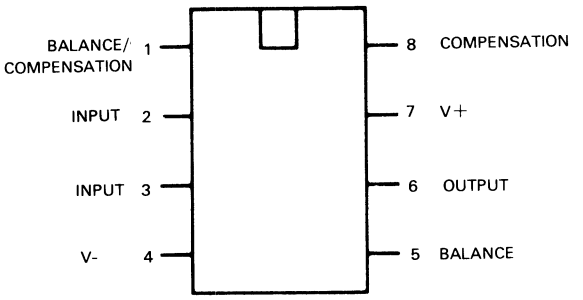
Memory Enable	Write Enable	Operation	Outputs
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

The 100000266 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

100000267

Operational Amplifier

PIN CONFIGURATION



The 100000267 is a general purpose operational amplifier. This amplifier offers overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30pF capacitor.

In addition, the circuit can be used as a comparator with differential inputs up to ±30V, and the output can be clamped at any desired level to make it compatible with logic circuits.

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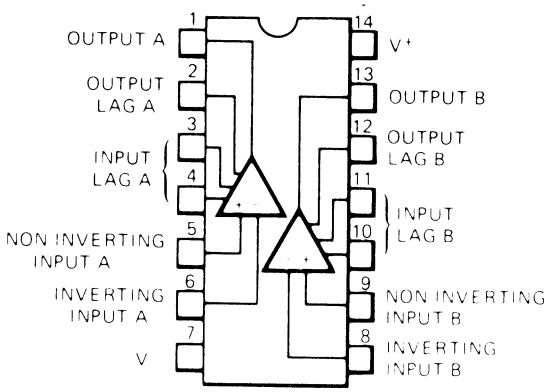
100000268

Dual Operational Amplifier

PIN CONFIGURATION

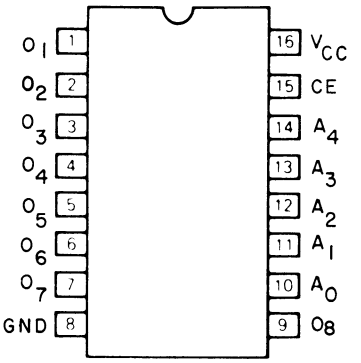


The 100000268 consists of two identical high gain operational amplifiers. These three-stage amplifiers use class A PNP transistor output stages with uncommitted collectors. The outputs may be ORed for use as a dual comparator or they may function as diodes in low threshold rectifying circuits.

100000269 through 100000280

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

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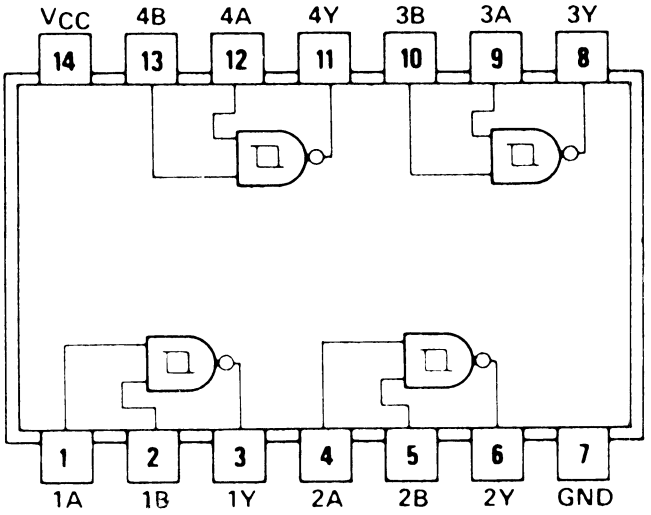
100000281

Quad 2-Input Positive-NAND Schmitt Trigger

PIN CONFIGURATION



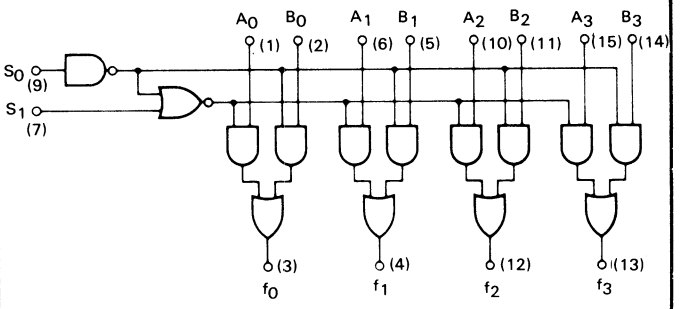
$Y = \overline{AB}$

NOTE *The 100000281 is a Schottky device.*

100000282

2-Input 4-Bit Digital Multiplexer

LOGIC DIAGRAM



V_{CC} = Pin 16

Gnd = Pin 8

$$f_n = \overline{(\overline{S_0} + S_1)(A_n) + \overline{S_0}\,\overline{B_n}}$$

TRUTH TABLE

S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

This 2-input, 4-bit digital multiplexer features non-inverting data paths.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

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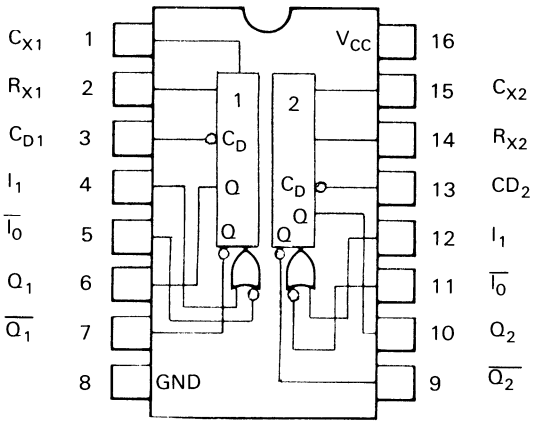
100000283

Dual Retriggerable Resettable Monostable Multivibrator

PIN CONFIGURATION



TRUTH TABLE

Pin Numbers			
5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geq V_{IH}$

L = LOW Voltage Level $\leq V_{IL}$

X = Don't Care

H→L = HIGH to LOW Voltage Level transition

L→H = LOW to HIGH Voltage Level transition

The Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components.

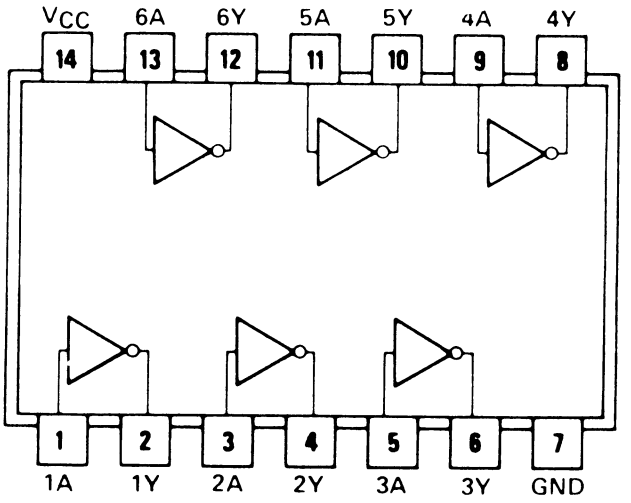
This device has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the device and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW.

NOTE *The 100000283 is a low power TTL device.*

100000284

Hex Inverter with Open Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{A}$

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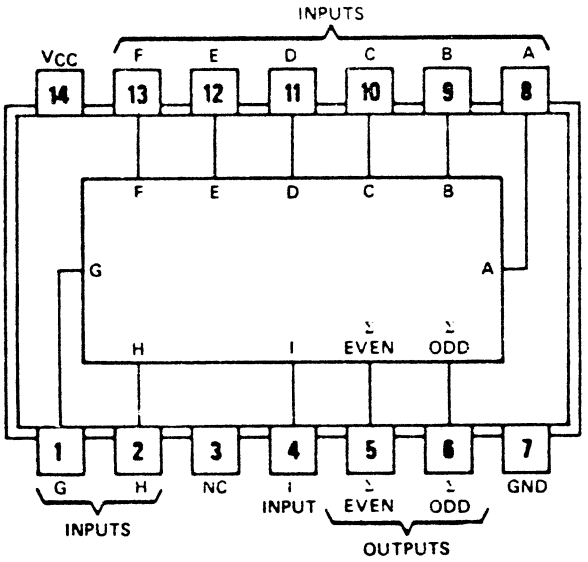
100000287

9-Bit Odd/Even Parity Generator/Checker

PIN CONFIGURATION



FUNCTION TABLE

Number of Inputs A Thru I That Are High	Outputs Σ Even	Outputs Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level
L = low level

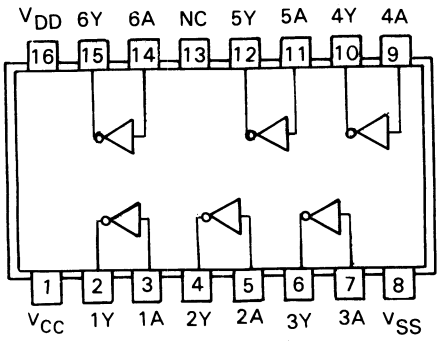
This universal, monolithic, nine-bit parity generator/checker utilizes Schottky-clamped TTL circuitry and features odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is expanded by cascading.

NOTE *The 100000287 is a Schottky device.*

100000288

Hex Inverting Buffer

PIN CONFIGURATION



$Y = \overline{A}$

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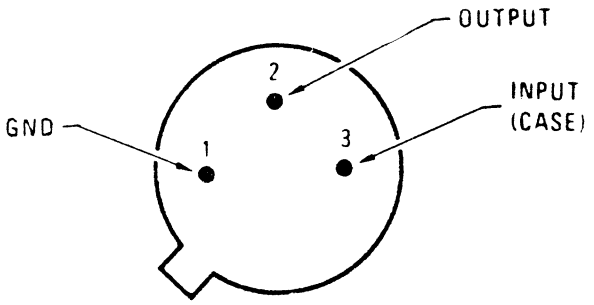
100000290

-12V, 1/2A, 5% Voltage Regulator

PIN CONFIGURATION



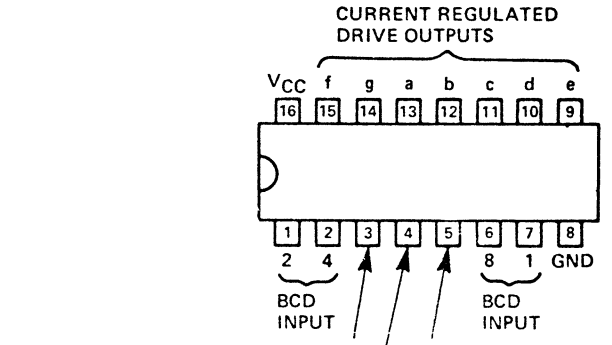
BOTTOM VIEW

The 100000290 is a three-terminal negative regulator. It has a fixed voltage output of -12V. This device needs only one external component, a compensation capacitor at the output.

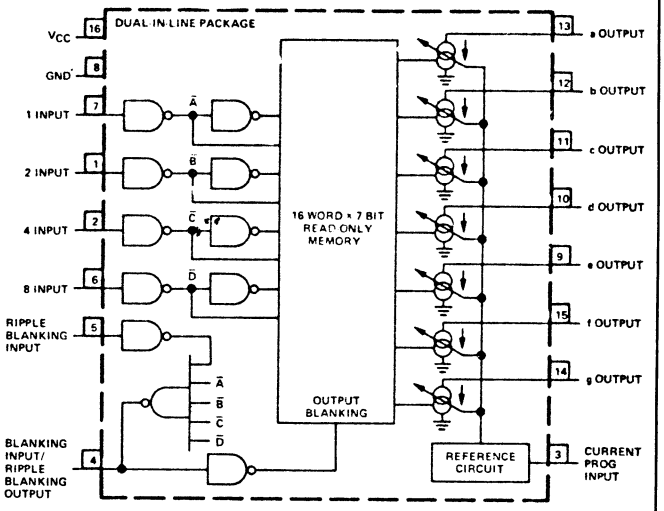
100000291

Decoder/Driver

PIN CONFIGURATION



BLOCK DIAGRAM



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100000291 (Cont.)

Decoder/Driver

TRUTH TABLE

	BCD INPUT					SEGMENT DRIVE OUTPUT							
DECIMAL OR FUNCTION	RBI	8	4	2	1	BI/ RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

NOTE: Logic "1" on all inputs and RBO is defined as the high TTL/DTL state. Logic "0" on outputs a – g is defined as the low or current sinking state (display on state). X is defined as "don't care" condition.

This device is a 7-segment gas discharge display cathode driver with BCD decoder.

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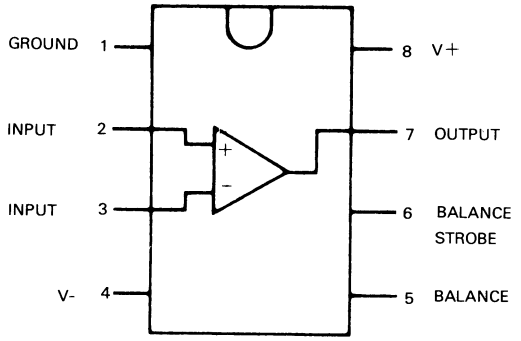
100000292

Voltage Comparator/Buffer

PIN CONFIGURATION



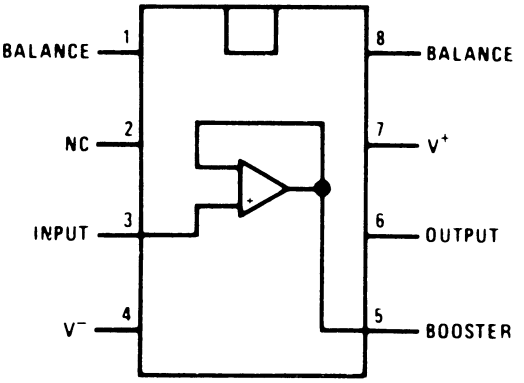
This voltage comparator is designed to operate over a wide range of supply voltages. Its output is compatible with RTL, DTL and TTL as well as MOS circuits.

Both the input and output can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'd.

100000293

Operational Amplifier

PIN CONFIGURATION



The 100000293 is a monolithic operational amplifier internally connected as a unity-gain non-inverting amplifier. The device has internal frequency compensation and provision for offset balancing.

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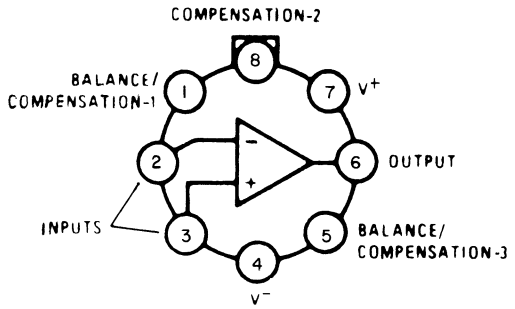
100000294

Operational Amplifier

PIN CONFIGURATION



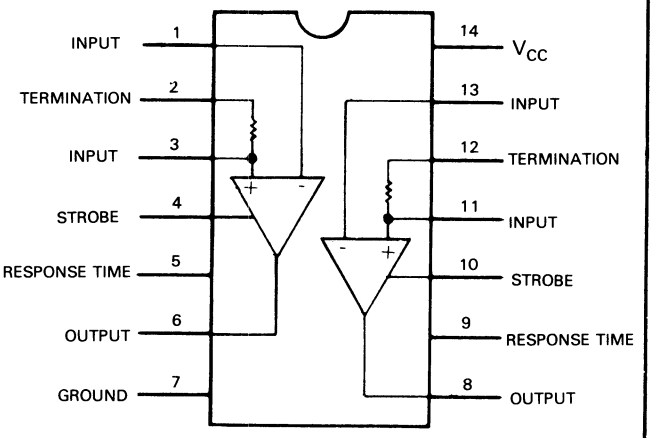
This precision high-speed operational amplifier has internal unity gain frequency compensation, which simplifies its application since no external components are necessary for operation. However, external frequency compensation may be added for optimum performance.

For inverting applications, feed-forward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. A single capacitor can be added to reduce the 0.1% settling time to under 1μs.

100000295

Dual Line Receiver

PIN CONFIGURATION



The 100000295 is a digital line receiver. The response time can be controlled with an external capacitor to eliminate noise spikes. The output is directly compatible with RTL, DTL or TTL integrated circuits.

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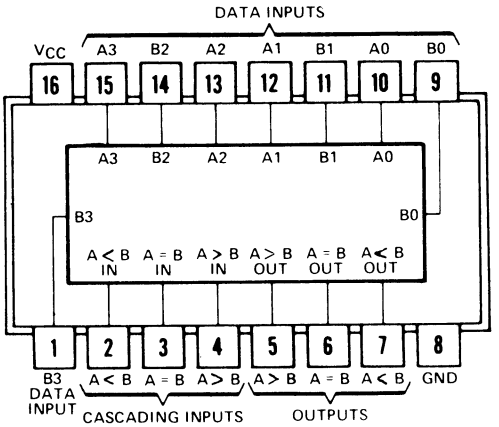
100000296

4-Bit Magnitude Comparator

PIN CONFIGURATION



FUNCTION TABLE

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B2	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = high level L = low level X = irrelevant

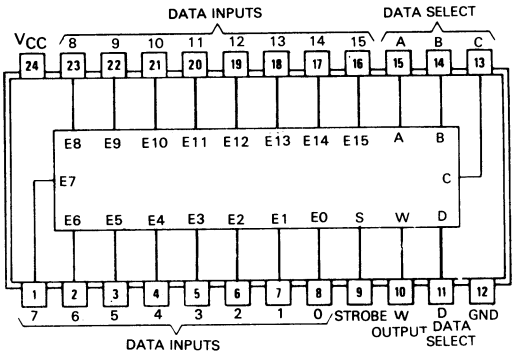
This four-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions for two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits are connected to the corresponding A>B, A<B, and A=B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A=B input.

NOTE *The 100000296 is a Schottky device.*

100000297

Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs					
Select				Strobe	Output
D	C	B	A	S	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

H = high level, L = low level, X = irrelevant.

$\overline{E0}$, $\overline{E1}$ .... $\overline{E15}$ = the complement of the level of the respective E input.

This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-sixteen data sources. The strobe input must be at a low logic level to enable this device.

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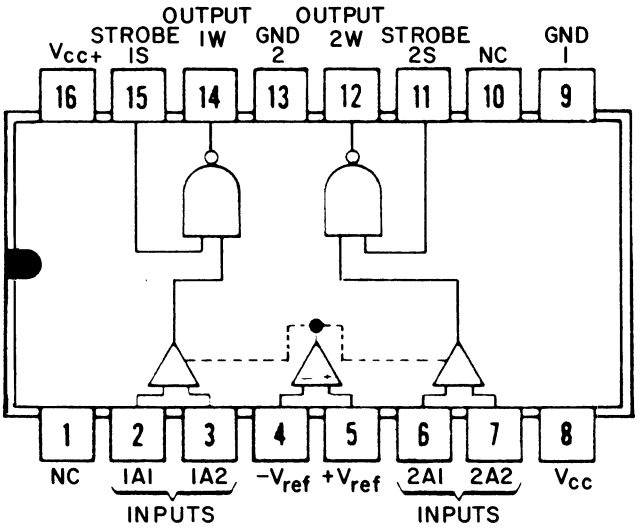
100000298 through 100000299

Dual Sense Amplifier

PIN CONFIGURATION



Positive logic: $W = \overline{AS}$

TRUTH TABLE

Inputs		Output
A	S	W
H	H	L
L	X	H
X	L	H

Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geqslant V_{Tmax}$	$V_{ID} \leqslant V_{Tmin}$	Irrelevant
S	$V_I \geqslant V_{IHmin}$	$V_I \leqslant V_{ILmax}$	Irrelevant

* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

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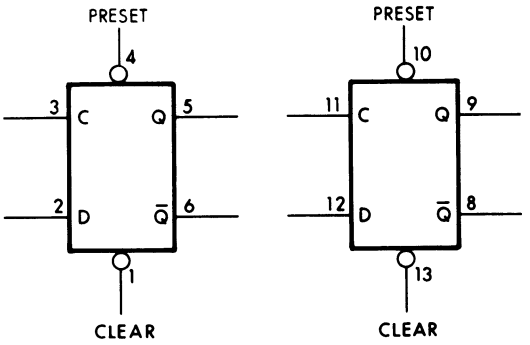
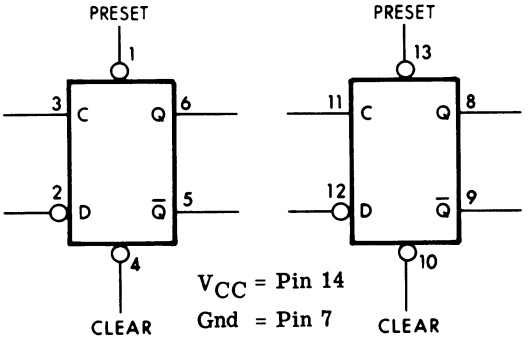
100000300

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



ALTERNATE PIN CONNECTIONS



V_{CC} = Pin 14
Gnd = Pin 7

FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

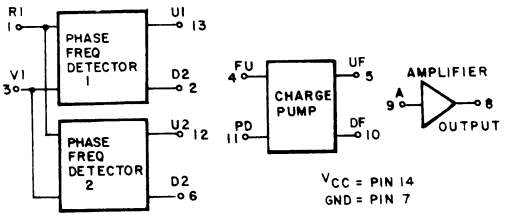
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000300 is a Schottky device.*

100000301

Phase-Frequency Detector

LOGIC DIAGRAM



FUNCTION TABLE

INPUT STATE	INPUT		OUTPUT			
	RI	VI	U1	D1	U2	D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

1. X indicates output state unknown
2. U1 and D1 outputs are sequential: i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational: i.e., they need only inputs shown to obtain outputs.

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

The 100000301 contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked loop applications.

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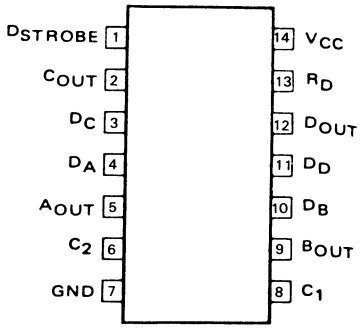
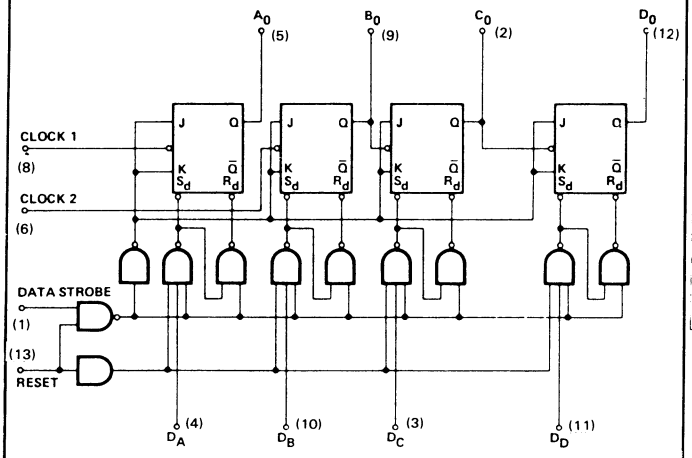
100000302

4-Bit 16-State Binary Counter/Storage Element

PIN CONFIGURATION



BLOCK DIAGRAM



This Schottky device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "0" at the strobe input will allow input data to associated outputs. A "0" at the reset will set all the outputs to zero.

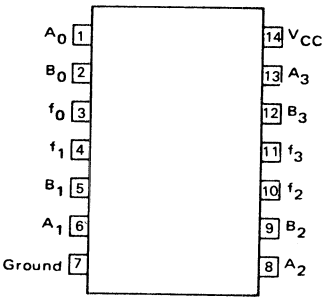
The counting operation is performed on the negative-going edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

NOTE: *This is a Schottky device.*

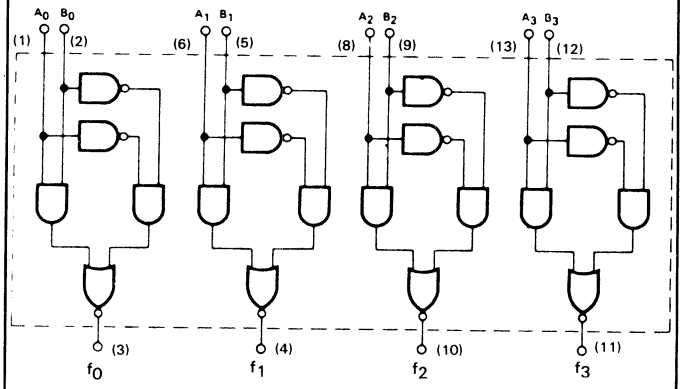
100000303

Quad Exclusive-OR Gate

PIN CONFIGURATION



BLOCK DIAGRAM



$$Y = A\bar{B} + \bar{A}B$$

TRUTH TABLE

A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

VCC = (14)
GND = (7)
( ) = Denotes Pin Numbers

NOTE *The 100000303 is a Schottky device.*

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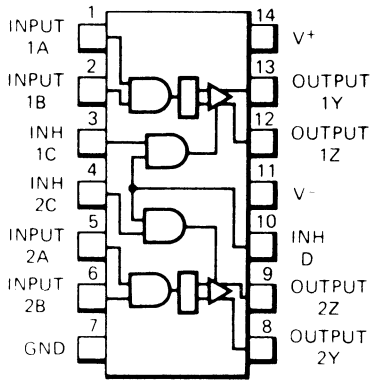
100000304

Dual Line Driver

PIN CONFIGURATION

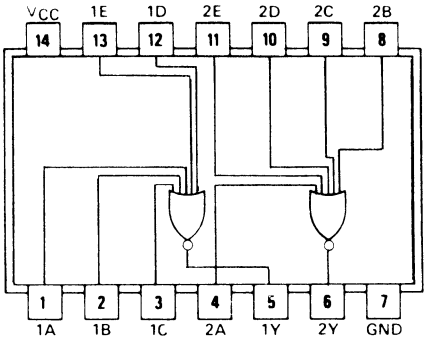


The 100000304 is a Dual Line Driver featuring independent channels with common supply voltage and ground terminals. The output current is nominally 12mA. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the terminals. The output current can be switched off by appropriate logic levels at the input terminals. The circuit also features an inhibit input that is common to both drivers. The common-mode voltage range of the driver outputs is -3V to +10V, which allows a common-mode voltage on the line without affecting the driver performance.

100000305

Dual 5-Input Positive-NOR Gate

PIN CONFIGURATION



Positive logic: $\overline{Y=A+B+C+D+E}$

NOTE *The 100000305 is a Schottky device.*

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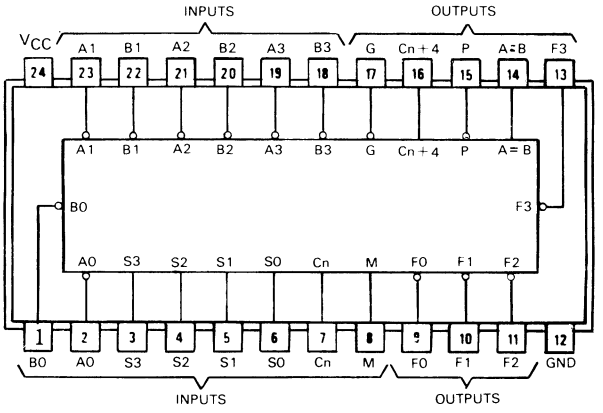
100000306

Arithmetic Logic Unit/Function Generator

PIN CONFIGURATION



Pin Designations

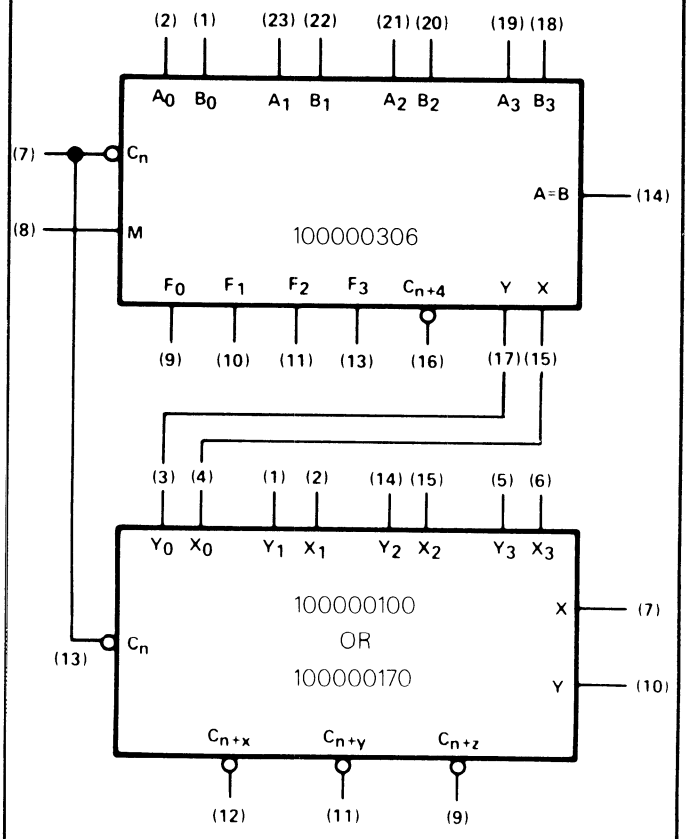
Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

Figure 1



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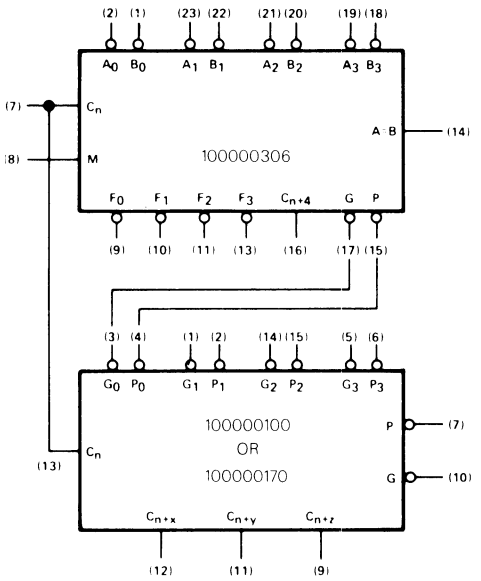
100000306 (Continued)

Figure 2



Selection S3 S2 S1 S0	Functions	Active-Low Data: C_n = L (no carry)	Active-Low Data: C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A Minus 1	F = A
L L L H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L L H L	F = $\overline{A}$ + B	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L H L H	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L H H L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H L L L	F = $\overline{AB}$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = $A\overline{B}$ Plus (A + B)	F = $A\overline{B}$ Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = $A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	F = $A\overline{B}$ Plus A	F = $A\overline{B}$ Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

Each bit is shifted to the next more significant position.

Selection S3 S2 S1 S0	M = H Logic Functions	Active-High Data M = L: Arithmetic Operations: C_n = H (no carry)	Active-High Data M = L: Arithmetic Operations: C_n = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A Plus 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L L H L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	F = $\overline{AB}$	F = A Plus AB	F = A Plus $\overline{AB}$ Plus 1
L H L H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L H H L	F = A $\oplus$ B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A$\overline{B}$	F = AB Minus 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H L L H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + B) Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

Each bit is shifted to the next more significant position

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

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100000306 (Continued)

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	A $\leqslant$ B	A $\geqslant$ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A $\geqslant$ B	A $\leqslant$ B

The 100000306 provides 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the 4 function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

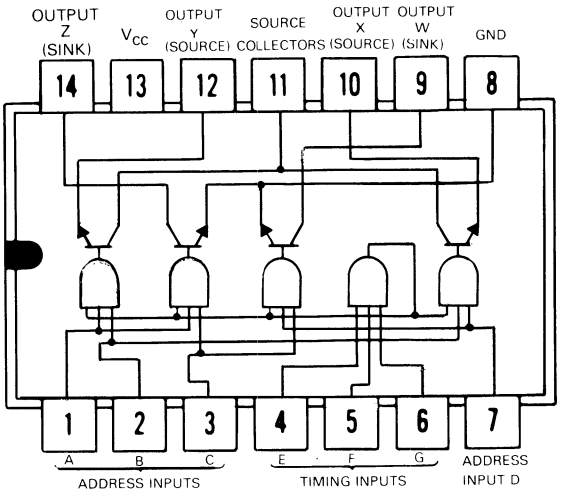
ALU Signal Designations

The 100000306 can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

100000307

Memory Driver with Decode Inputs

PIN CONFIGURATION



TRUTH TABLE

Inputs							Outputs			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	On	Off	Off	Off
0	1	0	1	1	1	1	Off	On	Off	Off
1	1	0	0	1	1	1	Off	Off	On	Off
1	0	1	0	1	1	1	Off	Off	Off	On
X	X	X	X	0	X	X	Off	Off	Off	Off
X	X	X	X	X	0	X	Off	Off	Off	Off
X	X	X	X	X	X	0	Off	Off	Off	Off

Notes:

X = Logical 1 or logical 0.

Not more than one output is allowed to be On at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

This monolithic memory driver with decode inputs is designed for use with magnetic memories. The device contains two 400 milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection; i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection; i.e., output switch-pair Y/Z or W/X, respectively.

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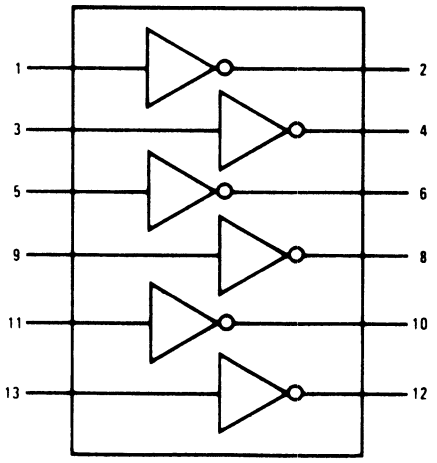
100000309

Hex Inverter

PIN CONFIGURATION



$Y = A$

V_{CC} = Pin 14

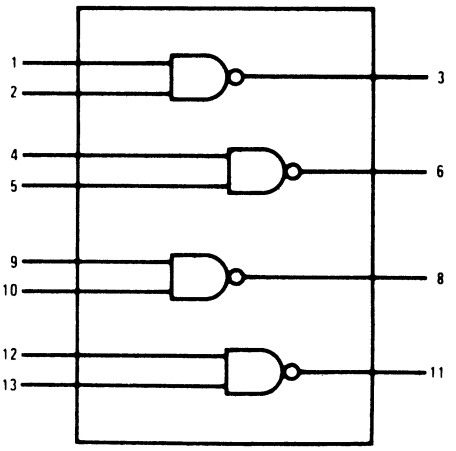
Gnd = Pin 7

NOTE: *This is a DTL device.*

100000310

Quad 2-Input NAND Gate

PIN CONFIGURATION



$Y = \overline{AB}$

V_{CC} = Pin 14

Gnd = Pin 7

NOTE: *This is a DTL device.*

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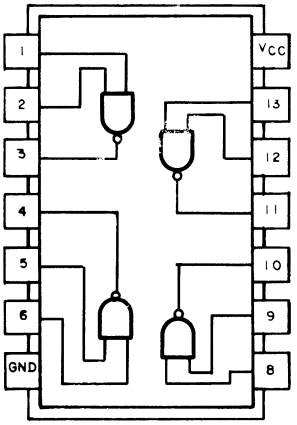
100000311

Quad 2-Input NAND Power Gate

PIN CONFIGURATION



$Y = \overline{AB}$

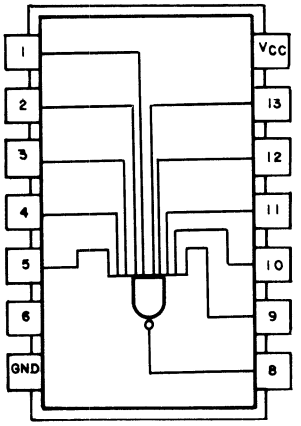
V_{CC} = Pin 14
Gnd = Pin 7

NOTE: *This device has diode transistor logic.*

100000312

10-Input NAND Gate

PIN CONFIGURATION



$Y = \overline{ABCDEFGHIJ}$

V_{CC} = Pin 14
Gnd = Pin 7

NOTE: *This device has diode transistor logic.*

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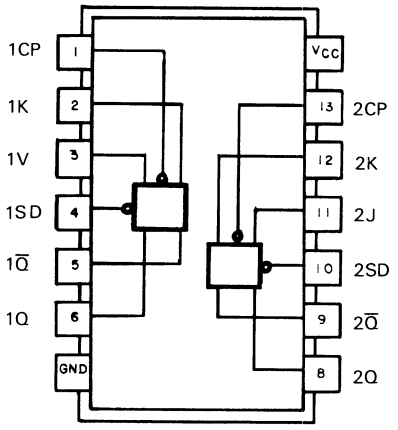
100000313

Dual J-K Flip-Flop with Individual Clocks and Presets

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

TRUTH TABLE

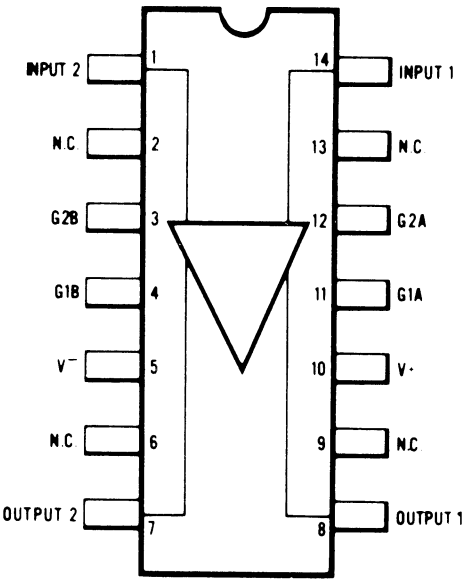
t_n		t_n+1
J	K	Q
L	L	Qn
H	H	H
H	H	$\overline{Q}n$

This device has diode transistor logic (DTL)

100000314

Differential Video Amplifier

PIN CONFIGURATION



This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

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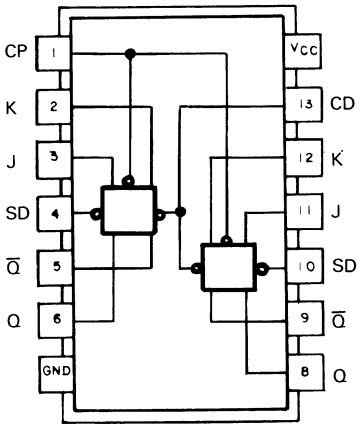
100000316

Dual J-K Flip-Flop with Common Clocks and Clears

PIN CONFIGURATION



TRUTH TABLE

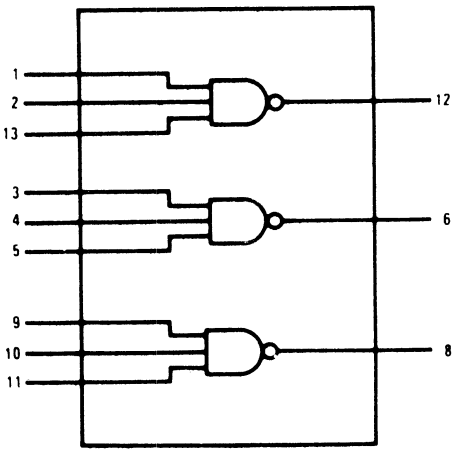
t_n		t_n+1
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

NOTE: *This device has diode transistor logic (DTL)*

100000317

Triple 3-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

$Y = \overline{ABC}$

NOTE: *This is a DTL device.*

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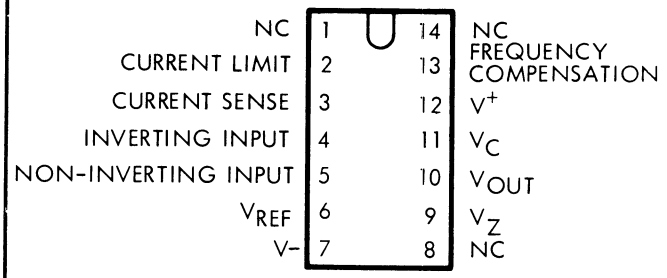
100000318

Precision Voltage Regulator

PIN CONFIGURATION

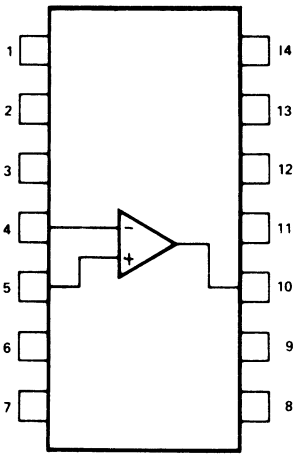


The 100000318 is a monolithic voltage regulator, consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown

100000319

High Performance Operational Amplifier

PIN CONFIGURATION



This device is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and temperature stability.

The device is short-circuit protected and allows for nulling of offset voltage.

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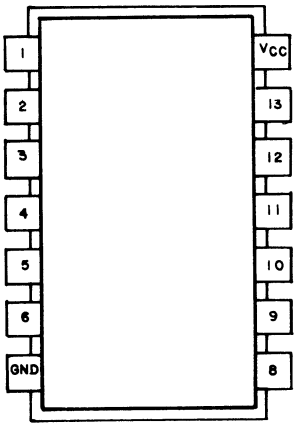
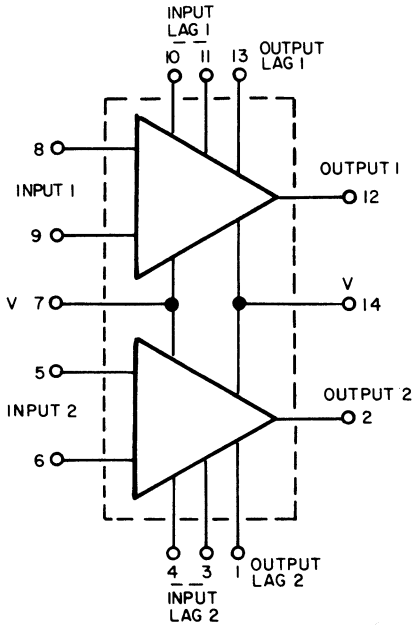
100000320

Monolithic Dual Operational Amplifier

PIN CONFIGURATION



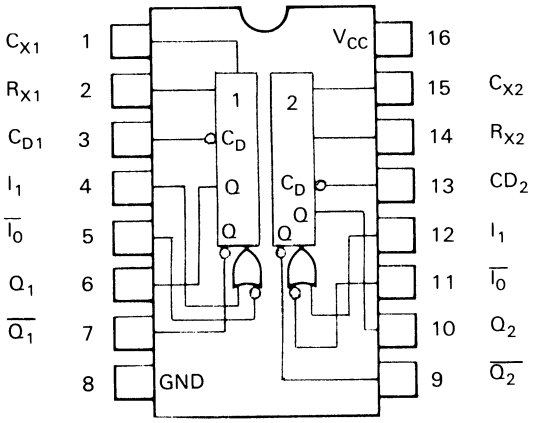
LOGIC DIAGRAM



100000321

Dual Retriggerable Resettable Monostable Multivibrator

PIN CONFIGURATION



TRUTH TABLE

Pin Numbers			
5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geq V_{IH}$

L = LOW Voltage Level $\leq V_{IL}$

X = Don't Care

H→L = HIGH to LOW Voltage Level transition

L→H = LOW to HIGH Voltage Level transition

The Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components.

This device has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the device and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW.

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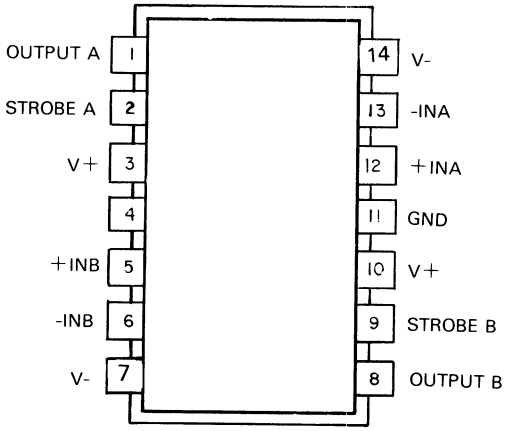
100000322

Dual Differential Comparator

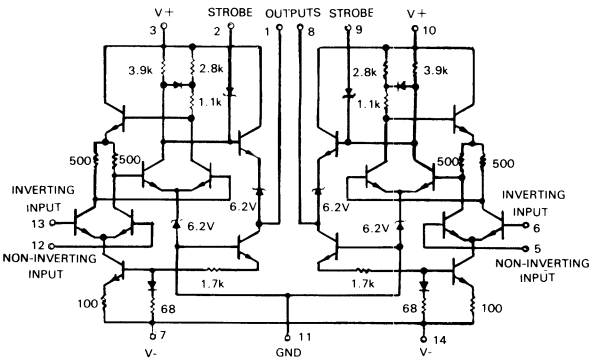
PIN CONFIGURATION



PIN DESIGNATIONS

V+ = Pin 3 and Pin 10
V- = Pin 7 and Pin 14
Gnd = Pin 11

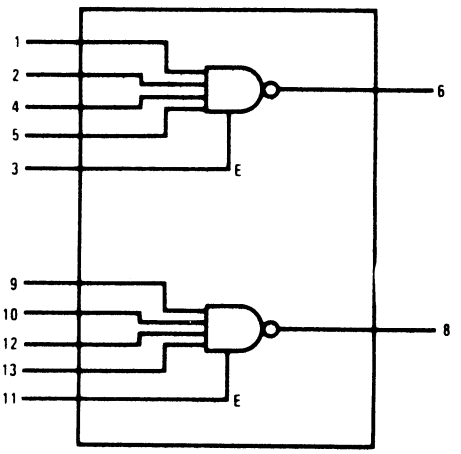
LOGIC DIAGRAM



100000323

Dual 4-Input NAND Power Gate with Expander

PIN CONFIGURATION



V_{CC} = Pin 14
Gnd = Pin 7

$Y = \overline{ABCDE}$

NOTE: *This is a DTL device.*

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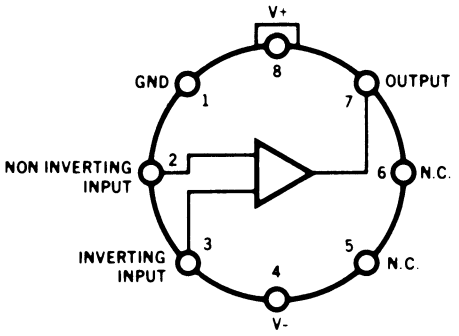
100000324

High Speed Differential Comparator

PIN CONFIGURATION



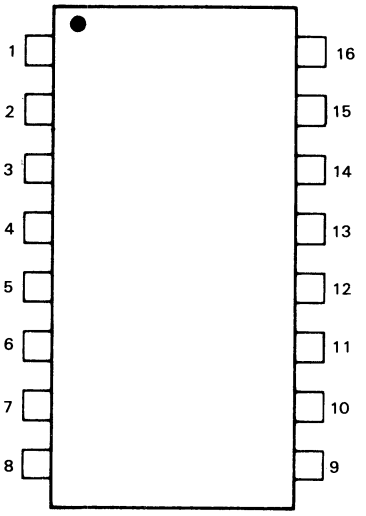
Note: Pin 4 connected to case.

The 100000324 is a differential voltage comparator intended for applications requiring high accuracy fast response times. Constructed on a single silicon chip, the device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters,a memory sense amplifier or a high-noise immunity line receiver.

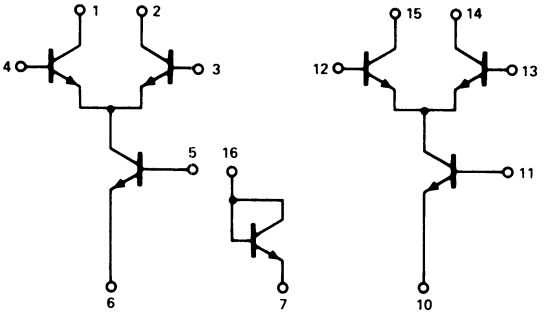
100000325

Dual Differential Amplifier

PIN CONFIGURATION



LOGIC DIAGRAM



The 100000325 is a monolithic dual high frequency differential amplifier with associated constant current source transistors and biasing diode. It is useful from DC to 100 MHz. The circuit arrangement provides for connection as two completely independent emitter coupled (differential) or cascade amplifiers. The bias diode allows stabilization of the current source currents over a large temperature range.

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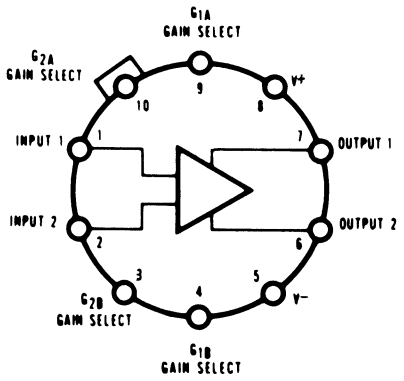
100000326

Differential Video Amplifier

PIN CONFIGURATION

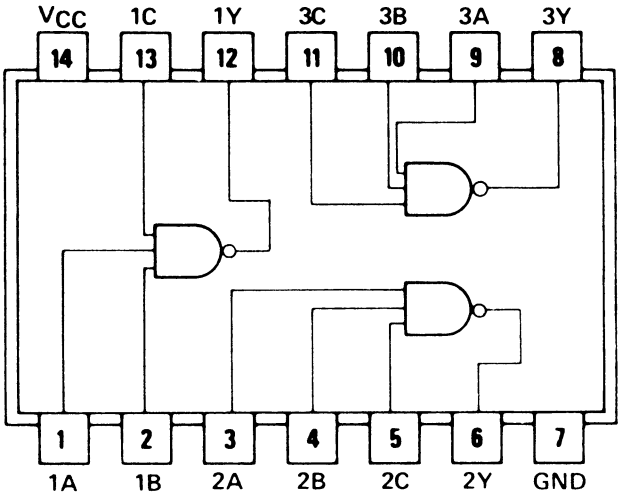


This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

100000327

Triple 3-Input Positive-NAND Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{ABC}$

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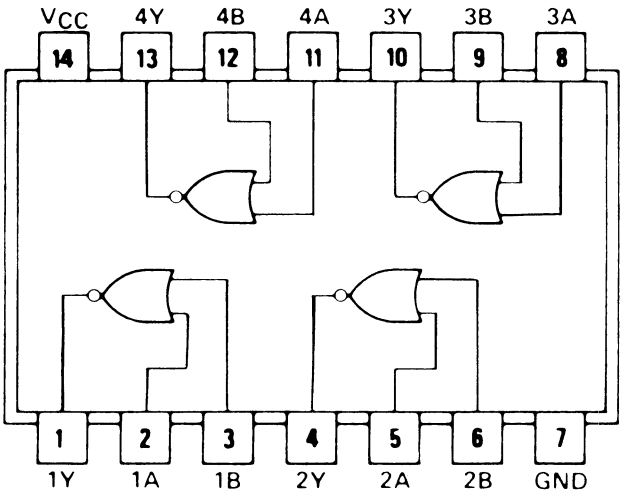
100000330

Quad 2-Input Positive-NOR Gate

PIN CONFIGURATION

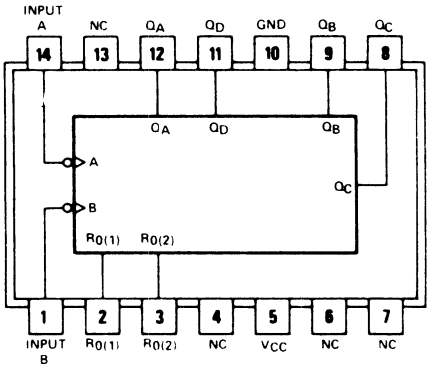


Positive logic: $Y = \overline{A+B}$

100000331

4-Bit Binary and Decade Counter

PIN CONFIGURATION



The 100000331 is a monolithic counter containing four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight. This counter has a gated zero reset.

Notes:

1. The B input is connected to the Q_A output.
2. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

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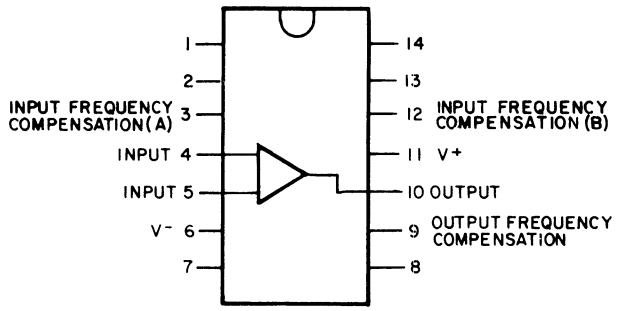
100000333

Operational Amplifier

PIN CONFIGURATION



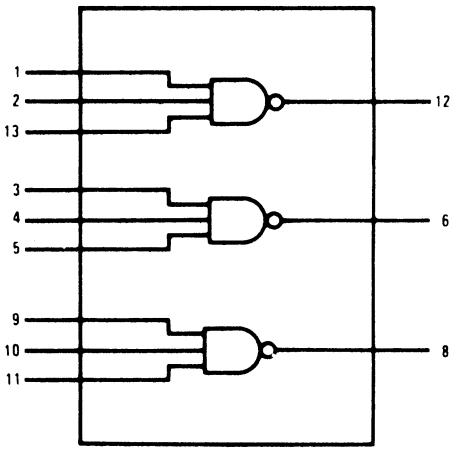
The 100000333 is a monolithic operational amplifier. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. The class B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Compensation can be tailored to optimize high-frequency performance for any gain setting.

100000334

Triple 3-Input NAND Gate

PIN CONFIGURATION



V_{CC} = Pin 14

Gnd = Pin 7

$Y = \overline{ABC}$

NOTE: *This is a DTL device.*

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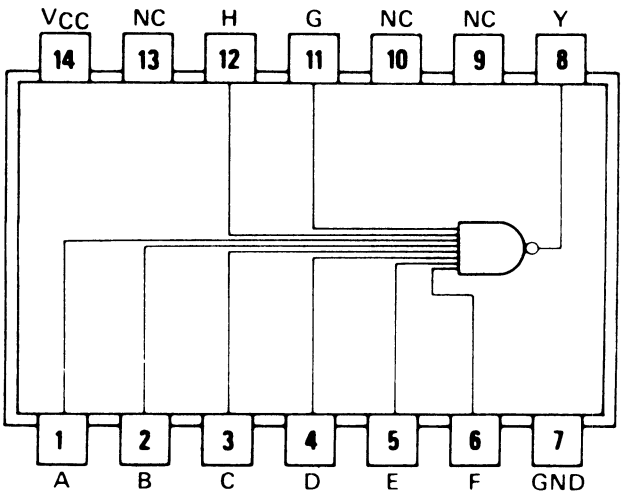
100000337

8-Input Positive-NAND Gate

PIN CONFIGURATION

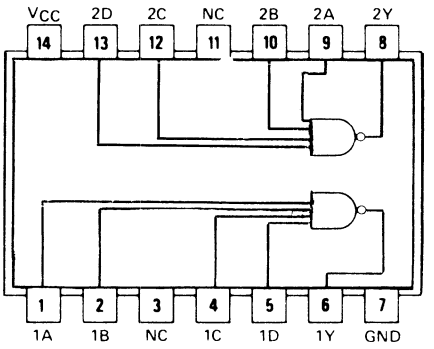


Positive logic: $Y = \overline{ABCDEFGH}$

100000338

Dual 4-Input Positive-NAND Buffer

PIN CONFIGURATION



Positive logic $Y=\overline{ABCD}$

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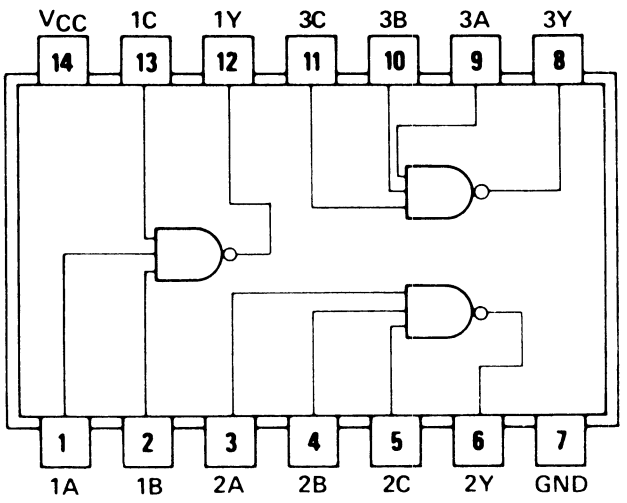
100000339

Triple 3-Input Positive-NAND Gate

PIN CONFIGURATION

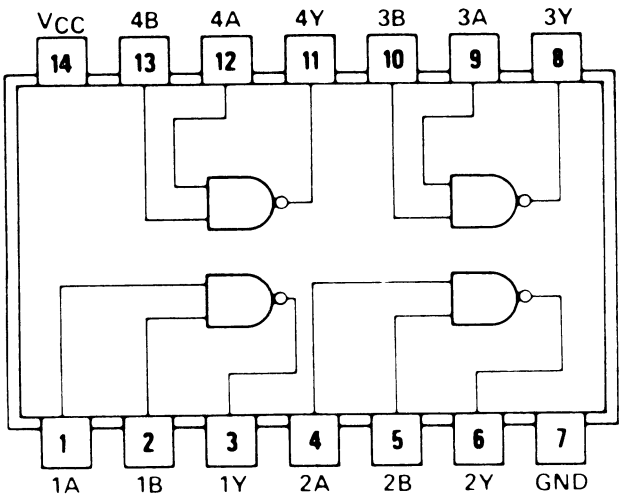


Positive logic: $Y = \overline{ABC}$

100000340

Quad 2-Input Positive-NAND Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

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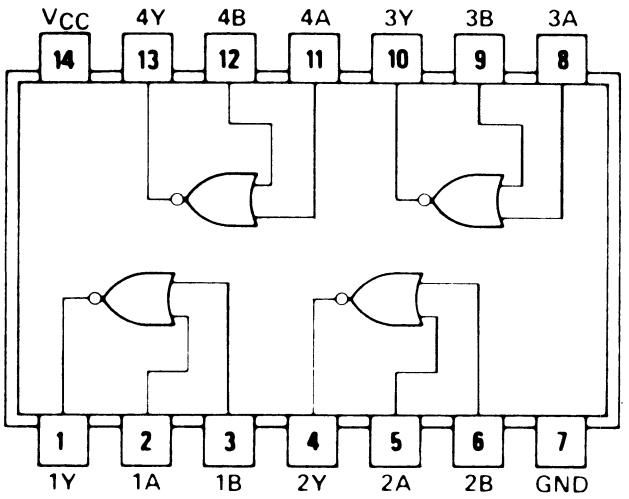
100000341

Quad 2-Input Positive-NOR Gate

PIN CONFIGURATION

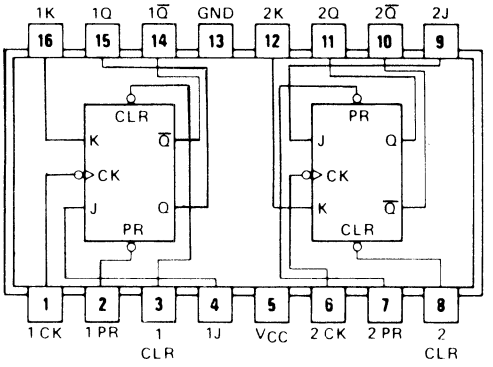


Positive logic: $Y = \overline{A+B}$

100000342

Dual J-K Flip-Flops with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

*This configuration is nonstable; that is it will not persist when preset and clean inputs return to their inactive (high) state.

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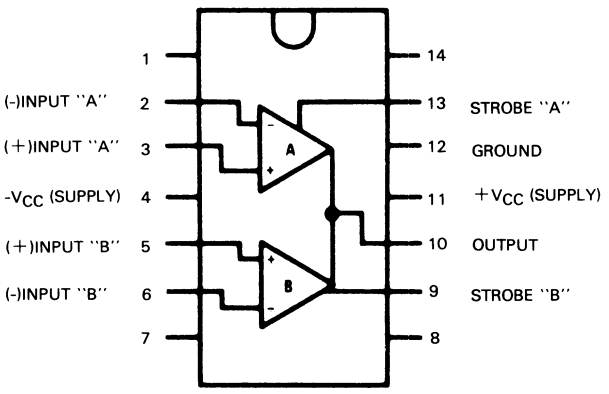
100000343

Dual Comparator

PIN CONFIGURATION



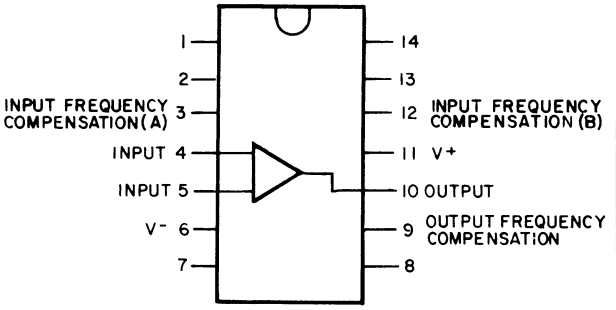
This device is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided.

100000344

Operational Amplifier

PIN CONFIGURATION



The 100000344 is a monolithic operational amplifier. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. The class B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Compensation can be tailored to optimize high-frequency performance for any gain setting.

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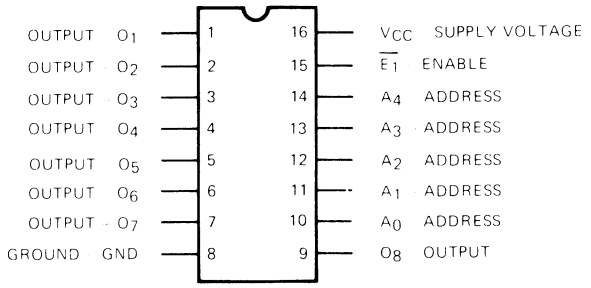
100000347 through 100000353

256-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This device is a field programmable, 256-bit, DTL and TTL compatible, bipolar read only memory.

The three-state output of this device provides a low impedance driver Q_2 for driving capacitance on the memory output; no pullup resistor is required. When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. In a system enviornment, up to 21 memory outputs of the read only memory can be connected to a common bus. All of the devices, except one, are placed in the high impedance state. The selected device is enabled and has the characteristics of a TTL totem pole output.

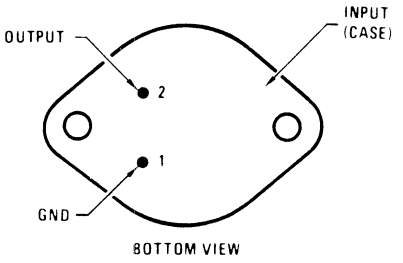
Memory Operation

The memory is addressed with inputs A_0 through A_4 which select one of 32 words. To enable the outputs for a readout, enable E_1 must be low. If the enable is high, the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

100000354

-12V, 1A, 20W, Voltage Regulator

PIN CONFIGURATION



The 100000354 is a three-terminal negative regulator. It has fixed output voltage of -12V and needs only one external component, a compensation capacitor at the output.

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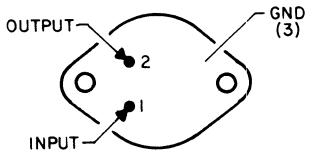
100000355

3-Terminal Positive Regulator

PIN CONFIGURATION



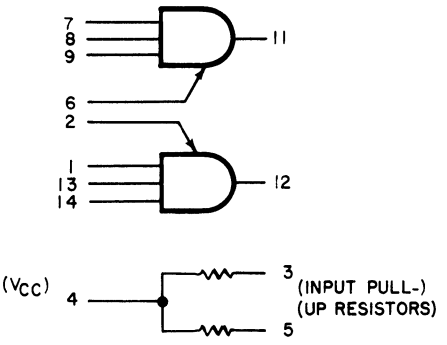
BOTTOM VIEW

The 100000355 Positive Regulator provides over 1.0 Amp of output current if adequate heat sinking is provided. Current limiting keeps the peak output current to a safe value. Safe area protection limits internal power dissipation. The thermal shutdown circuit prevents the IC from overheating when power dissipation exceeds the capacity of the heat sink.

100000356 and 100000357

Dual Pulse Shaper-Delay AND Gate

LOGIC DIAGRAM



Pin Designations

V_{CC} = Pin 4

Gnd = Pin 10

Y = ABCD

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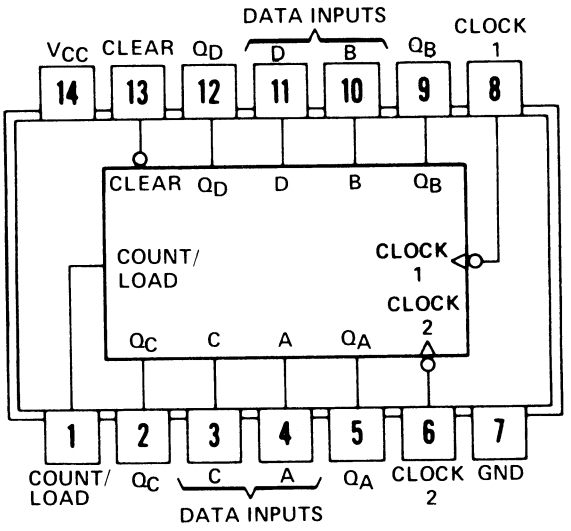
100000358

35-MHz Presettable Decade Counter

PIN CONFIGURATION



The 100000358 is a high-speed monolithic counter consisting of four d-c coupled master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter. The outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the inputs independent of the state of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count load is high and the clock inputs are inactive.

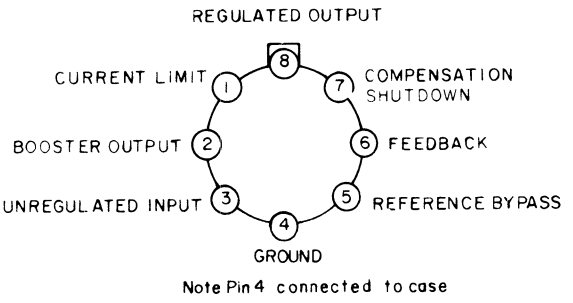
The 100000358 will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects. The circuits are compatible with most TTL and DTL logic families.

100000359

+4.5V -40V, 300mA Voltage Regulator

PIN CONFIGURATION



Note Pin 4 connected to case

The 100000359 is a positive voltage regulator. The design of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation.

This regulator also features fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating.

Note:

The 100000359 is specified for operation from -25°C to 85°C.

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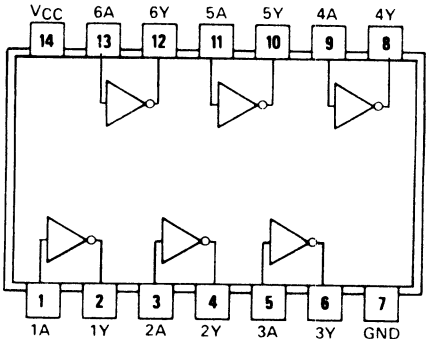
100000360

Hex Inverter

PIN CONFIGURATION

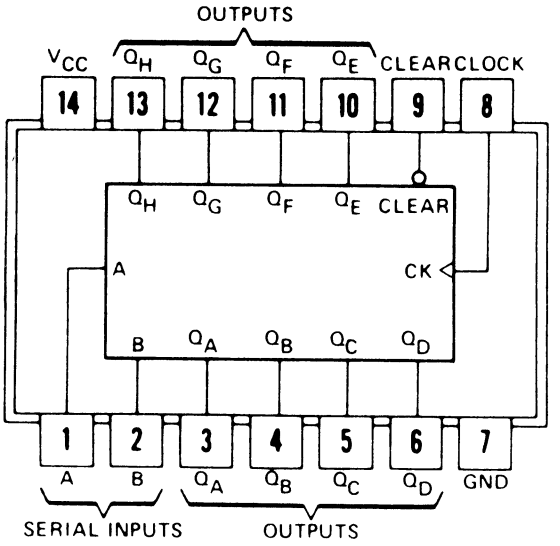


$Y = \overline{A}$

100000362

8-Bit Parallel-Out Serial-Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock, indicates a one-bit shift.

The 100000362 features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop.

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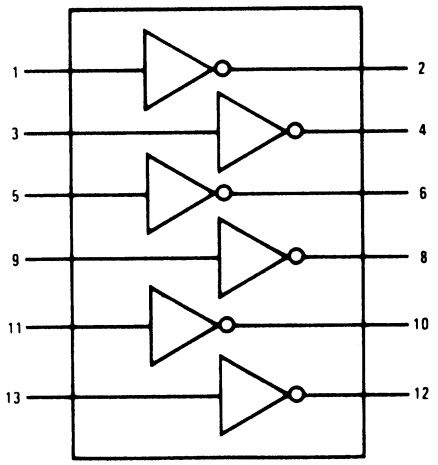
100000363

Hex Inverter

PIN CONFIGURATION



V_{CC} = Pin 14

Gnd = Pin 7

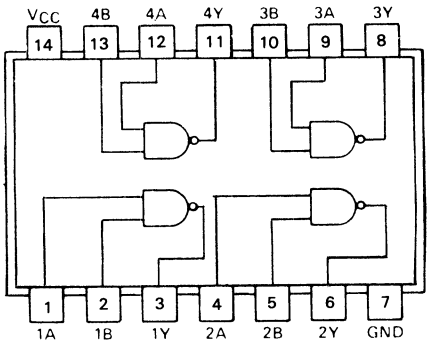
$Y = \overline{A}$

NOTE: *The 100000363 is a DTL device.*

100000364

Quad 2-Input Positive-NAND Gate with Open Collector Outputs

PIN CONFIGURATION



$Y = \overline{AB}$

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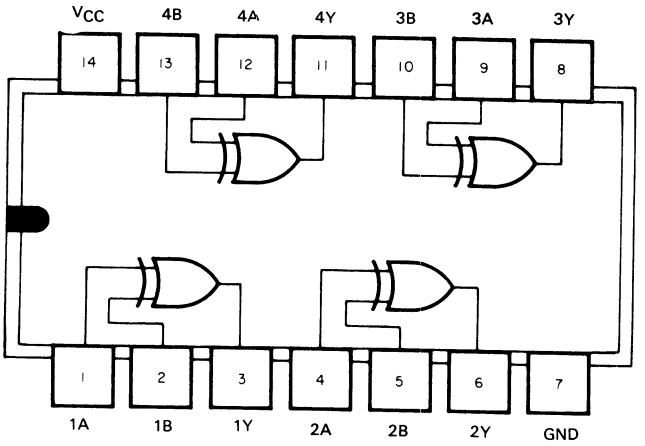
100000365

Quad 2-Input Exclusive-OR Gate

PIN CONFIGURATION



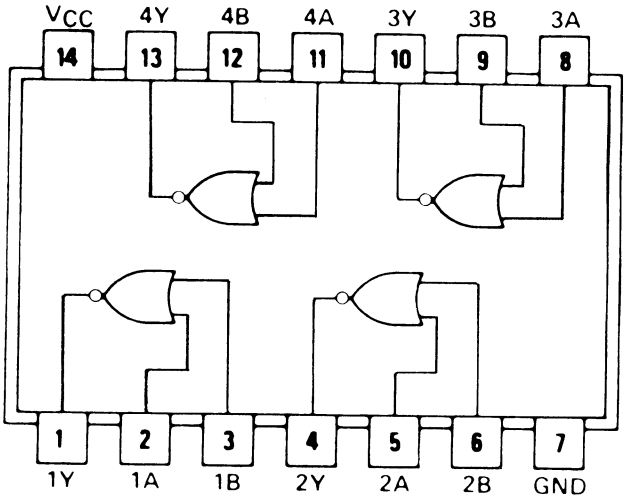
$$Y = \overline{A}B + A\overline{B}$$

NOTE *The 100000365 is a Schottky device.*

100000366

Quad 2-Input Positive-NOR Gate

PIN CONFIGURATION



NOTE *The 100000366 is a Schottky device.*

$$Y = \overline{A + B}$$

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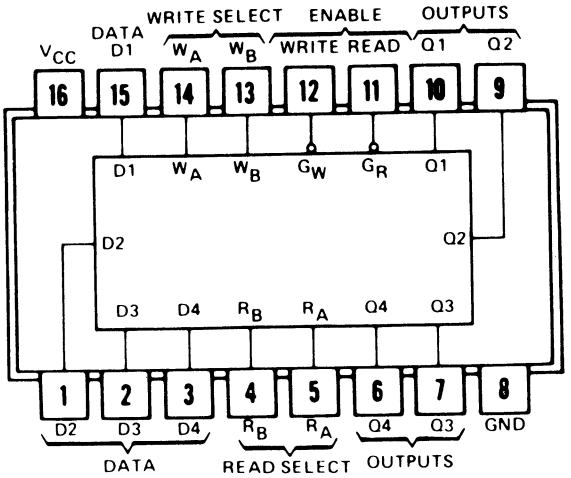
100000367

4-By-4 Register Files with 3-State Outputs

PIN CONFIGURATION



WRITE FUNCTION TABLE

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES: A. H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_0 = the level of Q before the indicated input conditions were established.

D. W0B1 = The first bit of word 0, etc.

The 100000367 16-bit TTL register file incorporates the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and seperate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form; that is, is a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

All inputs except read enable and write enable are buffered to lower the drive requirements. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The 100000367 is characterized for operation from 0 °C to 70 °C.

NOTE *The 100000367 is a low power Schottky device.*

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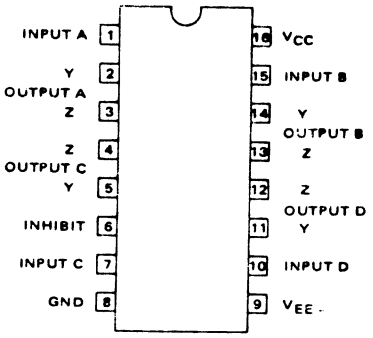
100000369

Quad Line Driver with Common Inhibit Input

PIN CONFIGURATION



TRUTH TABLE

(positive logic)

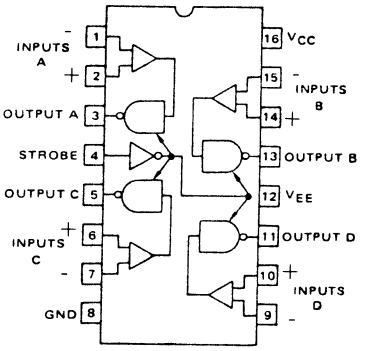
LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

100000370

Quad Line Receiver with 3-State Strobe Input and Open Collector Outputs

PIN CONFIGURATION



TRUTH TABLE

INPUT	STROBE	OUTPUT
$V_{ID} \geqslant +25mV$	L	off
	H	off
$-25mV \leqslant V_{ID} \leqslant +25mV$	L	I
	H	off
$V_{ID} \leqslant -25mV$	L	L
	H	off

L = Low Logic State

H = High Logic State

Z = Third (High Impedance) State

I = Indeterminate State

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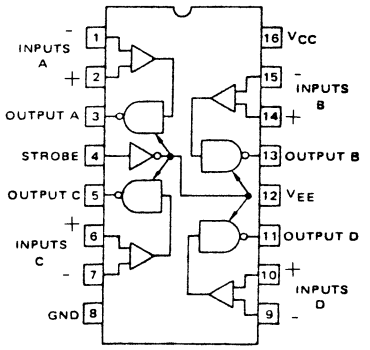
100000371

Quad Line Receiver with 3-State Strobe Input

PIN CONFIGURATION



TRUTH TABLE

INPUT	STROBE	OUTPUT
$V_{ID} \geqslant +25mV$	L	off
	H	off
$-25mV \leqslant V_{ID} \leqslant +25mV$	L	I
	H	off
$V_{ID} \leqslant -25mV$	L	L
	H	off

L = Low Logic State

H = High Logic State

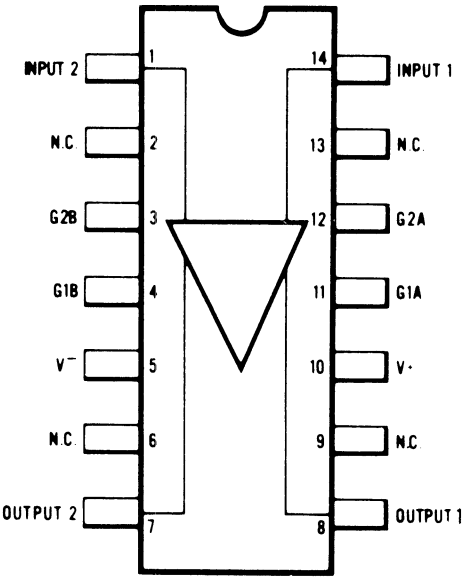
Z = Third (High Impedance) State

I = Indeterminate State

100000372

Differential Video Amplifier

PIN CONFIGURATION



This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

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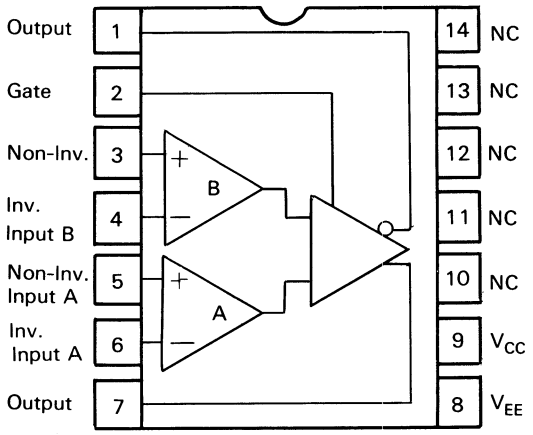
100000373

Gate Controlled 2-Channel Input Wideband Amplifier

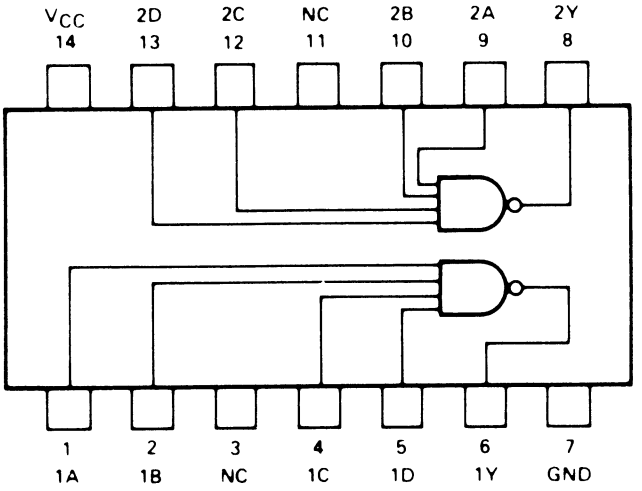
PIN CONFIGURATION



100000374

Dual 4-Input Positive-NAND Gate

PIN CONFIGURATION



$Y = \overline{ABCD}$

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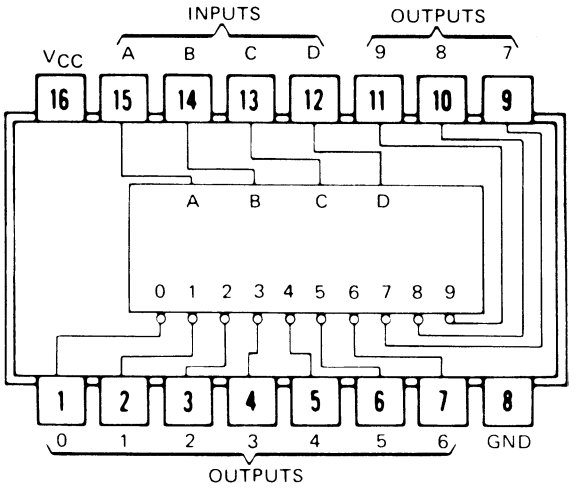
100000375

BCD To Decimal Decoder

PIN CONFIGURATION



TRUTH TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

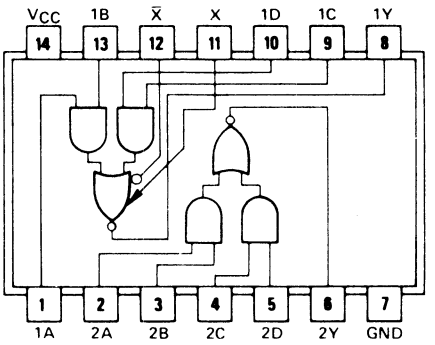
H = high level, L = low level

The 100000375 is a monolithic decimal decoder consisting of eight inverters and ten four-input Nand gates. The inverters are connected in pairs to make BCD input data available for decoding by the Nand gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions. This device features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

100000376

Dual 2-Wide 2-Input AND-OR-INVERT Gate (One Gate Expandable)

PIN CONFIGURATION



Positive logic: $1Y = \overline{AB + CD + X}$

$2Y = \overline{AB + CD}$

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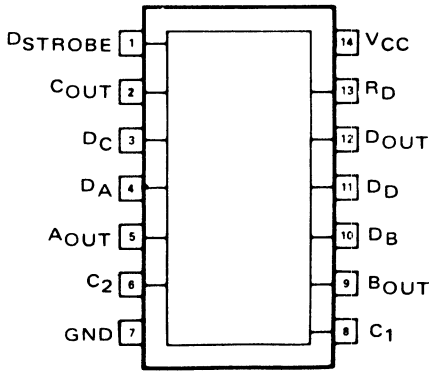
100000377

Divide-By-12 Counter/Storage Element

PIN CONFIGURATION



TRUTH TABLE

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*Connected for Divide-by-Twelve operation (output A connected to CP2)

The 100000377 Divide-by-Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

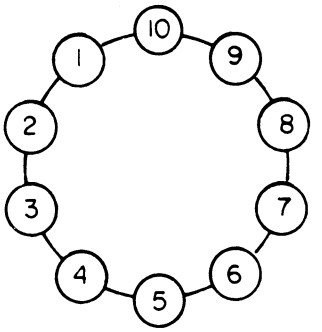
The 100000377 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, this device is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset funcitons are asynchronous with respect to the clock.

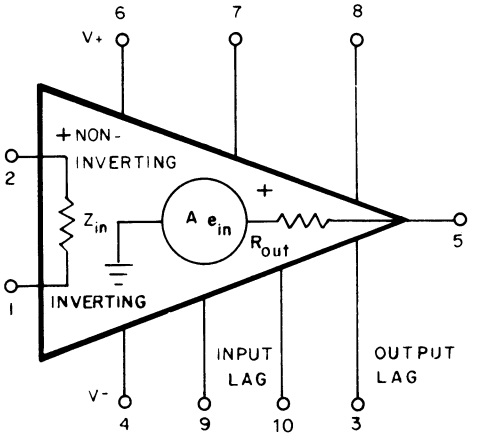
100000378

Monolithic Operational Amplifier

PIN CONFIGURATION



LOGIC DIAGRAM



The 100000378 is a monolithic operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

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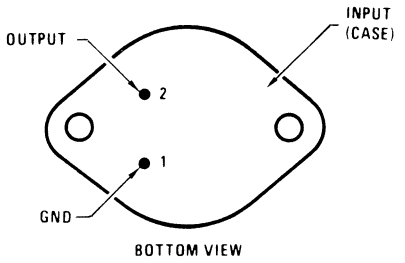
100000379

-5V, 1.5A, 20W, 5% Voltage Regulator

PIN CONFIGURATION

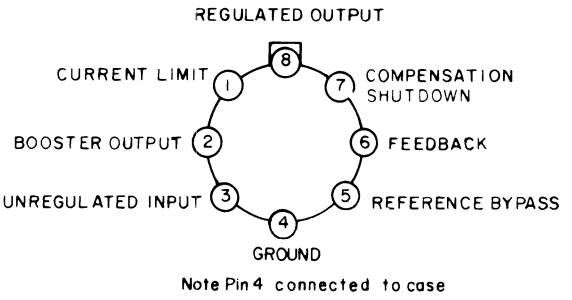


The 100000379 is a three-terminal negative regulator. It has a fixed output voltage of -5V and needs only one external component, a compensation capacitor at the output.

100000380

+4.5 -30V, 300mA
Positive Voltage Regulator

PIN CONFIGURATION



The 100000380 is a positive voltage regulator. The design of the biasing circuitry removes any minimum load current and at the same time reduces standby current drain, permitting higher voltage operation.

This regulator also features fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating.

Note:

The 100000380 is specified for operation from 0 deg. to 70 deg. C and for output voltages to 30V.

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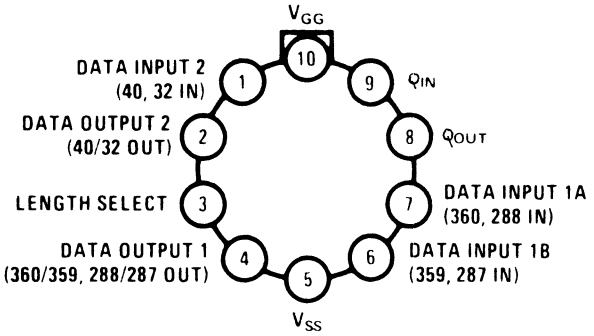
100000381

Dynamic Shift Register

PIN CONFIGURATION

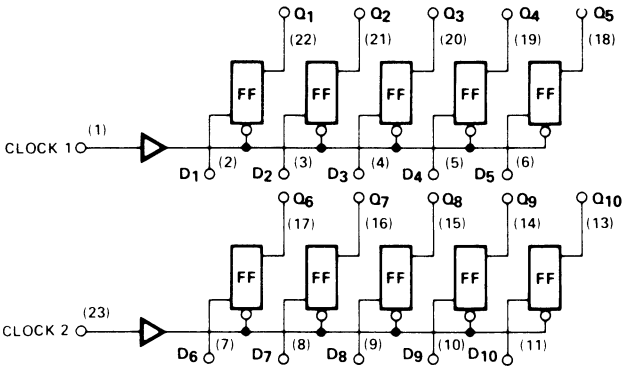


The 100000381 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. This device features DTL/TTL compatibility.

100000382

Buffer Registers

BLOCK DIAGRAM



V_{CC} = Pin 24

Gnd = Pin 12

TRUTH TABLE

D_n	Q_{n+1}
1	1
0	0

n is time prior to clock.
n+1 is time following clock.

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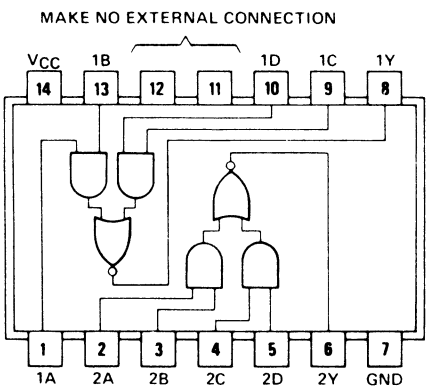
100000383

Dual 2-Wide 2-Input AND-OR-INVERT Gate

PIN CONFIGURATION

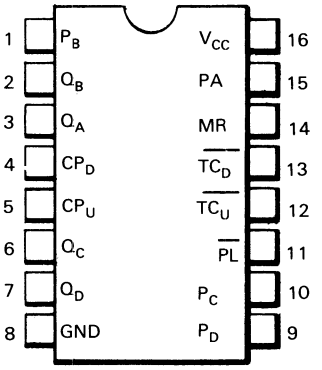


Positive logic: $Y=\overline{AB+CD}$

100000384

Up/Down Decade Counter

PIN CONFIGURATION



MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

These counters can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table.

Counting is synchronous, with the outputs changing state after the Low to High transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is High. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are Low simultaneously.) All counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence.

LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

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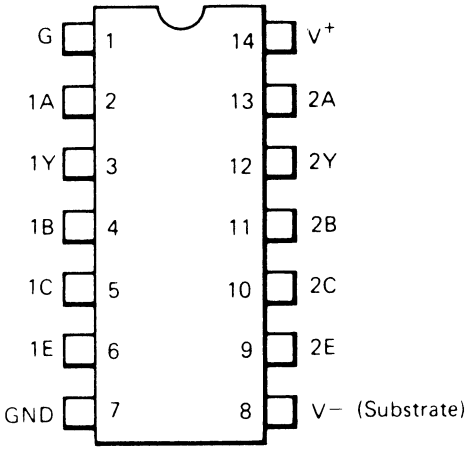
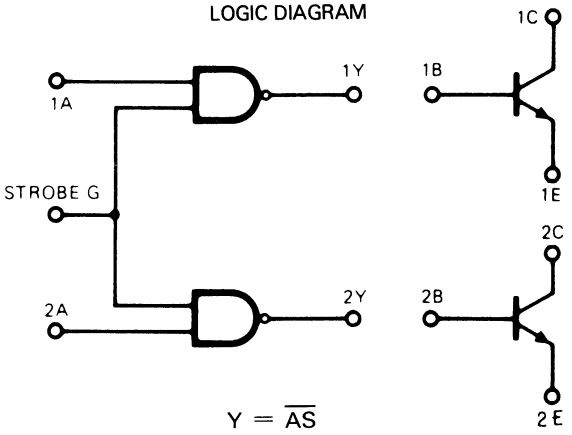
100000385

Dual Peripheral Driver

PIN CONFIGURATION



LOGIC DIAGRAM

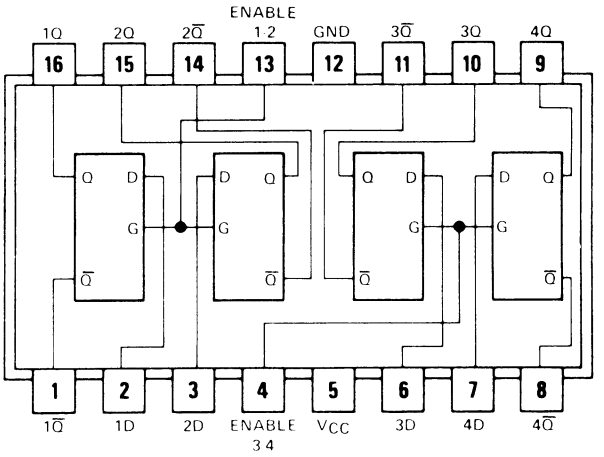


$Y = \overline{AS}$

100000387

4-Bit Bistable Latches

PIN CONFIGURATION



FUNCTION TABLE

(Each Latch)

Inputs		Ouputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level; L = low level; X = irrelevant.
Q_0 = the level of Q before the high-to-low transition of G.

These latches are suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

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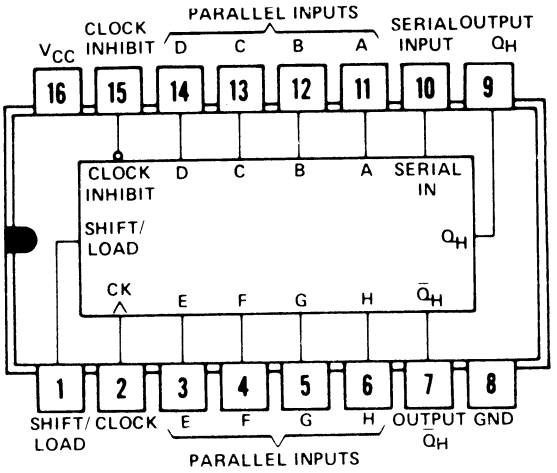
100000389

Parallel-Load 8-Bit Shift Register

PIN CONFIGURATION



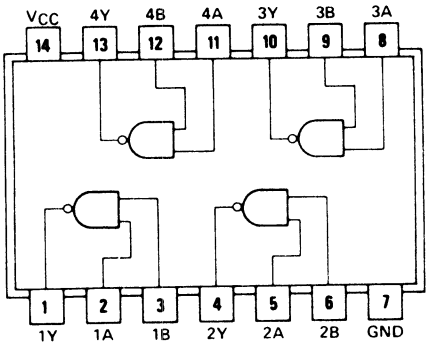
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

100000390

Quad 2-Input Positive-NAND Gate with Open Collector Outputs

PIN CONFIGURATION



$Y = \overline{AB}$

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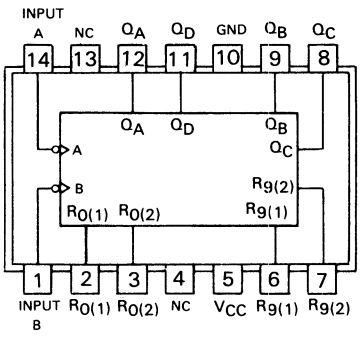
100000391

Decade Counter

PIN CONFIGURATION



The 100000391 contains 4 master-slave flip-flops and additional gating to provide a divide-by-2 counter and a 3-stage binary counter for which the count cycle length is divide-by-5.

This counter has a gated zero reset and has gated set-to-9 inputs for use in BCD nine's complement applications.

Notes:

1. The B input is connected to the QA output.

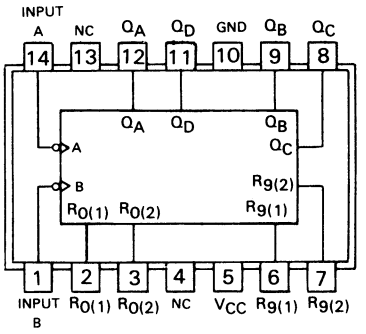
2. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

3. A symmetrical divide-by-10 count can be obtained by connecting the QD output to the A input and applying the input count to the B input which gives a divide-by-10 square wave at output QA.

100000392

4-Bit Binary Counter

PIN CONFIGURATION



The 100000392 contains 4 master-slave flip-flops and additional gating to provide a divide-by-2 counter and a 3-stage binary counter for which the count cycle length is divide-by-8. It has a gated zero reset.

Notes:

1. The B input is connected to the QA output.

2. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

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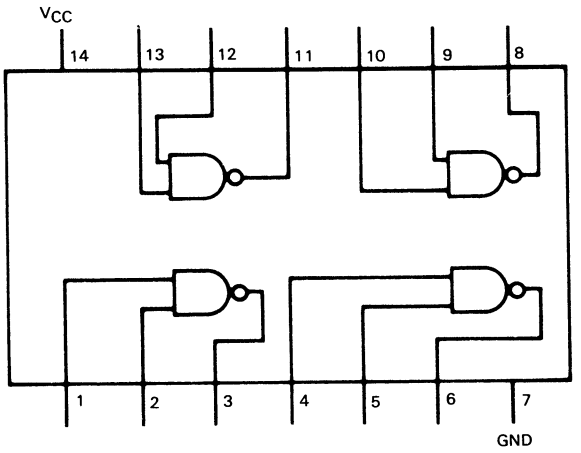
100000393

Quad 2-Input TTL-MOS Interface Gate

PIN CONFIGURATION

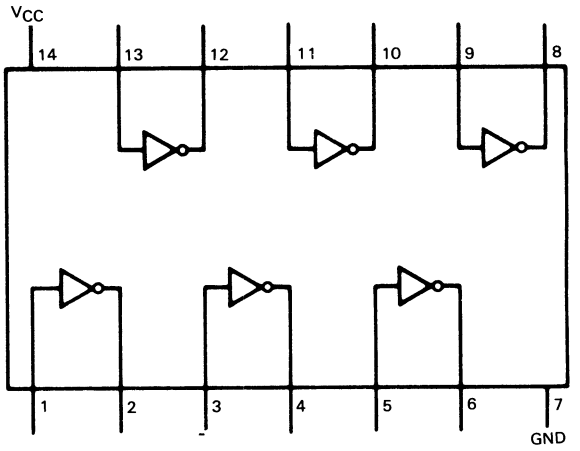


$Y = \overline{AB}$

100000394

TTL-MOS Hex Inverter

PIN CONFIGURATION



$Y = \overline{A}$

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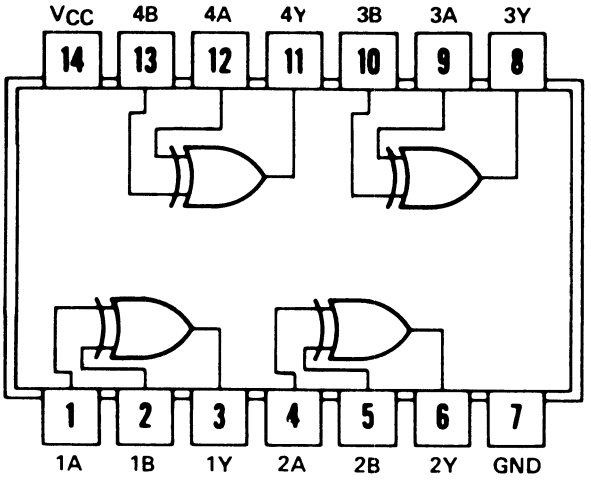
100000399

Quad 2-Input Exclusive-OR Gate with Open Collector Output

PIN CONFIGURATION



Positive logic: $Y=A \oplus B = \overline{A}B + A\overline{B}$

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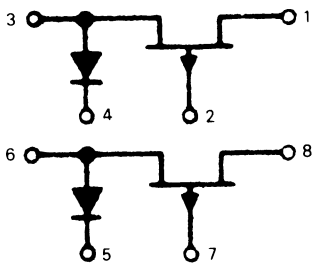
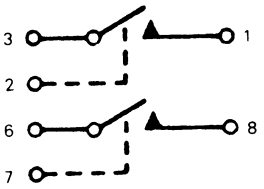
100000400

Dual SPST Analog Switch

SCHEMATIC DIAGRAM
8-PIN DIP



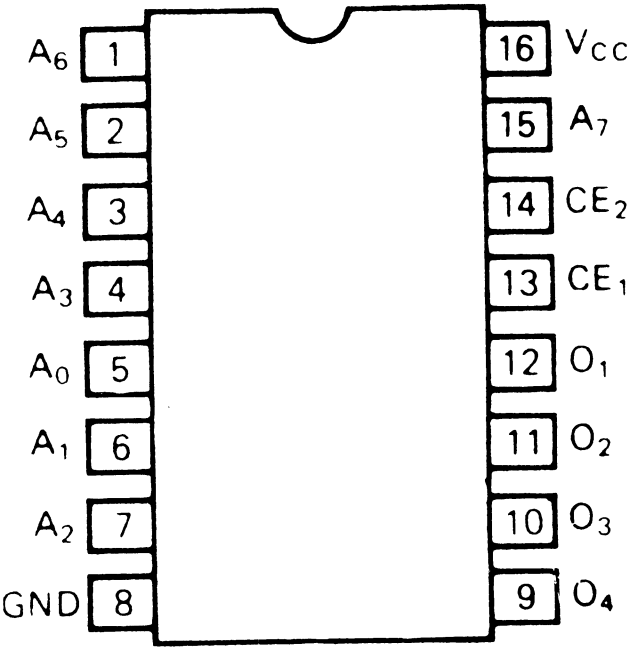
FUNCTIONAL DIAGRAM
SPST SWITCHES



100000401 through 100000415

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

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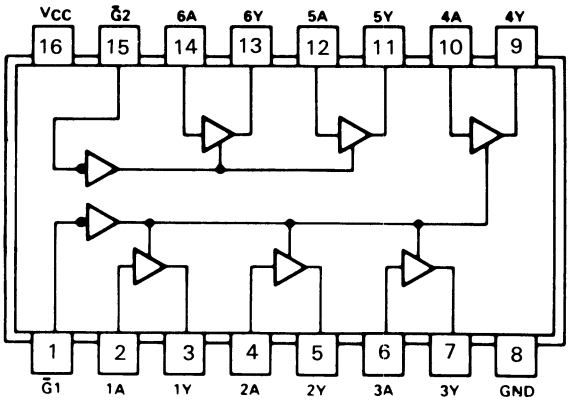
100000417

Hex Bus Driver with 3-State Outputs

PIN CONFIGURATION



FUNCTION TABLE

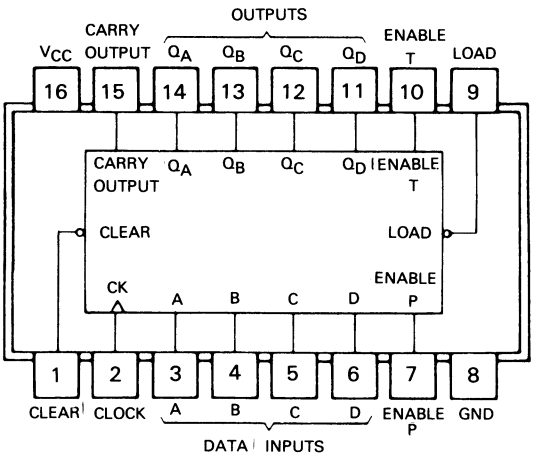
INPUTS		OUTPUT
G̅	A	Y
H	X	Z
L	H	H
L	L	L

H = high level, L = low level,
X = irrelevant, Z = high-impedance

100000418

Synchronous 4-Bit Counter

PIN CONFIGURATION



NOTE *The 100000418 is a low power Schottky device.*

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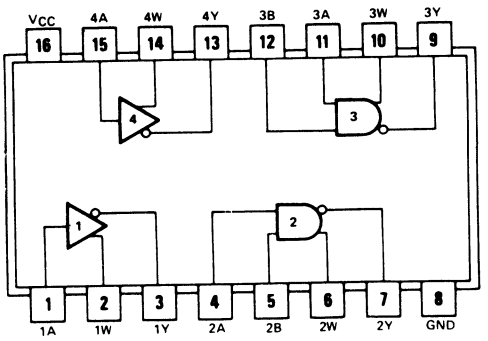
100000419

Quad Complementary-Output Element

PIN CONFIGURATION



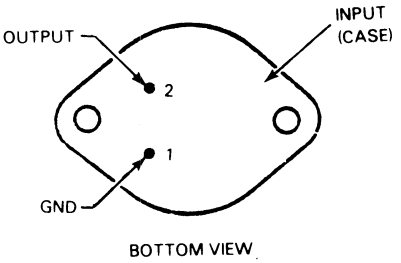
positive logic:

ELEMENTS 1 AND 4	ELEMENTS 2 AND 3
$Y = \overline{A}$	$Y = \overline{AB}$
$W = A$	$W = AB$

100000420

-15V, 1A, 20W Voltage Regulator

PIN CONFIGURATION



BOTTOM VIEW

The 100-000420 is a three-terminal negative voltage regulator with a fixed output voltage of -15V and up to 1.5A load current capability.

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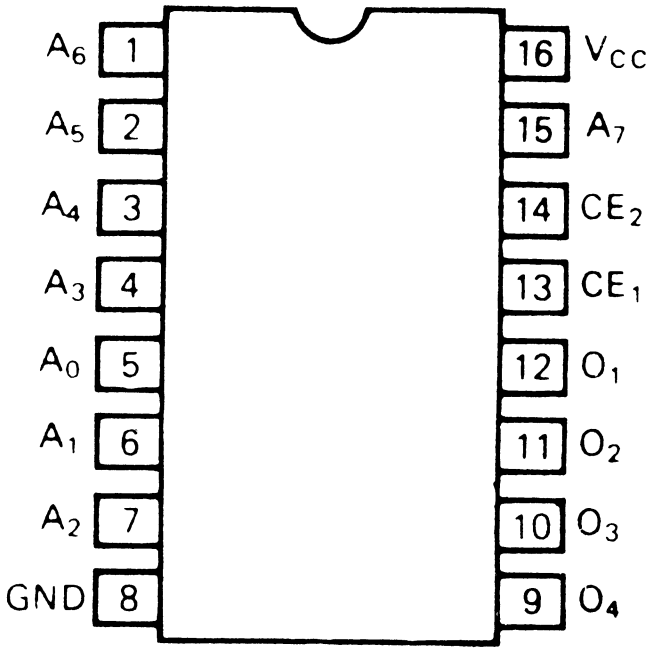
100000421 through 100000435

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



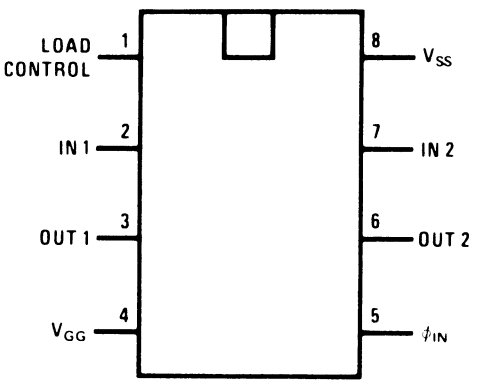
This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

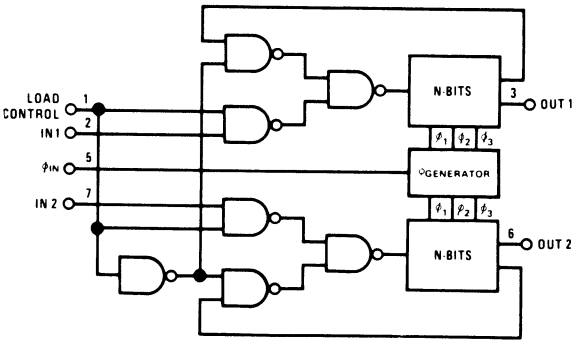
100000436

Dual 144-Bit Mask Programmable Static Shift Register

PIN CONFIGURATION



LOGIC DIAGRAM



TRUTH TABLE

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

The 100000436 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility.

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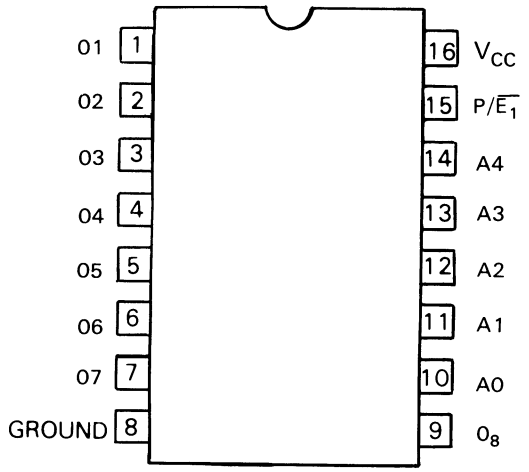
100000437 through 100000440

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

V_{CC} = PIN 16
GND = PIN 8

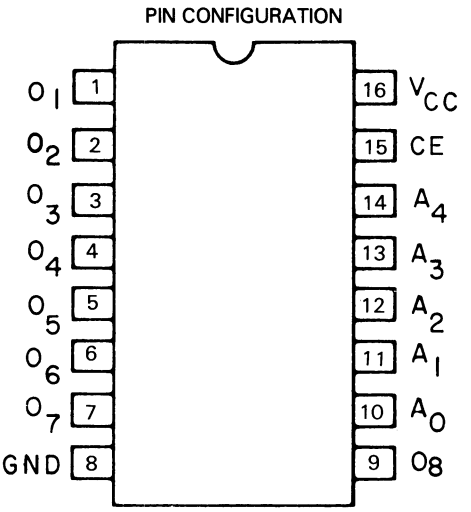
This 256-bit programmable read only memory is organized as 32 words by 8 bits. It has tri-state output and is specified for operation over the commercial temperature and voltage range. The device is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

100000441 through 100000462

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

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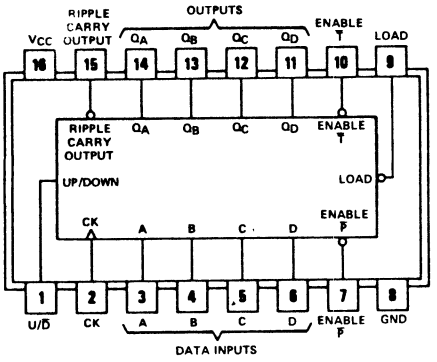
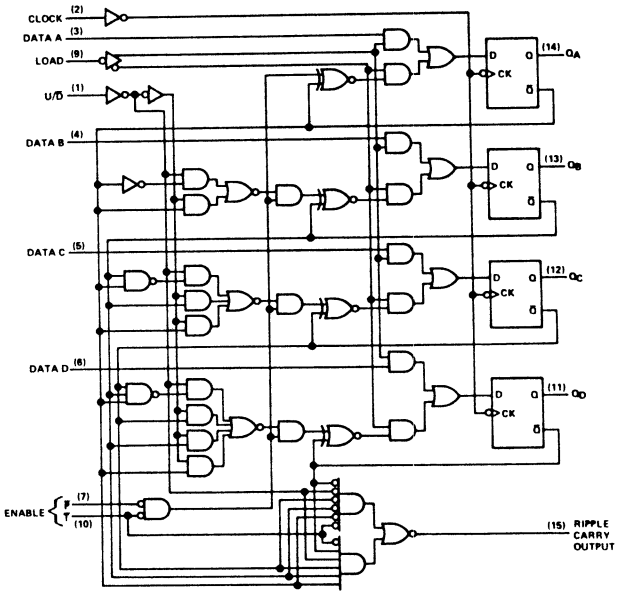
100000463

Synchronous 4-Bit Up/Down Counter

PIN CONFIGURATION



BLOCK DIAGRAM



The 100000463 is a synchronous 4-bit presettable binary counter with an internal look-ahead carry. The low-to-high transition of the clock triggers all four master-slave flip-flops. A low on the Load input disables the counter and causes the outputs to agree with the data inputs after the next low-to-high clock transition.

Both Count Enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. When the Up/Down input (U/$\overline{D}$) is high, the counter counts up; when it is low, the counter counts down. The T' inputs is fed forward to enable the carry output which produces a low output pulse. During a count up operation this pulse lasts almost as long as the QA output is high; during a count down operation it lasts almost as long as the QA output is low. This pulse is an overflow carry which can be used to enable successive counters. Changes on the $\overline{P}$ and $\overline{T}$ Enable, Load, and Up/Down inputs which would modify the operating mode do not affect the counter until clocking occurs.

NOTE *The 100000463 is a Schottky device.*

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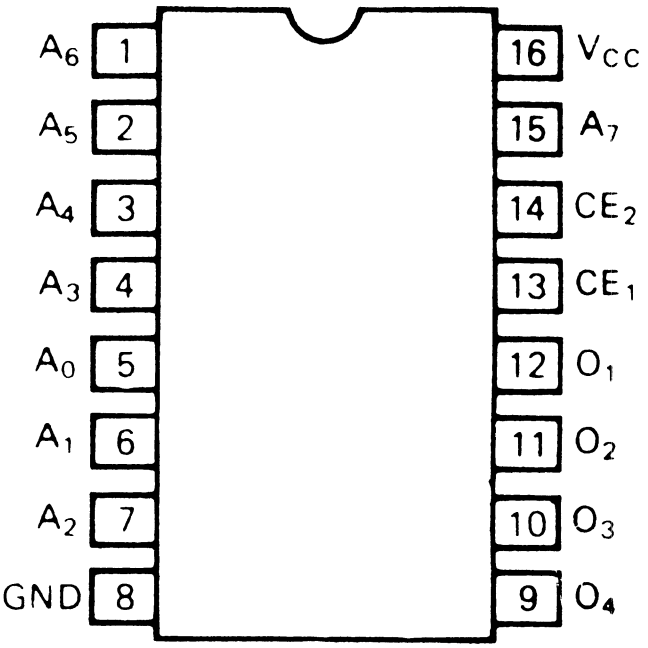
100000464

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



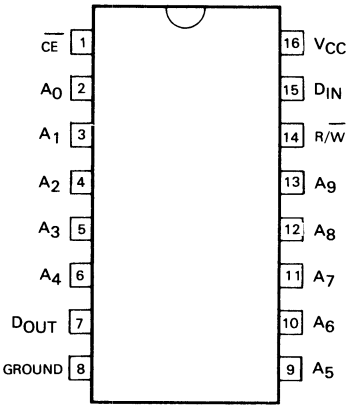
This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100000465

1024 X 1 Bit Bipolar RAM with Open Collector Outputs

PIN CONFIGURATION

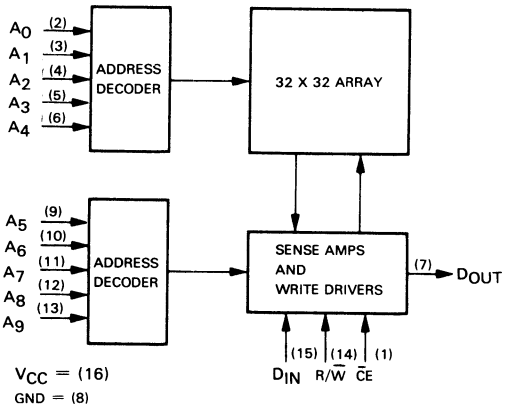


TRUTH TABLE

$\overline{CE}$	R/$\overline{W}$	D_I	MODE	OUTPUT
0	0	0	Write	High
0	0	1	Write	High
0	1	X	Read	Data
1	X	X	Chip Disabled	1

X= Don't care.

BLOCK DIAGRAM



The 100000465 is a high speed 1024-bit random access memory organized as 1024 words by one bit. It requires a single +5 volt power supply and features very low current PNP input structures. It is fully TTL compatible, and includes on-chip decoding and a chip enable input for ease of memory expansion.

NOTE: *This is a Schottky device.*

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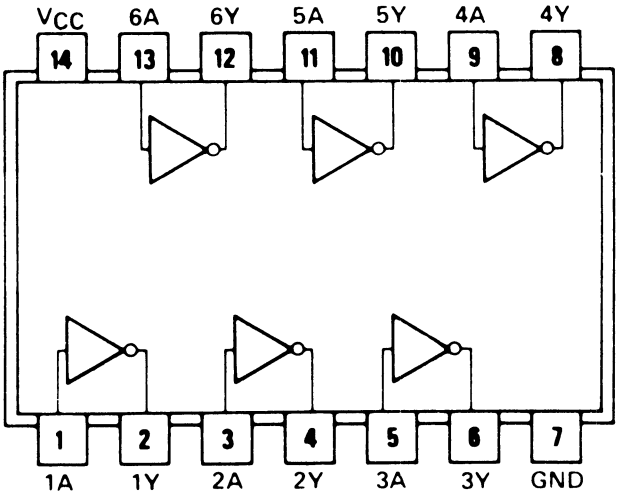
100000466

Hex Inverter

PIN CONFIGURATION

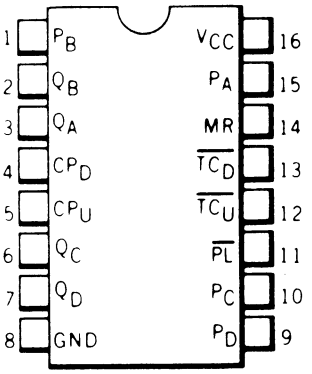


Positive logic: $Y = \overline{A}$

100000467

Up/Down Binary Counters

PIN CONFIGURATION



TRUTH TABLE

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

NOTE *The 100000467 is a low power Schottky device.*

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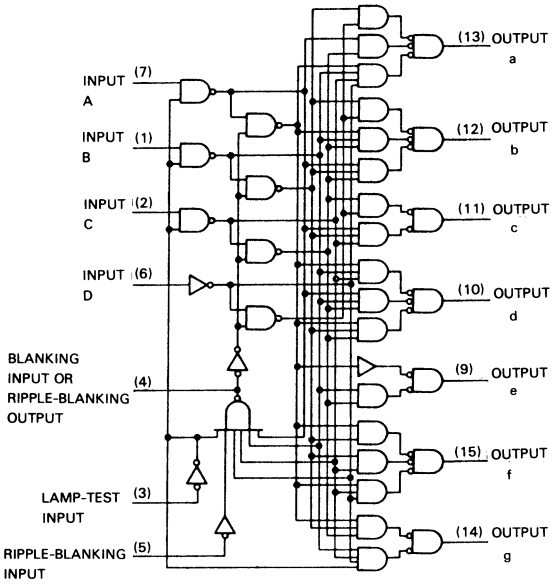
100000468

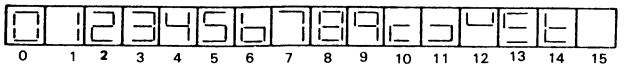
BCD-To-Seven-Segment Decoder/Driver

BLOCK DIAGRAM

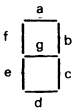


The 100000468 features active-high outputs for driving lamp buffers or common-cathode VLEDs. It contains an automatic leading and/or trailing edge zero-blanking controls (RBI, RBO). The test lamp operation can occur whenever the BI/RBO input is high. The overiding blanking input (B) can be used to inhibit the outputs or to control the lamp by pulsing. The inputs and outputs are compatible with TTL or DTL logic outputs.

NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS



SEGMENT IDENTIFICATION



FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO†	OUTPUTS a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	1
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

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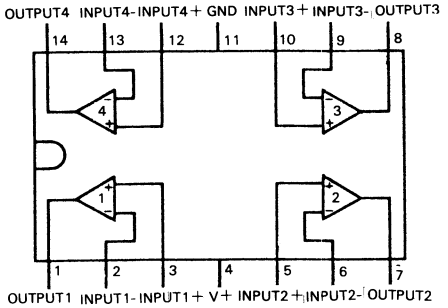
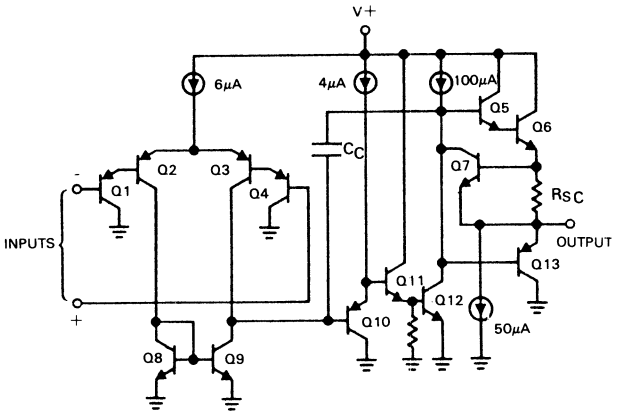
100000469

Quad Operational Amplifier/Buffer

PIN CONFIGURATION



LOGIC DIAGRAM



The 100000469 consists of four independent, high gain, internally frequency compensated operational amplifiers.

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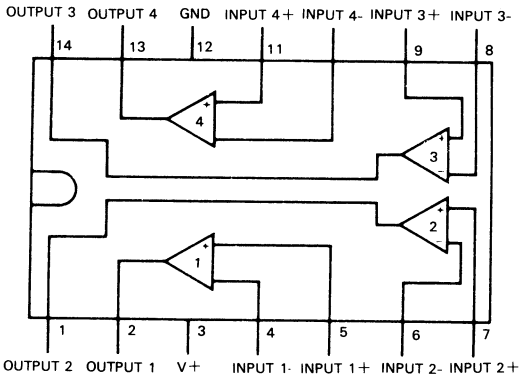
100000470

Quad Voltage Comparator

PIN CONFIGURATION



The 100000470 operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. The input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Pin Designations

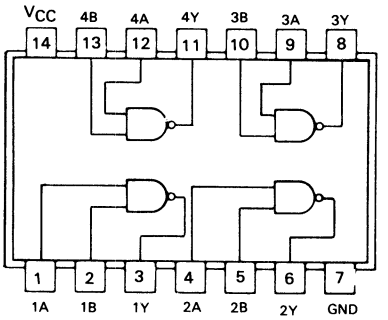
V+ = Pin 3

Gnd = Pin 12

100000472

Quad 2-Input Positive NAND Gate

PIN CONFIGURATION



NOTE *The 100000472 is a Schottky device.*

$Y = \overline{AB}$

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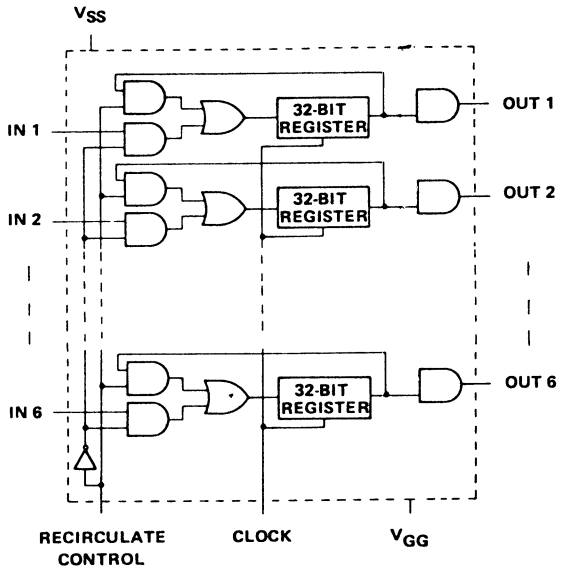
100000473

Hex 32-Bit Static Shift Register

BLOCK DIAGRAM



FUNCTION TABLE

RECIRCULATE	INPUT	FUNCTION
H	L	Recirculate
H	H	Recirculate
L	L	L is written
L	H	H is written

H = high level
L = low level

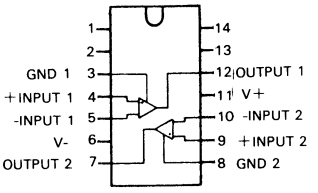
The 100000473 contains six 32-bit static shift registers. Data is transferred in or out of each register on the low-to-high clock transition. The clock must be kept high to store data for long periods.

Data is entered when the recirculate control is low. When this control is high, recirculation occurs on the low-to-high clock transition and data is presented continuously at the outputs. The data inputs are inhibited during recirculation.

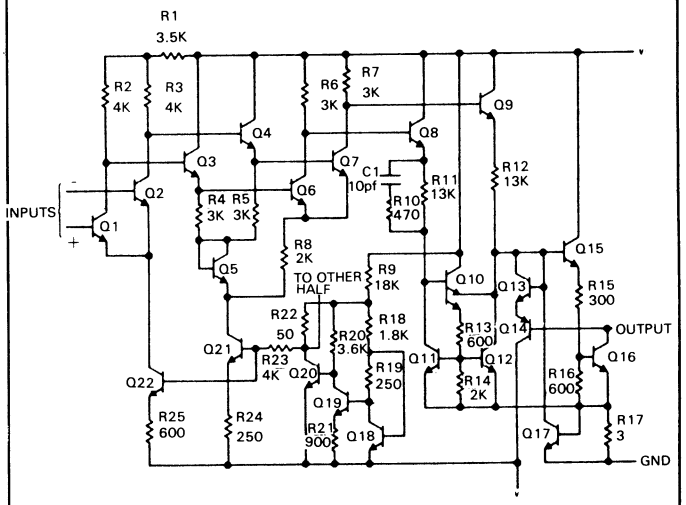
100000474

High-Speed Dual Comparator

PIN CONFIGURATION



LOGIC DIAGRAM



The 100000474 contains two high speed voltage comparators which operate over a wide range of voltages down to a single 5V logic supply and ground. They have uncommitted collector outputs which make them compatible with RTL, DTL and TTL and capable of driving lamps and relays up to 25 mA.

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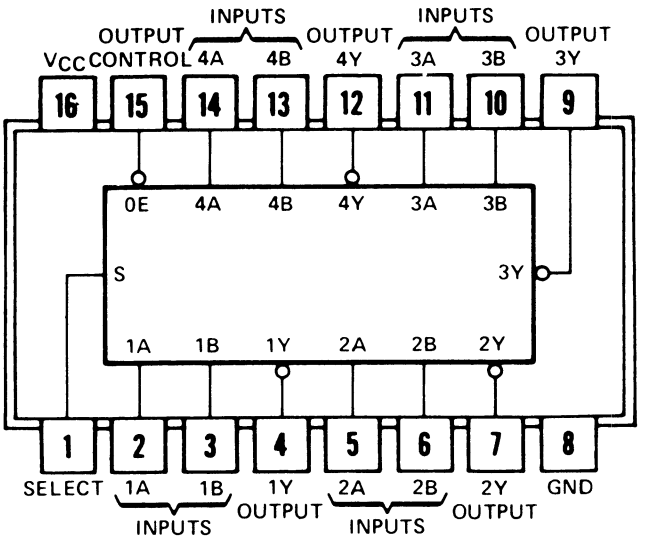
100000475

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE

Inputs			Output
Output Control	Select	A B	Y
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

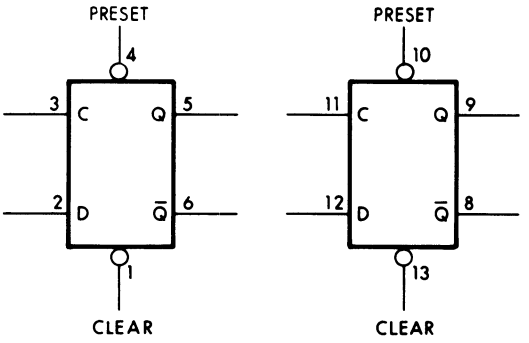
H = high level, L = low level, X = irrelevant,
Z = high impedance (off).

NOTE *The 100000475 is a low power Schottky device.*

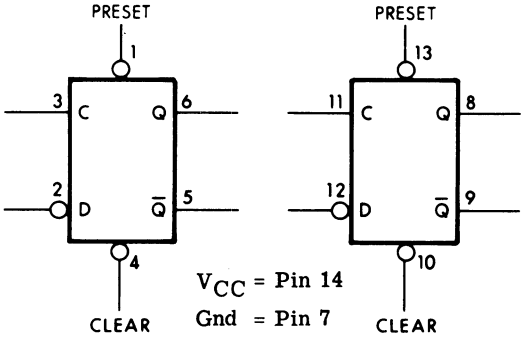
100000476

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



ALTERNATE PIN CONNECTIONS



V_{CC} = Pin 14
Gnd = Pin 7

FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000476 is a low power Schottky device.*

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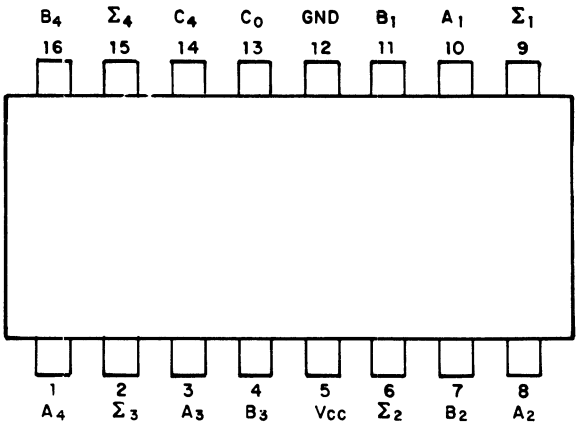
100000477

4-Bit Binary Full Adder (Look Ahead Carry)

PIN CONFIGURATION



TRUTH TABLE

INPUT				OUTPUT					
				WHEN $C_0 = 0$, WHEN $C_2 = 0$			WHEN $C_0 = 1$, WHEN $C_2 = 1$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note:

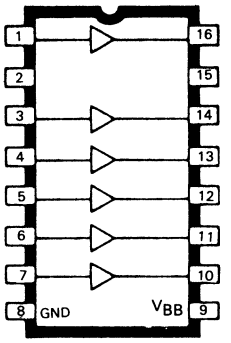
Input conditions at A1, A2, B1, B2, and C0 are used to determine outputs 1 and 2, and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs 3, 4, and C4.

NOTE *The 100000477 is a low power Schottky device.*

100000478 and 100000479

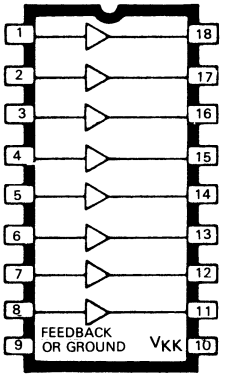
Display Drivers

PIN CONNECTIONS FOR 100000478



Y = A

PIN CONNECTIONS FOR 100000479



Y = A

These gas-discharged display digit drivers are designed for interfacing between MOS and other low-voltage circuitry.

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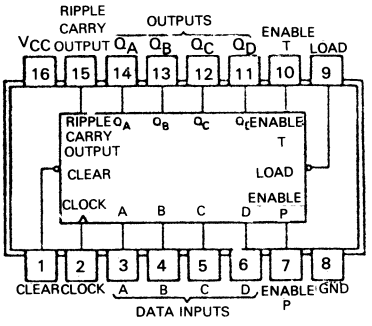
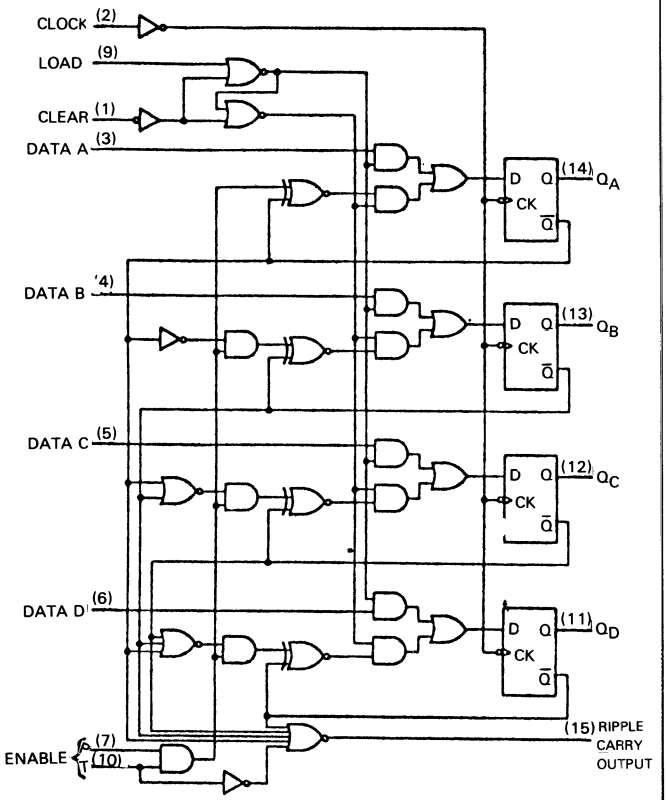
100000480

Synchronous 4-Bit Counter

PIN CONFIGURATION



BLOCK DIAGRAM



The 100000480 is a synchronous presettable counter with an internal look-ahead carry. The low-to-high transition of the buffered clock input triggers all four flip-flops to ensure synchronous operation.

The counter is preset by a low on the Load input which disables the counter and causes the outputs to agree with the setup data after the next low-to-high clock transition. A low on the synchronous Clear input sets the flip-flops to low on the next low-to-high transition of the clock.

The look-ahead carry allows 100000480s to be cascaded. Both count-enable inputs (P and T) must be high to count. The T input is fed forward to enable the ripple carry output. This output produces a pulse which lasts about as long as the QA output is high.

The clocking circuit is independent. Changes at the enable P, enable T, or Clear inputs do not effect on the operating mode until the next low-to-high clock transition occurs.

NOTE *The 100000480 is a Schottky device.*

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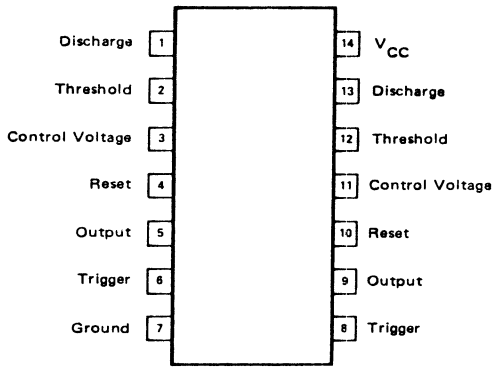
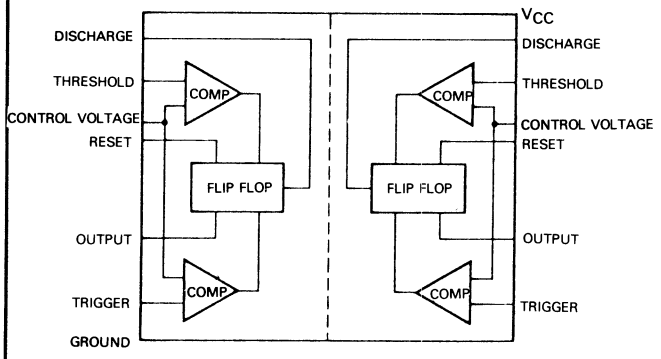
100000483

Dual Timing Circuit

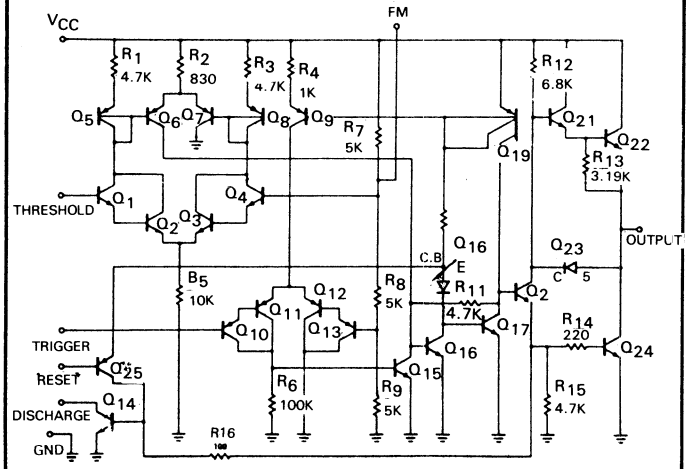
PIN CONFIGURATION



BLOCK DIAGRAM



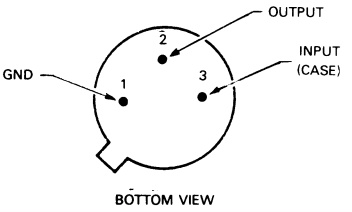
LOGIC DIAGRAM



The 100000483 is a dual timing circuit for producing accurate time delays or oscillation. An external resistor and capacitor provide the timing for each timer. The timers function independently except for sharing VCC and ground. They can be triggered and reset on falling waveforms. The outputs can sink or source 150 mA.

100000484

-5V, 1/2A, 2W, 5% Voltage Regulator



The 100000484 is a three-terminal negative regulator with a fixed output voltage of -5V. This device needs only one external component - a compensation capacitor at the output. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

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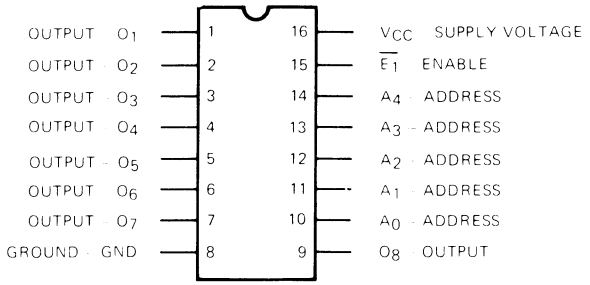
100000485 and 100000486

256-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This device is a field programmable, 1024-bit, DTL and TTL compatible, bipolar read only memory.

The three-state output of this device provides a low impedance drive Q_2 for driving capacitance on the memory output; no pullup resistor is required. When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. In a system environment, up to 21 memory outputs of the read only memory can be connected to a common bus. All of the devices, except one, are placed in the high impedance state. The selected device is enabled and has the characteristics of a TTL totem pole output.

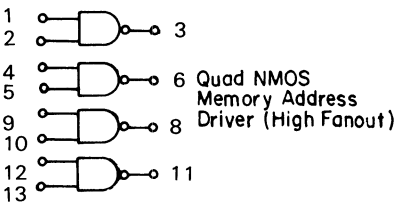
Memory Operation

The memory is addressed with inputs A_0 through A_4 which select one of 32 words. To enable the outputs for a readout, enable E_1 must be low. If the enable is high, the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

100000487

Quad MOS Clock Driver

LOGIC DIAGRAM



V_{CC} = 14
GND = 7

$Y = \overline{AB}$

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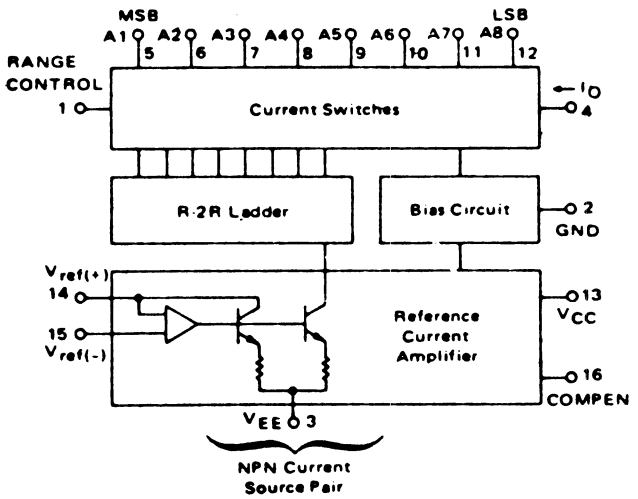
100000488

8-Bit Multiplying Digital-To-Analog Converter

BLOCK DIAGRAM

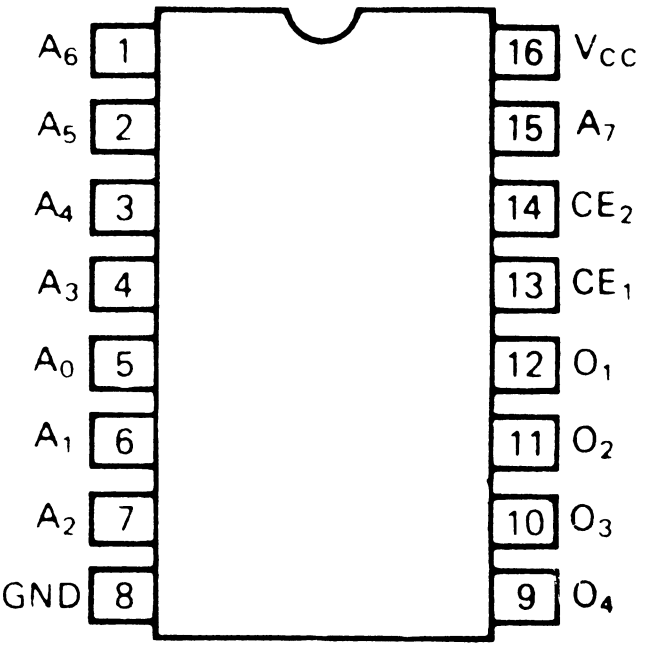


This IC is a high-speed digital-to-analog converter with current output. The output current is the linear product of the eight-bit input word and the analog input voltage.

100000489 through 100000498

256 x 4-Bit PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

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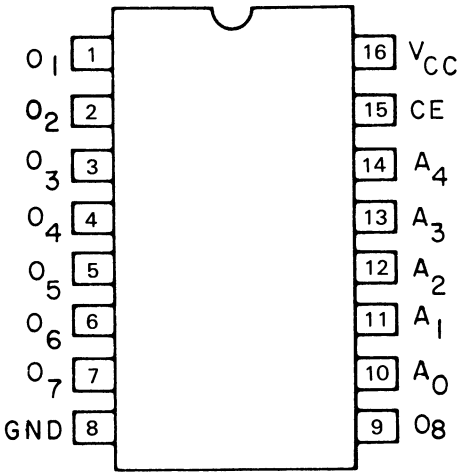
100000499 and 100000500

32 x 8 - Bit Bipolar PROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

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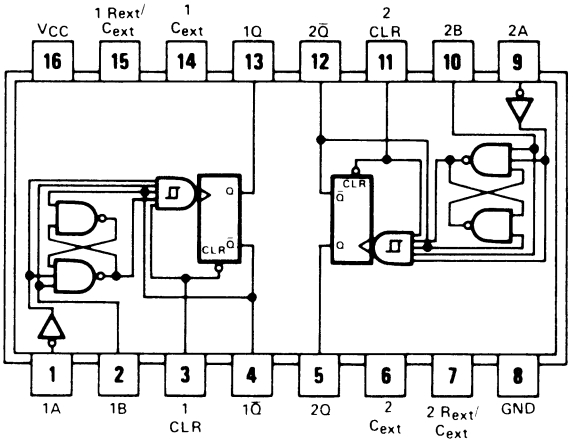
100000502

Dual Monostable Multivibrator with Schmitt-Trigger Inputs

PIN CONFIGURATION



FUNCTION TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
Also see description and switching characteristics				

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high-level pulse
⎍ = one low-level pulse
X = irrelevant

The 100000 502 is a monolithic dual multivibrator and features a negative-transition-triggered input and a positive-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1. 2volts. A high immunity to V_{CC} noise of typically 1. 5 volts is also provided by internal latching circuitry.

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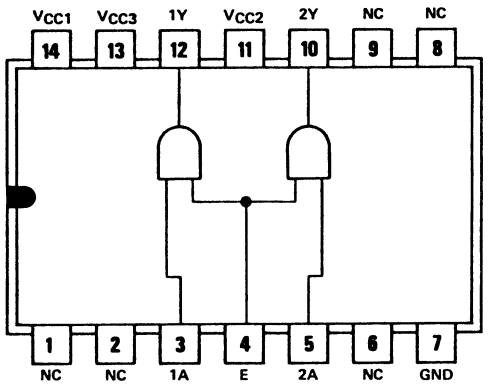
100000503

Dual Positive-AND TTL-to-MOS Driver

PIN CONFIGURATION



NC—No internal connection.

positive logic: Y = AE

The 100000503 accepts standard TTL and DTL inputs and produces high-current high-voltage ouputs for driving MOS circuits.

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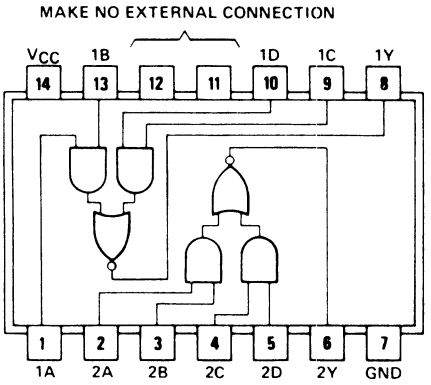
100000504

Dual 2-Wide 2-Input AND-OR-INVERT Gates

PIN CONFIGURATION



Positive logic: $Y=\overline{AB+CD}$

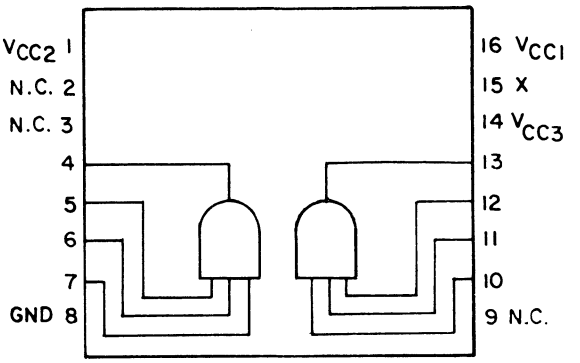
NOTE

The 100000504 is a Schottky device.

100000505

Dual Clock Driver

PIN CONFIGURATION



Y = ABC

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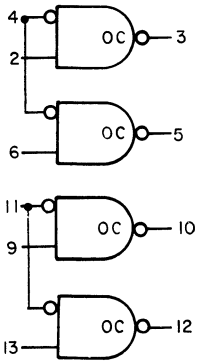
100000506

Quad Sense Amplifier with Open Collector Outputs

LOGIC DIAGRAM



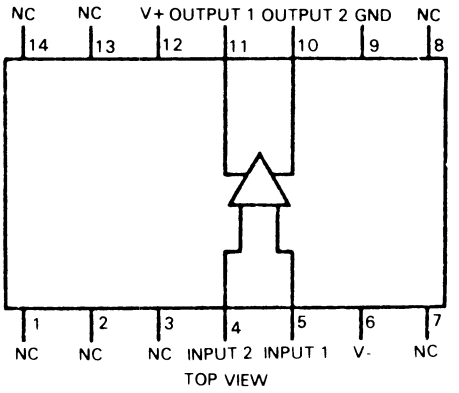
-5V—Pin 8
+5—Pin 1 & 14
Gnd—Pin 7

$Y = \overline{\overline{A}\overline{B}} = A + \overline{B}$
$Y_1 = \overline{\overline{A}\overline{C}} = A + \overline{C}$

100000507

High Speed Differential Comparator

PIN CONFIGURATION



TOP VIEW

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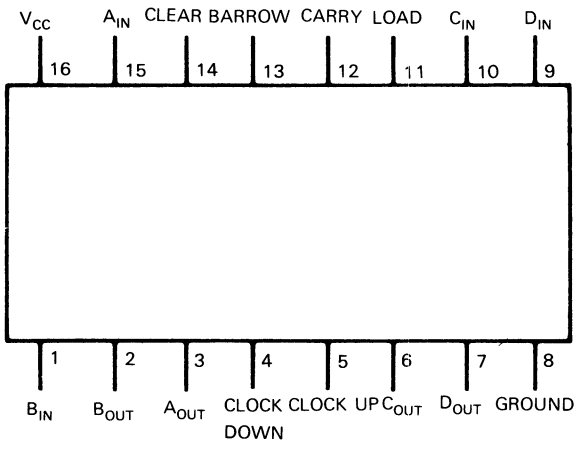
100000508

Up/Down Decade Counter

PIN CONFIGURATION



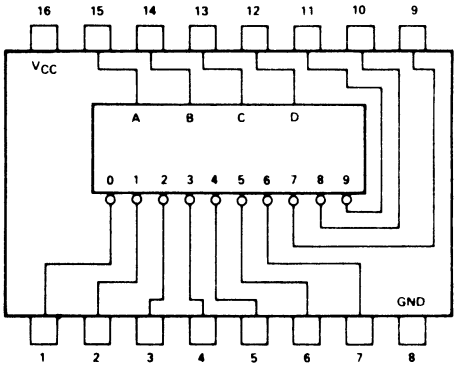
The 100000508 is a TTL, compatible, up-down decade counter which is capable of being preset to any number from 0 through 9. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines- one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 9. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

100000509

BCD To Decimal Decoder

PIN CONFIGURATION



TRUTH TABLE

INPUT

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

The 100000509 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 100000509 decodes a four bit BCD number to one of ten outputs.

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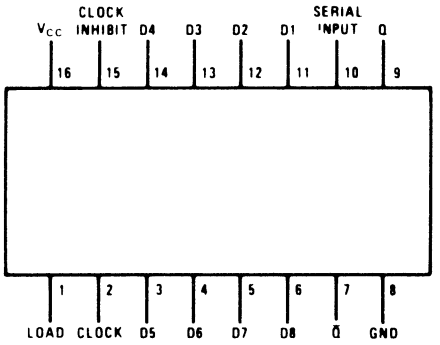
100000510

8-Bit Parallel-In Serial-Out Shift Register

PIN CONFIGURATION



The 100000510 utilizes compatible TTL circuitry to provide an eight-bit parallel-in serial-out shift register designed to operate at frequencies of 20MHz. The device also features gating to inhibit clocking, parallel load control, and both Q and $\overline{Q}$ outputs from the last flip-flop for added flexibility.

NOTES:

1. The Clock Inhibit input, when in the logical "1" state, will inhibit the Clock. It must be in the logical "0" state for clocking to occur.

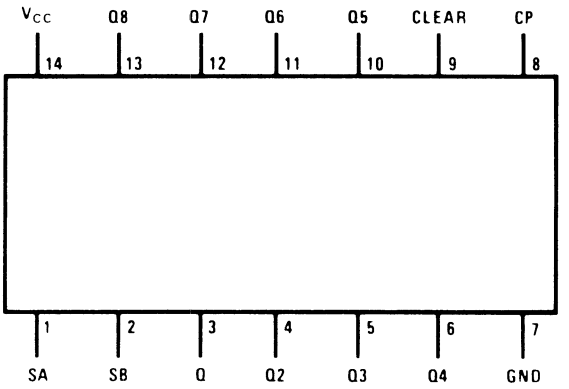
   There is no difference between the Clock Input and the Clock Inhibit input. Their functions may be reversed for ease of layout.

2. Clocking occurs on the positive-going transition of the Clock input.
3. Data on the D1 through D8 inputs will be entered on the negative-going transition of the Load input. This information is entered independent of the state of the Clock, Clock Inhibit, or Serial Input lines. Information on these parallel inputs may be changed while the Load line is enabled thus changing the information in the register.
4. The logic level applied to the Serial Input is entered into the first flip-flop when the register is clocked.

100000511

8-Bit Serial-In Parallel-Out Shift Register

PIN CONFIGURATION



TOP VIEW

The 100000511 utilizes compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register designed to operate at frequencies of 20MHz. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical 0, asynchronously sets all flip-flops to the logical 0 state. Because the flip-flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical 1 levels on SA and SB enter logical 1's into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

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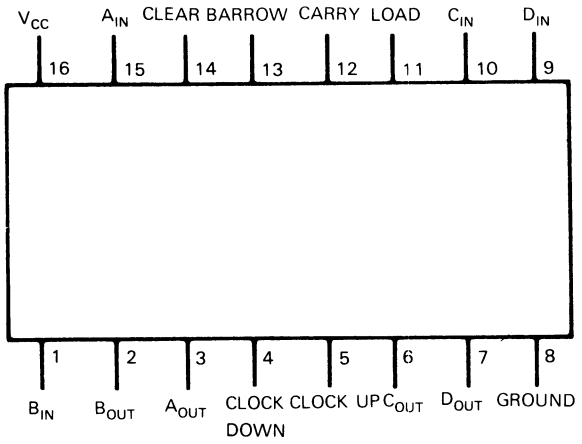
100000512

Up/Down Binary Counter

PIN CONFIGURATION



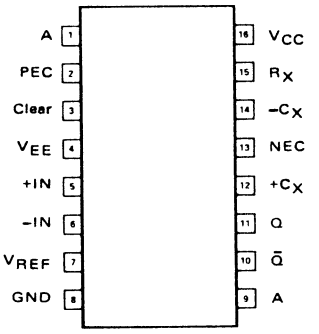
The 100000512 is a TTL compatible, up-down binary counter which is capable of being preset to any number from 0 through 15. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines-one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 15. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

100000513

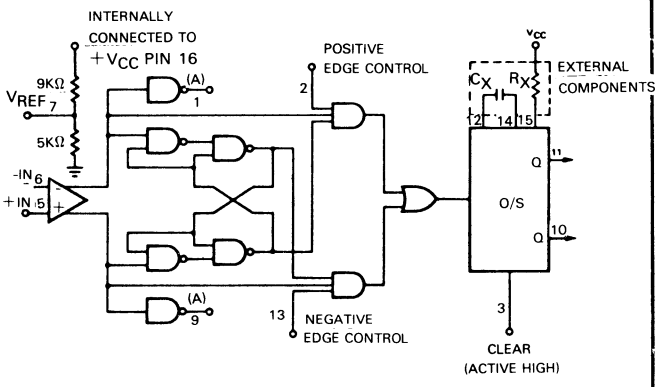
Bidirectional One Shot

PIN CONFIGURATION



V_{CC} = (4) (-5V ±5%)
V_{CC} = (16) (+5V ±5%)
GND = (8)
( ) = Denotes Pin Numbers

BLOCK DIAGRAM



The 100000513 consists of an analog comparator, digital control circuitry, and a monostable multivibrator. For input frequencies up to 8MHz, the device can act as a frequency doubler since it can trigger on both positive and negative transitions.

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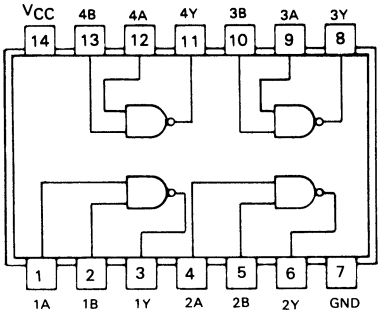
100000515

Quad 2-Input Positive-NAND Gate

PIN CONFIGURATION



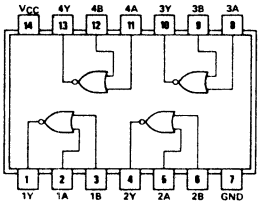
$Y = \overline{AB}$

NOTE *The 100000515 is a low power TTL device.*

100000516

Quad 2-Input Positive NOR Gate

PIN CONFIGURATION



The 100000516 is a positive NOR gate with totem-pole outputs.

$Y = \overline{A + B}$

NOTE: *This is a low power TTL device.*

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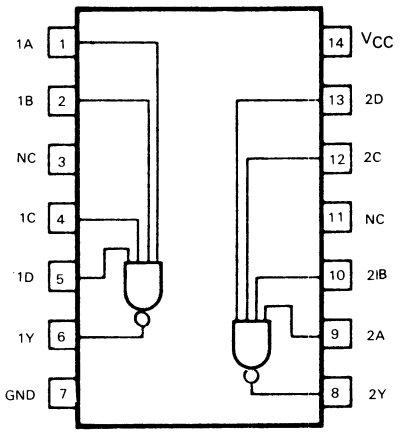
100000517

Dual 4-Input Positive NAND Gate

PIN CONFIGURATION



$Y = \overline{ABCD}$

The 100000517 is a low power TTL device with totem-pole outputs.

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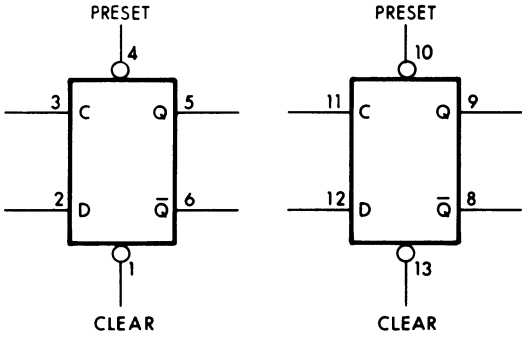
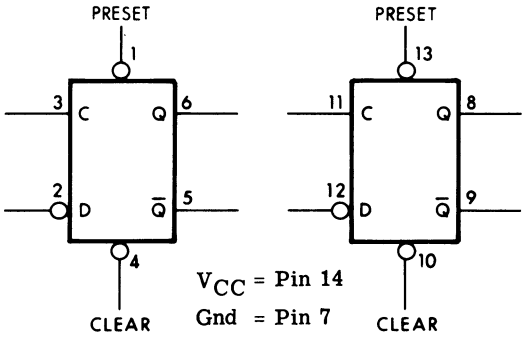
100000518

Dual D-Type Edge-Triggered Flip-Flop

PIN CONFIGURATION



ALTERNATE PIN CONNECTIONS



V_{CC} = Pin 14
Gnd = Pin 7

FUNCTION TABLE

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

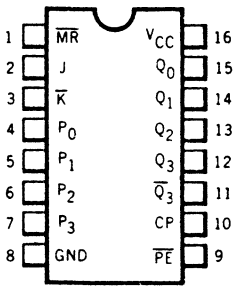
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

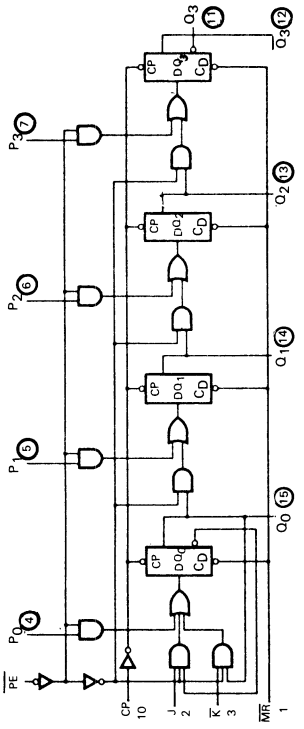
NOTE: *This is a low power TTL device.*

100000519

Low Power 4-Bit Shifter Register

PIN CONFIGURATION





TRUTH TABLE

OPERATING MODE	INPUTS (MR = H)							OUTPUTS @ t_{n+1}				
	PE	J	K̄	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
SHIFT MODE	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	L	X	X	X	X	$\overline{Q}_0$	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q}_2$
PARALLEL ENTRY MODE	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

*t_{n+1} = Indicates state after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTE: *This is a low power TTL device.*

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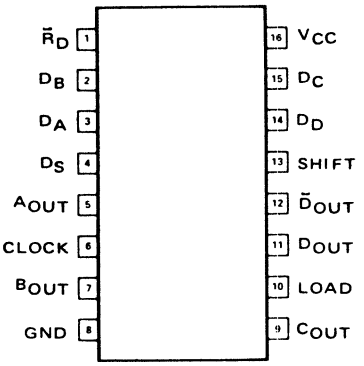
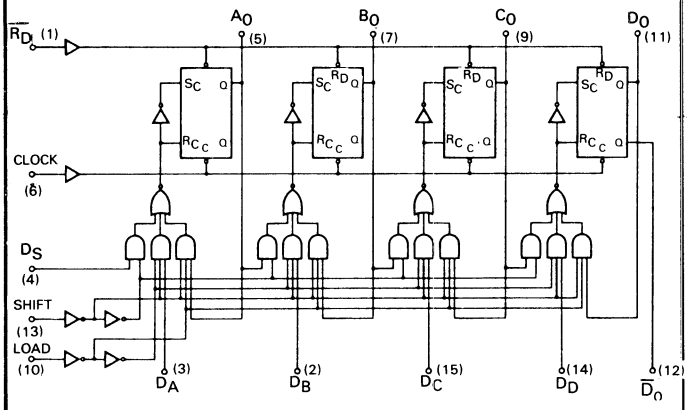
100000520

4-Bit Shift Register

PIN CONFIGURATION



BLOCK DIAGRAM



V_{CC} = (16)
GND = (8)
( ) = denotes pin numbers

TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

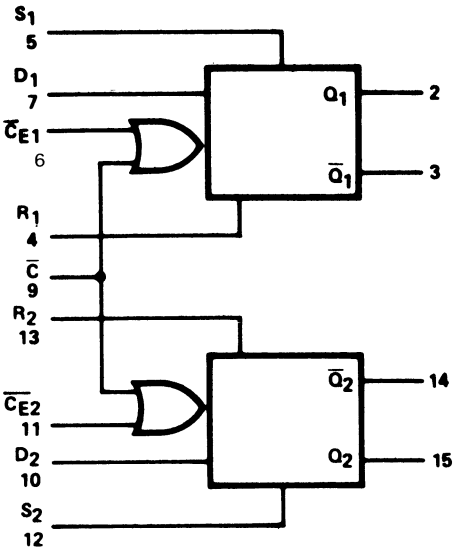
The 100000520 is a 4-bit shift register with both serial and parallel data entry capability. The single-ended, true inputs are loaded into the registers on the high-to-low clock transition. The load and shift control lines select three operating modes: serial shift right, parallel load, and hold.

NOTE *The 100000520 is a Schottky device.*

100000521

Dual D-Type Master-Slave Flip-Flop

BLOCK DIAGRAM



Vcc1 = 1, Vcc2 = 16, Vee = 8

NOTE: *The 100000521 is an ECL device.*

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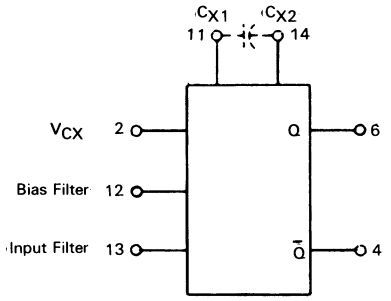
100000522

Voltage-Controlled Multivibrator

PIN CONFIGURATION

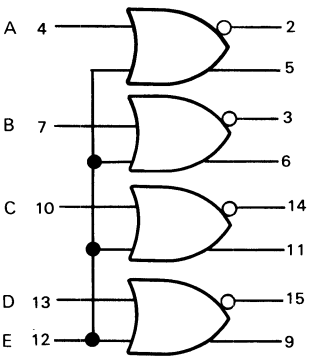


V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

100000523

Quad OR-NOR Gate

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

$Y_2 = \overline{A + E}$

$Y_5 = A + E$

The 100000523 is an ECL device.

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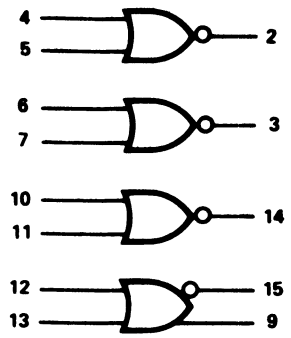
100000524

Quad 2-Input NOR Gate

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

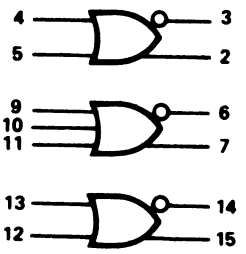
NOTE: *The 10000524 is an ECL device.*

$$Y = \overline{A + B}$$
$$Y_9 = A + B$$

100000525

Triple 2,3,2-Input OR-NOR Gate

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

NOTE: *The 100000525 is an ECL device.*

$$Y_3 = \overline{A + B}$$
$$Y_2 = A + B$$
$$Y_6 = \overline{A + B + C}$$
$$Y_7 = A + B + C$$

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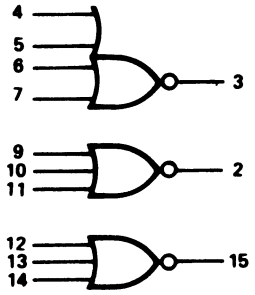
100000526

Triple 4,3,3-Input NOR Gate

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

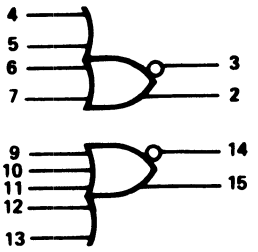
$$Y_3 = \overline{A + B + C + D}$$
$$Y_{2/15} = \overline{A + B + C}$$

NOTE: *This is an ECL device.*

100000527

Dual 4,5-Input OR-NOR Gate

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

$$Y_3 = \overline{A + B + C + D}$$
$$Y_2 = A + B + C + D$$
$$Y_{14} = \overline{A + B + C + D + E}$$
$$Y_{15} = A + B + C + D + E$$

NOTE: *This is an ECL device.*

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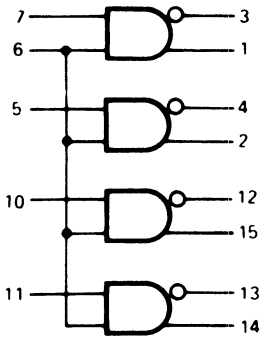
100000528

Quad TTL To ECL Translator

PIN CONFIGURATION



V_{CC} = 9 GND = 16 V_{EE} = 8

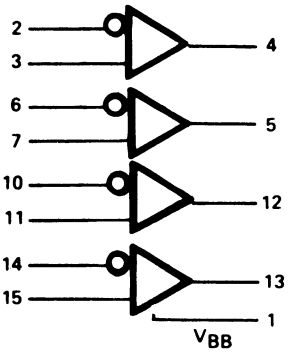
$$Y = AB$$
$$\overline{Y} = \overline{AB}$$

NOTE: *This is an ECL device.*

100000529

Quad ECL To TTL Translator with Totem-Pole Outputs

PIN CONFIGURATION



V_{CC} = 9 GND = 16 V_{EE} = 8

NOTE: *This is an ECL device.*

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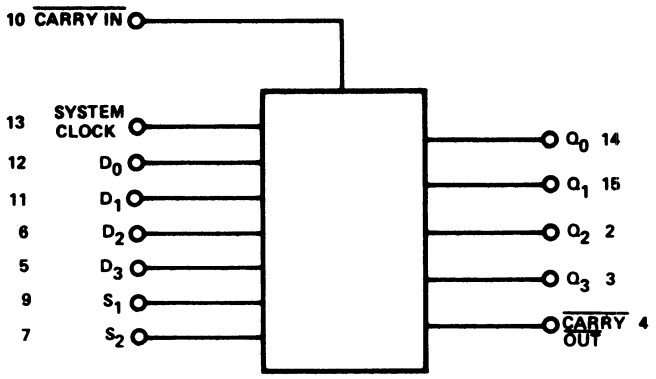
100000530

Universal Hexadecimal Counter

PIN CONFIGURATION



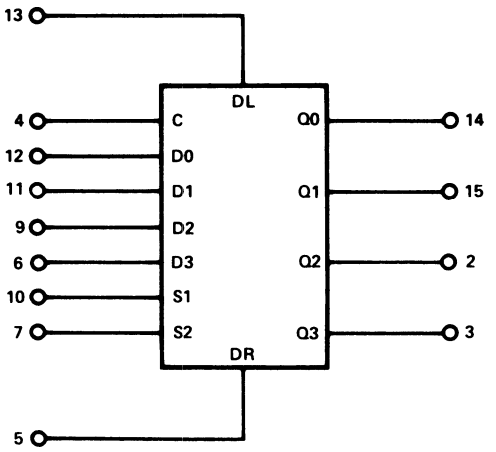
Vcc1 = 1, Vcc2 = 16, Vee = 8

NOTE: *Ths is an ECL device.*

100000531

4-Bit Shift Register

PIN CONFIGURATION



Vcc1 = 1, Vcc2 = 16, Vee = 8

NOTE: *Ths is an ECL device.*

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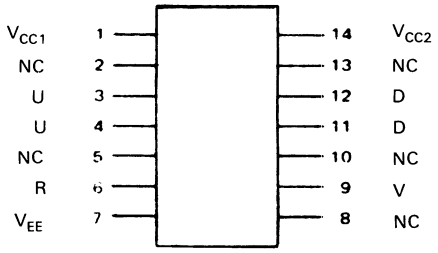
100000532

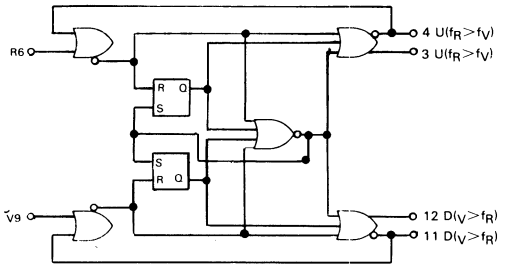
Phase-Frequency Detector

PIN CONFIGURATION



NC-No Connection

LOGIC DIAGRAM



V_{CC1}=PIN 1
V_{CC2}=PIN 14
V_{CC3}=PIN 7

NOTE: *Ths is an ECL device.*

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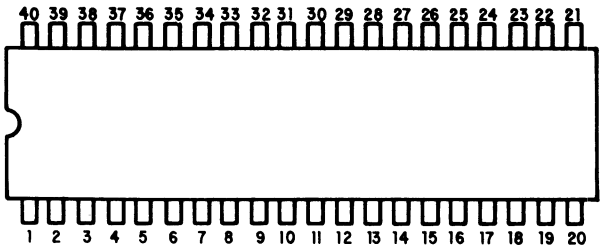
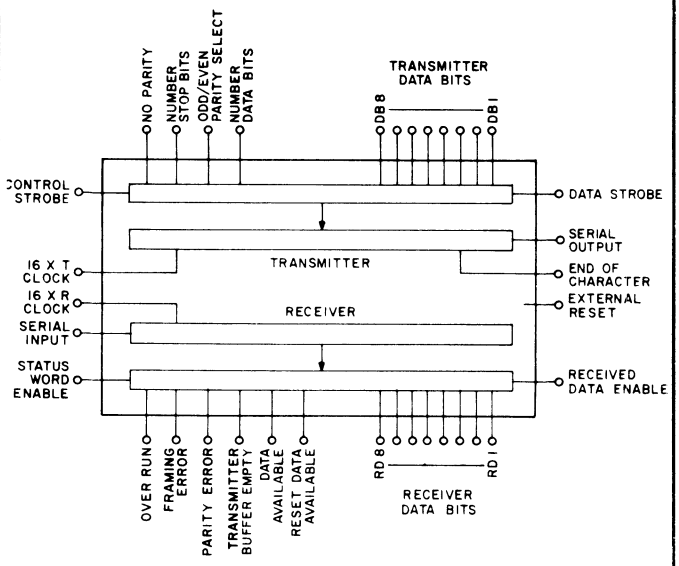
100000536

Asynchronous Receiver/Transmitter

PIN CONFIGURATION



BLOCK DIAGRAM



The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{gr}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.

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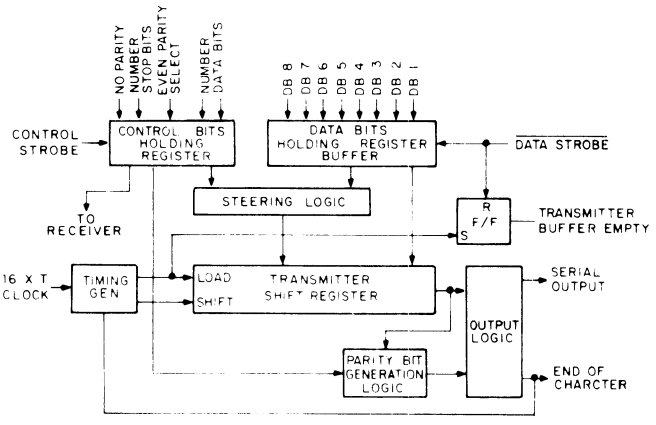
100000536 (Continued)

PIN FUNCTIONS (Cont.)

Pin No.	Name	Symbol	Function
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character. NB1 NB2 Bits Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER BLOCK DIAGRAM



Transmitter Operation

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously mentioned.

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100000536
(Continued)

Receiver Operation

Initializing

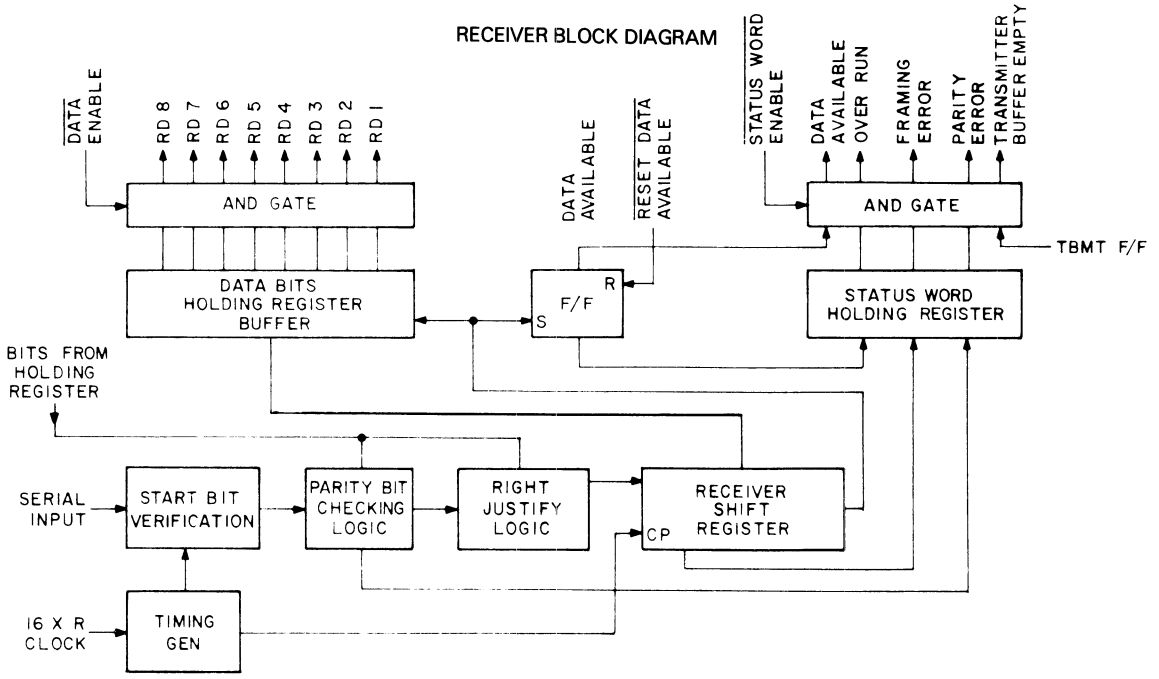
Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16X clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditioning set to a logic "0".

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

RECEIVER BLOCK DIAGRAM



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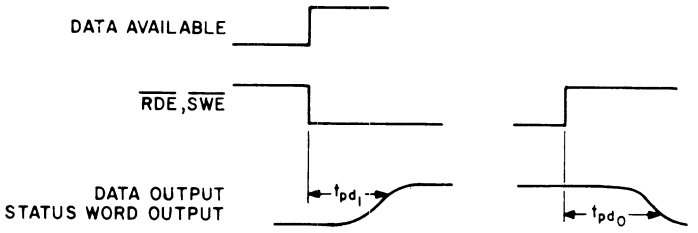
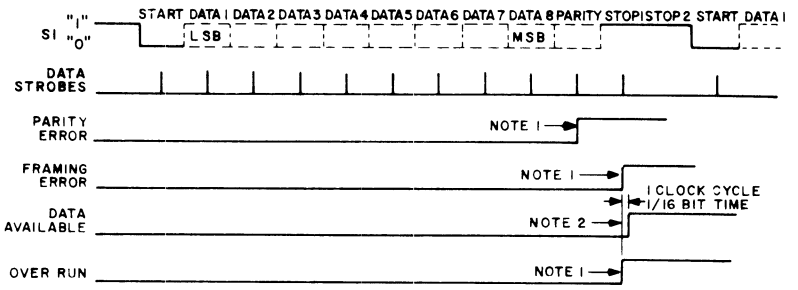
100000536
(Continued)

RECEIVER PROPOGATION DELAY TIMING DIAGRAM



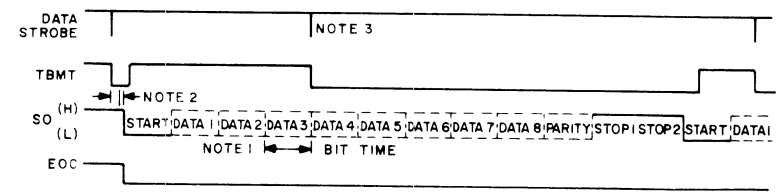
RECEIVER TIMING DIAGRAM



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGH JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

TRANSMITTER TIMING DIAGRAM



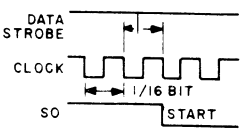
NOTE: TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1.

DETAIL:



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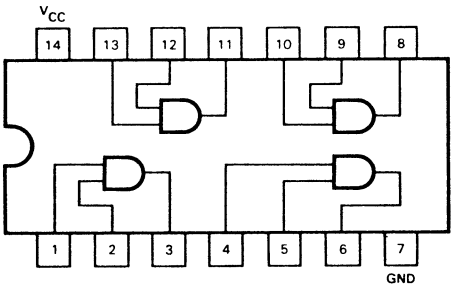
100000537

Quad 2-Input AND Gate

PIN CONFIGURATION



$Y = AB$

NOTE *The 100000537 is a Schottky device.*

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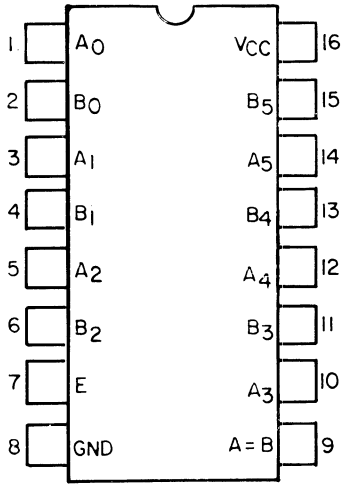
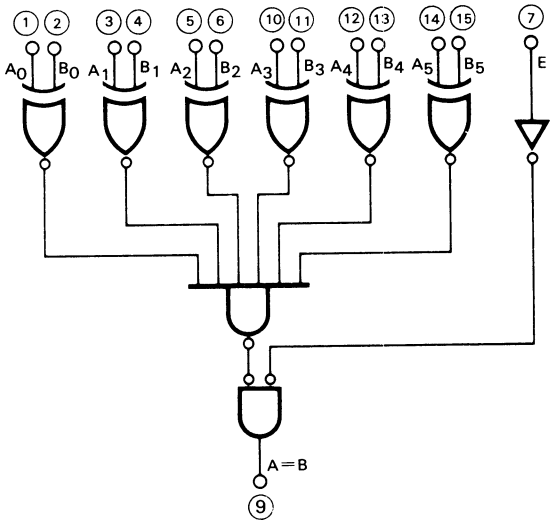
100000540

High Speed 6-Bit Identity Comparitor

PIN CONFIGURATION



LOGIC DIAGRAM



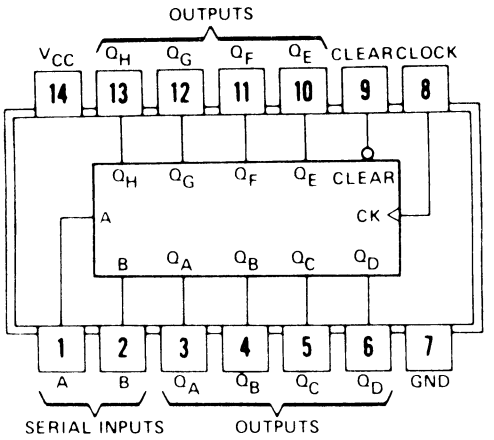
The 100000540 is a very high speed 6-Bit Identity Comparator. The device compares two words of up to 6-bits and indicates identity in less than 12 ns It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable Input (E) is LOW, it forces the output LOW. The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL product families.

NOTE *The 100000540 is a Schottky device.*

100000541

8-Bit Parallel-Out Serial Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B ...	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Notes:

H = high level (steady state),
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

The 100000541 features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the set-up requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock

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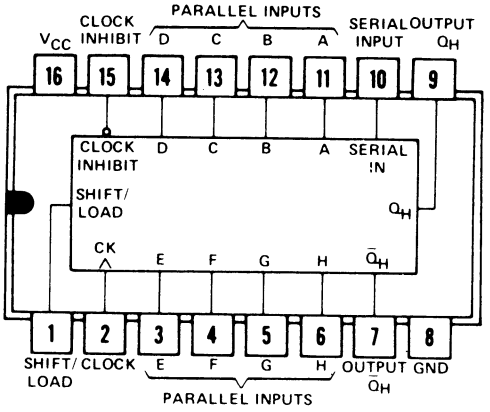
100000542

Parallel-Load 8-Bit Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Notes:

H = high level (steady state),
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a. . . h = the level of steady-state input at inputs A thru H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

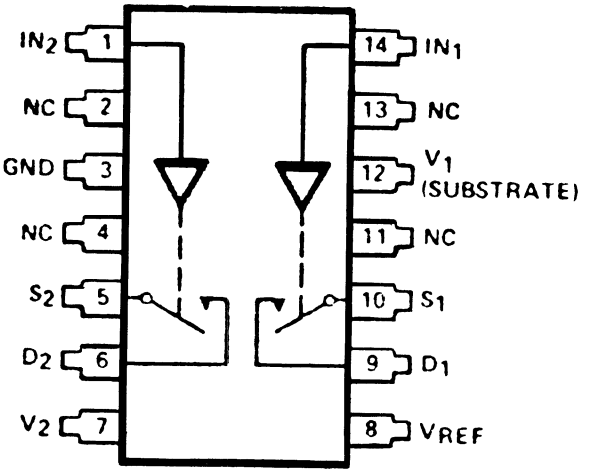
Q_{An}, Q_{Gn}, = the level of Q_A, or Q_G, respectively before the most recent ↑ transition of the clock.

The 100000542 is an 8-bit serial shift register which shifts the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. This register also features gated clock inputs and complementary outputs from the eighth bit.

100000543

Dual Analog Current Switch

PIN CONFIGURATION



When the input is LOW, S is connected to D

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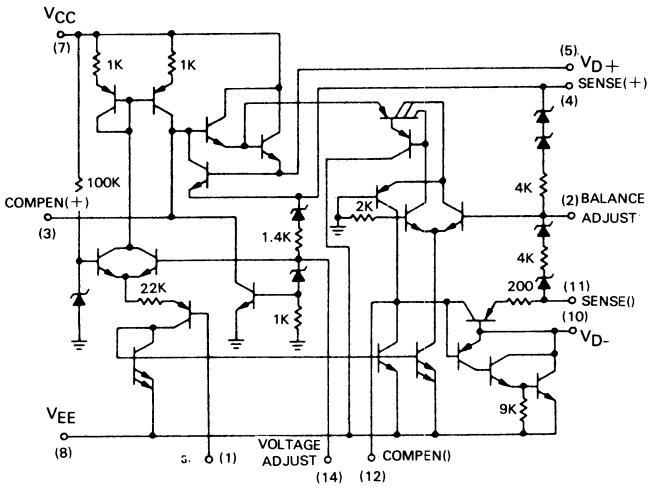
100000544

Dual ±15-Volt 100 mA Voltage Regulator

LOGIC DIAGRAM



The 100000544 is a dual polarity tracking voltage regulator. It is set internally to provide balanced positive and negative 15-volt output voltages for currents up to 100 mA. An external adjustment is provided for changing both outputs simultaneously from 8.0 to 20 volts. The 100000544 can use input voltages up to ±30 volts. Provision is made for adjustable current limiting. The device is in a ceramic package, and has 14 pins.

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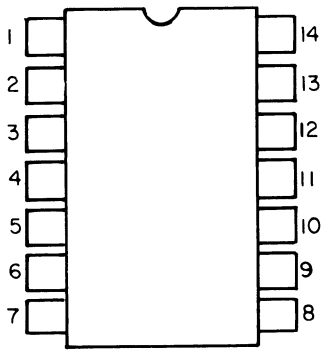
100000545

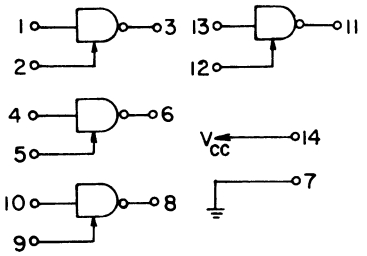
Quad Line Receiver

PIN CONFIGURATION



$Y = \overline{AE}$

LOGIC DIAGRAM

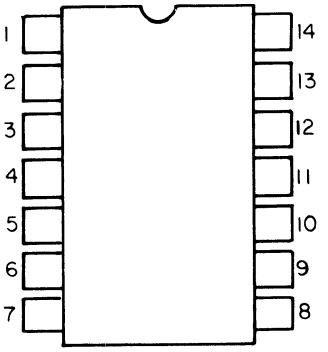


The 100000545 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

100000546

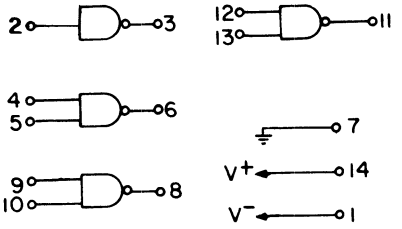
Quad MDTL Line Driver

PIN CONFIGURATION



$Y = \overline{AB}$

LOGIC DIAGRAM



The 100000546 is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment in conformance with EIA Standard No. RS-232C.

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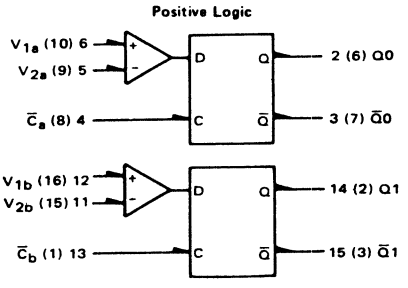
100000548

Dual A/D Comparator

BLOCK DIAGRAM



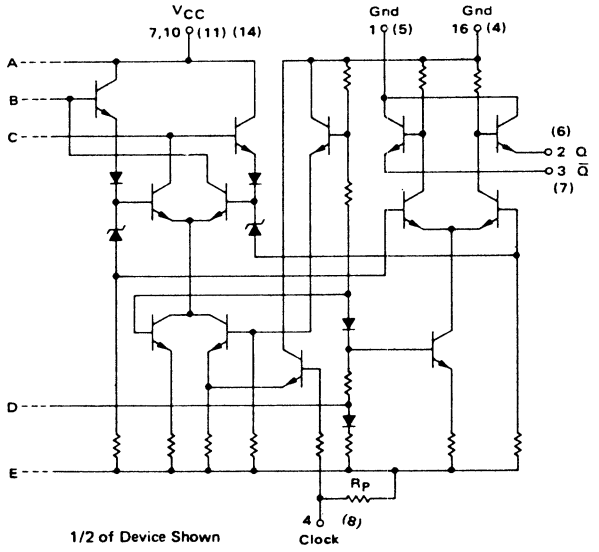
V_{CC} = +5.0 V = Pin 7,10 - (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1,16 (4) (5)

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

LOGIC DIAGRAM



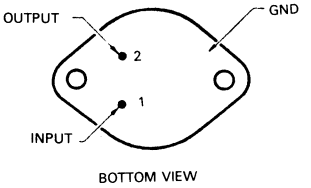
The 100000548 is a very high speed comparator utilizing differential amplifier inputs to sense analog signals above or below a reference level.

When the clock input $\overline{Ca}$ ($\overline{Cb}$) is high, Q0 (Q1) will be high if V1a > V1b (V2a > V2b). The outputs are latched in their present state on the high-to-low clock transition.

100000549

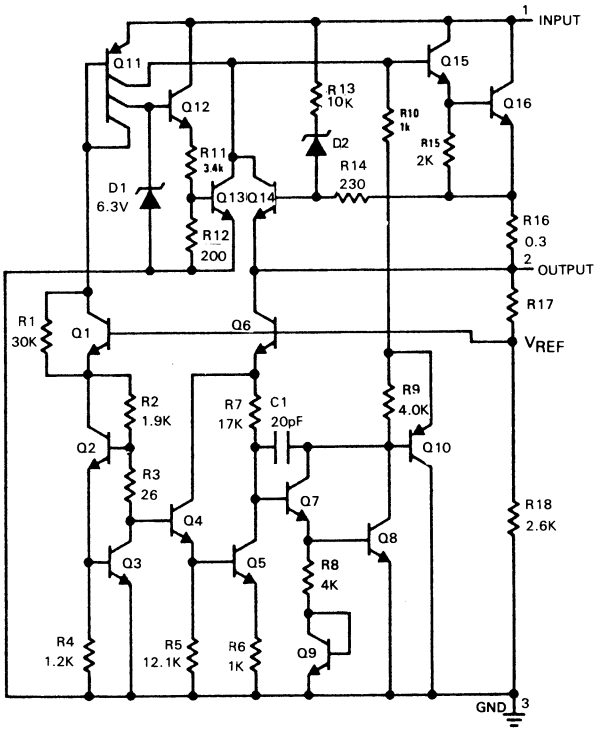
+12V 1.5A, 3% Fixed Voltage Regulator

PIN CONFIGURATION



BOTTOM VIEW

LOGIC DIAGRAM



The 100000549 is a three terminal 12-volt fixed voltage regulator which can provide 1.5A with adequate heat sinking. It features a current limiter and an internal thermal overload protection circuit.

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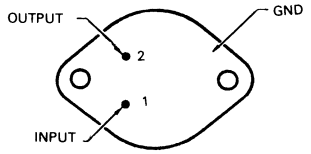
100000564

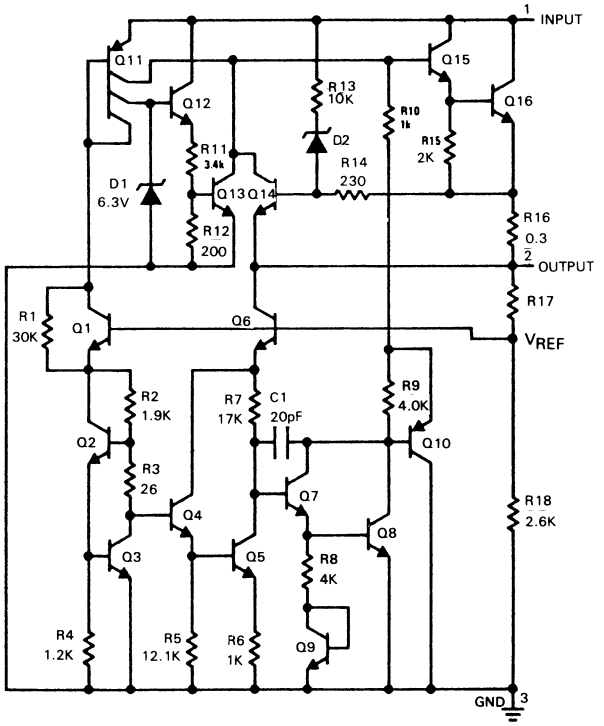
+5V 1.5A, 3% Fixed Voltage Regulator

PIN CONFIGURATION



BOTTOM VIEW

LOGIC DIAGRAM

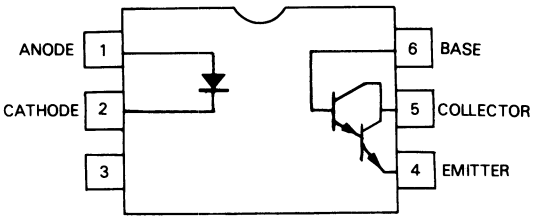


The 100000564 is a three terminal 5-volt fixed voltage regulator which can provide 1.5A with adequate heat sinking. It features a current limiter and an internal thermal overload protection circuit.

100000565

NPN Photo Darlington, Optically Coupled

PIN CONFIGURATION



This device is a light emitting diode, optically coupled to a photo transistor in a Darlington amplifier arrangement.

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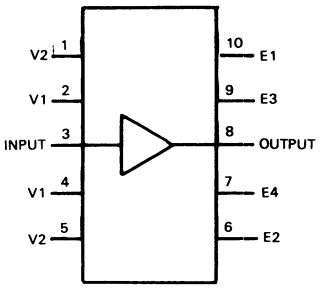
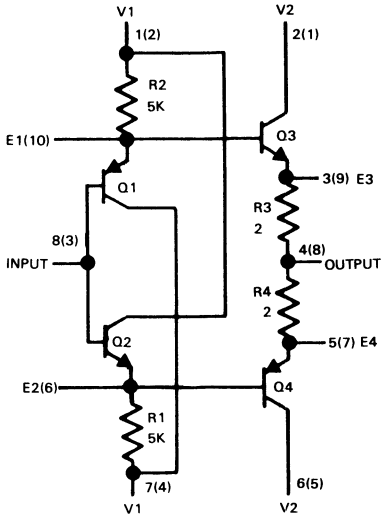
100000566

Current Amplifier

PIN CONFIGURATION



LOGIC DIAGRAM



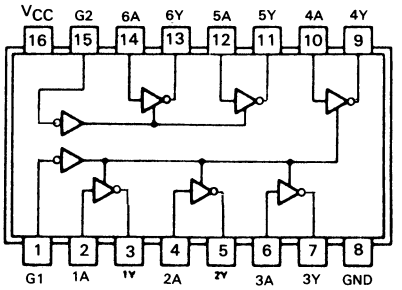
This device has:

- DC to 30 MHZ bondwidth
- Output voltage swing that approaches supply voltage
- 400 mA pulsed output current
- Slew rate is typically 200 VμS
- Operation from $\pm$5V to $\pm$20V

100000575

Hex Buffer Inverter

PIN CONFIGURATION



$$Y = \overline{\overline{A}\,\overline{G}} = A + G$$

The 100000575 contains six bus drivers. It has a 4-line and a 2-line enable input and 3-state, inverted data outputs.

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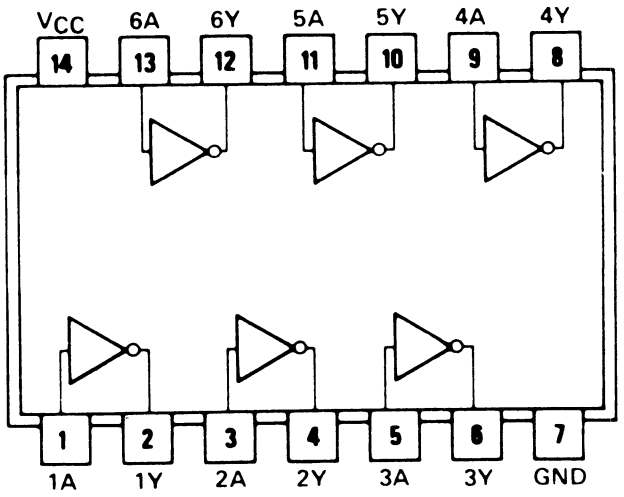
100000576

Hex Inverter

PIN CONFIGURATION



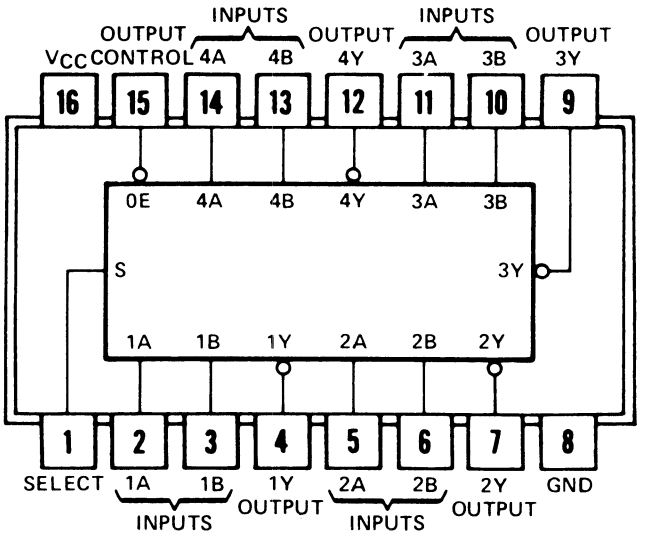
Positive logic: $Y = \overline{A}$

NOTE *The 100000576 is a low power Schottky device.*

100000577

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Output
Output Control	Select	A B	Y
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

NOTE *The 100000577 is a low power Schottky device.*

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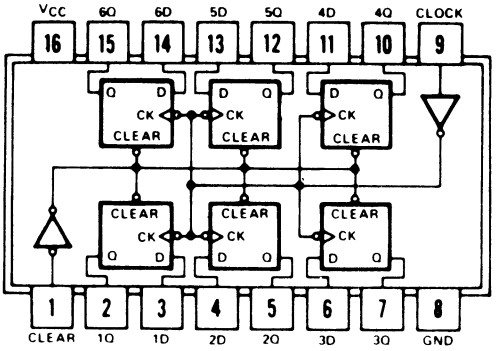
100000578

Hex D-Type Flip-Flop with Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

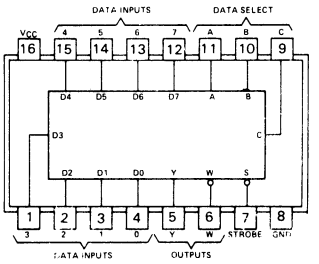
Notes:

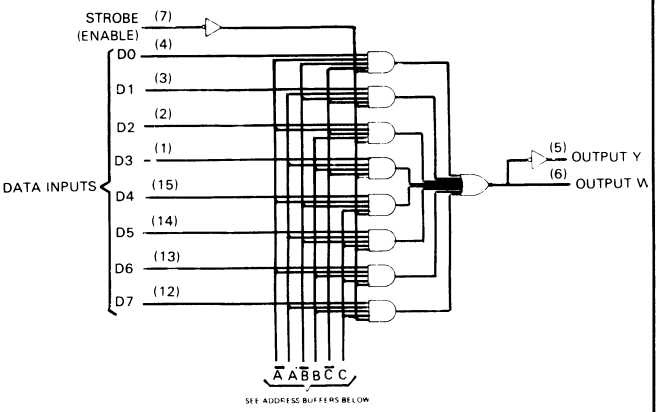
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

NOTE *The 100000578 is a low power Schottky device.*

100000579

Data Selector/Multiplexer





INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

The 100000579 contains full on-chip binary decoding to select one-of-eight data sources. It has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output low.

NOTE *The 100000579 is a low power Schottky device.*

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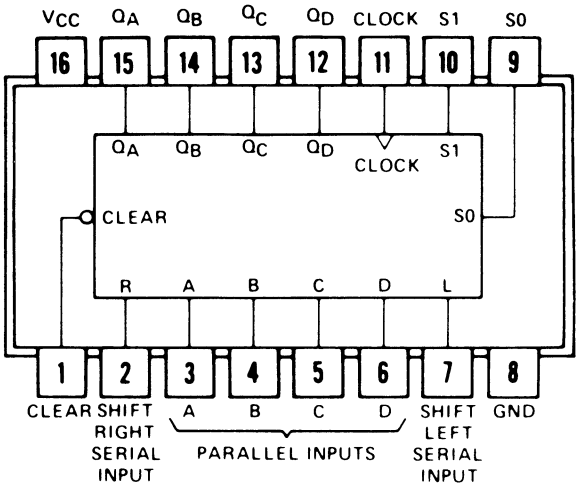
100000580

4-Bit Bidirectional Universal Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL							
	S_1	S_0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

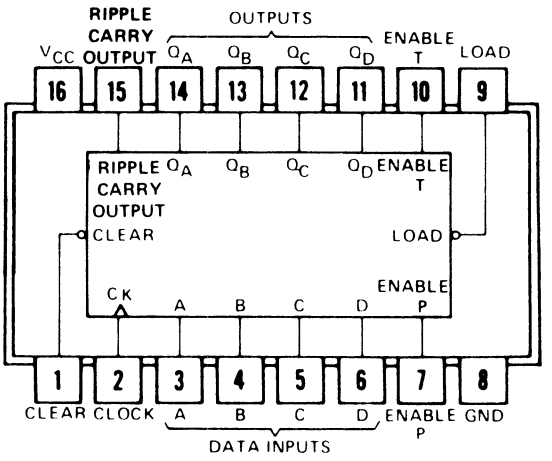
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

NOTE *The 100000580 is a low power Schottky device.*

100000581

Synchronous 4-Bit Counter

PIN CONFIGURATION



Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

NOTE *The 100000581 is a low power Schottky device.*

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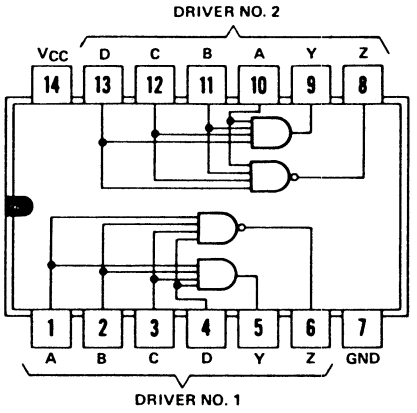
100000582

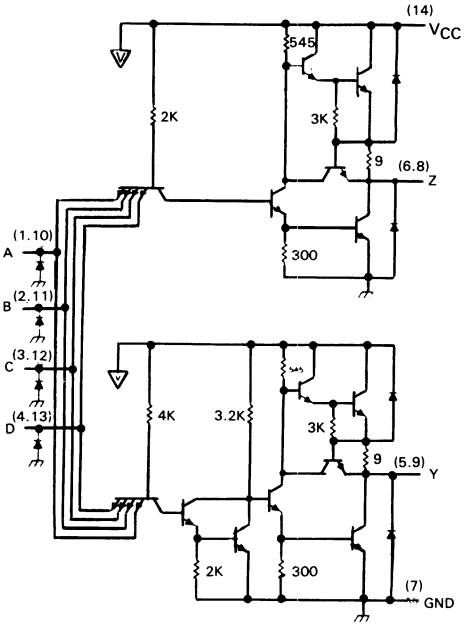
Dual Differential Line Drivers

PIN CONFIGURATION



positive logic: $Y = ABCD$, $Z = \overline{ABCD}$

LOGIC DIAGRAM
(each driver)



Resistor values shown are nominal and in ohms.

▽ . . . V_{CC} bus

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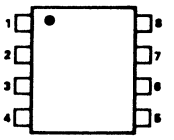
100000584

Dual 128-Bit Static Shift Register

PIN CONFIGURATION



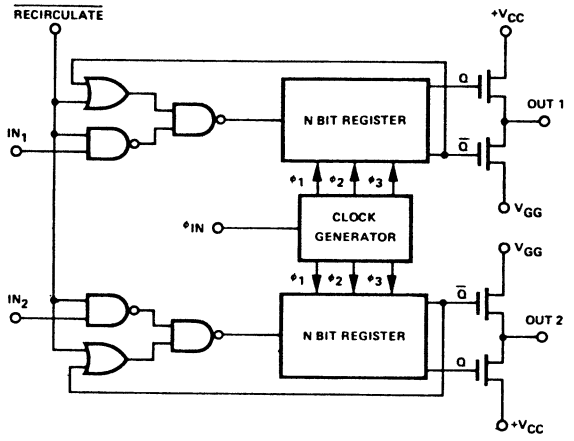
1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
8. V_{CC}
7. IN_2
6. OUT_2
5. ϕIN

TRUTH TABLE

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

BLOCK DIAGRAM

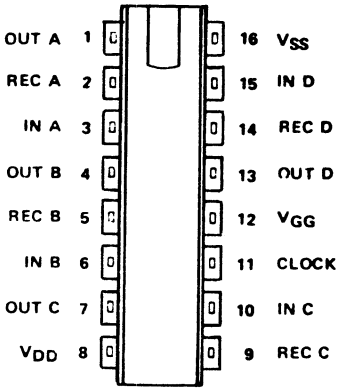


The 100000584 contains two 128-bit static shift registers. The clock and the signal inputs of these registers can be driven directly by MOS or bipolar integrated circuits. The registers have push-pull outputs.

100000585

Quad 80-Bit Dynamic Shift Register

PIN CONFIGURATION



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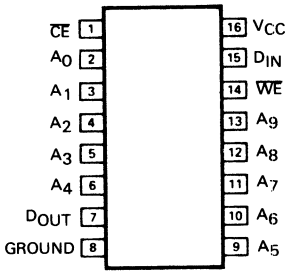
100000586

1024 x 1 - Bit Bipolar RAM

PIN CONFIGURATION

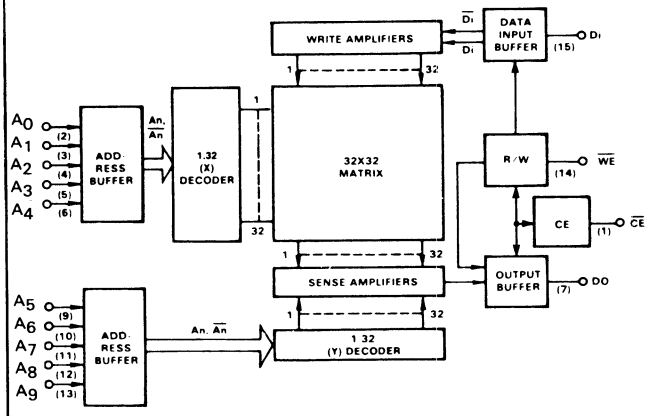


TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D	D_{OUT}
Read	0	1	X	Stored data
Write "0"	0	0	0	High-Z
Write "1"	0	0	1	High-Z
Disabled	1	X	X	High-Z

X = Don't care.

BLOCK DIAGRAM



The 100000586 is a 1024-bit random access memory. It features on-chip address decoding, a chip enable, an tri-state non-inverting outputs.

NOTE *The 100000586 is a Schottky device.*

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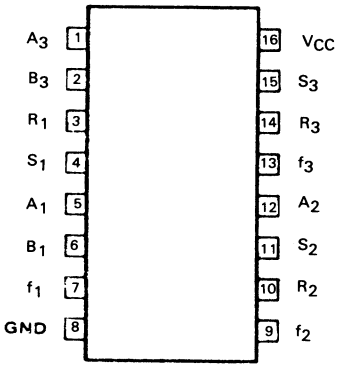
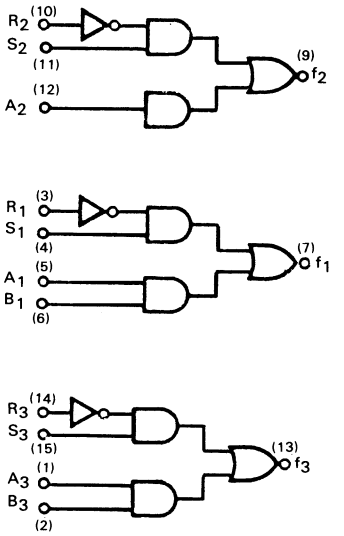
100000587

Triple Line Receiver with Hysteresis

PIN CONFIGURATION



LOGIC DIAGRAM

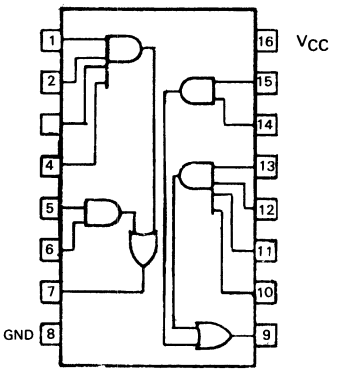


$$Y = \overline{(\bar{A}B) + (CD)}$$

100000588

Dual Line Driver

PIN CONFIGURATION



$$Y = (ABCD) + (EF)$$

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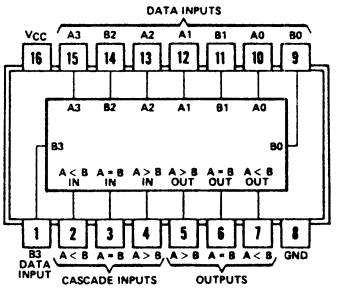
100000589

4-Bit Magnitude Comparators

PIN CONFIGURATION



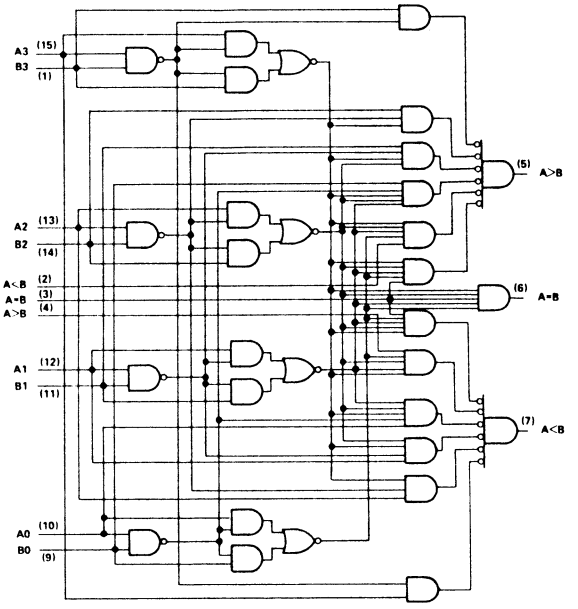
positive logic: see function tables

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



The 100000589 is a 4-bit magnitude comparator which compares straight binary and straight BCD (8-4-2-1) codes. Two 4-bit words (A,B) are compared and the following decisions concerning them are available at the outputs: A > B, A < B, and A = B. This device can be expanded to compare any number of bits without using external gates. To do this, the outputs of the device handling the less-significant bits are connected to the corresponding outputs of the device handling the more-significant bits. The A = B input of the device handling the least-significant bits must have a high-voltage applied to it. The cascading paths are implemented with only a two-gate-level delay to reduce the comparision times for longer words.

NOTE *The 100000589 is a low power Schottky device.*

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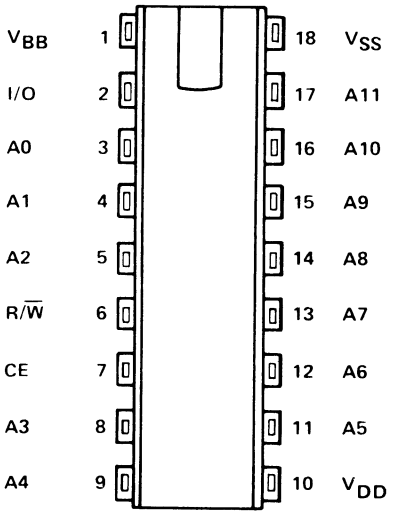
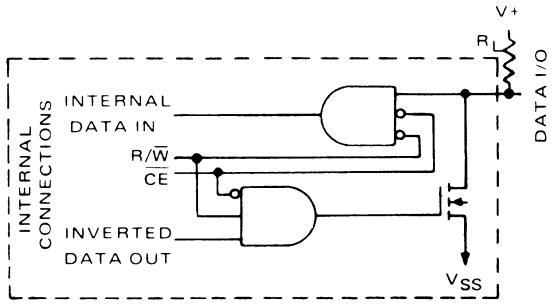
100000590

4096 x 1-Bit Dynamic RAM

PIN CONFIGURATION



BLOCK DIAGRAM

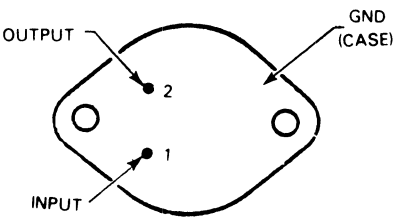


All inputs except the chip-enable are fully TTL-compatible and require no pull-up resistors. The TTL-compatible open-drain buffer is guaranteed to drive 1 TTL gate. The low capacitance of the address and control inputs precludes the need for specialized drivers. The 100000590 uses only one clock (chip-enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can by driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance. This NMOS device has tri-state output.

100000591

+5 Volt, 3 amp, 30W, 5% Regulator

PIN CONFIGURATION



BOTTOM VIEW

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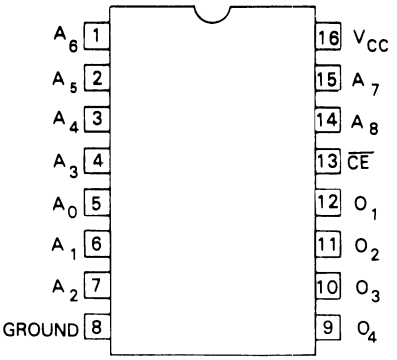
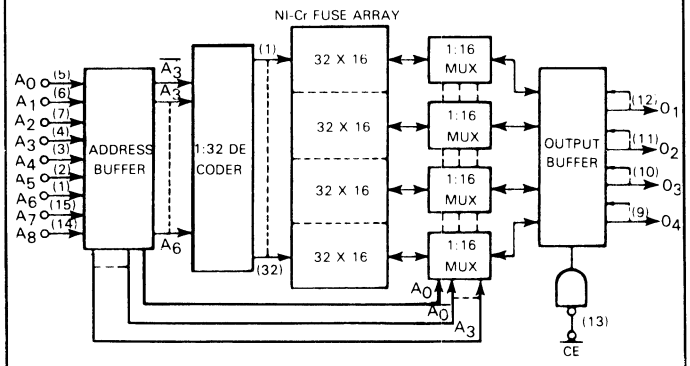
100000592

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

NOTE *The 100000592 is a Schottky device.*

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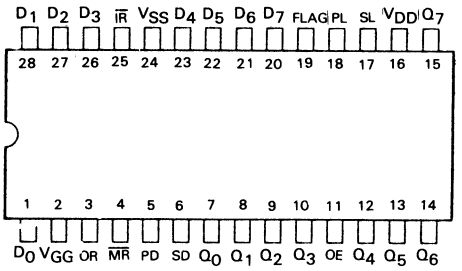
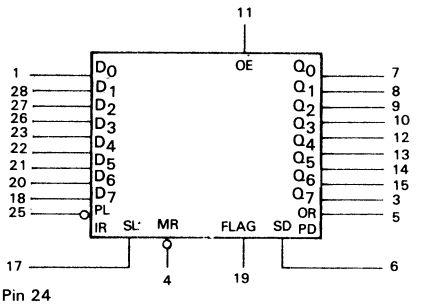
100000593

32 x 8 First-In First-Out Memory

PIN CONFIGURATION

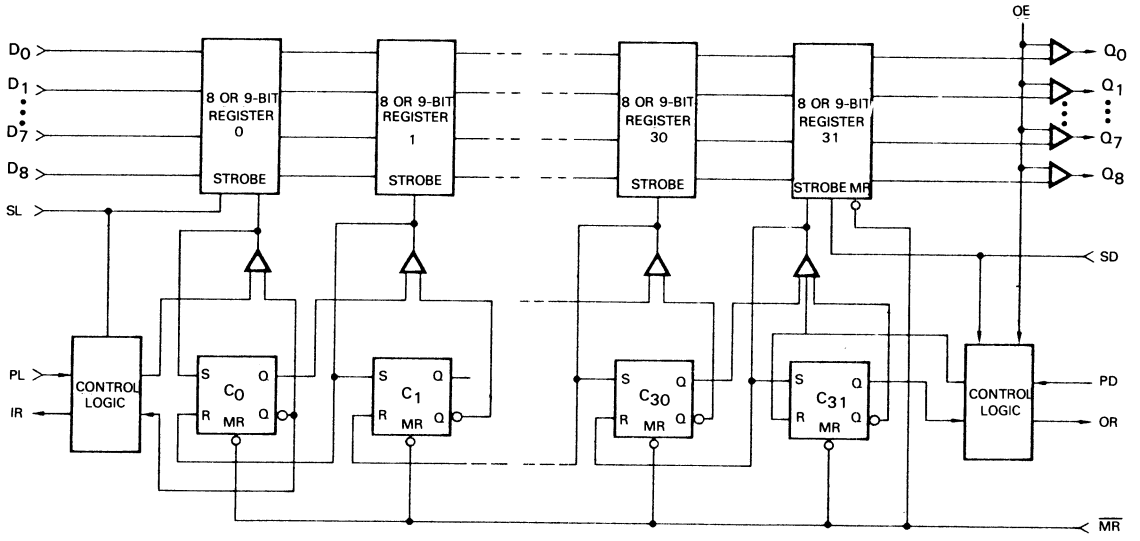


LOGIC SYMBOLS



V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2

BLOCK DIAGRAM



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100000593
(Continued)

The 100000593 is a 32 word 8-bit first-in-first-out (FIFO) memory. It features three independent read and write controls and tri-state outputs which are controlled by an output enable (OE). It consists of 32 data registers and one 32-bit control register (see block diagram). The control register determines the movement of data through the data registers. A "1" in any control register bit indicates that a data word is stored in the corresponding data register. Whenever the nth control register bit contains a 1, a strobe is generated which transfers the data from the nth data register into the (n+1)th data register, clears the nth control register and sets the (n+1)th control register bit. In this way, data moves up through the data registers to the outputs as long as there are empty data registers above it. It stops moving up when the control register bit for the next data register contains a "1".

Initially data is loaded into the first data register via the data inputs on a low-to-high transition of the parallel load input (PL). The corresponding control register bit is set to "1" and the input ready output (IR) goes low. A low on IR indicates that the first data register is unable to accept data. If the second data register is empty, then the moving up process begins when PL goes low. IR will go high to indicate that the FIFO can accept another word.

Output ready (OR) goes high when the control register bit for the last data register is set to "1". It indicates that there is valid data on the outputs. A parallel dump command (PD) outputs the data word and clears the last control register bit to allow data to move up again.

A flag output (FLAG) indicates whether the FIFO is more or less than half full. This flag goes high when the 13th, 14th, 15th, or 16th word is loaded into the FIFO and stays high until there are less than 15+1/-2 words in the memory.

The master reset ($\overline{MR}$) clears all the control register bits and sets all the outputs low.

The 100000593 can also read or write serial bit streams. In this case, it acts like a 256 by 1 bit FIFO. Serial data is loaded via the D0 input using the serial load command (SL). The remaining data inputs (D1-D7) must be grounded. The SL command operates like the PL command. Data shifts through the first data register until 8 bits have been loaded. These bits move up from data register to data register as they would if they had been parallel loaded.

When the serial load or serial dump command are used, the corresponding parallel control line must be grounded, and likewise, when the parallel load or parallel dump commands are used, the corresponding serial control line must be grounded.

Because the input ready signal is active low a peculiarity occurs when several devices are placed end-to-end. When the second unit of two 100000593s fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n FIFOs connected end-to-end store 31n+1 words (instead of 32n).

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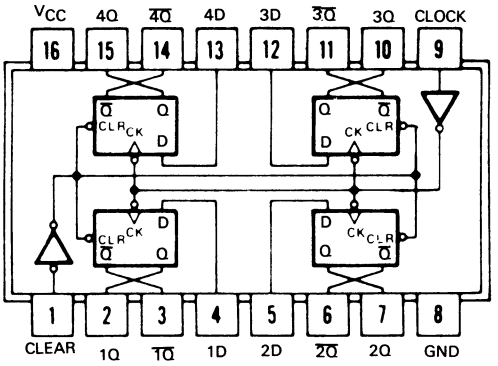
100000594

Quad D Flip Flop with Clear



FUNCTION TABLE

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

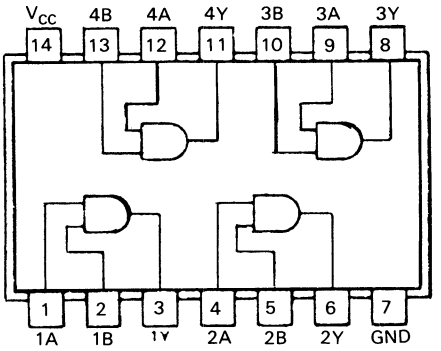
Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

NOTE *The 100000594 is a low power Schottky device.*

100000595

Quad 2-Input Positive-AND Gate



NOTE *The 100000595 is a low power Schottky device.*

Y = AB

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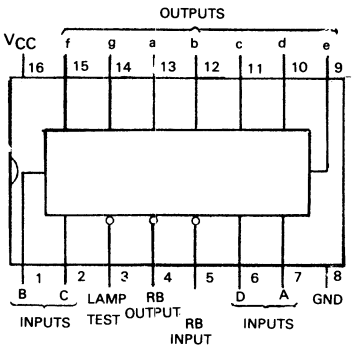
100000596

BCD-To-7-Segment LED Driver

PIN CONFIGURATION



TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical "1" when output functions 0–15 are desired, and the ripple-blanking input (RBI) must be open or at a logical "1" if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical "0" is applied directly to the blanking input (forced condition) all segment outputs go to a logical "1" regardless of the state of any other input condition.

Note 3: When the ripple-blanking input (RBI) and inputs A, B, C and D are at logical "0," with the lamp test input at logical "1," all segment outputs go to a logical "1" and the ripple-blanking output (RBO) goes to a logical "0" (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical "1," and a logical "0" is applied to the lamp-test input, all segment outputs go to a logical "0."

This device decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format and BCD numbers above 9 into unique patterns that verify operation.

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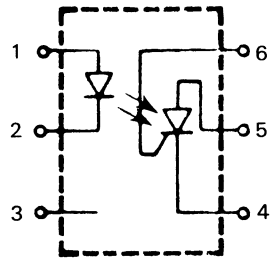
100000597

Ga As Infrared Emitting Diode & Light Activated SCR

PIN CONFIGURATION

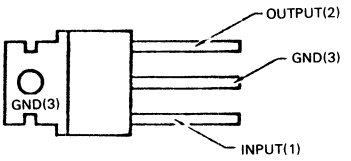


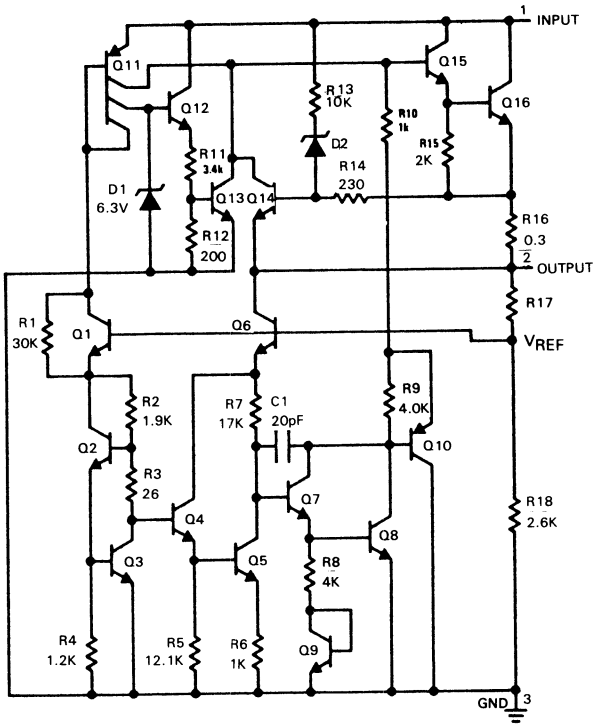
The 100000597 is a gallium arsenide, infrared emitting diode coupled with a light activated silicon controlled rectifier.

100000598

+12V 1.5A, 3% Fixed Voltage Regulator

PIN CONFIGURATION





The 100000598 is a three terminal 12-volt fixed voltage regulator which can provide 1.5A with adequate heat sinking. It features a current limiter and an internal thermal overload protection circuit.

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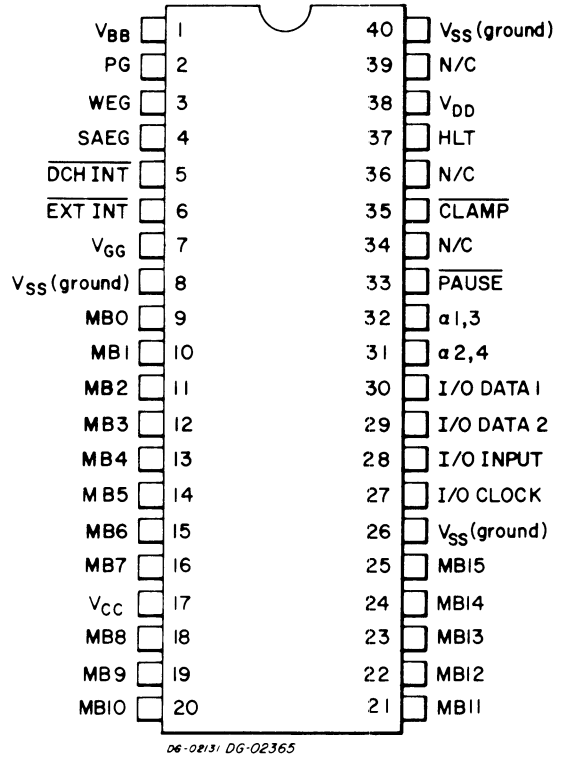
100000601

Microprocessor

PIN CONFIGURATION



DG-02131 DG-02365

The microprocessor (CPU) is a complete central-processing unit in a 40-pin package. It contains all the control logic and data manipulation logic required to perform the data processing operations typically performed by the central processing unit of a minicomputer.

It has an extensive and proven instructtion set, a program interrupt facility and a data channel facility similar to those of Data General's NOVA 3 computer. The instruction set includes memory reference instructions (including instructions that alter program flow), arithmetic/logical instructions, multiply/divide instructions, stack instructions, trap instructions and I/O instructions. The program interrupt facility alters program flow at the request of a peripheral. The data channel facility transfers data between a peripheral and a memory element at the request of the peripheral.

The CPU contains four 16-bit accumulators, a 15-bit program counter, a 15-bit stack pointer and a 15-bit frame pointer.

The CPU communicates with 32,768 memory locations via three memory control pins and sixteen memory address/data pins. During one memory operation, it may transfer sixteen bits of data from and/or to one memory location.

The CPU communicates with 61 peripherals via four I/O data pins and two I/O request pins. During one I/O operation, it transfers sixteen bits of data to or from one peripheral.

The CPU is designed to operate with the other circuits in the microNOVA product line. It is ordinarily connected to memory transceivers and an I/O transceiver to form a CPU module. Furthermore, the CPU is designed so that memory elements that communicate with the CPU via the memory control pins and memory address/data pins may be conveniently formed of 4K dynamic RAMs. Similarly, peripherals that communicate with the CPU via the I/O data pins and I/O request pins may be conveniently designed around an I/O controller.

For more information see document 014-000074, *microNOVA Integrated Circuits.*

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100000601 (Continued)

Registers

The CPU stores information within itself in thirteen registers. The name of each register and the amount of information that is stored in it is listed in the following table.

Register	Size
accumulator 0	16 bits
accumulator 1	16 bits
accumulator 2	16 bits
accumulator 3	16 bits
stack pointer	15 bits
frame pointer	15 bits
program counter	15 bits
carry bit	1 bit
interrupt enable bit	1 bit
real-time-clock enable bit	1 bit
stack-overflow request bit	1 bit
real-time-clock request bit	1 bit
refresh address counter	6 bits

In registers that hold fifteen or sixteen bits of information, the bits are numbered. The bits in 15-bit registers are numbered from 1 to 15. The bits in 16-bit registers are numbered from 0 to 15.

Pins

The CPU transmits and receives information via thirty of its forty pins. (The other pins supply power to the CPU or are unused.) The thirty pins may be divided into functional groups as shown in the following table.

Functional Group	Pins
Clock Pins	alpha 1,3 alpha 2,4
Memory Control Pins	PG SAEG WEG
Memory Address/Data Pins	MB[0-15]
I/O Data Pins	I/O CLOCK I/O DATA1 I/O DATA2 I/O INPUT
I/O Request Pins	$\overline{\text{EXT INT}}$ $\overline{\text{DCH INT}}$
Other Pins	CLAMP HALT $\overline{\text{PAUSE}}$

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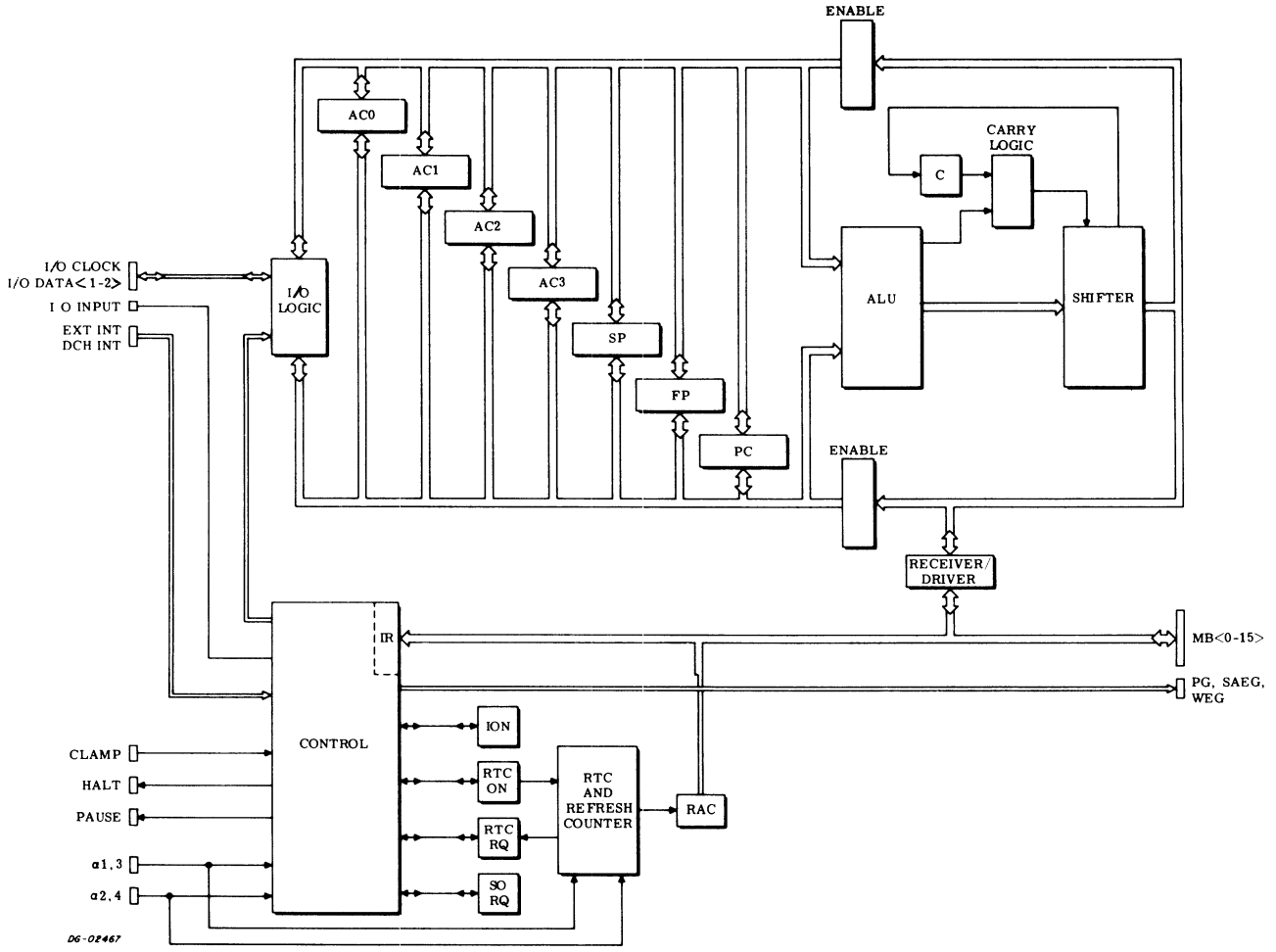
100000601
(Continued)

BLOCK DIAGRAM



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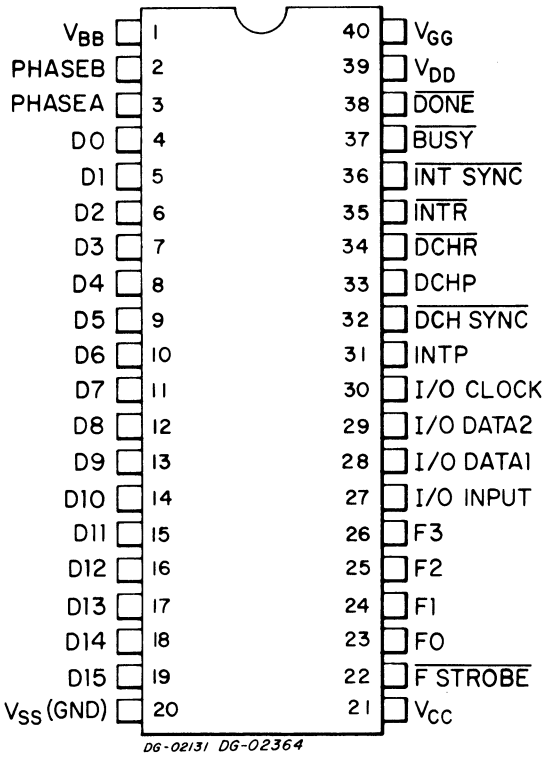
100000603

I/O Controller

PIN CONFIGURATION



DG-02131 DG-02364

The I/O controller (IOC) is a circuit that facilitates the design of peripherals that operate in the microNOVA computer system. The IOC is mounted in a 40-pin package.

The IOC performs operations that are commonly performed by peripherals in the microNOVA computer system. It decodes and executes I/O commands and data-channel-acknowledge codes received from the CPU. It transforms serial format in which the CPU transmits data to parallel format convenient within peripherals and vice-versa. It makes program interrupt and data channel requests in accordance with the microNOVA system constraints related to the request enable code and interrupt and data channel priority chains among controllers.

Pins

The pins via which the IOC receives and transmits information may be divided into groups as shown in the following table:

Group	Pins	Purpose
clock pins	PHASE A PHASE B	receive timing information
I/O data pins	I/O CLOCK I/O DATA1 I/O DATA2 I/O INPUT	receive and transmit data on I/O bus (via IOC I/O transceiver)
priority pins	INTP DCHP	receive priority information
function code pins	$\overline{\text{FSTROBE}}$ F[0-3]	transmit control information to other components
device data pins	D[0-15]	transmit data to other components or peripherals and receive data from them
busy/done, request pins	$\overline{\text{BUSY}}$ $\overline{\text{DONE}}$ $\overline{\text{INT}}$ $\overline{\text{INTR}}$	transmit and receive control pulses to/from busy/done logic and interrupt-request logic
data channel request pins	$\overline{\text{DCH SYNC}}$ DCHR	receive data channel requests from other components or peripherals and transmit them on I/O bus

For more information see document 014-000074, *microNOVA Integrated Circuits.*

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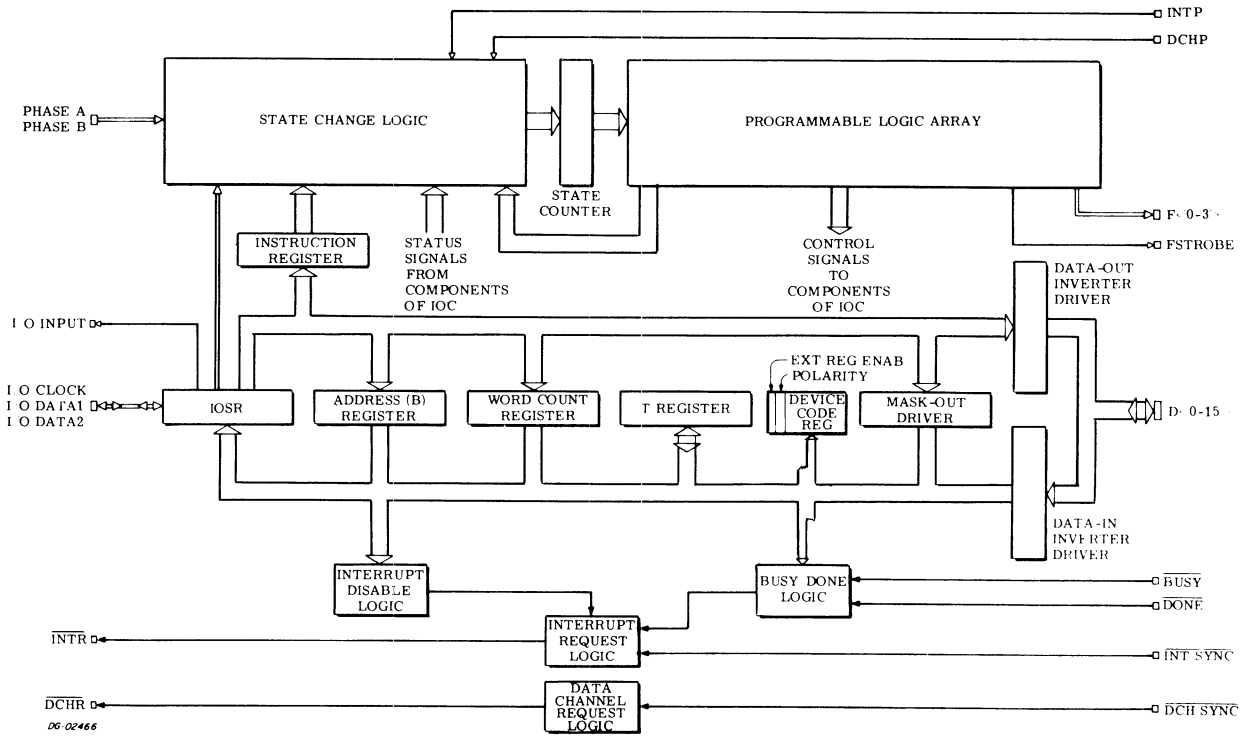
100000603
(Continued)

BLOCK DIAGRAM



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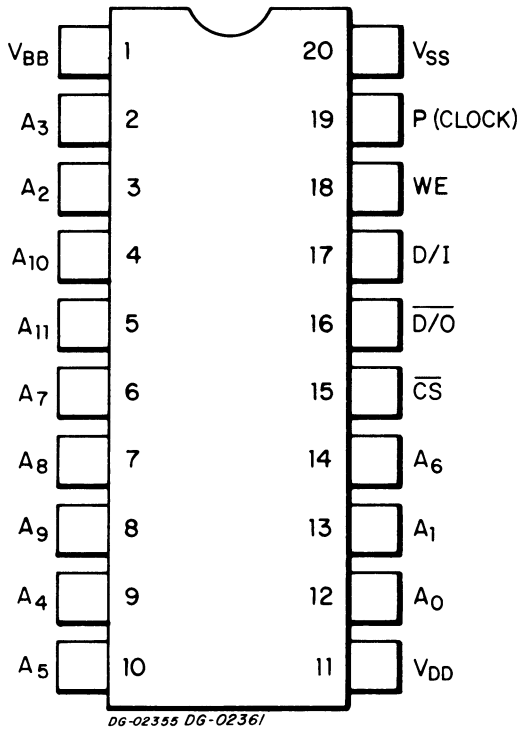
100000606

4-K RAM

PIN CONFIGURATION



DG-02355 DG-02361

4K DYNAMIC RAM

The 4K dynamic RAM is a 4096-bit dynamic random-access memory in a 20-pin package. It performs read, write and refresh operations. A read operation may be performed in 300 nanoseconds; a write or refresh operation may be performed in 600 nanoseconds.

Read and write operations are performed on one bit at a time. The bit to be read or written is selected by a 12-bit address.

Refresh operations are performed on sixty-four bits simultaneously; all bits in the RAM must be refreshed every 2.4 milliseconds. The bits to be refreshed are selected by a 6-bit address.

The RAM receives addresses via twelve address pins. An address is latched at the beginning of a read, write or refresh operation so that it need not be maintained on the pins for the duration of the operation.

The RAM is designed so that sixteen of them may be conveniently connected to form a 4K x 16-bit memory module that operates in the microNOVA computer system. In such a module, the RAMs are supported by two address drivers and four sense amplifiers.

Pins

The pins of the memory and brief descriptions of their functions are given in the following table.

TRUTH TABLE

Pin	function
P	clock input
$\overline{CS}$	chip select
WE	write-enable
A[0-11]	address inputs
D/O	data output
D/I	data input

For more information see document 014-000074, *microNOVA Integrated Circuits.*

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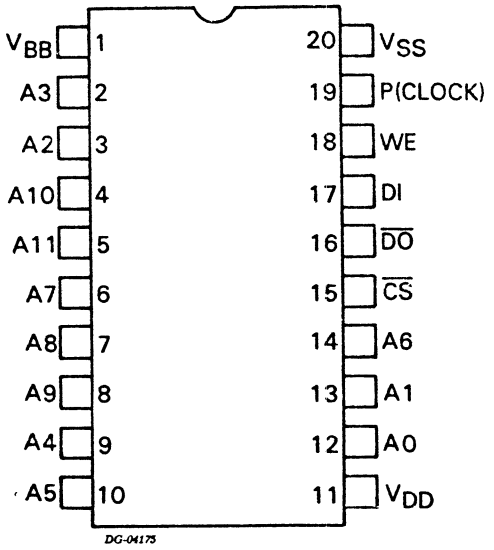
100000607 through 100000610

2K X 1 Dynamic Random Access Memory

PIN CONFIGURATION



NMOS DYNAMIC RANDOM ACCESS MEMORY IN A 20 PIN PLASTIC PACKAGE

ORGANIZED AS 2048 BY 1 BIT

FAST 180nS ACCESS TIME

FAST INTERNAL LATCHES FOR ADDRESS AND CHIP SELECT

REFRESHES 64 BITS AT A TIME

OPEN DRAIN OUTPUT

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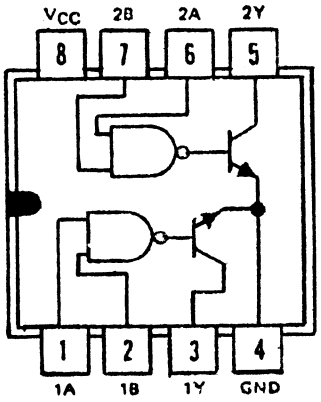
100000625

Dual Bus Driver

PIN CONFIGURATION



positive logic: Y = AB

TRUTH TABLE

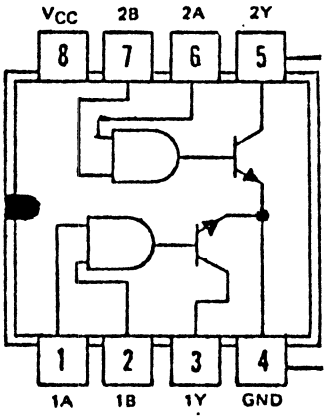
A	B	Y
L	L	L (ONSTATE)
L	H	L (ONSTATE)
H	L	L (ONSTATE)
H	H	H (OFFSTATE)

H = High Level
L = Low Level

100000626

Dual Bus Driver

PIN CONFIGURATION



$Y = \overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H (OFFSTATE)
L	H	H (OFFSTATE)
H	L	H (OFFSTATE)
H	H	L (ONSTATE)

H = High Level
L = Low Level

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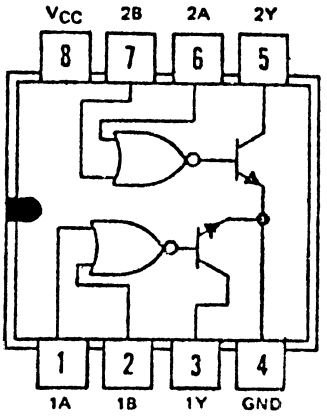
100000627

Dual Bus Driver

PIN CONFIGURATION



positive logic: $Y = A + B$

TRUTH TABLE

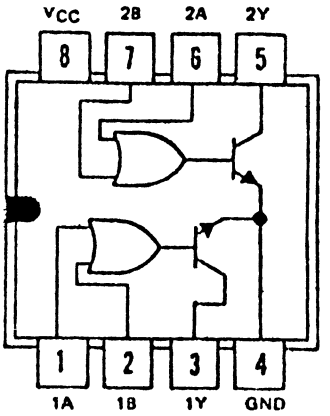
A	B	Y
L	L	L (ONSTATE)
L	H	H (OFFSTATE)
H	L	H (OFFSTATE)
H	H	H (OFFSTATE)

H = High Level
L = Low Level

100000628

Dual Bus Driver

PIN CONFIGURATION



positive logic: $Y = \overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H (OFFSTATE)
L	H	L (ONSTATE)
H	L	L (ONSTATE)
H	H	L (ONSTATE)

H = High Level
L = Low Level

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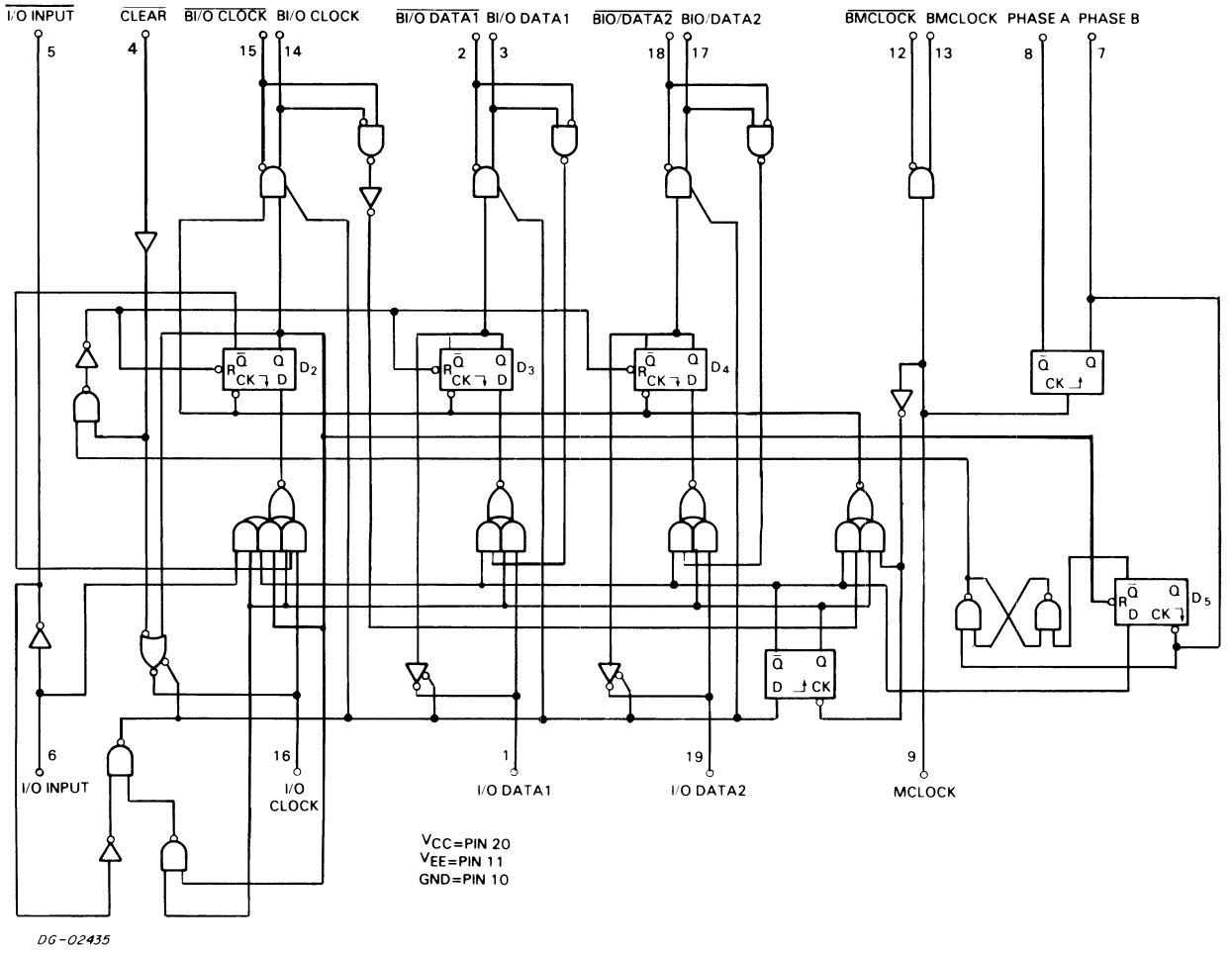
100000629

CPU I/O Transceiver

BLOCK DIAGRAM



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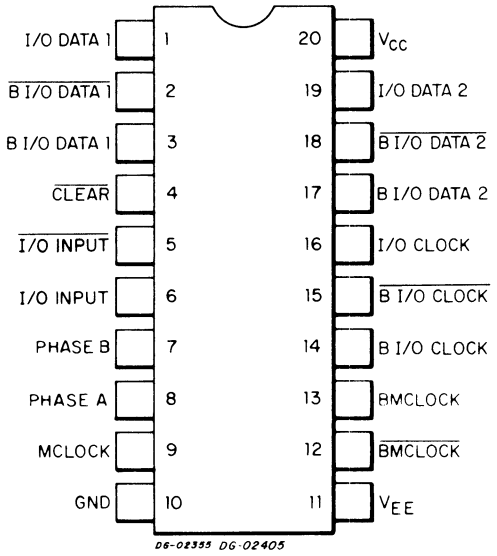
100000629 (Continued)

PIN CONFIGURATION

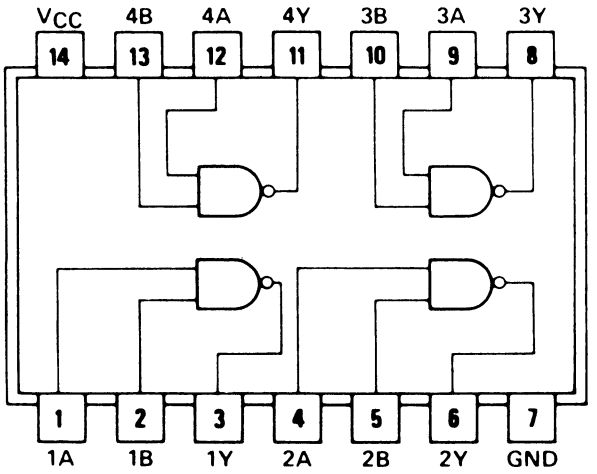


For more information see document 014-000074, *microNOVA Integrated Circuits.*

100000630

Quad 2-Input Positive-NAND Buffer with Open Collector Outputs

PIN CONFIGURATION



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

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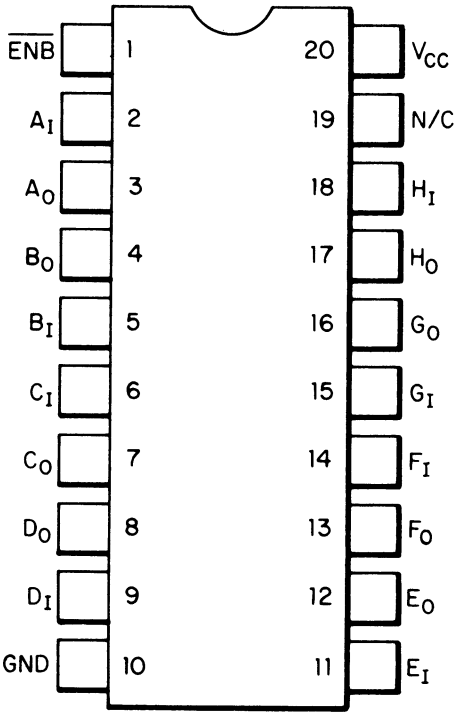
100000633

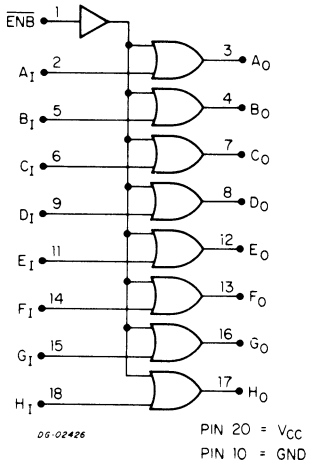
Octal Driver

PIN CONFIGURATION



$Y = A\overline{E}$

LOGIC DIAGRAM



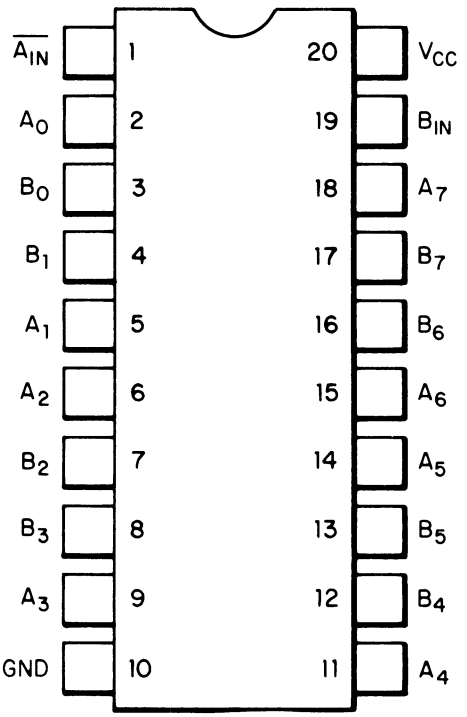
NOTE *The 100000633 has open collector output.*

For more information see document 014-000074, *microNOVA Integrated Circuits.*

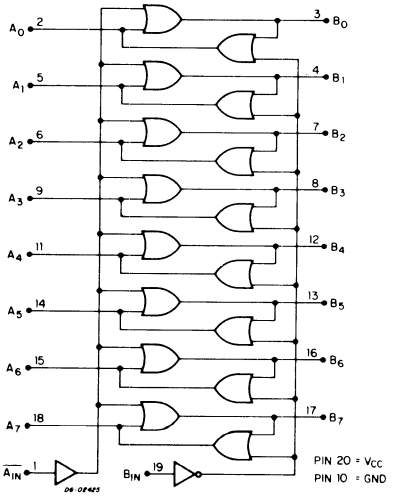
100000634

Memory Transceiver

PIN CONFIGURATION



LOGIC DIAGRAM



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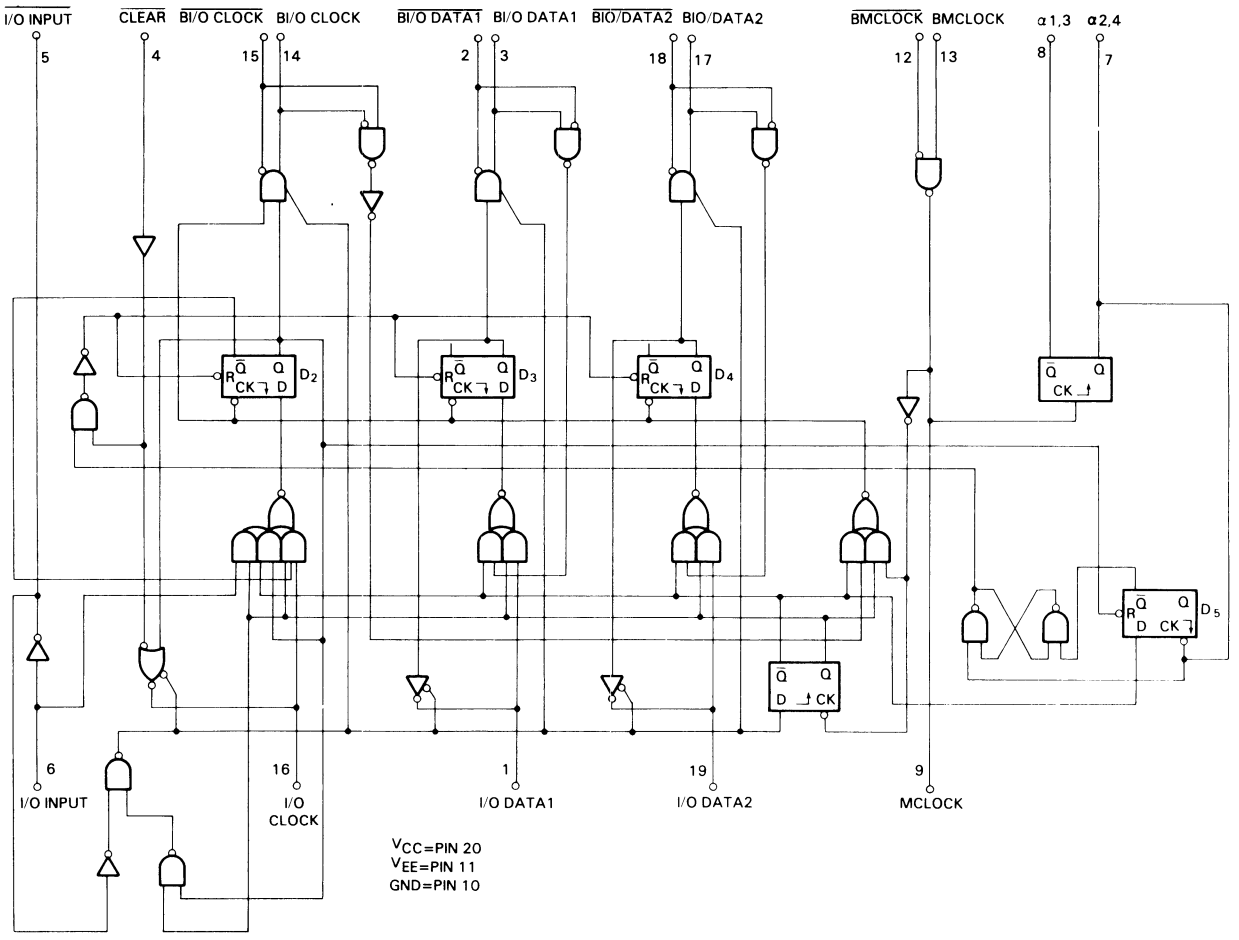
100000636

IOC I/O Transceiver

BLOCK DIAGRAM



DG 02346

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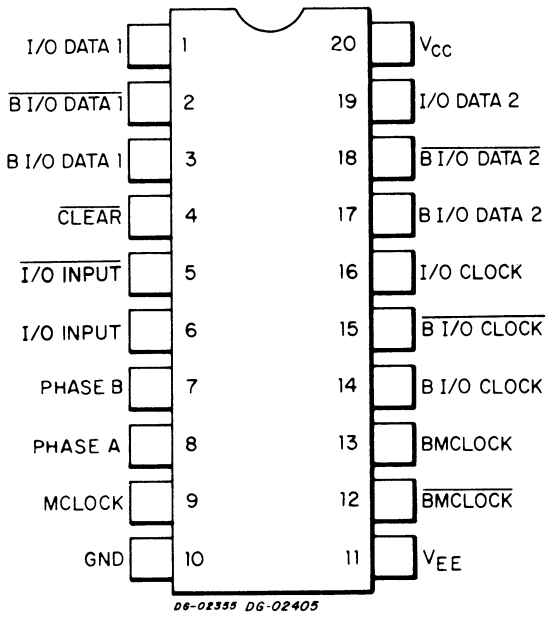
100000636 (Continued)

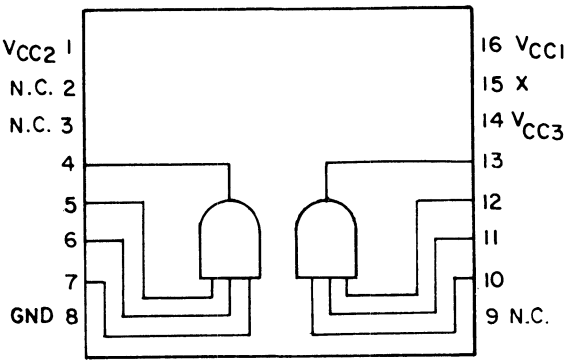
PIN CONFIGURATION



For more information see document 014-000074, *microNOVA Integrated Circuits.*

100000637 through 100000639

Dual Clock Driver



Y = ABC

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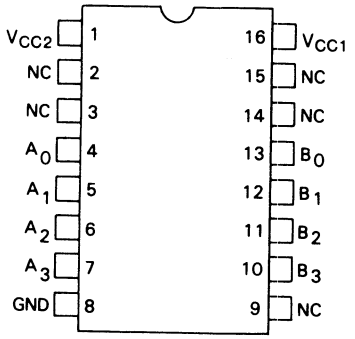
100000640

Dual CPU and IOC Clock Driver

PIN CONFIGURATION

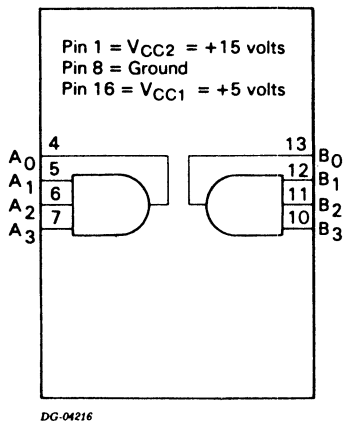


NC = no connection

DG-04215

$Y = ABC$

BLOCK DIAGRAM

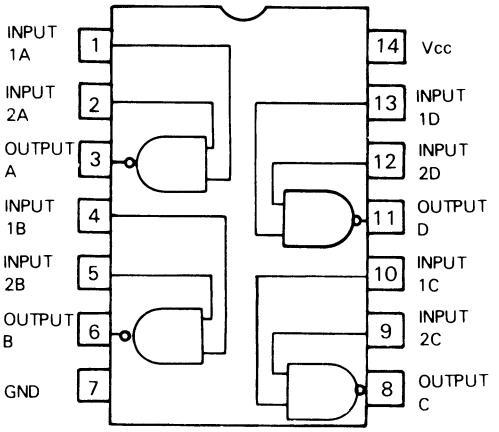


DG-04216

100000641

Quad NMOS Address Line Driver

PIN CONFIGURATION



$Y = \overline{AB}$

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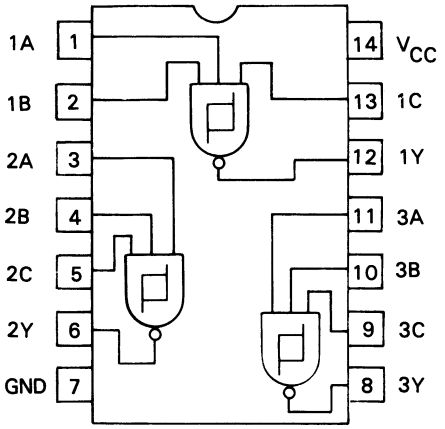
100000642

Triple-3 Input Nand-Schmitt Triggers

PIN CONFIGURATION



$Y = \overline{ABC}$

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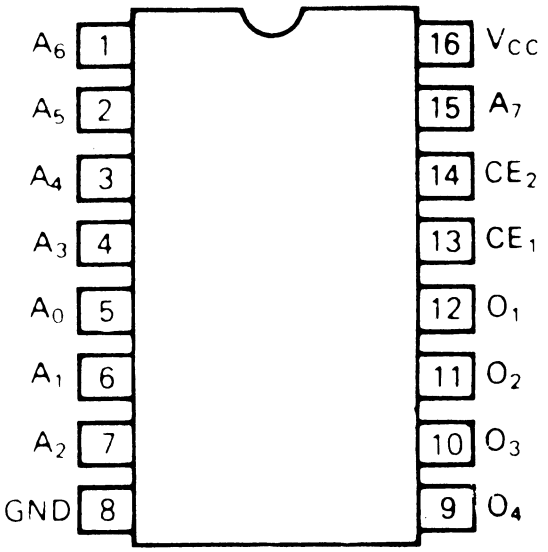
100000700 through 100000770

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



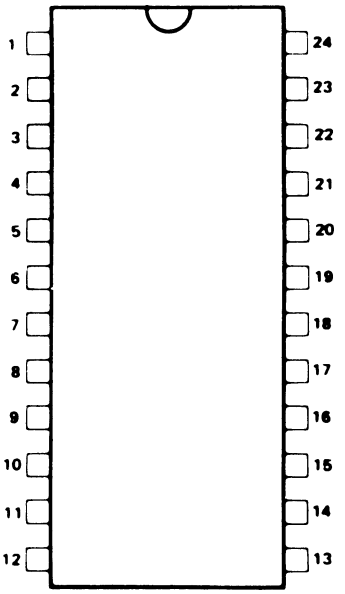
This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100000771

Character Generator

PIN CONFIGURATION



PIN DESIGNATIONS

1.	V_{BB}	24.	CS 1
2.	V_{DD}	23.	CS 2
3.	V_{GG}	22.	CS 3
4.	Address 7	21.	Out 9
5.	Out 8	20.	Out 7
6.	Out 6	19.	Out 5
7.	Out 4	18.	Out 3
8.	Out 2	17.	Out 1
9.	Address 6	16.	Out 10
10.	Address 5	15.	Address 2
11.	Address 4	14.	Address 1
12.	Address 3	13.	V_{SS}

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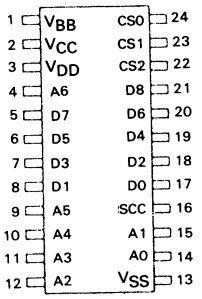
100000772 through 100000776

Column Select Character Generator

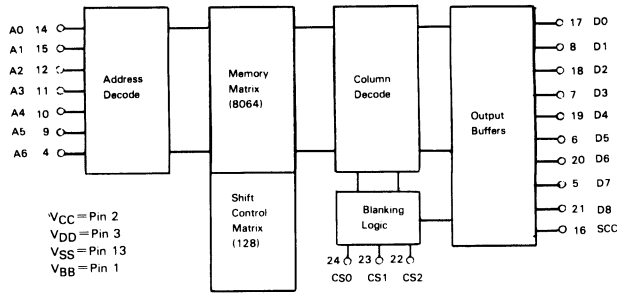
PIN CONFIGURATION



TRUTH TABLE

CS2	CS1	CS0	OUTPUT
0	0	0	0
0	0	1	C1
0	1	0	C2
0	1	1	C3
1	0	0	C4
1	0	1	C5
1	1	0	C6
1	1	1	C7

BLOCK DIAGRAM



These devices are mask-programmable 8192-bit vertical scan (column select) character generators. They contain 128 characters in a 7 x 9 matrix. A Shift Control Command (SCC) bit can be programmed so that a high logic level will appear at the SCC output, in addition to the coding at D0-D8, to indicate a character is to be shifted.

Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. A 7-bit address code (A0-A6) is used to select one of the 128 available characters programmed in the memory. To output a character addressed by A0-A6, a column select code (CS0-CS2) is sequentially applied (see truth table). Each column is read at outputs D0-D8.

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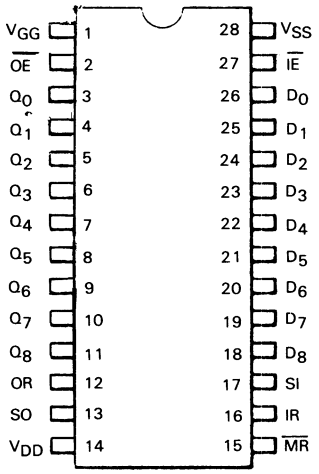
100000777

40 X 9 First-In First-Out Memory

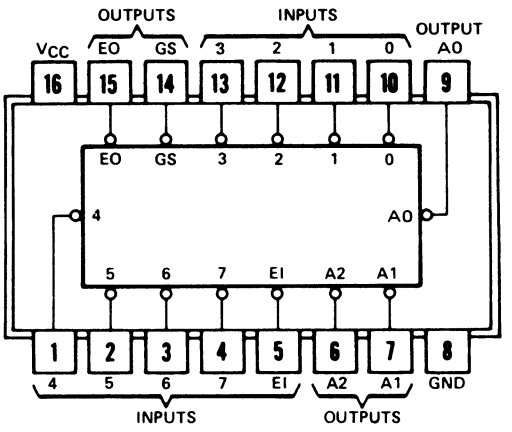
PIN CONFIGURATION



100000778

8-Line-To-3-Line Priority Encoder

PIN CONFIGURATION



FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

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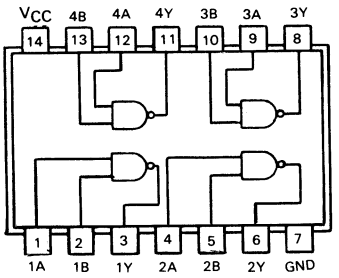
100000779

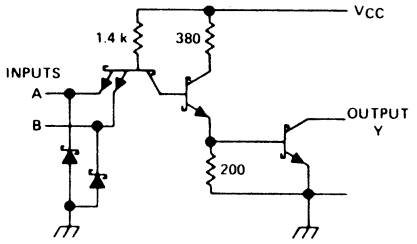
Quad 2-Input NAND Buffer

PIN CONFIGURATION



positive logic:
$Y = \overline{AB}$

LOGIC DIAGRAM



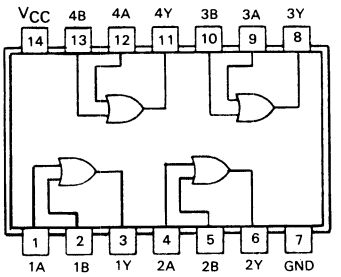
The 100000779 consists of four 2-input NAND buffers with open collector-outputs.

NOTE *The 100000779 is a Schottky device.*

100000780

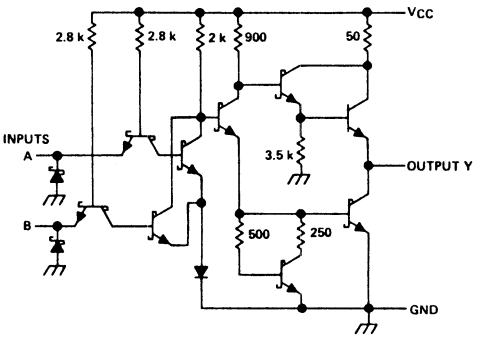
Quad 2-Input OR Gate

PIN CONFIGURATION



positive logic:
Y = A+B

LOGIC DIAGRAM



The 100000780 consists of four 2-input OR gates with totem-pole outputs.

NOTE *The 100000780 is a Schottky device.*

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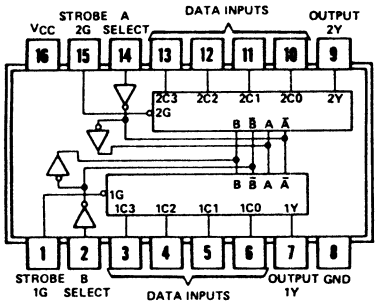
100000781

Dual 4-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



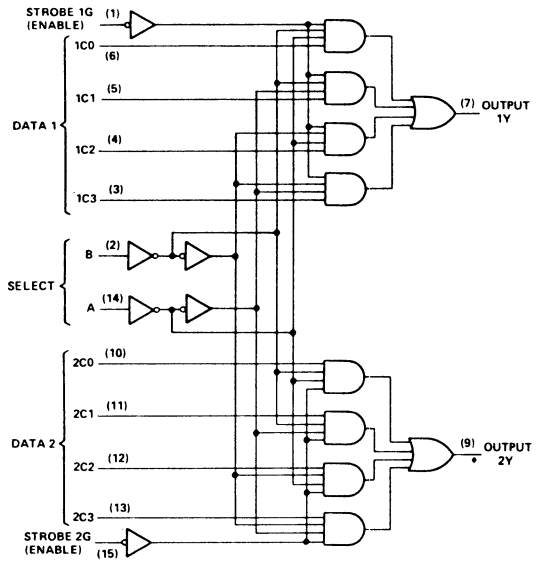
positive logic: see function table

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



The 100000781 contains inverters and drivers which provide complemetary, on-chip decoding data selection for the AND-OR-invert gates. Each of the two 4-line sections has its own strobe input. The outputs are high-fan-out, low impedance, totem-pole outputs.

NOTE *The 100000781 is a low power Schottky device.*

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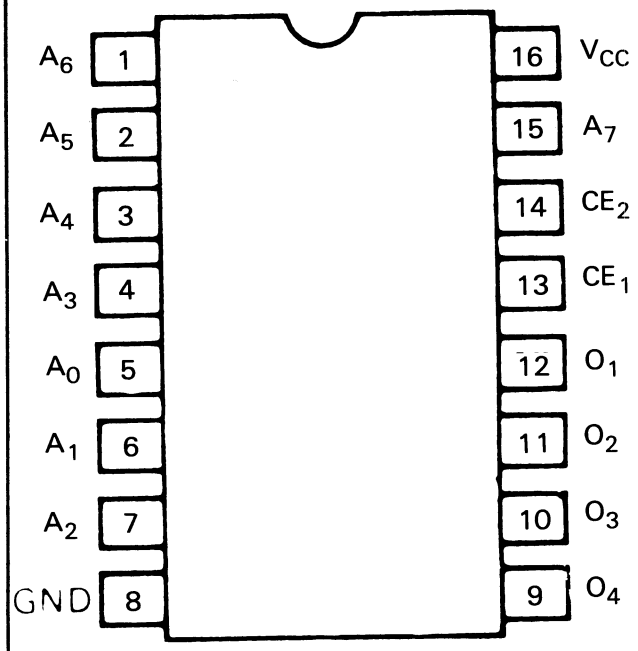
100000782 through 100000785

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



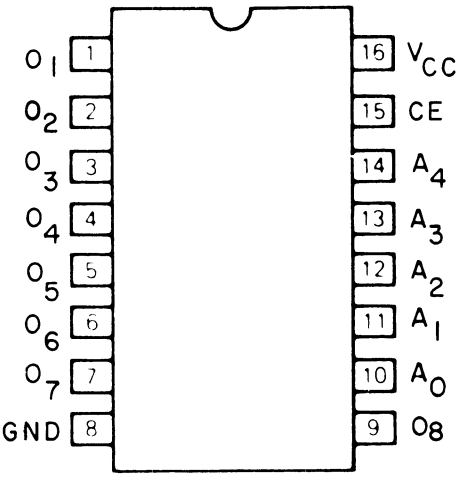
This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100000786 through 100000788

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

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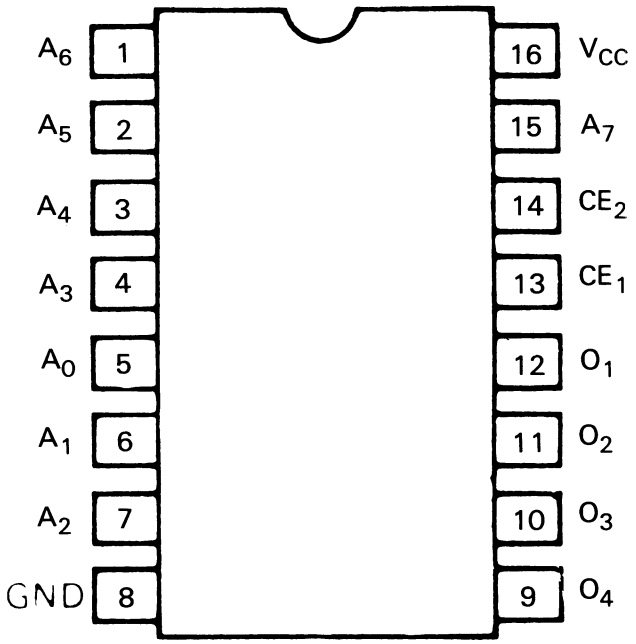
100000789 and 100000790

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



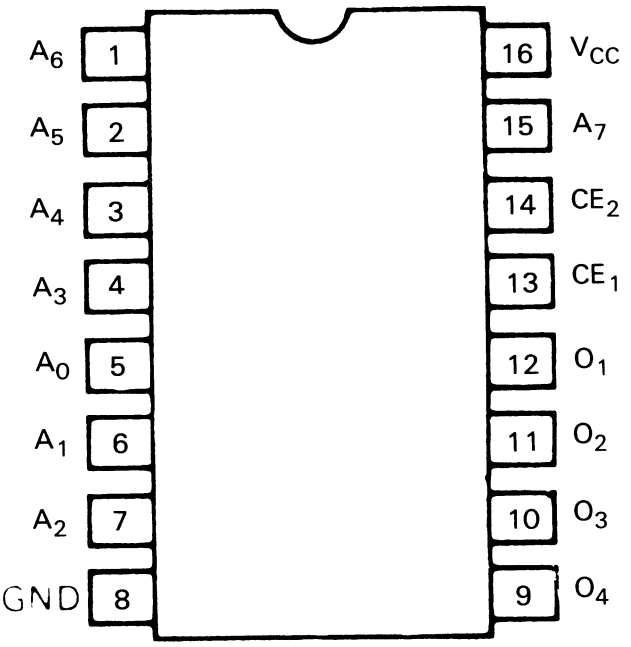
This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100000791 and 100000792

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

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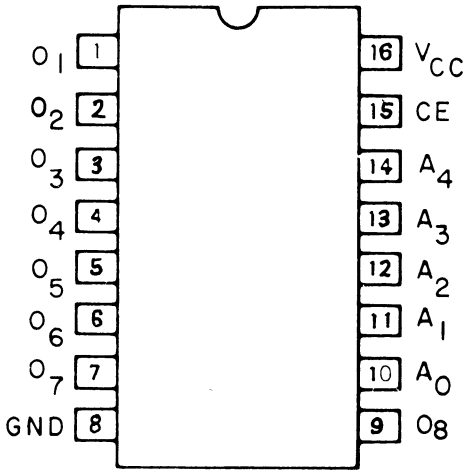
100000793

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION

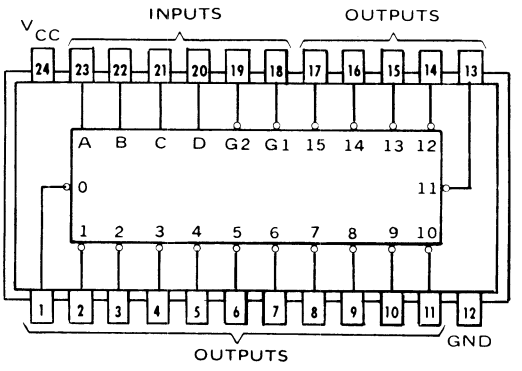


These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

100000794

4-Line-To-16-Line Decoder/Demultiplexer

PIN CONFIGURATION



The DGC 100-0000794 monolithic, 4-line-to-16-line decoder utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

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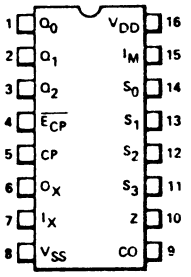
100000795

Programmable Bit Rate Generator

PIN CONFIGURATION



PIN NAMES

CP	External Clock Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

CLOCK MODES AND INITIALIZATION

I_X	$\overline{E_{CP}}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎍	Reset During First CP = HIGH Time

Note : Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576 MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
⎍⎍ = 1st HIGH Level Clock Pulse After $\overline{E_{CP}}$ Goes LOW
⎍⎍⎍ Clock Pulses

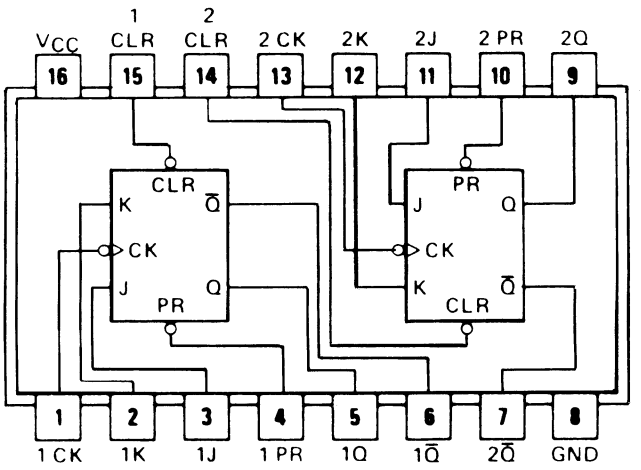
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

100000796

Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear

PIN CONFIGURATION



FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state).
L = low level (steady state).
X = irrelevant.
↓ = transition from high to low level.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

NOTE *The 100000796 is a low power Schottky device.*

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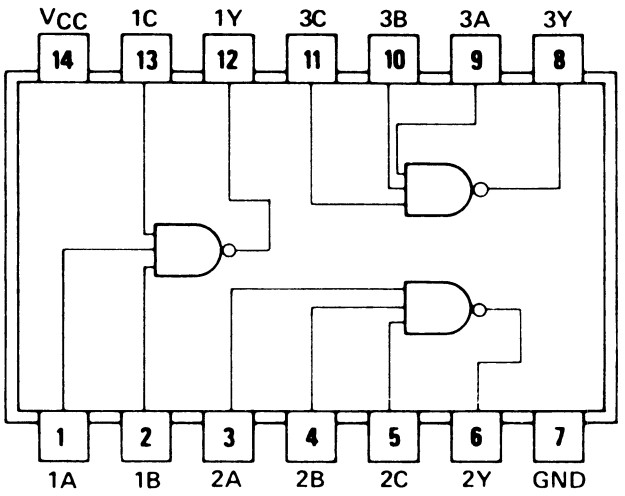
100000797

Triple 3-Input Positive-NAND Gate

PIN CONFIGURATION



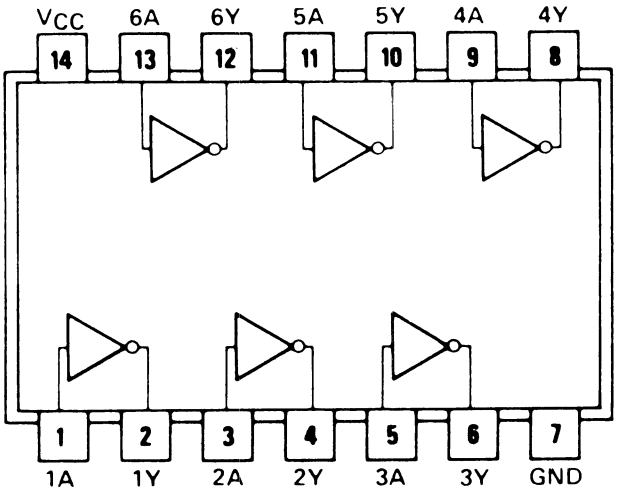
Positive logic: $Y = \overline{ABC}$

NOTE *The 100000797 is a low power Schottky device.*

100000798

Hex Inverter with Open Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{A}$

NOTE *The 100000798 is a low power Schottky device.*

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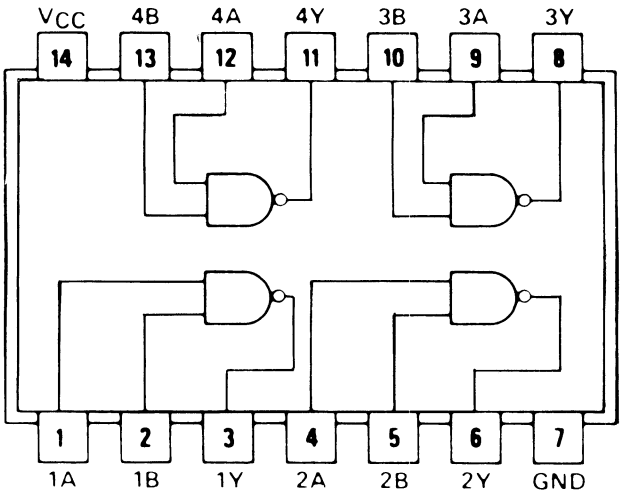
100000799

Quad 2-Input Positive-NAND Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

NOTE *The 100000799 is a low power Schottky device.*

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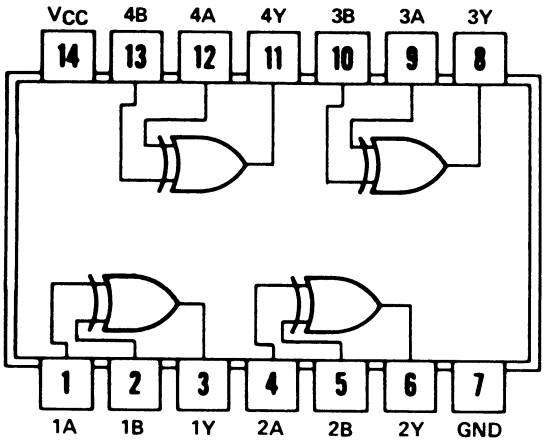
100000900

Quad 2-Input Exclusive-OR Gate with Open Collector Output

PIN CONFIGURATION



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

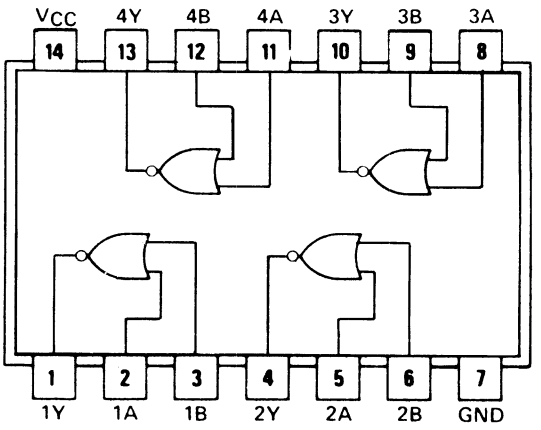
H = high level, L = low level

NOTE *The 100000900 is a low power Schottky device.*

100000901

Quad 2-Input NOR Line Driver

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B}$

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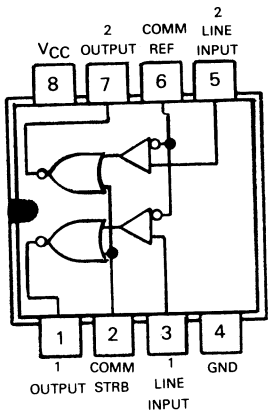
100000902

Dual Line Receiver

PIN CONFIGURATION



This device consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. It has a common reference voltage pin and a common strobe.

FUNCTION TABLE

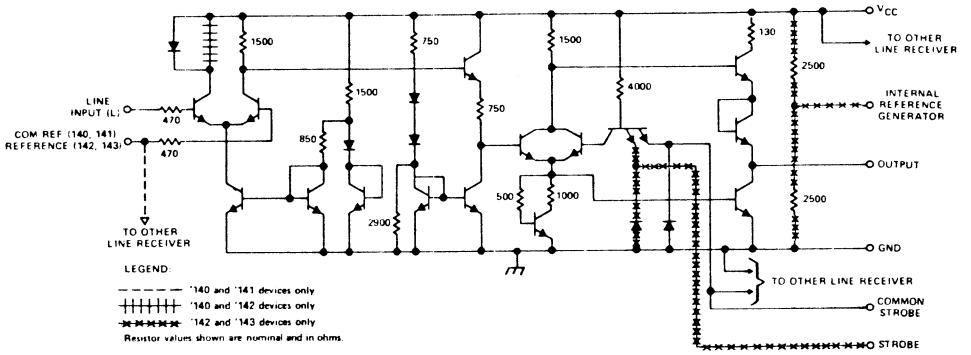
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	H
$> V_{ref} + 100$ mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

LOGIC DIAGRAM

(each receiver)



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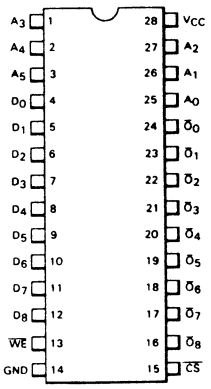
100000904

64 X 9 Read-Write Memory

PIN CONFIGURATION



TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"*
L	L	H	H	WRITE "1"*
L	H	X	$\overline{D_{OUT}}$*	READ

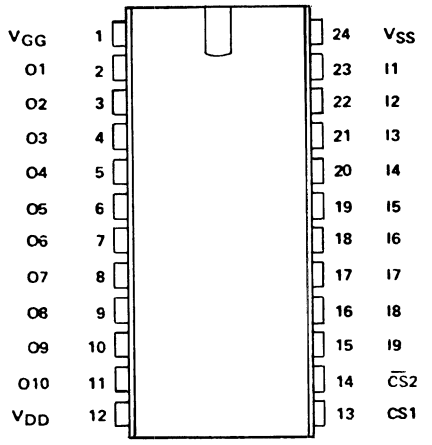
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
* Memory inverts from Data In to Data Output

NOTE *The 100000904 is a Schottky device.*

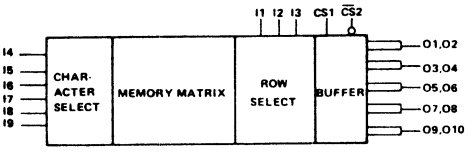
100000905

64 X 5 X 7 Static USASCII Character Generator

PIN CONFIGURATION



LOGIC DIAGRAM



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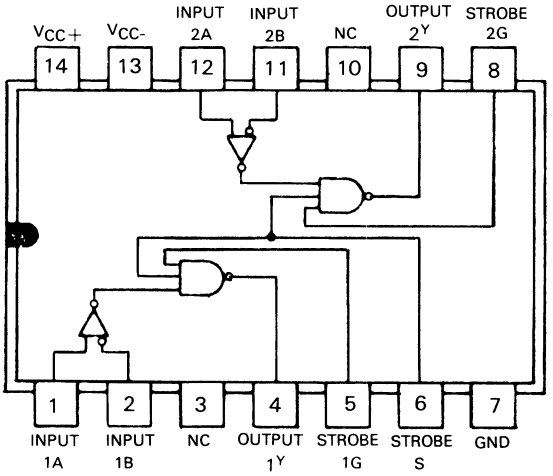
100000906

Dual Line Receiver

PIN CONFIGURATION



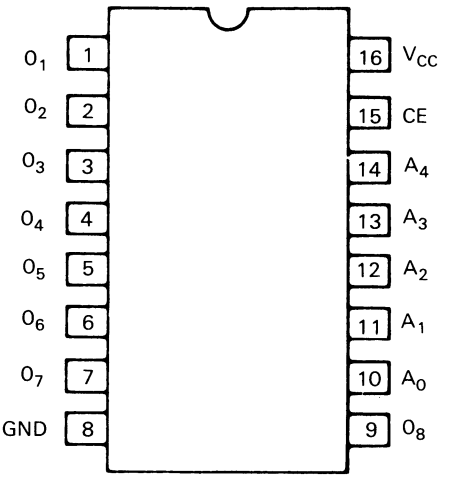
TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

100000907 and 100000908

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

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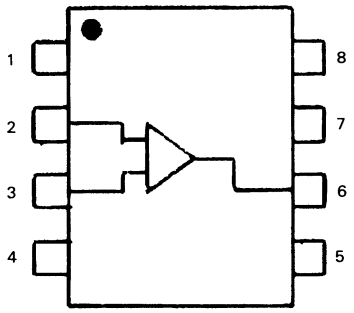
100001001

Operational Amplifier

PIN CONFIGURATION



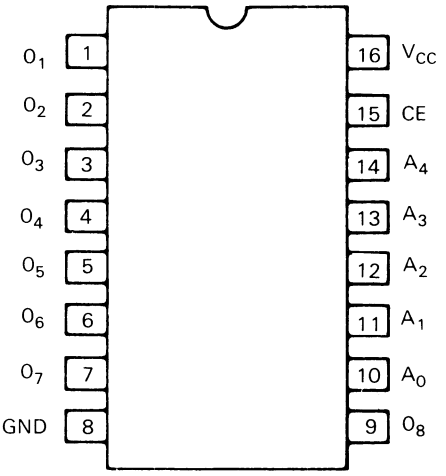
8-PIN DIP

1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V-
5. Offset Null
6. Output
7. V+
8. Freq. Comp.

100001002 and 100001003

32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

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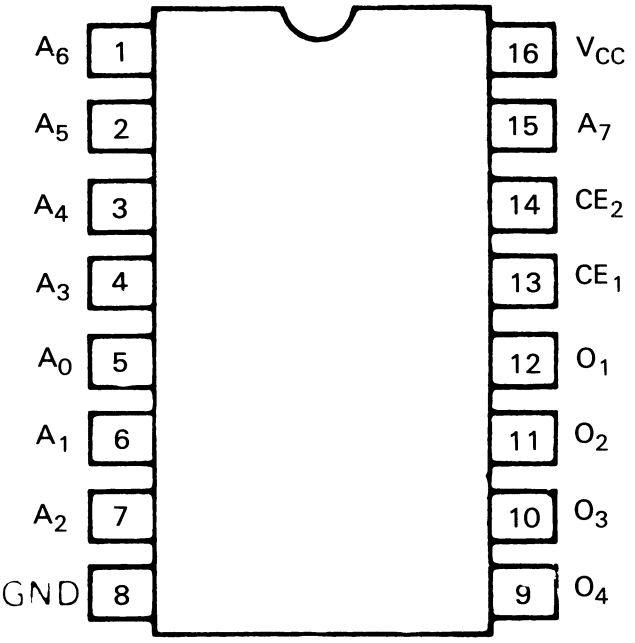
100001006 through 100001009

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



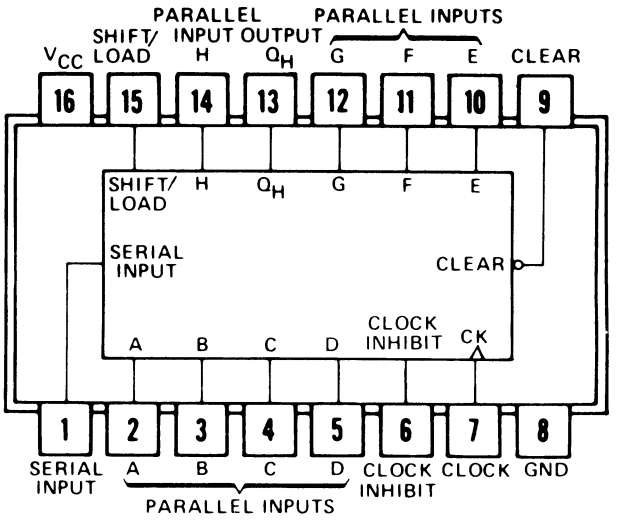
This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100001011

8-Bit Shift Register

PIN CONFIGURATION



FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a .... h = the level of steady-state input at A thru H respectively.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

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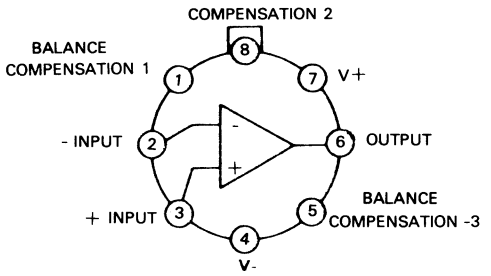
100001012

Operational Amplifier

PIN CONFIGURATION

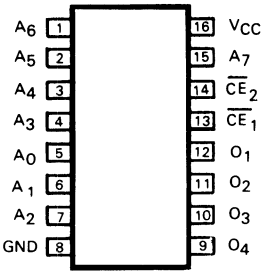


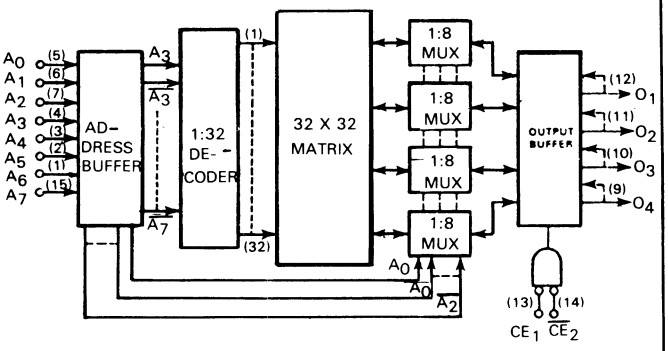
The 100001012 is a high speed operational amplifier. It is internally compensated for unity gain applications with a 60 degree phase margin, a minimum slew rate of 50V/usec, and a typical bandwidth of 12MHz. External feedforward compensation can be added to increase the slew rate to over 100V/usec and almost double the bandwidth for inverting applications. It features offset voltages below 2mV, maximum offset drifts of 10uV/degree C, and offset currents below 50 nA maximum.

100001013

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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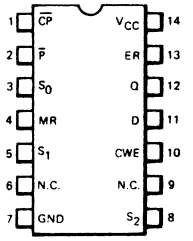
100001014

CRC Generator/Checker

PIN CONFIGURATION

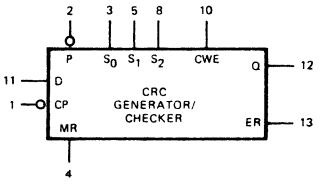


Pins 6 and 9 not connected.

PIN NAMES

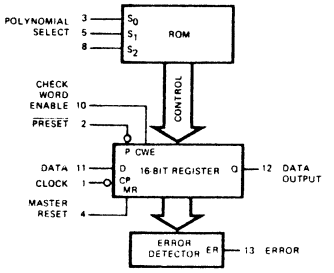
$S_0 - S_2$	Polynomial Select Inputs
D	Data Input
$\overline{CP}$	Clock (Operates on HIGH to LOW Transition) Input
CWE	Check Word Enable Input
$\overline{P}$	Preset (Active LOW) Input
MR	Master Reset (Active HIGH) Input
Q	Data Output
ER	Error Output

LOGIC SYMBOL



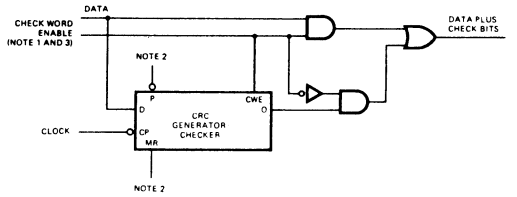
V_{CC} = Pin 14
GND = Pin 7

BLOCK DIAGRAM



V_{CC} = 14
GND = 7

CHECK WORD GENERATION

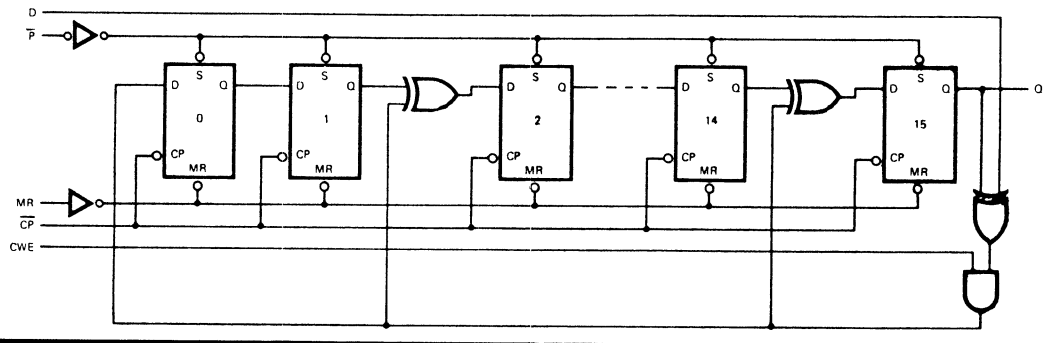


NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

TABLE 1

SELECT CODE S_2	S_1	S_0	POLYNOMIAL	REMARKS
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	*
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$



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100001014
(Continued)

The 100001014 is a Cyclic Redundancy Check/Generator which detects transmission errors on serial data streams. For encoding (check word generation) the data stream is divided by a selected polynomial. The remainder of this division is the check word which is appended to the data stream. To check for errors, the bit stream containing the data and the check word is divided by the same polynomial. The remainder is zero if there are no detectable errors. The 100001014 implements the polynomials listed in Table 1 using the select inputs S0 through S2.

The 100001014 consists of a 16-bit register, a ROM, and control circuitry (see block diagram). The inputs S0 through S2 select a polynomial by establishing a shift mode operation on the register with exclusive OR gates at the appropriate inputs. The data stream is applied to the Data Input (D) on the high-to-low transition of the clock ($\overline{CP}$) . This data is gated with the most significant Output (Q) of the register and controls the exclusive OR gates. While data is being entered, the Check Word Enable (CWE) must be high. When the last data bit is entered, the CWE is brought low. The check word bits shift out of the register and are appended to the data stream using external gating.

To check data, the CWE is held high while the data and the check word are shifted into the 100001014 via the D input on the high-to-low transition of the clock. If no errors have been detected, the register bits are all low and the Error Output (ER) is low. If an error has been detected, ER is high.

The register is cleared by a high on the Master Reset Input (MR). A low on the Preset Input ($\overline{P}$) sets all the register bits if a 16-bit polynomial is selected; if a 12 or 8-bit polynomial is selected, only the most significant 12 or 8 register bits are set and the remaining bit are cleared.

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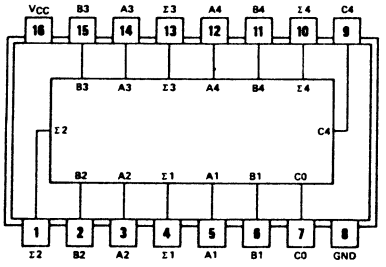
100001015

4-Bit Binary Full Adder With Fast Carry

PIN CONFIGURATION



positive logic: see function table

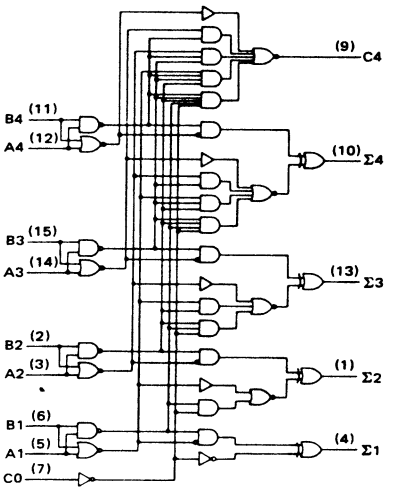
FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

BLOCK DIAGRAM



The 100001015 performs an addition operation of two 4-bit binary words. It provides a sum output for each bit and the resultant carry (C4) is obtained from the fourth bit. It features a full internal look-ahead carry across all four bits.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without logic inversion.

NOTE *The 100001015 is a Schottky device.*

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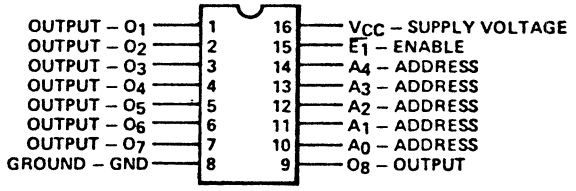
100001016

32 x 8-Bit Bipolar PROM

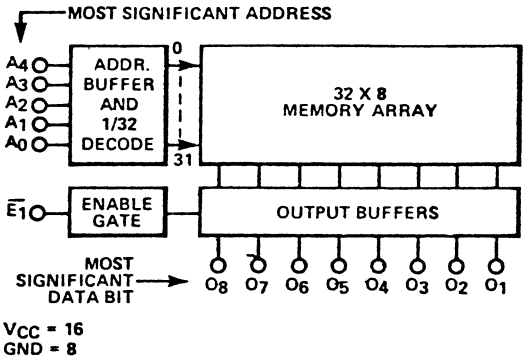
PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

Pin 15 is the programming pin.

BLOCK DIAGRAM



VCC = 16
GND = 8

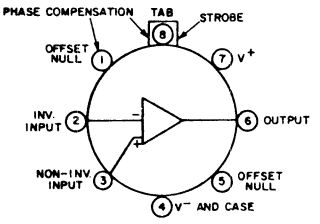
This 256-bit bipolar programmable read only memory is organized as 32 words by 8 bits. It has open-collector outputs.

NOTE: *This is a Schottky device.*

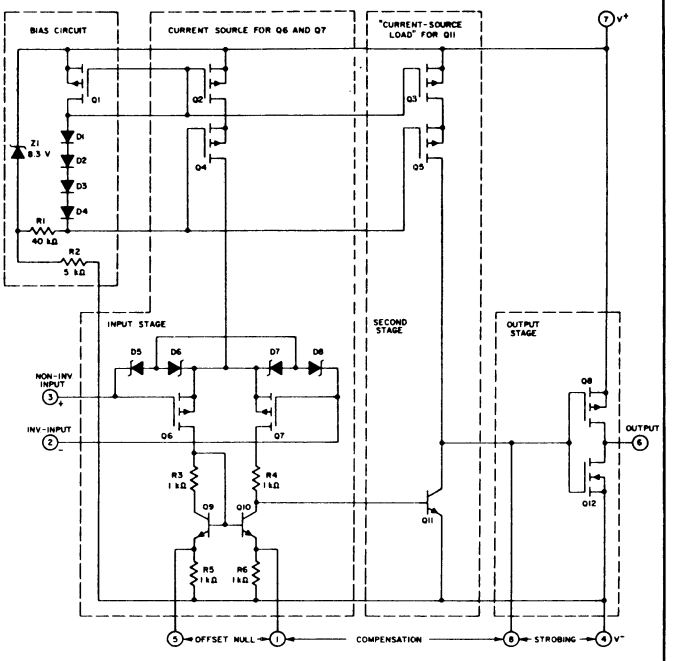
100001017

COS/MOS Operational Amplifier

PIN CONFIGURATION



LOGIC DIAGRAM



NOTE: DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

The 100001017 operational amplifier can be phase complemented with a single external capacitor. It has terminals for adjusting the offset voltage in applications requiring offset-null capability and a terminal which allows strobing the output stage.

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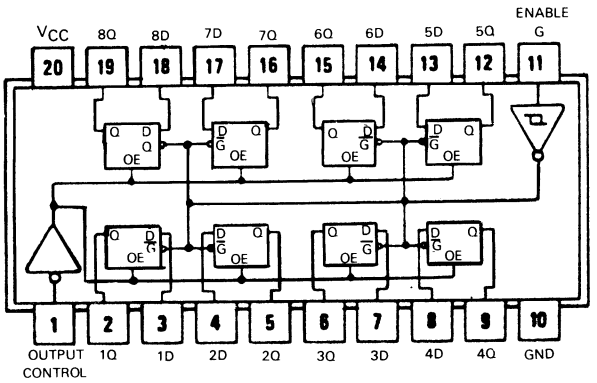
100001018

Octal D-Type Transparent Latches

PIN CONFIGURATION



TRUTH TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 ≡ the level of Q before the indicated stead-state input conditions were established.
H ≡ high level
L ≡ low level
Hi-Z ≡ high impedance
X ≡ irrelevant
↑ ≡ transition from low to high level

The 100001018 contains eight D-type latches. When the enble G is high, the Q outputs follow the D inputs. When this enable goes low, the outputs are latched at the data states that were setup.

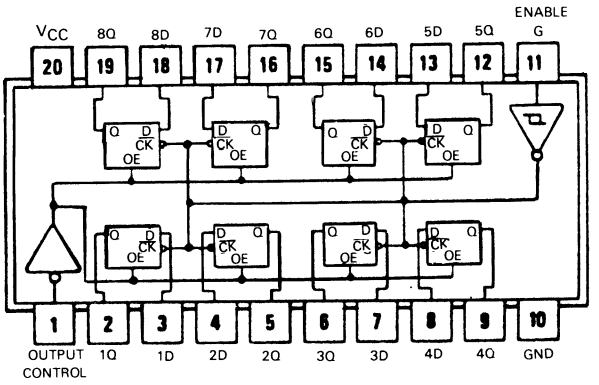
These latches have totem-pole 3-state outputs for driving highly-capacitive or relatively low-impedance loads.

NOTE *The 100001018 is a Schottky device.*

100001019

Octal D-Type Edge-Triggered Flip-Flops

PIN CONFIGURATION



TRUTH TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 ≡ the level of Q before the indicated stead-state input conditions were established.
H ≡ high level
L ≡ low level
Hi-Z ≡ high impedance
X ≡ irrelevant
↑ ≡ transition from low to high level

The 100001019 contains eight edge-triggered D-types flip-flops. On the low-to-high clock transition, the Q outputs are set to the data states setup on the D inputs.

These flip-flops have totem-pole 3 state outputs for driving highly-capacitive or relatively low-impedance loads.

NOTE *The 100001019 is a Schottky device.*

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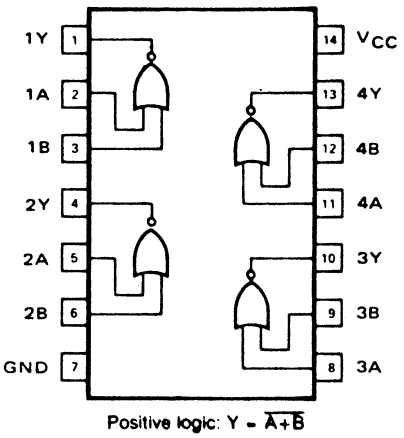
100001020

Quad 2-Input NOR Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B}$

NOTE *The 100001020 is a low power Schottky device.*

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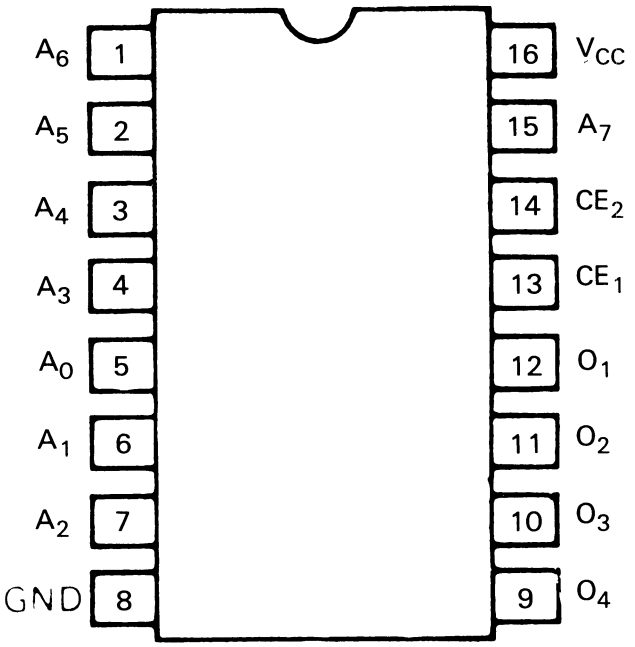
100001023 through 100001026

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



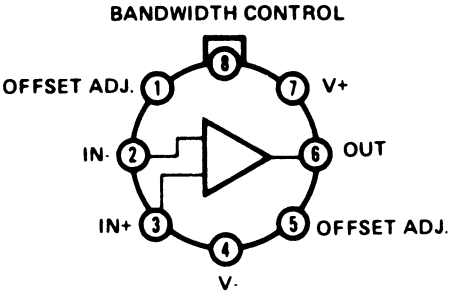
This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bi tread only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

100001027

High Impedance Operational Amplifier

PIN CONFIGURATION



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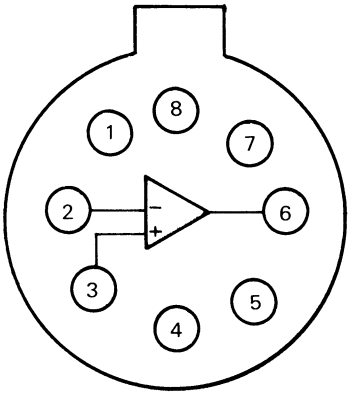
100001028

Monolithic JFET Input Operational Amplifier

Metal can package

Top View



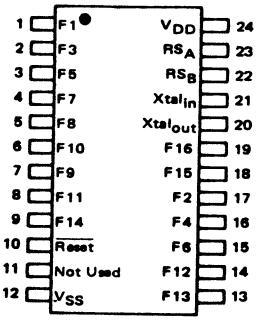
NOTE: *Pin 4 is connected to case.*

This JFET input operational amplifier has an input offset voltage of 1mV, and an input offset current of 3 pA. The input bias current is 30 pA.

100001029

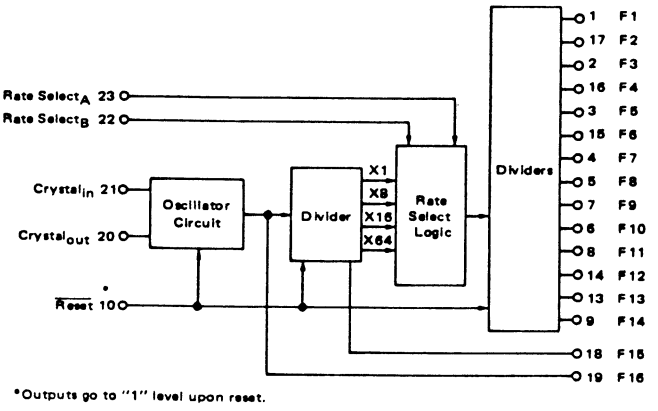
Bit Rate Generator

PIN CONFIGURATION



V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



*Outputs go to "1" level upon reset.

This bit rate generator utilizes a frequency divider network to provide sixteen different output clock rates. A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates. An external clock may be applied to pin 21.

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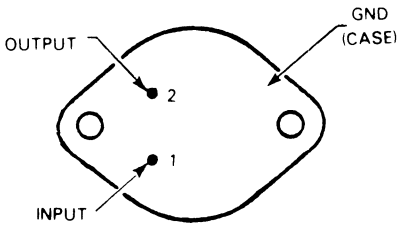
100001041

-5V 3A, 20W, 5% Fixed Voltage Regulator

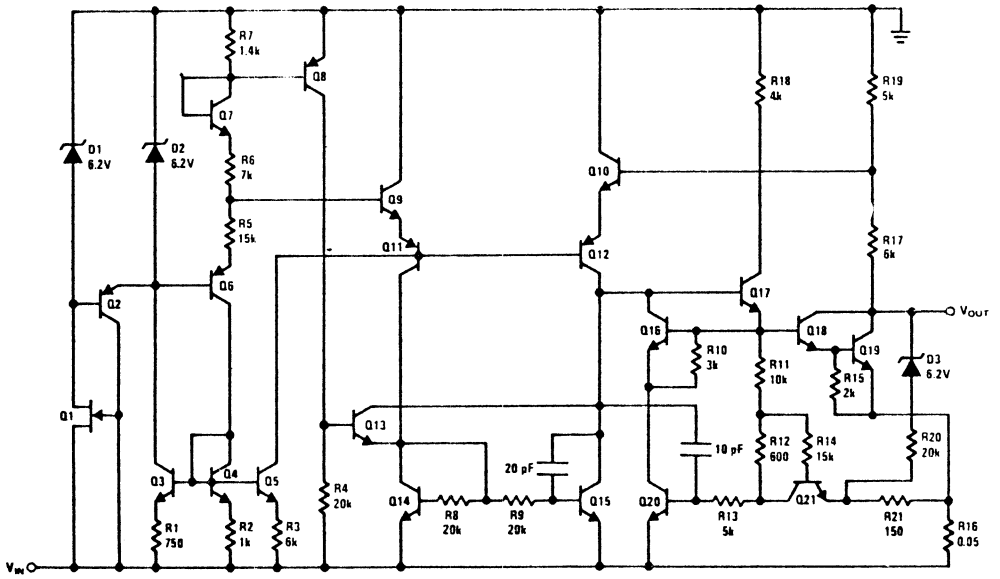
PIN CONFIGURATION



BOTTOM VIEW

The 100001041 is a three terminal negative voltage regulator with a fixed voltage of -5 volts. It features a current limiter and thermal overload protection circuit.

LOGIC DIAGRAM



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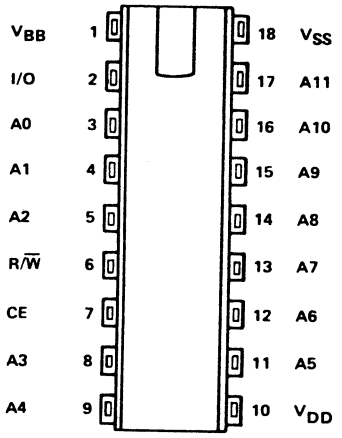
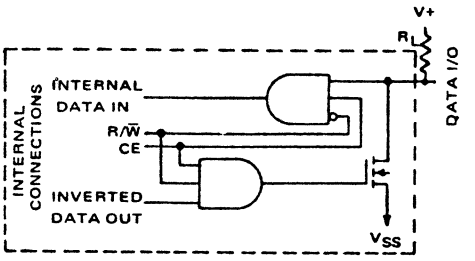
100001042

4096 x 1-Bit Dynamic RAM

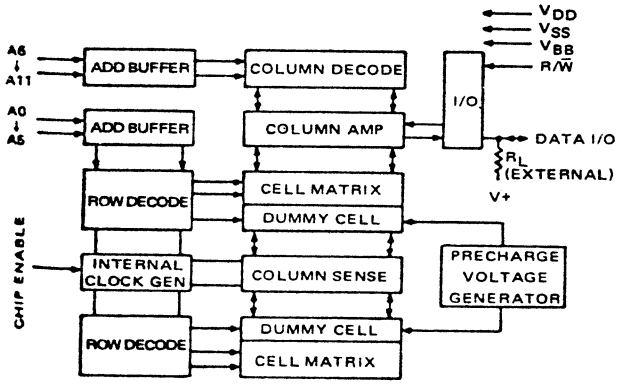
PIN CONFIGURATION



I/O LOGIC



BLOCK DIAGRAM



The 100001042 is a 4096-bit random access memory organized as 4096 words by one bit per word. A single external clock input is required. All read, write, and read-modify-write operations occur when the chip enable input (CE) is high. When the chip enable is low, the memory is disabled and automatically precharged.

The read or write mode is selected through the read/write ($\overline{R/W}$) input. When this input is low, the read mode selected and the data input is disabled. When this input is high, the write mode is selected and the data output is disabled.

All addresses (A0-A11) must be stable on or before the rising edge of the chip-enable pulse. Address registers are provided on the chip.

Data inputs and outputs are multiplexed on a common input/output terminal (I/O), which is controlled by the $\overline{R/W}$ input. Data is written during a write or read-modify-write cycle when the chip enable is high. Data written into the memory is read out in its true form.

Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses (A0 through A5) at least every 2 milliseconds. Addressing any row refreshes all 64 bits in that row.

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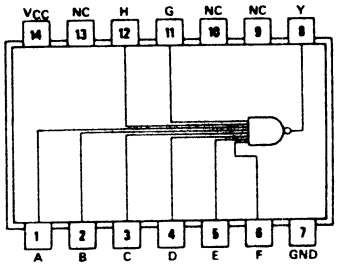
100001045

8-Input NAND Gate

PIN CONFIGURATION



positive logic:
$Y = \overline{ABCDEFGH}$

NOTE *The 100001045 is a Schottky device.*

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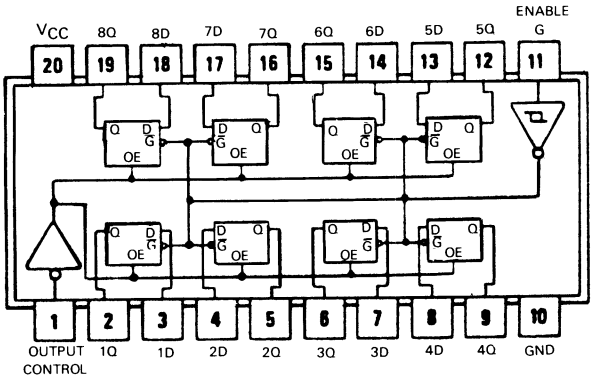
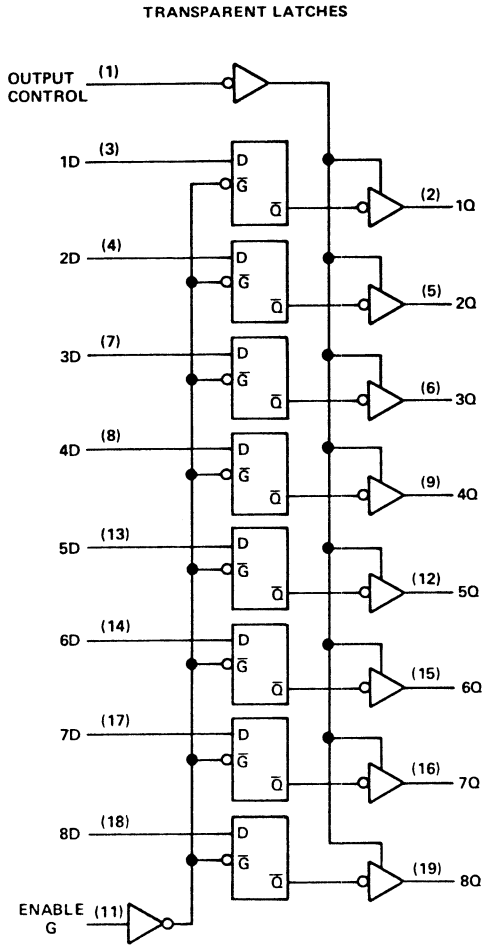
100001046

Octal D-Type Transparent Latch With Tri-State Output

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

The 100001046 consists of eight, transparent D-type latches with totem-pole three-state outputs. When the enable (G) is high the Q outputs will follow the data ((D) inputs. When the enable goes low, the output will be latched at the level of the data that was setup.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

NOTE *The 100001046 is a low power Schottky device.*

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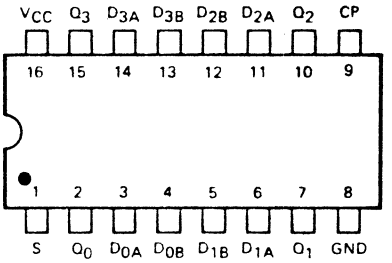
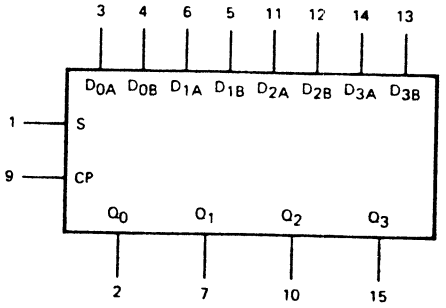
100001047 and 100001048

Quad Two-Input Registers

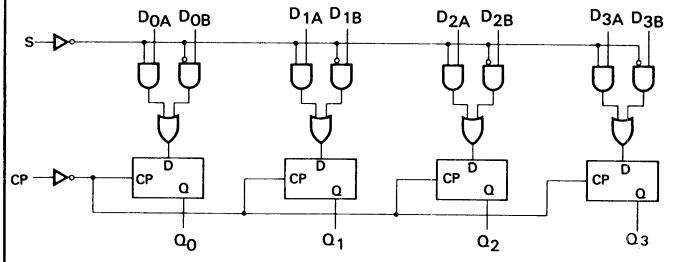
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM



The 100001047 and 100001048 are registers containing four D flip-flops with a buffered common clock and a two input multiplexer at the input of each flip-flop. The multiplexers are controlled by the common select line S. Data selected by S is stored in the flip-flops on the low-to-high transition of the clock. When the S input is low, the DiA data is stored in the register; when it is high, the DiB data is stored.

NOTE: *The 100001047 is a Schottky device. The 100001047 is a lower power Schottky device.*

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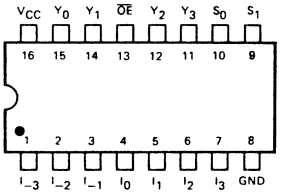
100001049

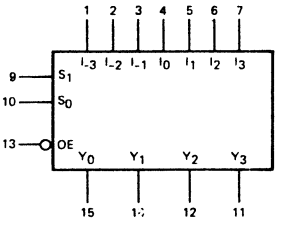
Four-Bit Shifter With Three-State Outputs

PIN CONFIGURATION



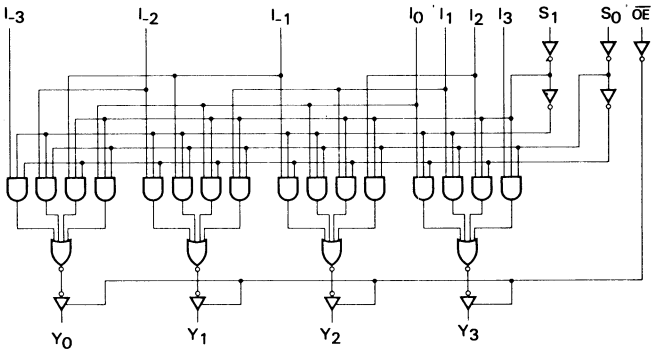
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM



LOGIC EQUATIONS

$$Y_0 = \bar{S}_0 \bar{S}_1 I_0 + S_0 \bar{S}_1 I_{-1} + \bar{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$
$$Y_1 = \bar{S}_0 \bar{S}_1 I_1 + S_0 \bar{S}_1 I_0 + \bar{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$
$$Y_2 = \bar{S}_0 \bar{S}_1 I_2 + S_0 \bar{S}_1 I_1 + \bar{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$
$$Y_3 = \bar{S}_0 \bar{S}_1 I_3 + S_0 \bar{S}_1 I_2 + \bar{S}_0 S_1 I_1 + S_0 S_1 I_0$$

TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

DEFINITION OF FUNCTIONAL TERMS

I_i The seven data inputs of the shifter.

$\overline{OE}$ Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.

S_0, S_1 Select inputs. Controls the number of places the inputs are shifted.

Y_i The four outputs of the shifter.

The 100001049 accepts a 4-bit word and shifts it 0,1,2 or 3 places depending on the values of the 2-bit select field S0 and S1. Its tri-state outputs are controlled by an active-low enable.

NOTE *The 100001049 is a Schottky device.*

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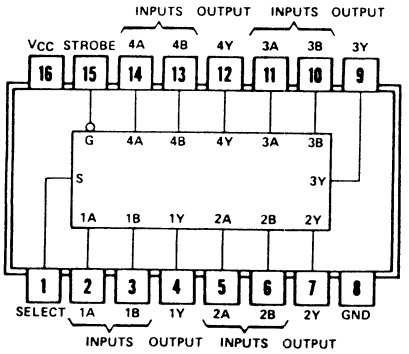
100001050

Quad 2-Line-To-1-Line Data Selector/Multiplexer

PIN CONFIGURATION



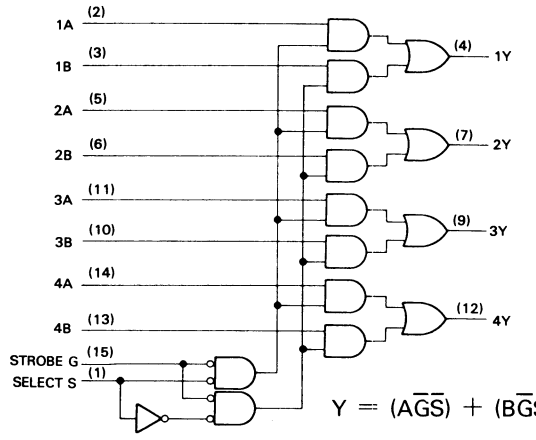
positive logic:
Low level at S selects A inputs
High level at S selects B inputs

FUNCTION TABLE

INPUTS				
STROBE	SELECT	A	B	OUTPUT Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

LOGIC DIAGRAM



This data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A four-bit word is selected from one of two sources and is routed to the four outputs. The device presents true data.

NOTE *The 100001050 is a low power Schottky device.*

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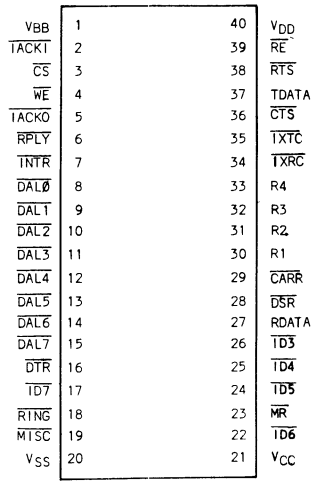
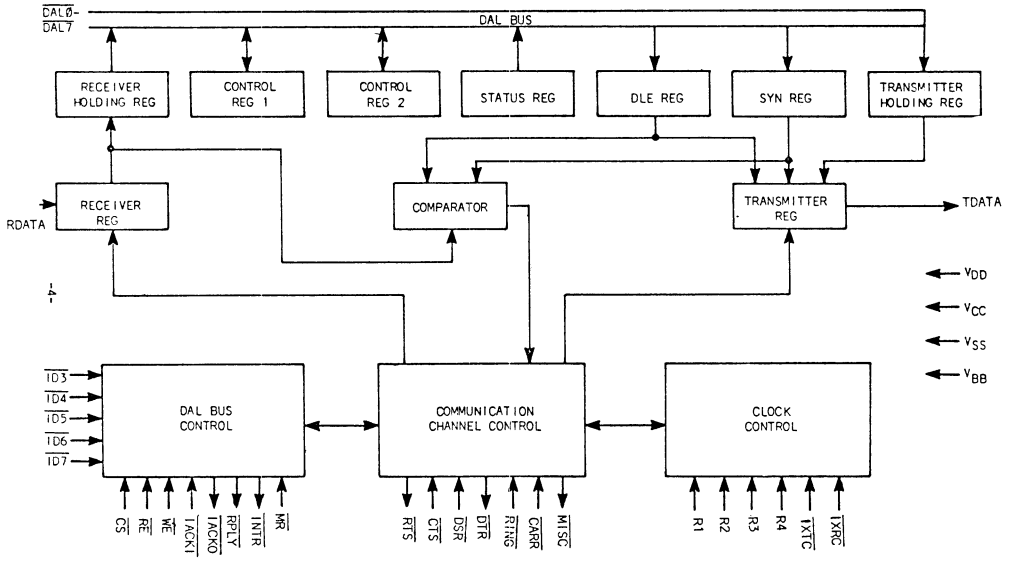
100001057

Asynchronous/Synchronous Receiver/Transmitter

PIN CONFIGURATION



LOGIC DIAGRAM



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100001057

(Continued)

CONTROL REGISTER 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0 - LOOP MODE 1 - NORMAL MODE	ASYNC 0 - NOW BREAK MODE 1 - BREAK MODE SYNC 0 -NOW TRANSMITTER TRANSPARENT MODE 1 -TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0 - 1 1/2 or 2 STOP BIT SELECTION 1 - SINGLE STOP BIT SELECTION ASYN (TRANS. DISABLED) 0 - $\overline{\text{MISC}}$ OUT = 1 1 - $\overline{\text{MISC}}$ OUT = 0 SYNC (OR 16 = 0) 0 - NO PARITY GENERATED 1 - TRANSMIT PARITY ENABLED SYNC (OR 16 = 1) 0 - NO FORCE DLE 1 - FORCE DLE	ASYNC 0-NOW ECHO MODE 1-AUTO ECHO MODE SYNC (CR12 = 1) 0 - DLE STRIPPING NOT ENABLED 1 - DLE STRIPPING ENABLED SYNC (CR12 = 0) 0 - $\overline{\text{MISC}}$ OUT = 1 1 - $\overline{\text{MISC}}$ OUT = 0	ASYNC 0 - NO PARITY ENABLED 1 - PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0 - RECEIVER PARITY CHECK IS DISABLED 1 - RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0 - RECEIVER DISABLED 1 - RECEIVER ENABLED	SYNC/ASYNC 0 - SETS $\overline{\text{RTS}}$ OUT = 1 1 - SETS $\overline{\text{RTS}}$ OUT = 0	SYNC/ASYNC 0 - SETS $\overline{\text{DTR}}$ OUT = 1 1 - SETS $\overline{\text{DTR}}$ OUT = 0

CONTROL REGISTER 2

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0 -ASYNCHRONOUS MODE 1 - SYNCHRONOUS MODE	SYNC/ASYNC 0 - ODD PARITY SELECT 1 - EVEN PARITY SELECT	ASYNC 0 - RECEIVER CLOCK DETERMINED BY BITS 2-0 1 - RECEIVER CLK = RATE 1 SYNC (CR16 = 0) 0 - NO SYN STRIP 1 - SYN STRIP SYNC (CR16 = 1) 0 - NO DLE-SYN STRIP 1 - DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - 1X CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK + 2 110 - RATE 4 CLOCK + 4 111 - RATE 4 CLOCK + 8

STATUS REGISTER

Bit	7	6	5	4	3	2	1	Ø
	•Data Set Change	•Data Set Ready	•Carrier Detector	•Framing Error •Syn Detect	•DLE Detect •Parity Error	•Overrun Error	•Data Received	•Transmitter Holding Register Empty

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100001057

(Continued)

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1 21 40 20	POWER SUPPLIES	V_{BB} V_{CC} V_{DD} V_{SS}	-5V +5V +12V Ground
23	MASTER RESET	$\overline{MR}$	• The Control and Status Registers and other controls are cleared when this input is low.
8-15	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	• Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
17,22, 24,25, 26	SELECT CODE	$\overline{ID7}$-$\overline{ID3}$	• Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
3	CHIP SELECT	$\overline{CS}$	• The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations.
39	READ ENABLE	$\overline{RE}$	• This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL.
4	WRITE ENABLE	$\overline{WE}$	• This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	INTERRUPT	$\overline{INTR}$	• This open drain output is made low when one of the communication interrupt conditions occur.
2	INTERRUPT ACKNOWLEDGE IN	$\overline{IACKI}$	• This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes $\overline{IACKO}$ a low.

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100001057
(Continued)

PIN NO.	PIN NAME	SYMBOL	FUNCTION
29	CARRIER DETECTOR	$\overline{\text{CARR}}$ ($\overline{\text{CF}}$)	• This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
35	TRANSMITTER TIMING	$\overline{\text{IXTC}}$ ($\overline{\text{DB}}$)	• This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
34	RECEIVER TIMING	$\overline{\text{IXRC}}$ ($\overline{\text{DD}}$)	• This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	MISCELLANEOUS	$\overline{\text{MISC}}$	• This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

The 100001057 functions as an interface between a serial data communications channel and a parallel system and is capable of full-duplex operation in synchronous or asynchronous systems. It is designed to operate in bus oriented systems with a controller or a processor controlling its operation via the bus.

The main components of this device are a receiver, transmitter, and a control and bus interface (see block diagram).

Two 8-bit control registers determine the operating mode of the 100001057. The contents of these registers are given in the Control Register 1 and Control Register 2 tables. Control register 1 can be changed at any time. Control register 2, however, should not be changed unless both the receiver and the transmitter sections are in an idle state.

The contents of the status register specify the data conditions of the receiver and the transmitter and the status of data set. The contents of this register are given in the Status Register table.

All data, control, and status words are tranferred via the data access lines (DAL0-7). Other lines are used for addressing the device and controlling the input/output operations.

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100001057 (Continued)

PIN NO.	PIN NAME	SYMBOL	FUNCTION
5	INTERRUPT ACKNOWLEDGE OUT	IACKO	• This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	REPLY	RPLY	• This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
30-33	CLOCK RATES	R1-R4	• These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
37	TRANSMITTED DATA	TDATA (BA)	• This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
27	RECEIVED DATA	RDATA (BB)	• This input receives serial data into the ASTRO.
38	REQUEST TO SEND	RTS (CA)	• This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
36	CLEAR TO SEND	CTS (CB)	• This input, when low, enables the transmitter section of the ASTRO.
28	DATA SET READY	DSR (CC)	• This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
16	DATA TERMINAL READY	DTR (CD)	• This output is generated by a bit in the Control Register and indicates Controller readiness.
18	RING INDICATOR	RING (CE)	• This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.

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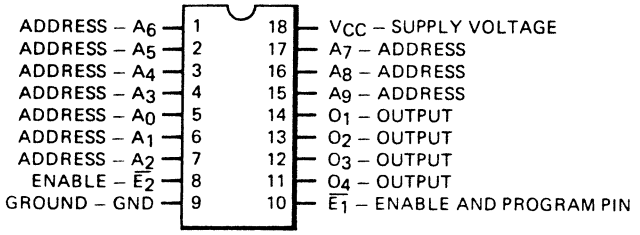
100001059

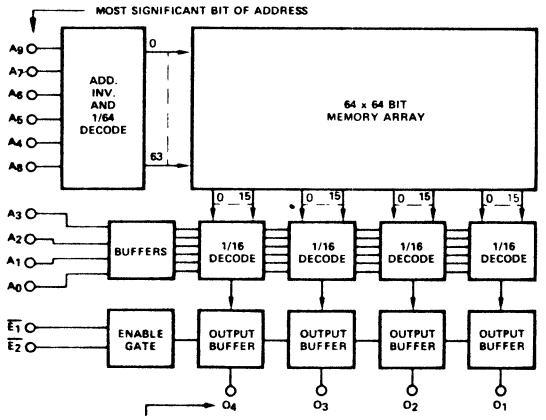
1024 x 4-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ and $\overline{E_2}$ must be LOW.

BLOCK DIAGRAM



VCC = 18
GND = 9

This 4096-bit programmable read only memory is organized as 1024 words by 4 bits. It includes on-chip address decoding, two chip enables ($\overline{E1}$, $\overline{E2}$) and open collector outputs.

The memory is addressed with inputs A0 through A9, which select one of 1024 words. A word is read out on the outputs O1 through O4. Both enables $\overline{E1}$ and $\overline{E2}$ must be low to read. If either enable is high, the outputs are held off, permitting wire ORing of open collector outputs of several packages.

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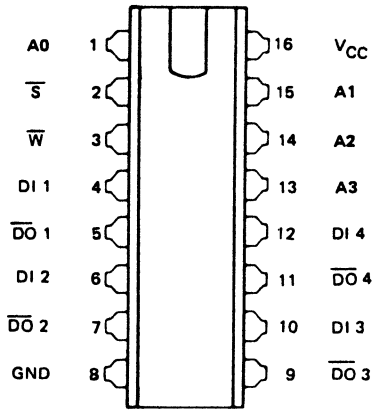
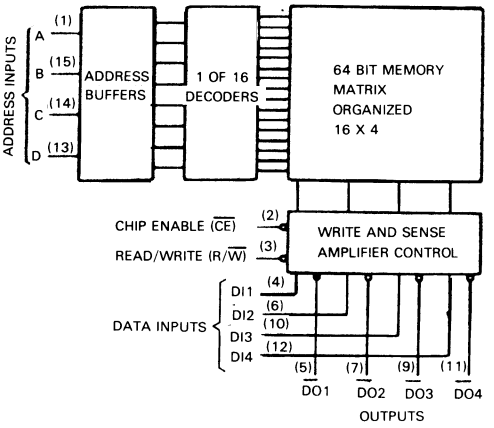
100001060

16 x 4-Bit RAM

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	High Impedance
Read	L	H	Complement of Data Entered
Inhibit	H	X	High Impedance

H ≡ high level, L ≡ low level, X ≡ irrelevant

This 64-bit random access memory is organized as 16 words by 4 bits. It features on-chip address decoding, a chip-select input, and tri-state output.

Data is written into the selected location when the chip-select input ($\overline{S}$) and the write-enable input ($\overline{W}$) are low. The output is in a high-impedance state when the write enable input is low. When a number of outputs are bus-connected, this high impedance state will neither load nor drive the bus line. However, the bus line can be driven by another active output or a passive pullup.

Stored data is the complement of the data applied at the input during the write cycle. The data at a selected address is read when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the output is in the high-impedance state.

NOTE *The 100001060 is a Schottky device.*

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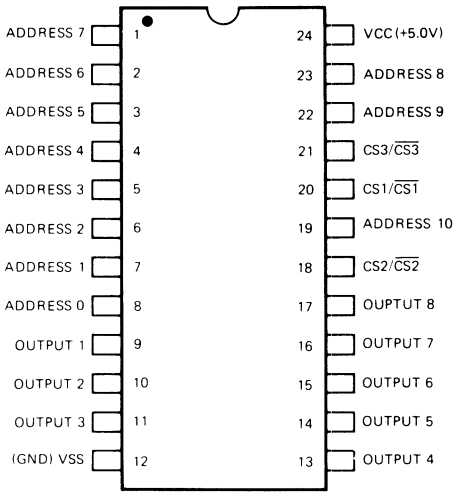
100001061

2048 X 8 Static MOS PROM

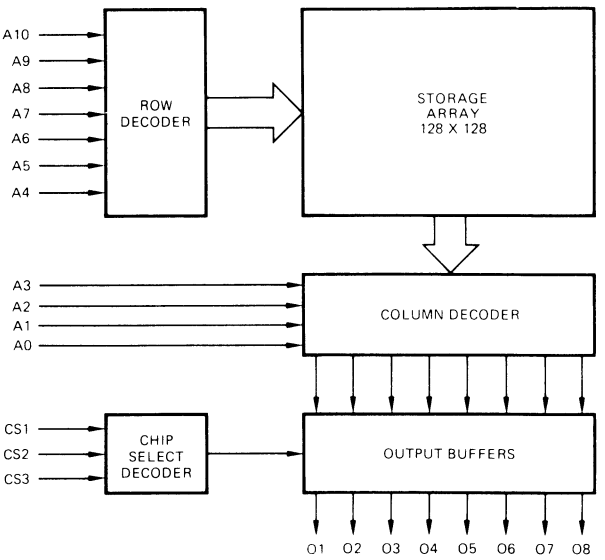
PIN CONFIGURATION



Top View

Pin 1 is marked for orientation.

BLOCK DIAGRAM



Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity is specified, thus allowing the addressing of 8 memory chips without external gating. Also this device is TTL compatible and N-channel silicon gate MOS technology is used.

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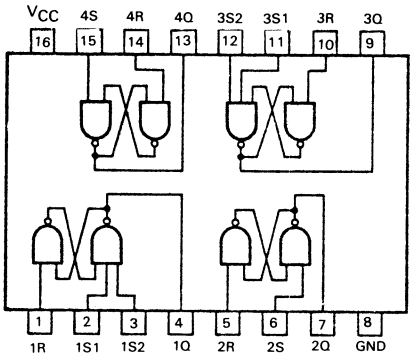
100001063

Quadruple $\overline{S}$-$\overline{R}$ Latch

PIN CONFIGURATION

B-F-W PACKAGE



POSITIVE LOGIC: SEE FUNCTION TABLE

FUNCTION TABLE

INPUT		OUTPUT
$\overline{S}$*	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H 1

H = high level
L = low level
Q0 = the level of Q before these input conditions were established
*For latches with double S inputs:
H = both S inputs high
L = one or both S inputs low
This input may not persist when the S and R inputs return to their inactive (H) level.

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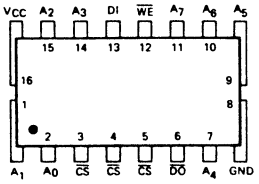
100001064

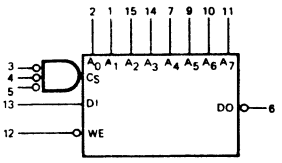
256 x 1-Bit Bipolar RAM

PIN CONFIGURATION



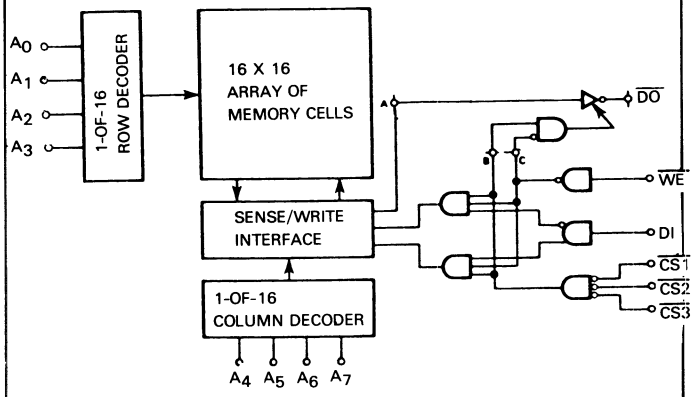
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

LOGIC DIAGRAM



This 256-bit random access memory is organized as 256 words by 1 bit. It has an 8-bit address field (A0-A7), separate data input and output lines ($\overline{DI}$, $\overline{DO}$, respectively), three active-low chip select inputs ($\overline{CS}$), and a tri-state output.

The chip is selected when all three select inputs are low.

When the write-enable ($\overline{WE}$) is low and the chip is selected, the data on the data input is written into the location specified by the address inputs. The output floats during this operation. As a result, the data bus can be used by other memories or open-collector devices which are tied to the inverting data output.

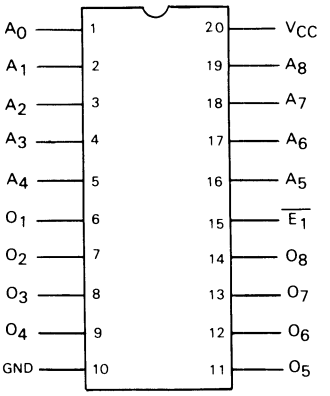
When the write-enable is high and the chip is selected, the data in the location specified by the adddress inputs is read out and inverted at the output.

NOTE *The 100001064 is a low power Schottky device.*

100001065

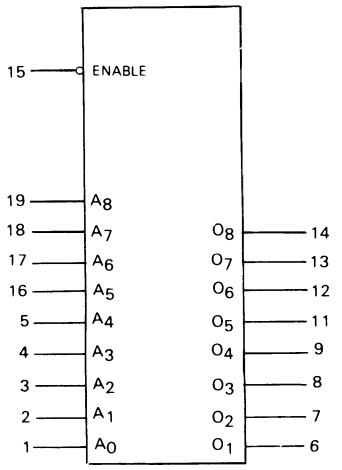
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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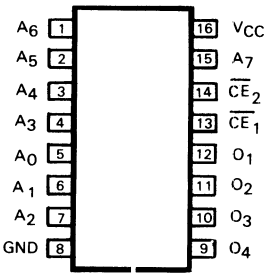
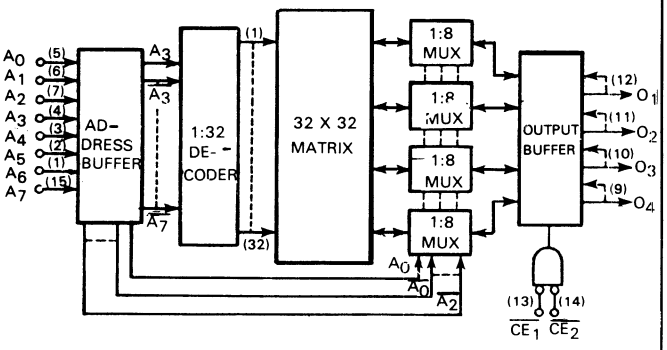
100001071

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



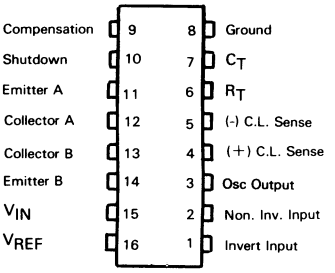
This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

NOTE *The 100001071 is a Schottky device.*

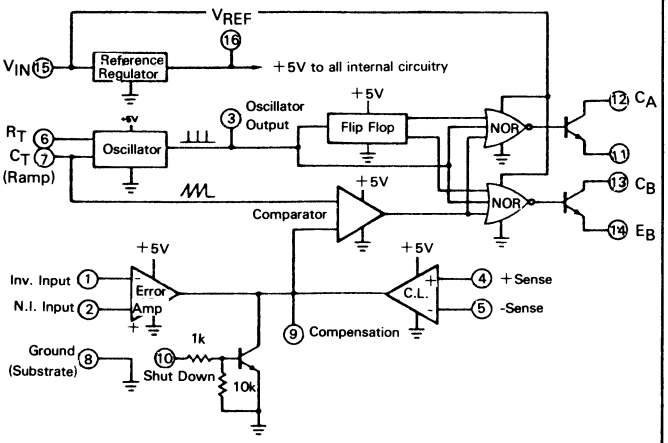
100001072

Regulating Pulse Width Modulator

PIN CONFIGURATION



BLOCK DIAGRAM



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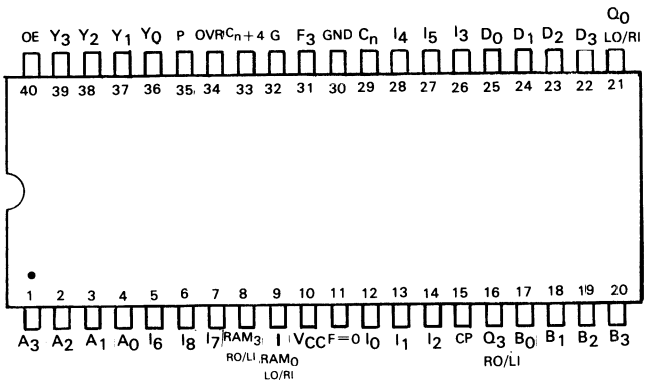
100001073

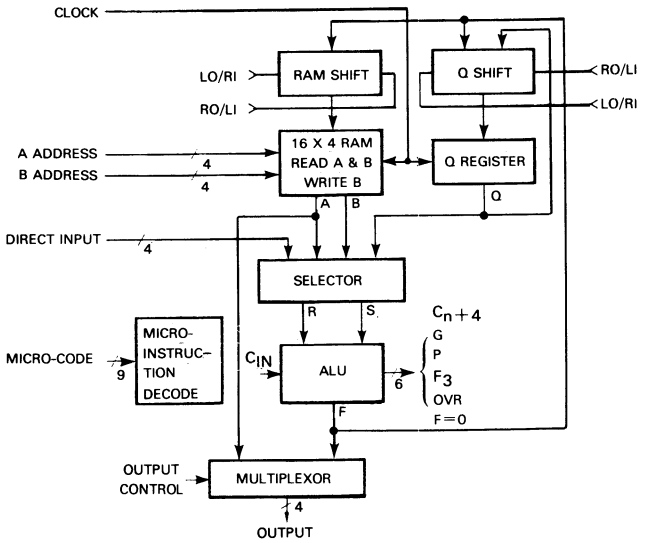
Four-Bit Bipolar Microprocessor Slice

PIN CONFIGURATION



Note: Pin 1 is marked for orientation

MICROPROCESSOR SLICE BLOCK DIAGRAM



ALU LOGIC MODE FUNCTIONS

$I_5 I_4 I_3 I_2 I_1 I_0$	Octal I_{543} I_{210}	Group	Function
1 0 0 0 0 0	40	AND	A∧Q
0 0 1	41		A∧B
1 0 1	45		D∧A
1 1 0	46		D∧Q
0 1 1 0 0 0	30	OR	A∨Q
0 0 1	31		A∨B
1 0 1	35		D∨A
1 1 0	36		D∨Q
1 1 0 0 0 0	60	EX-OR	A∨̄Q
0 0 1	61		A∨̄B
1 0 1	65		D∨̄A
1 1 0	66		D∨̄Q
1 1 1 0 0 0	70	EX-NOR	$\overline{A \vee Q}$
0 0 1	71		$\overline{A \vee B}$
1 0 1	75		$\overline{D \vee A}$
1 1 0	76		$\overline{D \vee Q}$
1 1 1 0 1 0	72	INVERT	$\overline{Q}$
0 1 1	73		$\overline{B}$
1 0 0	74		$\overline{A}$
1 1 1	77		$\overline{D}$
1 1 0 0 1 0	62	PASS	Q
0 1 1	63		B
1 0 0	64		A
1 1 1	67		D
0 1 1 0 1 0	32	PASS	Q
0 1 1	33		B
1 0 0	34		A
1 1 1	37		D
1 0 0 0 1 0	42	"ZERO"	0
0 1 1	43		0
1 0 0	44		0
1 1 1	47		0
1 0 1 0 0 0	50	MASK	$\overline{A} \wedge Q$
0 0 1	51		$\overline{A} \wedge B$
1 0 1	55		$\overline{D} \wedge A$
1 1 0	56		$\overline{D} \wedge Q$

ALU ARITHMETIC MODE FUNCTIONS

	Octal	$C_n = 0$		$C_n = 1$	
$I_5 I_4 I_3 I_2 I_1 I_0$	I_{543} I_{210}	Group	Function	Group	Function
0 0 0 0 0 0	0 0	ADD	A+Q	ADD plus one	A+Q+1
0 0 1	0 1		A+B		A+B+1
1 0 1	0 5		D+A		D+A+1
1 1 0	0 6		D+Q		D+Q+1
0 0 0 0 1 0	0 2	PASS	Q	Increment	Q+1
0 1 1	0 3		B		B+1
1 0 0	0 4		A		A+1
1 1 1	0 7		D		D+1
0 0 1 0 1 0	1 2	Decrement	Q−1	PASS	Q
0 1 1	1 3		B−1		B
1 0 0	1 4		A−1		A
0 1 0 1 1 1	2 7		D−1		D
0 1 0 0 1 0	2 2	1's Comp.	−Q−1	2's Comp	−Q
0 1 1	2 3		−B−1		−B
1 0 0	2 4		−A−1		−A
0 0 1 1 1 1	1 7		−D−1		−D
0 0 1 0 0 0	1 0	Subtract (1's Comp)	Q−A−1	Subtract (2's Comp)	Q−A
0 0 1	1 1		B−A−1		B−A
1 0 1	1 5		A−D−1		A−D
1 1 0	1 6		Q−D−1		Q−D
0 1 0 0 0 0	2 0		A−Q−1		A−Q
0 0 1	2 1		A−B−1		A−B
1 0 1	2 5		D−A−1		D−A
1 1 0	2 6		D−Q−1		D−Q

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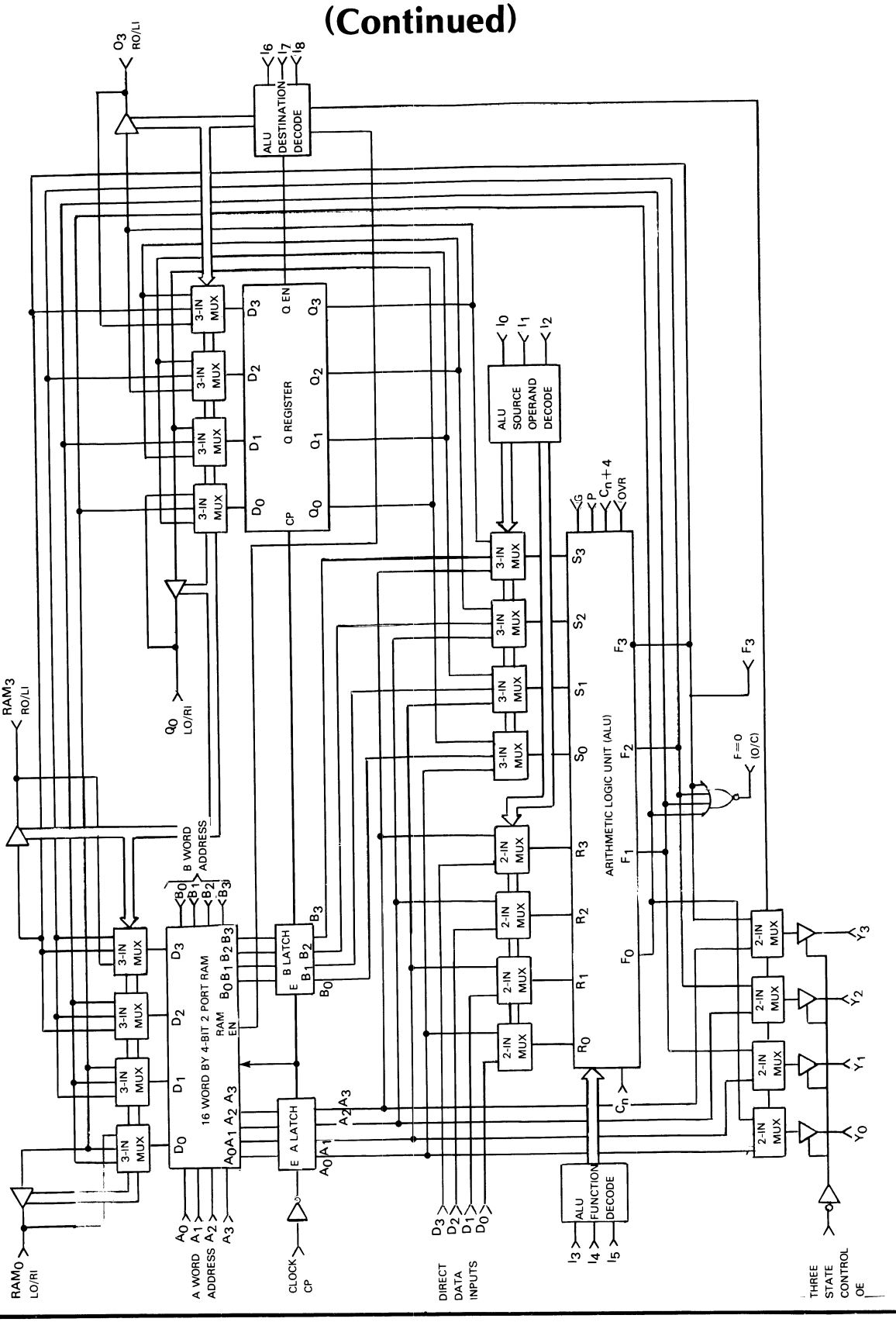
100001073
(Continued)

MICROPROCESSOR BLOCK DIAGRAM



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100001073
(Continued)

The 100001073 is a four-bit slice cascadable to any number of bits. The two main components shown in the detailed block diagram are the 16-word by 4-bit dual-port RAM and the high-speed ALU.

Data can be read simultaneously from the A-port and the B-port of the random access memory (RAM) using the 4-bit A and B address field inputs, respectively. The same code can be applied to the A select field and B select field in which case the identical data will appear at both the RAM A-port and B-port outputs.

When enabled by the RAM write enable (RAM EN), data is always written into the file (word) defined by the B address field. The RAM data input field is driven by a 3-input multiplexer. This 3-input multiplexer scheme allows the data to be shifted up (right) one bit position, shifted down (left) one bit position, or not shifted.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. When the clock is low, these latches hold the RAM data to eliminate any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) performs three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers can be inhibited so no data is passed.

The ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) as inputs (source operands), while the ALU S-input multiplexer has the RAM A-port, the RAM B-port, and the Q register as inputs (source operands). The microinstruction inputs used to select these source operands are the I0, I1, and I2 inputs.

The D input is the 4-bit wide direct data field input through which all data enters into the working registers inside the device. This input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file used primarily for multiplication and division routines. It can also be used as an accumulator or holding register.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I3, I4, and I5 microinstruction inputs are used to select the ALU function. The ALUs of several 100001073s are usually cascaded in a look-ahead carry mode. The Carry generate $(\overline{G})'$ and carry propagate $(\overline{P})$ outputs are used with a carry-look-ahead generator. A carry-out, Cn+4, is also available as an output for use as the carry flag in a status register. Both carry-in (Cn) and carry-out (Cn+4) are active high.

The ALU has three other status-oriented outputs: F3, F=0, and overflow (OVR). The F3 output is the most significant (sign) bit of the ALU. It can be used to determine positive or negative results without enabling the three-state data outputs. F3 is non-inverting with respect to the sign bit output Y3. The F=0 is an open collector output which is used for zero detect because it is high when all F outputs are low. When a overflow condition exists, the overflow output (OVR) is high.

The ALU data output goes to several places. It can be a data output of the 100001073 and it can also be stored in the RAM or the Q register. The ALU destination functions are defined by the I6, I7, and I8 microinstruction inputs.

The four-bit data output field (Y) has three-state outputs which are enabled by the output control (OE)'. When OE' is high, the Y outputs are in the high-impedance state.

A two-input multiplexer is used at the data output to select either the outputs of the RAM A-port or the ALU (F) as Y outputs. This selection is controlled by the I6, I7, and I8 microinstruction inputs.

The three-input multiplexer which drives the RAM inputs allows the ALU outputs to be entered non-shifted, shifted up one position or shifted down one position. The shifter has two ports: RAM0-LO/RI and RAM3-RO/LI. Both ports consist of a buffer-driver with a three-state output and an input to the multiplexer. In shift up mode, the RO buffer and the RI multiplexer input are enabled, while in shift down mode, the LO buffer and LI input are enabled. In the no-shift mode, both the LO and RO buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I6, I7, and I8 microinstruction inputs.

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100001073
(Continued)

The Q register is also driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports: Q0-LO/RI and Q3-RO/LI. These ports operate in the same way as the RAM shifter and are controlled by I6, I7, and I8.

The RAM, the Q register, and the A and B data latches are controlled by the clock input. When enabled, data is clocked into the Q register on the low-to-high clock transition. When the clock input is high, the A and B latches are open and pass the data present at the RAM outputs. When the clock input is low, the latches are closed and retain the last data entered. If the RAM-EN is enabled, new data is written into the RAM file (word) which is specified by the B address field when the clock input is low.

The 100001073 has tri-state outputs.

NOTE *The 100001073 is a low power Schottky device.*

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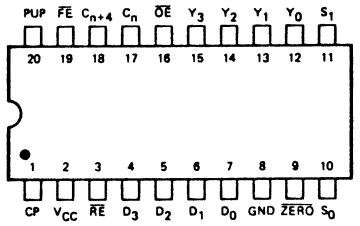
100001074

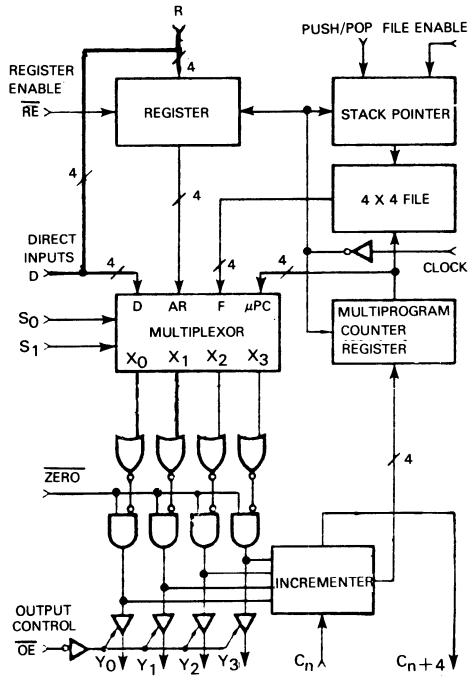
Microprogram Sequencer

PIN CONFIGURATION



Note: Pin 1 is marked for orientation.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



DEFINITION OF TERMS

C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External

A*	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

Inputs

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs

Y_i	Address outputs. (Address inputs to control memory.)

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100001074
(Continued)

ADDRESS SELECTION

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

OUTPUT CONTROL

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

OUTPUT AND INTERNAL NEXT-CYCLE REGISTER STATES

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

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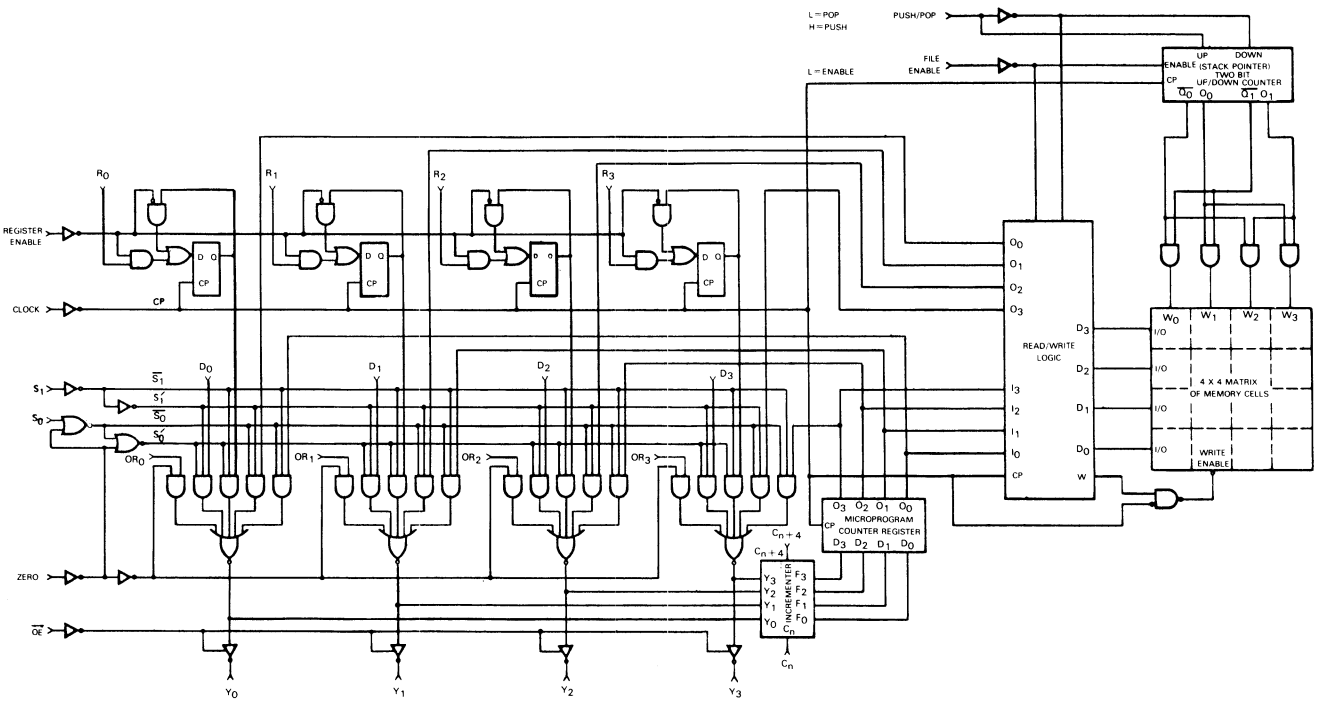
100001074
(Continued)

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



Note: R_i and D_i connected together and OR_i removed.

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100001074
(Continued)

The 100001074 is a bipolar microprogram sequencer consisting of a 4-bit cascadable slice. Two 100001074s can address up to 256 words of microprogram and three devices can address up to 4K words of microprogram.

A four-input multiplexer is used select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. The S0 and S1 inputs control this multiplexer.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is low, data enters the register on the low-to-high transition of the clock. The 4-bit direct data inputs are also used as inputs to the register to permit an N-way branch where N is any word in the microcode.

The microprogram counter (uPC) consists of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (Cn) and carry-out (Cn+4). When the least significant carry-in to the incrementer is high, the current Y output word plus one is loaded into the microprogram register on the next clock cycle. In this way, sequential microinstructions can be executed. When the least-significant Cn is low, the incrementer passes the Y unmodified and this same word is loaded into the microprogram register on the next clock cycle. In this way, the same microinstruction can be executed any number of times by using the least-significant Cn as the control.

The file is a 4 x 4 stack which provides the return address linkage when executing microsubroutines. It contains a stack pointer (SP) which points to the last file word written. This permits stack reference operations to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. The Push operation is enabled when the file enable is low and the push/pop input is high. When this happens the stack pointer increments and the file is written with the appropriate return linkage (the next microinstruction address after the subroutine jump which initiated the Push). A Pop operation is enabled when the file enable is low and the push/pop input is low. The stack pointer decrements on the next low-to-high clock transition. When the file enable is high, no action is taken by the stack pointer regardless of any other input.

When the Zero input is low, all Y outputs are low regardless of any other inputs (except $\overline{OE}$). Each Y output bit has an independent OR input so a conditional logic one can be forced at each Y output to allow jumping to different microinstructions on programmed conditions.

The 100001074 has tri-state outputs.

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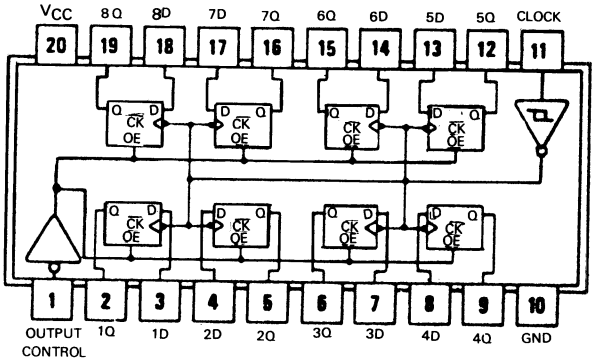
100001075

Octal D-Type Edge-Triggered Flip-Flops with Tri-State Outputs

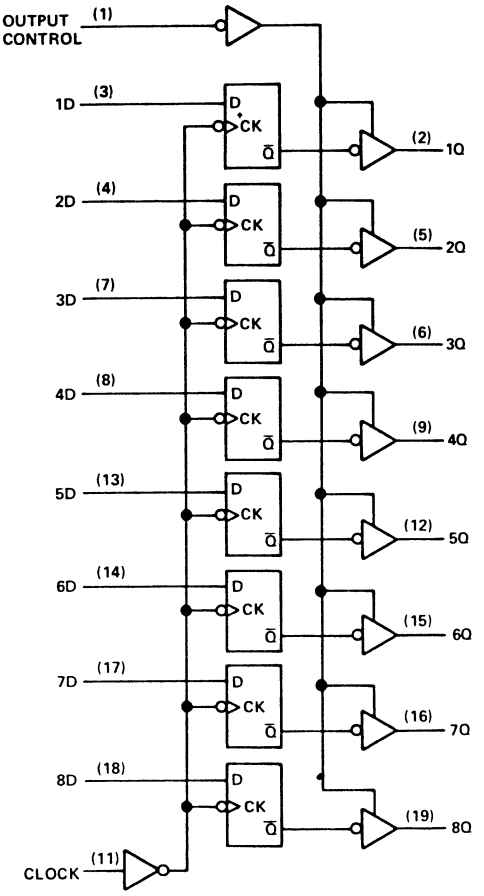
PIN CONFIGURATION



FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

BLOCK DIAGRAM



The 100001075 is an 8-bit register containing edge triggered D-type flip-flops with totem-pole tri-state outputs. The D inputs are applied to the Q outputs on the positive transition of the clock.

The buffered output control will place the outputs in a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs can neither load nor drive the bus lines. Data can be retained or new data entered even when the outputs are off.

NOTE *The 100001075 is a low power Schottky device.*

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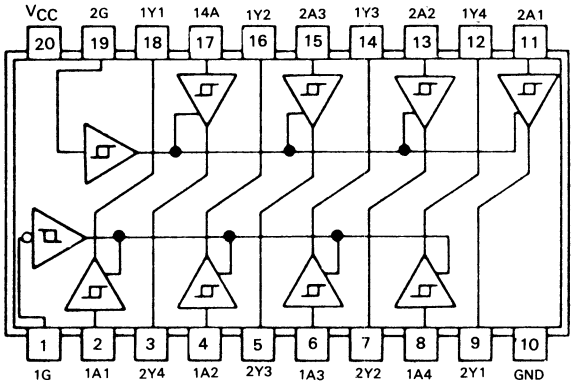
100001076

Octal Buffer And Line Driver With 3-State Outputs

PIN CONFIGURATION



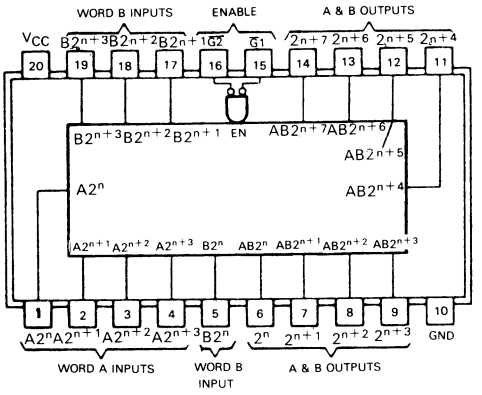
This device features three-state outputs, and selectable combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

NOTE *The 100001076 is a low power Schottky device.*

100001077

4-Bit-by-4-Bit Binary Multiplier

PIN CONFIGURATION



positive logic: When either (or both) $\overline{G}$ input(s) is (are) high, all eight outputs are off.

The 100001077 is a 4-bit by 4-bit parallel multiplier which produces 8-bit products. For words longer than 4 bits, these multipliers can be combined to produce sub-multiple partial products. These partial products can be combined in Wallace trees to obtain the final product. The device has tri-state output.

NOTE *The 100001077 is a Schottky device.*

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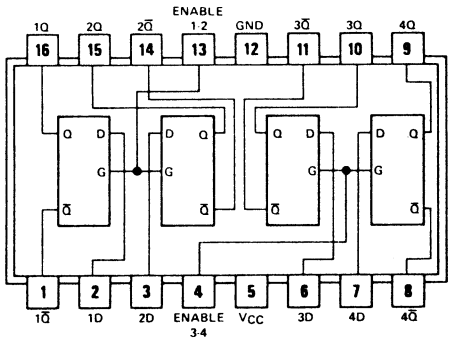
100001078

4-Bit Bistable Latch

PIN CONFIGURATION



logic: see function table

FUNCTION TABLE

(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

The 100001078 is a 4-bit latch with Q and $\overline{Q}$ outputs. Data present at the D inputs is transferred to the Q outputs when the enable G is high. As long as the enable remains high, the Q outputs will follow the D inputs. When the enable goes low, the data present at the time of the transition is held at the Q output until the enable goes high.

NOTE *The 100001078 is a low power Schottky device.*

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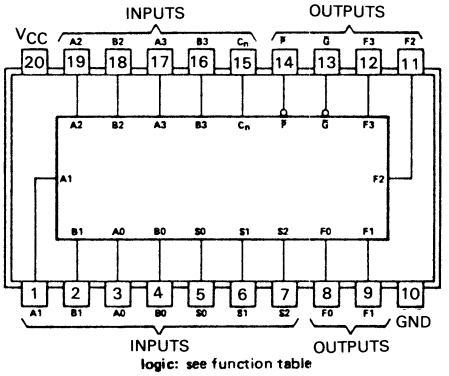
100001079

Arithmetic Logic Unit/Function Generator

PIN CONFIGURATION



logic: see function table

FUNCTION TABLE

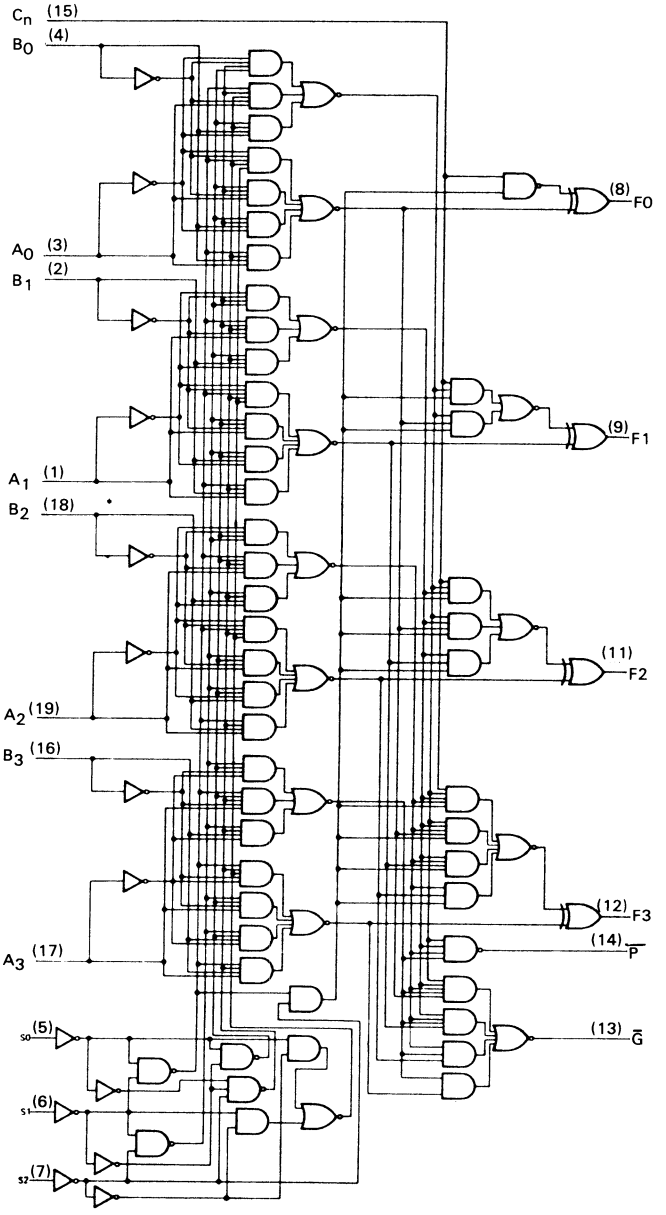
SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$	14	INVERTED CARRY PROPAGATE OUTPUT
$\overline{G}$	13	INVERTED CARRY GENERATE OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

LOGIC DIAGRAM



The 100001079 arithmetic unit/function generator performs eight binary logic/arithmetic operations on two 4-bit words. The function select lines (S0-S2) determine the operation. A full look-ahead carry provides carry generation for the four bits by means of the two cascade outputs $\overline{P}$ and $\overline{G}$. The outputs can either be cleared (low) or preset (high).

NOTE *The 100001079 is a Schottky device.*

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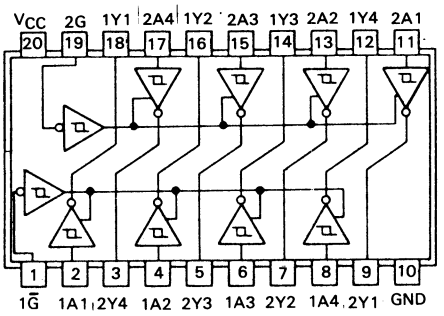
100001080

Octal Buffer And Line Driver

PIN CONFIGURATION



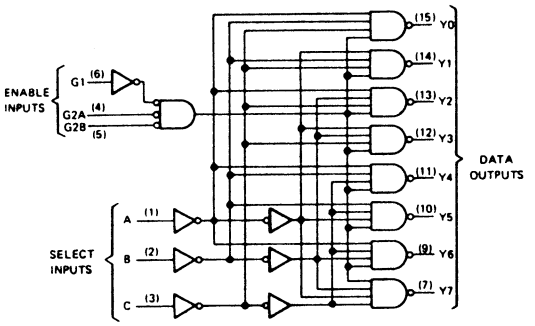
This device features tri-state outputs, and selectable combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

NOTE *The 100001080 is a low power Schottky device.*

100001081

3-to-8-Line Decoder/Demultiplexer

BLOCK DIAGRAM



NOTE *The 100001081 is a low power Schottky device.*

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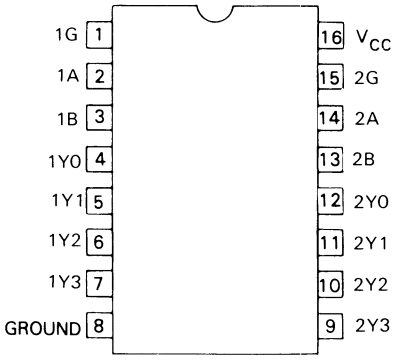
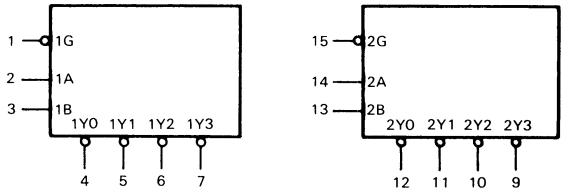
100001082

2-to-4-Line Decoder/Demultiplexer

PIN CONFIGURATION



Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

This is a dual 2-line to 4-line decoder/multiplexer unit. Each decoder has two buffered select inputs, A and B, which are decoded to one of four Y outputs.

An active LOW enable can be used for gating, or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

NOTE *The 100001082 is a low power Schottky device.*

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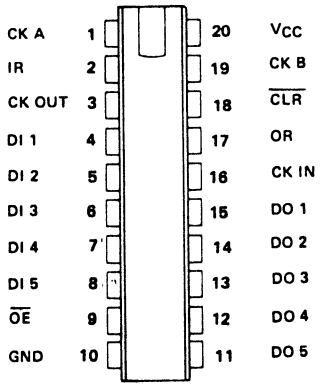
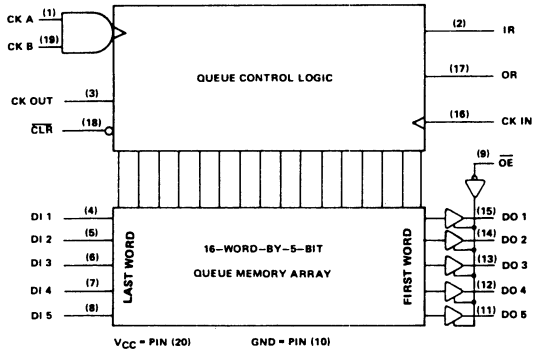
100001083

16 X 5-Bit Asynchronous First-In/First-Out Memory

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

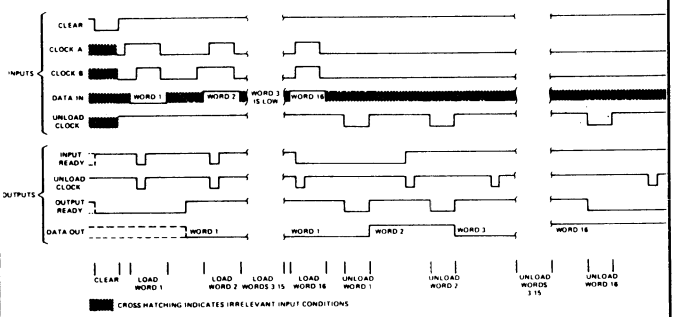
INPUT FUNCTIONS

Input	Pin	Description
CK A	1	Load Clock A
DI 1 - DI 5	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
CK IN	16	Unload Clock Input
$\overline{CLR}$	18	Clear
CK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

OUTPUT FUNCTIONS

Output	Pin	Description
IR	2	Input Ready
CK OUT	3	Unload Clock Output
DO 5 - DO 1	11 - 15	Data Outputs
OR	17	Output Ready

TYPICAL WAVEFORMS



The 100001083 is an 80-bit First-In/First-Out (FIFO) memory organized as 16 words by 5 bits. It processes data in parallel format, word by word, at rates from DC to 10MHz.

The read and write operations are independent using separate synchronous clocks. Data is written into the FIFO on the low-to-high transition of either of the load clock inputs. One clock must be held high during the write operation. Data is read out of the FIFO on the low-to-high transition of the unload clock.

Three outputs provide the status of the FIFO. The input ready output monitors the last word location (location data is read into) and is high whenever this location is available for data. The unload clock output also monitors this location and generates a low signal when it is empty. The output ready output is high when the first word location (location providing data to the outputs) contains valid data and the unload clock is high.

The data outputs are tri-state with a common output enable. When the output enable is low, the data outputs function as totem-pole outputs. A high forces each data output to a high-impedance state while all other inputs and outputs are active.

On the high-to-low transition, the clear input clears the control logic and sets the output ready to a low. The data outputs do not change as a result of the clear input, but the low level of the output ready signifies invalid data.

NOTE *The 100001083 is a Schottky device.*

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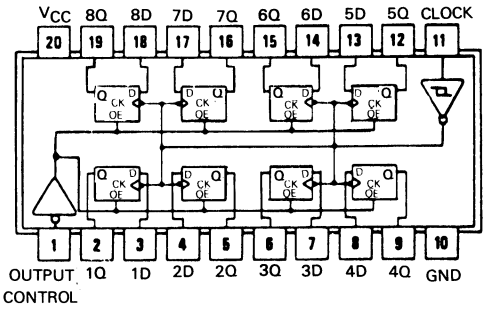
100001084

Octal D-Type Flip-Flop With Clear

PIN CONFIGURATION



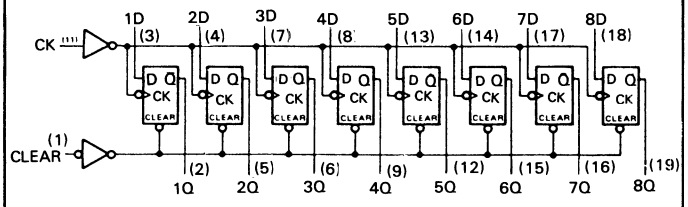
positive logic: see function table

FUNCTION TABLE

(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

BLOCK DIAGRAM



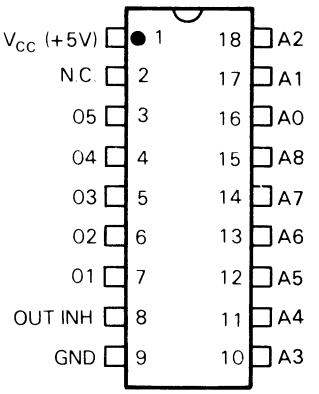
The 100001084 contains eight D-type flip-flops which are triggered on the positive-going edge of the clock pulse.

NOTE *The 100001084 is a low power Schottky device.*

100001085 through 100001089

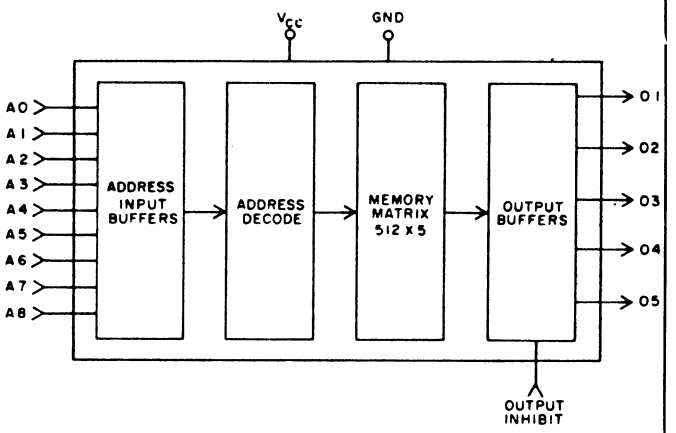
512 x 5-Bit Bipolar PROM

PIN CONFIGURATION



DG-04983

BLOCK DIAGRAM



These 2560-bit read only memories are organized as 512 words by 5 bits and feature tri-state outputs.

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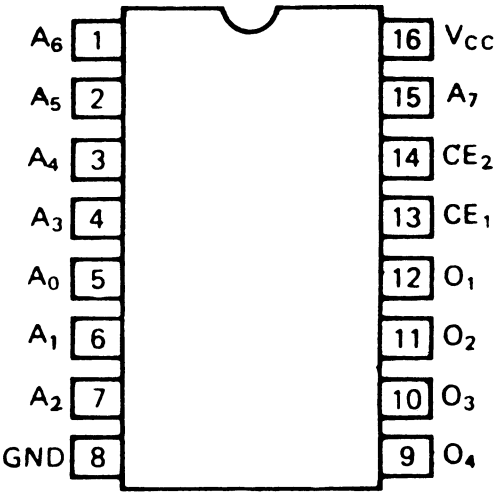
100001090 through 100001097

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION

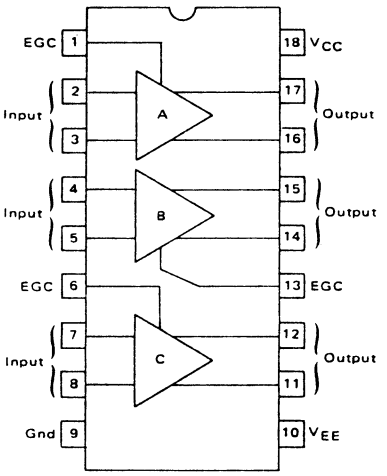


These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

100001098

Triple Wideband Preamplifier With Electronic Gain Control (EGC)

PIN CONFIGURATION



The 100001098 provides three independent preamplifiers with individual electronic gain control. Each preamplifier has differential inputs and outputs for operation in completely balanced systems.

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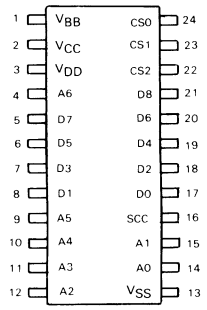
100001099

Column Select Character Generator

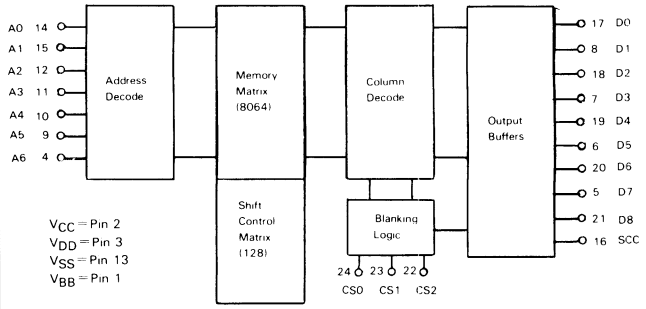
PIN CONFIGURATION



COLUMN SELECT TRUTH TABLE

CS2	CS1	CS0	OUTPUT
0	0	0	0
0	0	1	C1
0	1	0	C2
0	1	1	C3
1	0	0	C4
1	0	1	C5
1	1	0	C6
1	1	1	C7

BLOCK DIAGRAM



This device is a mask-programmable 8192-bit vertical scan (column select) character generator. It contains 128 characters in a 7 x 9 matrix. A Shift Control Command (SCC) bit can be programmed so that a high logic level will appear at the SCC output, in addition to the coding at D0-D8, to indicate that a character is to be shifted.

Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. A 7-bit address code (A0-A6) is used to select one of the 127 available characters programmed in the memory. To output a character addressed by A0-A6, a column select code (CS0-CS2) is sequentially applied. Each column is read at outputs D0-D8. the address inputs.

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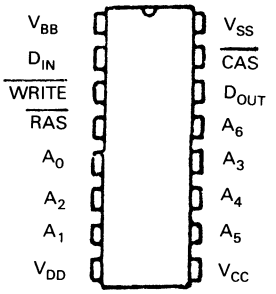
100001100

16384 X 1 Bit NMOS RAM

PIN CONFIGURATION



A0 - A6	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
VBB	Power (-5V)
VCC	Power (+5V)
VDD	Power (+12V)
VSS	Ground

Each device contains 16384 (16384 x 1) addressable storage cells and the necessary circuitry to address, write, read and refresh each cell without pattern dependence.

The 14 address bits required to decode 1 of the 16384 cell locations are multiplexed onto the 7 address inputs (A0 - A6) and latched into the on-chip address latches by externally applying two negative going TTL-level clocks ($\overline{RAS}$ and $\overline{CAS}$). The first clock, the ROW ADDRESS STROBE ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the COLUMN ADDRESS STROBE ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. $\overline{CAS}$ can be externally actived as soon as the Row Address Hold time (tRAH) has been satisfied and the address inputs have been changed from ROW address to COLUMN address information.

Data is written while $\overline{RAS}$ is active. The latter falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data into the on-chip data latch.

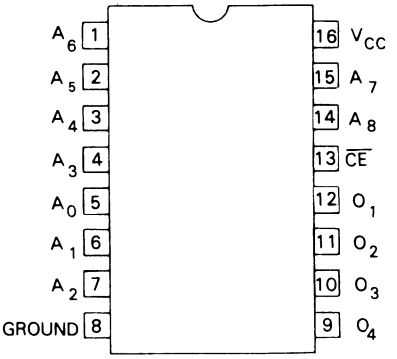
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (Low).

This is an NMOS device.

100001101 through 100001142

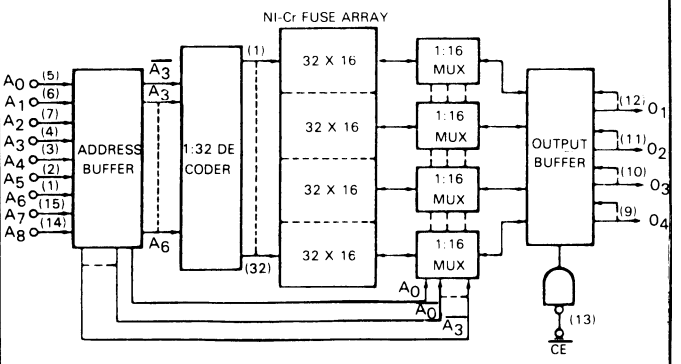
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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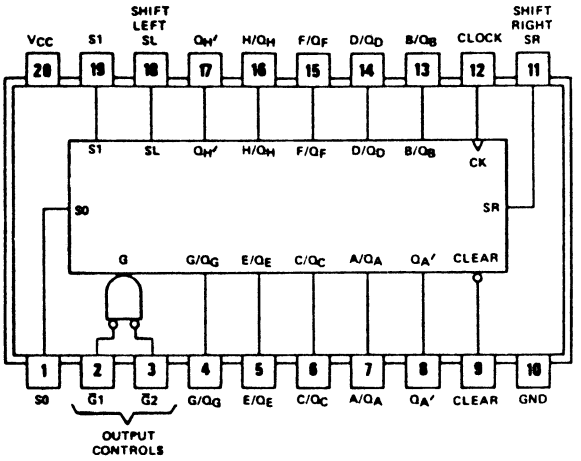
100001150

8-Bit Universal Shift/Storage Register

PIN CONFIGURATION



FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

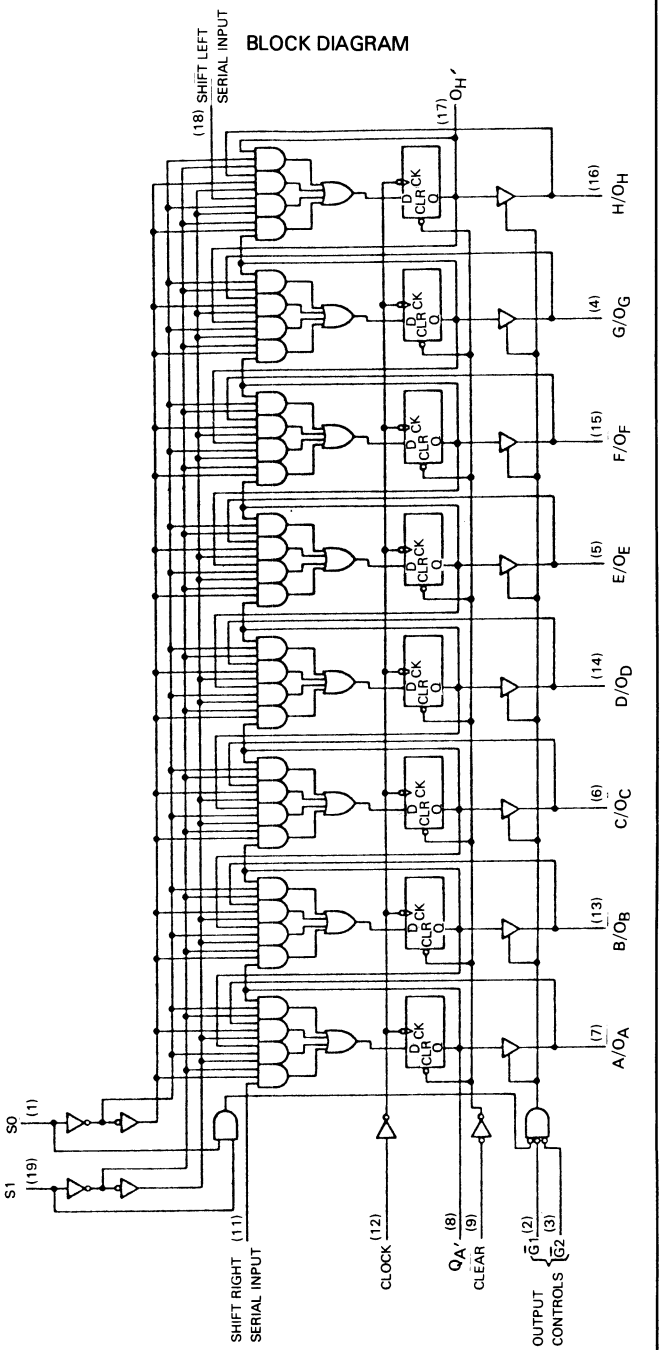
a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

The 100001150 is controlled by two function select inputs and two output control outputs which select the four operating modes listed in the function table.

In load mode, the tri-state outputs are in a high-impedance state to permit data to be clocked into the register. Data can be read when the outputs are enabled in any mode. The register can be cleared at any time using the clear input.

NOTE *The 100001150 is a low power Schottky device.*

BLOCK DIAGRAM



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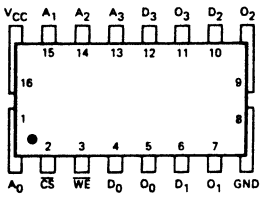
100001151

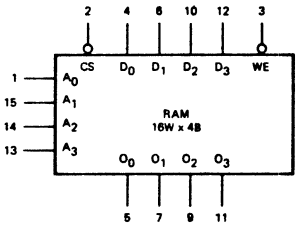
16 x 4-Bit RAM

PIN CONFIGURATION



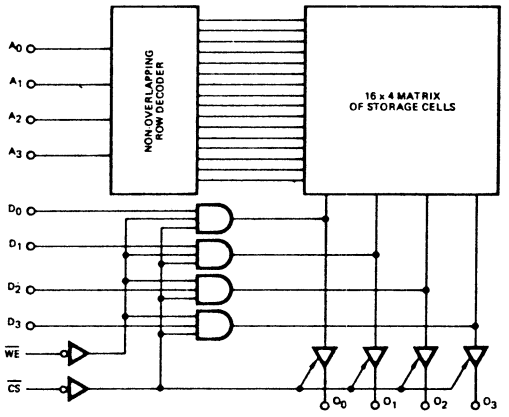
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

BLOCK DIAGRAM



The 100001151 is a 64-bit random access memory organized as 16 words by 4 bits. It includes an active low chip select input ($\overline{CS}$) and tri-state outputs.

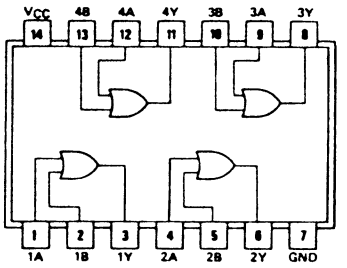
Data on the inputs D0 to D3 is written into the addressed memory word when the write line ($\overline{WE}$) is low and the chip is selected. Data is read out on the outputs O0 to O3 when the write line is high and the chip is selected. The outputs are in an inactive high impedance state during the write operation or when the chip select is high.

NOTE *The 100001151 is a Schottky device.*

100001152

Quad 2-Input OR Gate

PIN CONFIGURATION



NOTE *The 100001152 is a low power Schottky device.*

$$Y = A + B$$

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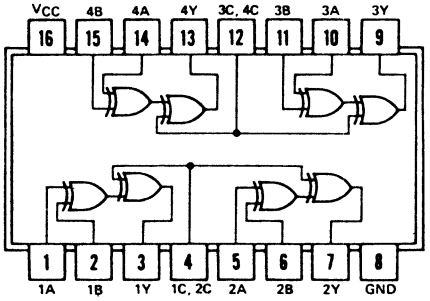
100001153

Quad Exclusive-OR/NOR Gates

PIN CONFIGURATION



positive logic: $Y = (A \oplus B) \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

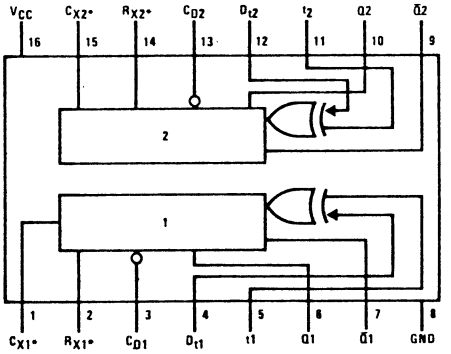
H = high level, L = low level

NOTE *The 100001153 is a Schottky device.*

100001154

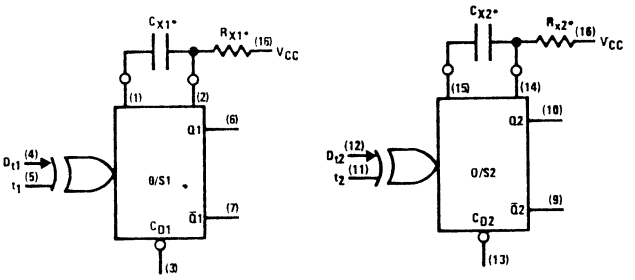
Dual Retriggerable Resettable One Shot

PIN CONFIGURATION



*Pins for external timing

LOGIC DIAGRAMS



*A non-inverting buffer with delay

TRUTH TABLE

t	D_t	C_D	OPERATION
L → H	L	H	Trigger
H	H → L	H	Trigger
H → L	H	H	Trigger
L	L → H	H	Trigger
H → L	Same as t	H	Trigger
L → H	Same as t	H	Trigger
X	X	L	Reset

The 100001154 contains two retriggerable, resettable monostable multivibrators. Each has a standard trigger input and a delay trigger input which are exclusive ORed together. In the dual-edge triggering mode, the two inputs are tied together. On either the postive or negative transition the exclusive OR is satisfied for the length of time equal to the delay on the delay input, and the one-shot is triggered or retriggered.

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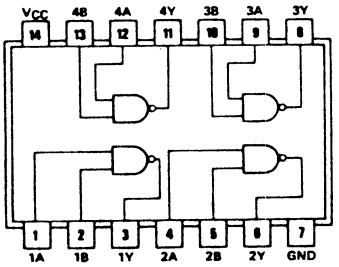
100001174

Quad 2-Input High Voltage Interface NAND Gates

PIN CONFIGURATION



positive logic:
$Y = \overline{AB}$

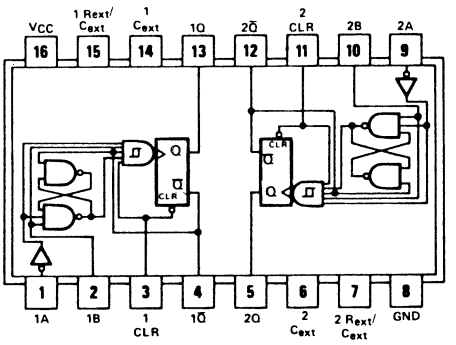
The 100001174 has open-collector outputs.

NOTE *The 100001174 is a low power Schottky device.*

100001175

Dual Monostable Multivibrator With Schmitt-Trigger Inputs

PIN CONFIGURATION



positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

FUNCTION TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high-level pulse
⎎ = one low-level pulse
X = irrelevant

The 100001175 consists of two multivibrators each of which has a negative and a positive transition triggered input. Either input can be used as an inhibit input.

Triggering occurs at a particular voltage level. The outputs depend on the timing components and are independent of transitions on the A and B inputs once they are fired. The ouput can be cleared any time by the clear input (CLR).

NOTE *The 100001175 is a low power Schottky device.*

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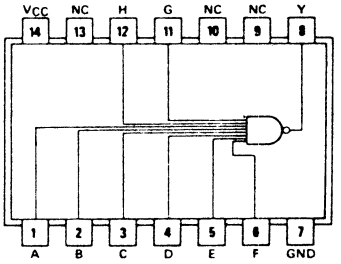
100001176

8-Input NAND Gate

PIN CONFIGURATION



positive logic:

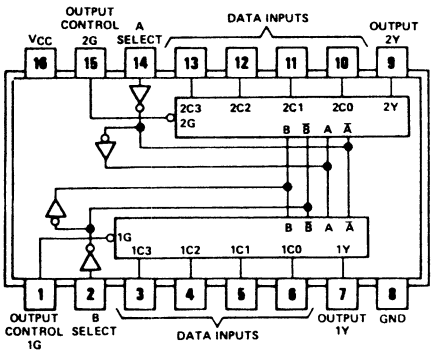
$Y = \overline{ABCDEFGH}$

NOTE *The 100001176 is a low power Schottky device.*

100001177

Dual 4-Line-To-1-Line Data Selector/Multiplexer With Three-State Outputs

PIN CONFIGURATION



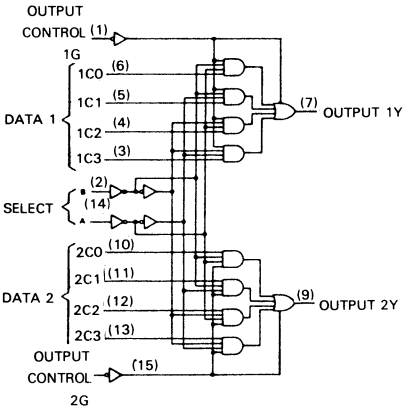
FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

BLOCK DIAGRAM



The 100001177 data selector/multiplexor contains inverters and drivers which provide complementary, on-chip, decoding data selection to the AND-OR gates. Each of the two four line sections has it own output control inputs. Its outputs are tri-state.

NOTE *The 100001177 is a low power Schottky device.*

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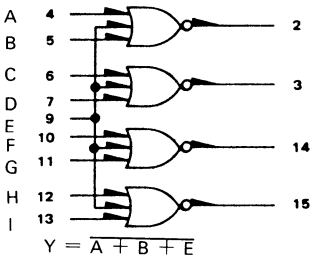
100001178

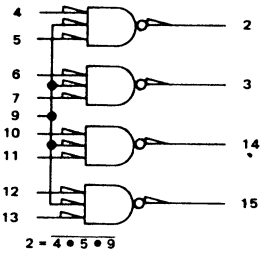
Quad 2-Input NOR Gate With Strobe

LOGIC DIAGRAMS

POSITIVE LOGIC



NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

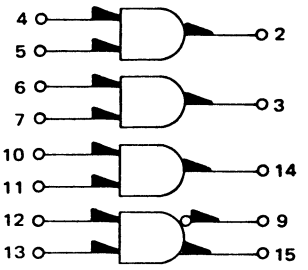
Each of the four NOR gates on the 100001177 has three inputs. Two are independent and the other is common to all the gates. The outputs are open emitter. It is in a 16-pin package.

NOTE: *This is an ECL device.*

100001179

Quad 2-Input AND Gate

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$$Y = AB$$
$$\overline{Y}_9 = \overline{AB}$$

NOTE: *This is an ECL device with a 16-pin ceramic package.*

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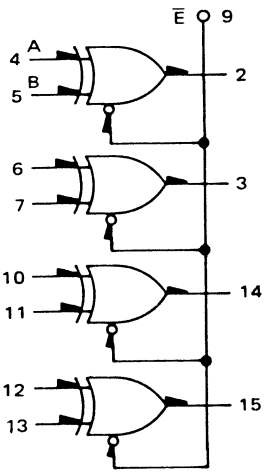
100001180

Quad Exclusive OR Gate

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$$Y = (\bar{A}B + A\bar{B})\,\bar{E}$$

TRUTH TABLE

A	B	Ē	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

ϕ = Don't Care

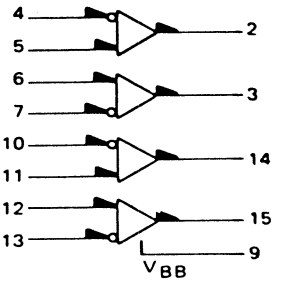
The 100001180 consists of four exclusive OR gates with a common enable. The open emitter outputs allow direct connection of the outputs to a bus.

NOTE: *This is an ECL device.*

100001181

Quad Line Receiver

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

The 100001181 contains four differential amplifiers for use in sensing differential signals. The base bias supply (VBB) is available at pin 9 so the device can be used in applications where a constant reference voltage is necessary. Each unused amplifier must have one input connected to VBB to prevent the current source bias network from being disturbed.

NOTE: *This is an ECL device.*

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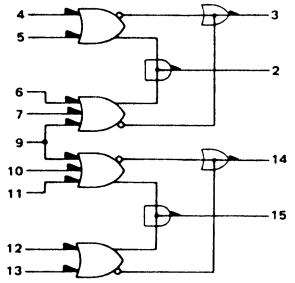
100001182

Dual 2-Wide 2-3-Input OR-AND/OR-AND-Invert Gate

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

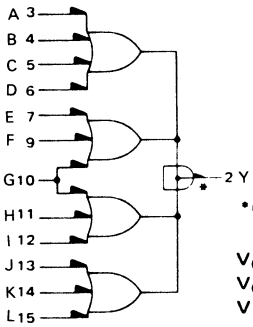
$$Y_3 = \overline{(A + B)} + \overline{(C + D + E)}$$
$$Y_2 = (A + B)(C + D + E)$$

NOTE: *This is an ECL device.*

100001183

4-Wide 4-3-3-3-Input OR-AND Gate

LOGIC DIAGRAM



*Collector Dot

V_{CC1} = Pin 1
V_{CC2} = Pin 2
V_{EE} = Pin 8

$$Y = (A + B + C + D)(E + F + G)(G + H + I)(J + K + L)$$

NOTE: *This is an ECL device.*

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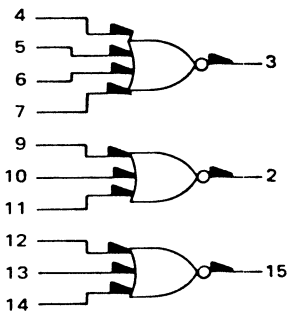
100001184

Triple 4-3-3-Input Bus Driver

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$$Y_3 = \overline{A + B + C + D}$$
$$Y_2 = \overline{A + B + C}$$

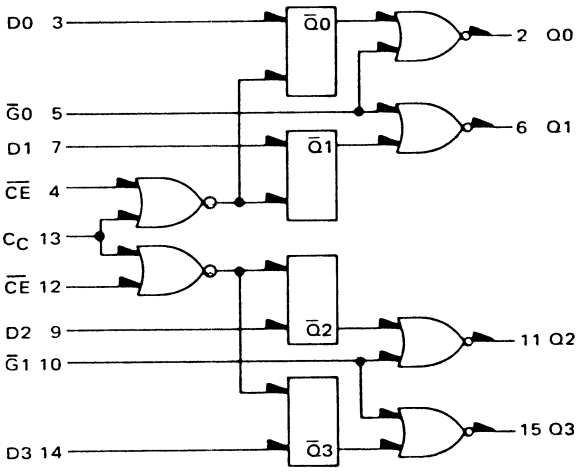
The 100001184 consists of three NOR gates designed for bus driving. When low, each gate output appears as a high impedance to the bus because the output emitter-followers are turned off.

NOTE: *This is an ECL device.*

100001185

Quad Latch (Negative Clock)

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

$\overline{Q}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
$C = C_C + \overline{CE}$

The 100001185 consists of four bistable latch circuits with D type inputs, gated Q outputs, and open emitter outputs. The outputs follow the D inputs when the clock is low. Information is latched on the positive going transition of the clock.

NOTE: *This is an ECL device.*

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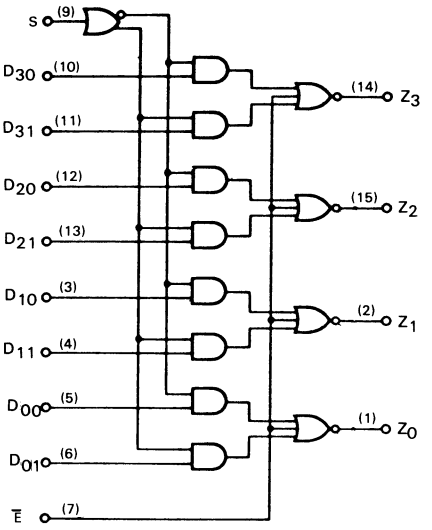
100001186

Quad 2-To-1 Multiplexers

LOGIC DIAGRAM



$V_{CC1} = V_{CC2} = 1$,
$V_{EE} = 8$
POSITIVE LOGIC:HIGH LEVEL = "1"

TRUTH TABLE

INPUTS				OUTPUTS
Dno	Dni	S	E	Zn
X	X	X	H	L
L	X	L	L	H
H	X	L	L	L
X	L	H	L	H
X	H	H	L	L

X = Don't care

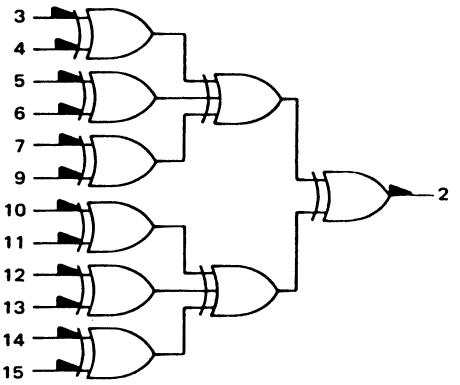
These multiplexers transmit data on either of two input pins to a common output pin in response to a single control signal. They also feature a common enable input, high Z input pulldown resistors, and inverting open emitter outputs.

NOTE: *This is an ECL device.*

100001187

12-Bit Parity Generator/Checker

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

The 100001187 consists of nine exclusive OR gates which are connected to provide odd parity checking or generation. When an odd number of inputs are high, the output goes high. Unconnected inputs are pulled to low logic levels to allow parity detection and generation for less than 12 bits.

NOTE: *This is an ECL device.*

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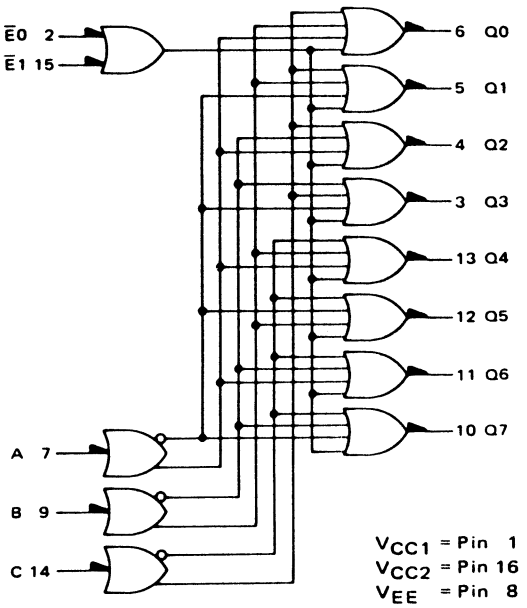
100001188

Binary To 1-8 Line Decoder

LOGIC DIAGRAM



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
Ē1	Ē0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	φ	φ	φ	φ	H	H	H	H	H	H	H	H
φ	H	φ	φ	φ	H	H	H	H	H	H	H	H

φ = Don't Care

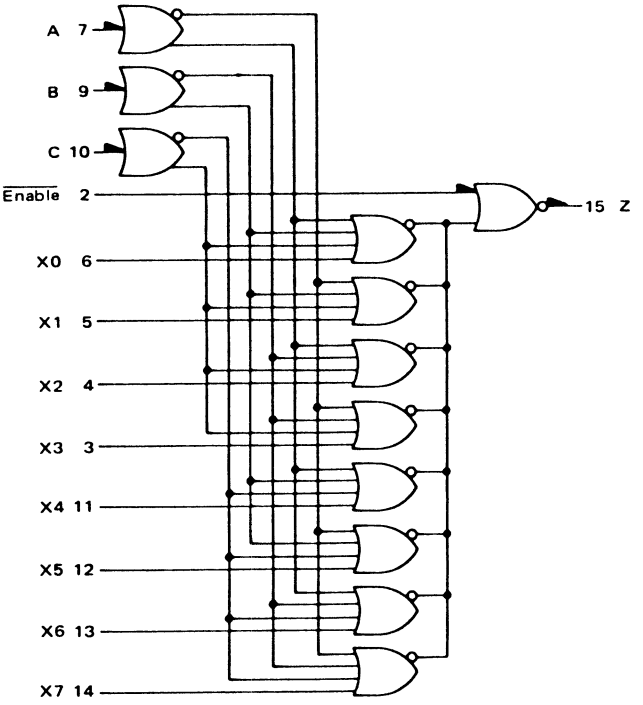
The 10000118 decodes a three bit input word to a one of eight line output. The selected output is low while all other outputs are high. When either or both the enable inputs are high, all out outputs are forced high. This device has high Z input pulldown resistors and open emitter outputs.

NOTE: *The 100001188 is an ECL device.*

100001189

8-Line Multiplexer

LOGIC DIAGRAM



TRUTH TABLE

ENABLE	ADDRESS INPUTS			Z
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	φ	φ	φ	L

φ = Don't Care

The 100001189 is an eight-channel data selector which transfers data present at one-of-eight inputs to the output. The data is transferred according to the three bit code present on the address inputs. An enable input allows for bit expansion.

NOTE: *The 100001189 is an ECL device.*

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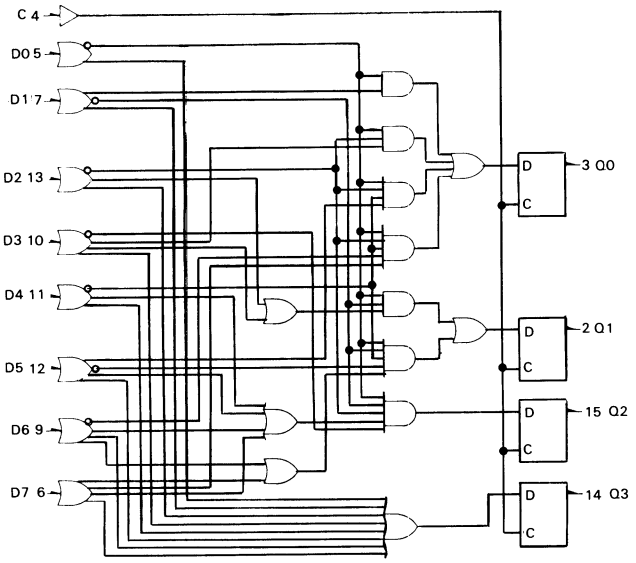
100001190

8-Input-Priority Encoder

BLOCK DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	L
L	H	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	L	H
L	L	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	L	H	L
L	L	L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H
L	L	L	L	H	ϕ	ϕ	ϕ	H	H	L	L
L	L	L	L	L	H	ϕ	ϕ	H	H	L	H
L	L	L	L	L	L	H	ϕ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ϕ = Don't Care

The 100001190 is designed to encode eight inputs to a binary coded output. The output code is that of the highest order input and all other inputs of lower priority are ignored. Each output includes a latch which allows for synchronous operation. The outputs follow the inputs when the clock is low and latch when the clock goes high.

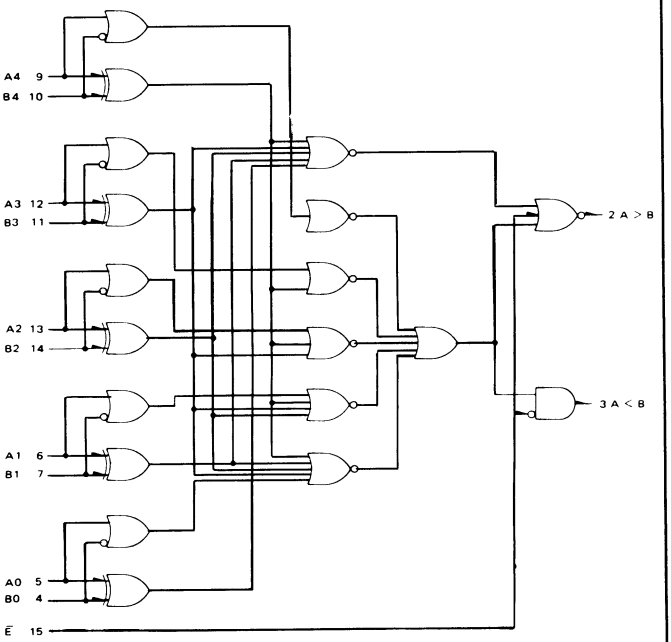
The three binary outputs are low when input D0 is high while the Q3 output is high when any input is high. This permits expansion into another priority encoder when more than eight inputs are required.

NOTE: *This is an ECL device.*

100001191

5-Bit Magnitude Comparator

BLOCK DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Inputs			Outputs	
Ē	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

The 100001191 is a 5-bit comparator which compares the magnitude of two binary words. The two outputs are A < B and A > B. A = B can be produced by NORing the two outputs with an external gate. When the enable is high, both outputs are forced low.

NOTE: *This is an ECL device.*

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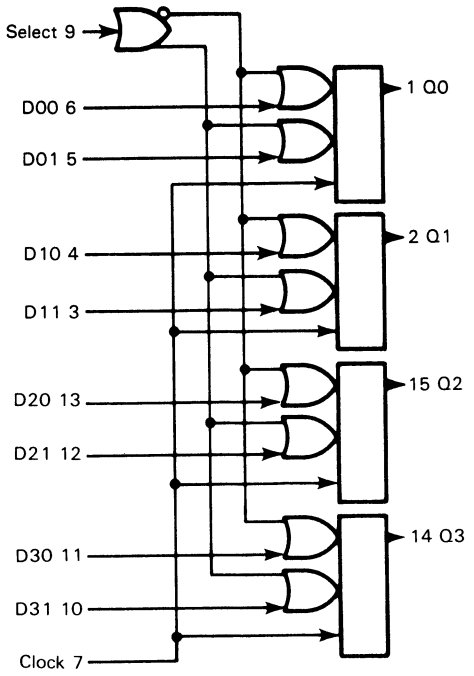
100001192

Quad 2-Input MUX w/Latch

BLOCK DIAGRAM



P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

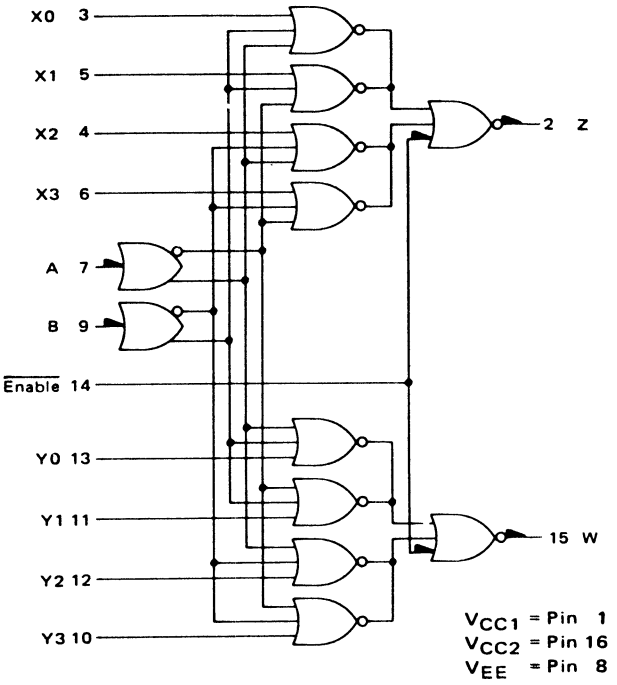
The 100001192 consists of four 2-input multiplexers with latches. The multiplexers use a common clock and common data select inputs. The select input determines which data inputs is enabled. When the select is high, data inputs D00, D10, D20, and D30 are enabled. When it is low, data inputs D01, D11, D21, and D31 are enabled. When the clock is low, any change on the data input will be reflected at the outputs. The outputs are latched on the positive transition of the clock.

NOTE: *This is an ECL device.*

100001193

Dual 4-to-1 Line Multiplexer

BLOCK DIAGRAM



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\bar{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

The 100001193 consists of four 4-input multiplexers with an output enable ($\overline{\text{Enable}}$). The select inputs determine one data input for each multiplexer. When the output enable is high, it forces both outputs low.

NOTE: *This is an ECL device.*

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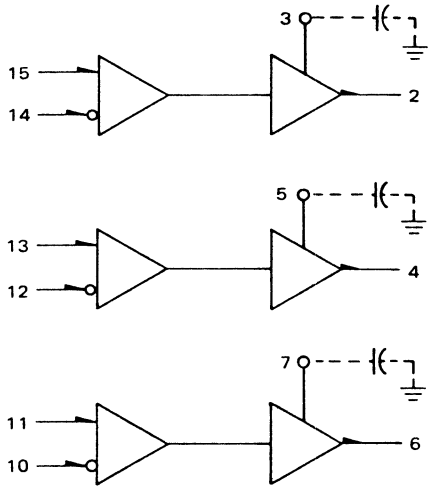
100001194

Triple MECL-to-MOS Translator (N-Channel)

LOGIC DIAGRAM



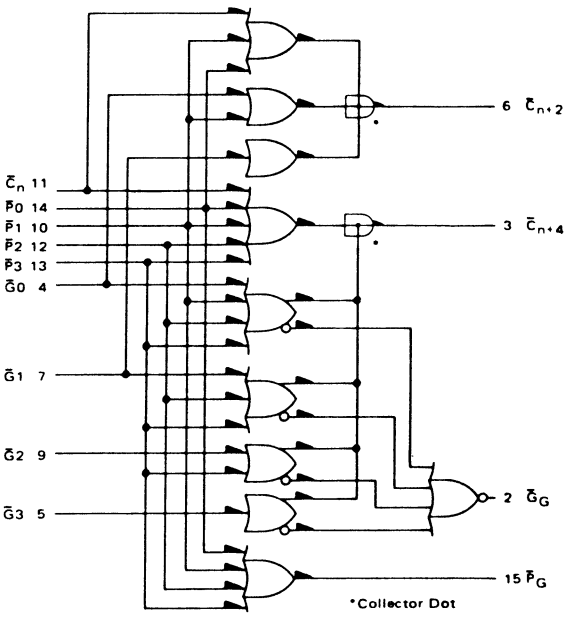
V_{CC} = Gnd = Pins 1, 16
V_{EE} = Pin 8 = -5.2 Vdc ± 5%
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10%)

NOTE: *This is an ECL device.*

100001195

Look Ahead Carry Block

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

NOTE: *This is an ECL device.*

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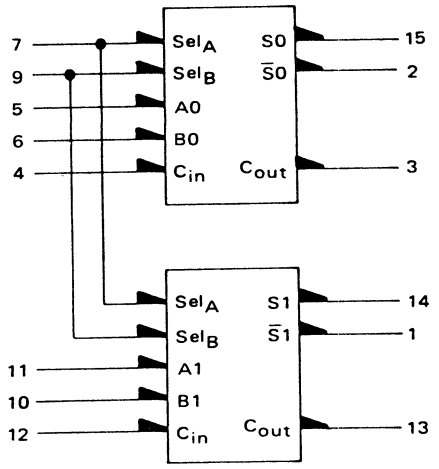
100001196

Dual 2-Bit High-Speed Adder/Subtractor

PIN CONFIGURATION



V_{CC} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

FUNCTION TABLE

FUNCTION	INPUTS Sel_A	Sel_B	A0	B0	C_{in}	OUTPUTS S0	$\overline{S0}$	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	L	H	L
	H	L	L	L	H	H	L	L
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	H
	H	L	H	L	L	L	H	L
	H	L	H	L	H	H	L	H
	H	L	H	H	L	L	H	H
	H	L	H	H	H	H	L	H
REVERSE SUBTRACT	L	H	L	L	L	L	H	L
	L	H	L	L	H	H	L	L
	L	H	L	H	L	L	H	L
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	H
	L	H	H	H	L	L	H	H
	L	H	H	H	H	H	L	H
	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	L
	L	L	L	H	L	L	H	L
	L	L	L	H	H	H	L	H
	L	L	H	L	L	L	H	L
	L	L	H	L	H	H	L	H
	L	L	H	H	L	L	H	H
	L	L	H	H	H	H	L	H

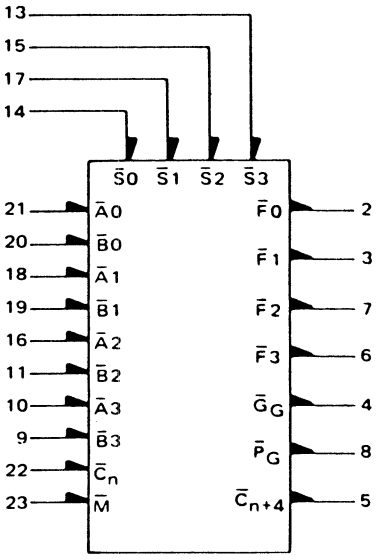
The inputs for the 100001196 adder/subtractor are Carry-in, Operand A, and Operand B. Its outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs function as a control line to invert A for subtract and to invert B.

NOTE: *This is an ECL device.*

100001197

4-Bit Arithmetic Logic Unit

PIN CONFIGURATION



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

FUNCTION TABLE

POSITIVE LOGIC

Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	F = $\overline{A}$	F = A plus 0
L	L	L	H	F = $\overline{A}$ + $\overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	F = $\overline{A}$ + B	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	F = $\overline{A}$ • $\overline{B}$	F = (A + B) plus 0
L	H	L	H	F = $\overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	F = A ⊕ B	F = A plus B
L	H	H	H	F = A + $\overline{B}$	F = A plus (A + B)
H	L	L	L	F = $\overline{A}$ • $\overline{B}$	F = (A + $\overline{B}$) plus 0
H	L	L	H	F = A ⊙ B	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	F = A • $\overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

NOTE: *This is an ECL device.*

The 100001197 is an arithmetic unit which can perform 16 arithmetic operations on two 4-bit words. The select inputs (S0-S3) determine which operation is performed (see the function table).

The group carry propagate (PG) and carry generate (GG) allow for fast operations on long words using a second order look-ahead. The internal carry is enabled when the mode control input (M) is low.

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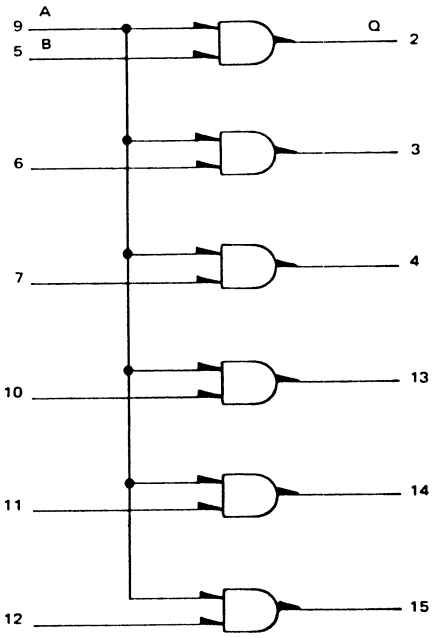
100001198

Hex AND Gate

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$Y = AB$

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

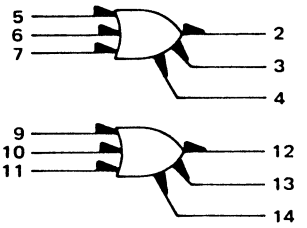
The 100001198 contains six AND gates with a common enable. The open emitter outputs allow wire-ORing.

NOTE: *The 100001198 is an ECL device.*

100001199

Dual 3-Input/3-Output OR Gate

LOGIC DIAGRAM



V_{CC1} = 1, 15
V_{CC2} = 16
V_{EE} = 8

$Y = A + B + C$

NOTE: *The 100001199 is an ECL device.*

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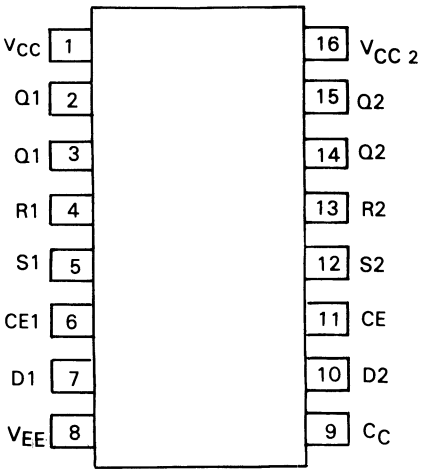
100001200

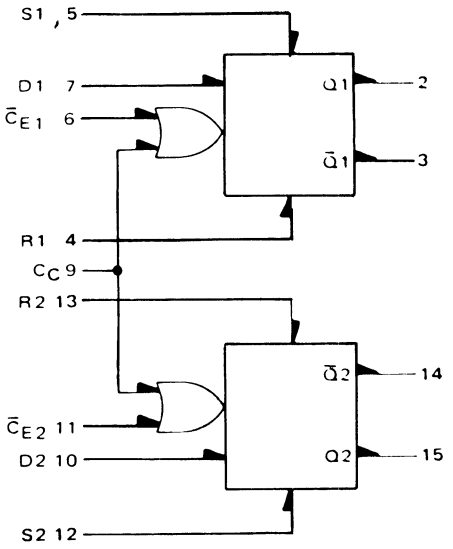
Dual D Flip-Flop

PIN CONFIGURATION



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM

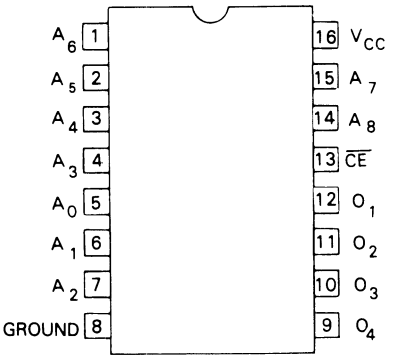


NOTE: *100001200 is an ECL device.*

100001201 through 100001204

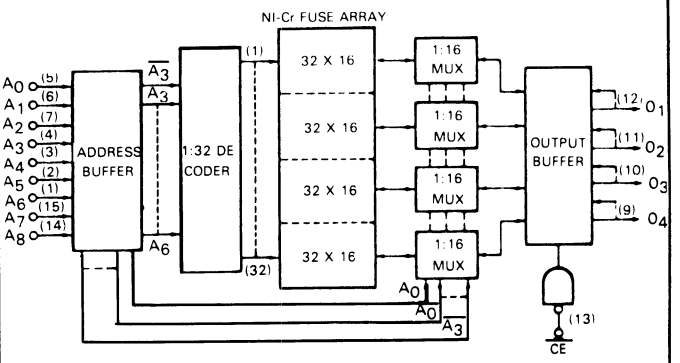
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

NOTE *100001201 through 100001204 are Schottky devices.*

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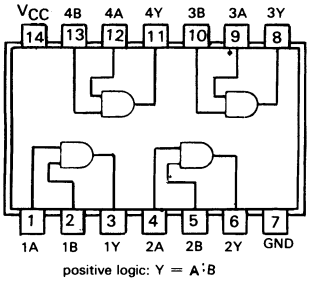
100001206

Quad 2-Input AND Gate

PIN CONFIGURATION



positive logic: Y = A·B

$$Y = AB$$

The 100001206 consists of four 2-input AND gates with open-collector outputs.

NOTE *The 100001206 is a low power Schottky device.*

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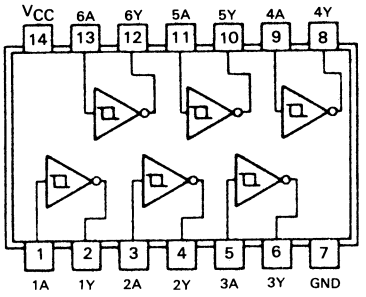
100001207

Hex Schmitt-Trigger Inverters

PIN CONFIGURATION



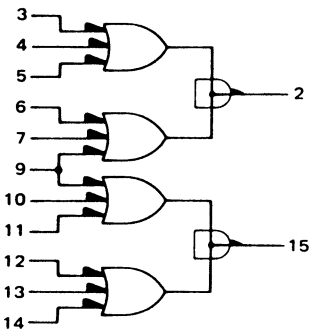
positive logic:
$Y = \overline{A}$

NOTE *The 100001207 is a low power Schottky device.*

100001208

Dual 2-Wide 3-Input OR-AND Gate

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

$$Y = (A + B + C)(D + E + F)$$

NOTE: *The 100001208 is an ECL device.*

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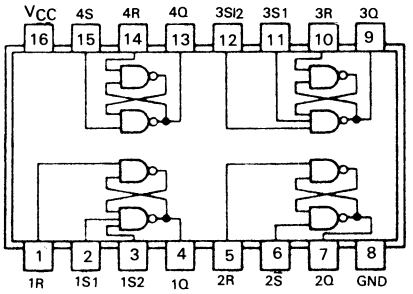
100001209

Quad $\overline{S}$ - $\overline{R}$ Latches

PIN CONFIGURATION



FUNCTION TABLE

INPUTS $\overline{S}$†	$\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

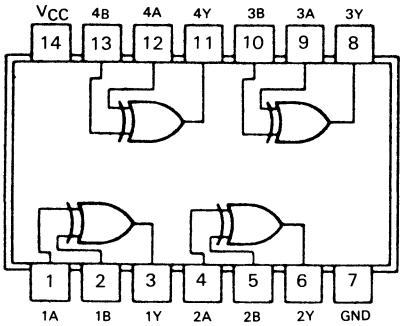
H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

NOTE *The 100001209 is a low power Schottky device.*

100001210

Quad 2-Input Exclusive-OR Gates

PIN CONFIGURATION



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS A	B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

NOTE *The 100001210 is a low power Schottky device.*

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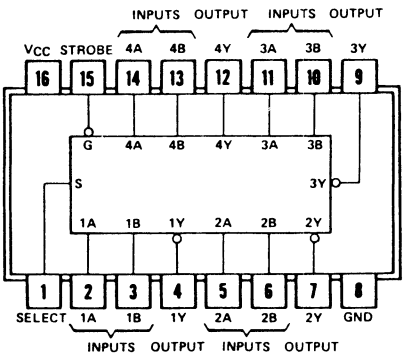
100001211

Quad 2-Line-To-1-Line Data Selector/Multiplexer with Inverted Outputs

PIN CONFIGURATION



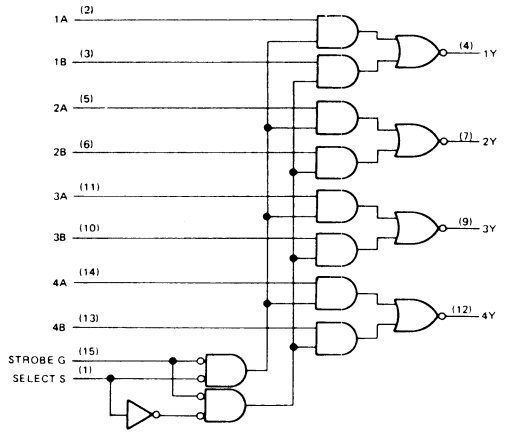
positive logic:
Low level at S selects A inputs
High level at S selects B inputs

FUNCTION TABLE

INPUTS				
STROBE	SELECT	A	B	OUTPUT Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



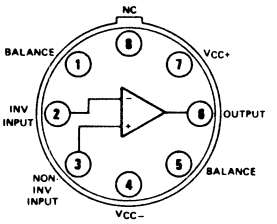
The 100001211 is a selector/multiplexor with inverters and drivers to supply on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The device presents inverted data.

NOTE *The 100001211 is a low power Schottky device.*

100001212

JFET-Input Operational Amplifier

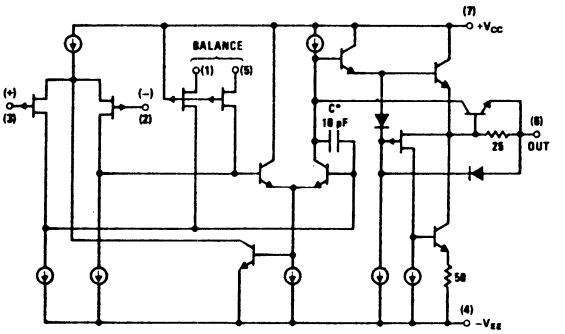
PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

LOGIC DIAGRAM



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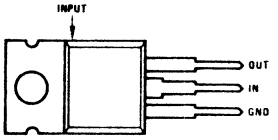
100001213

-15V 1A, 15W, 5% Fixed Voltage Regulator

PIN CONFIGURATION

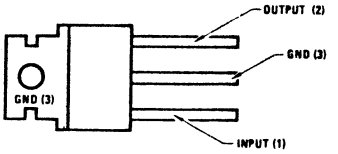


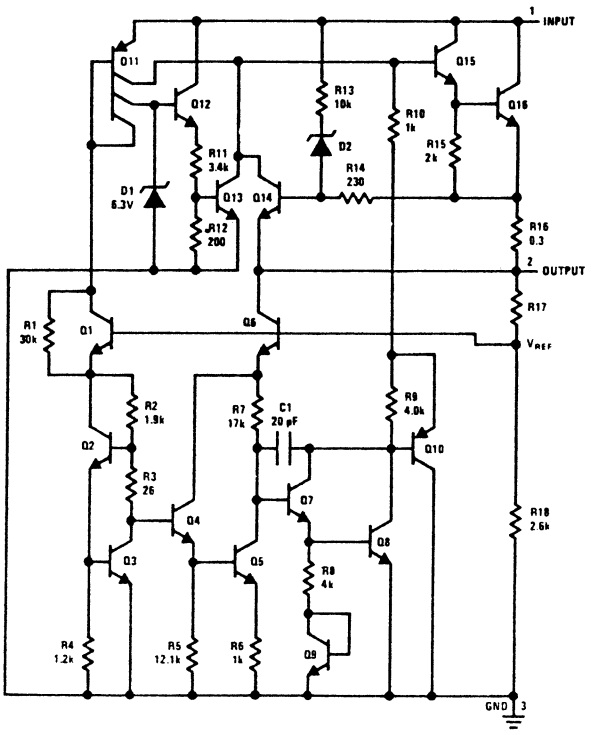
The 100001213 is a three terminal negative regulator with a fixed -15 volt output. It includes a current limiter and a thermal overload protection circuit.

100001214

+15V 1A, 3% Fixed Voltage Regulator

PIN CONFIGURATION





The 100001214 is a three terminal regulator with a fixed 15 volt output. It includes an short circuit current limiter and a thermal overload protection circuit.

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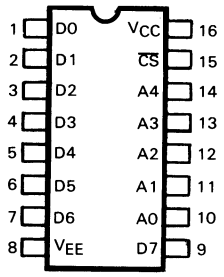
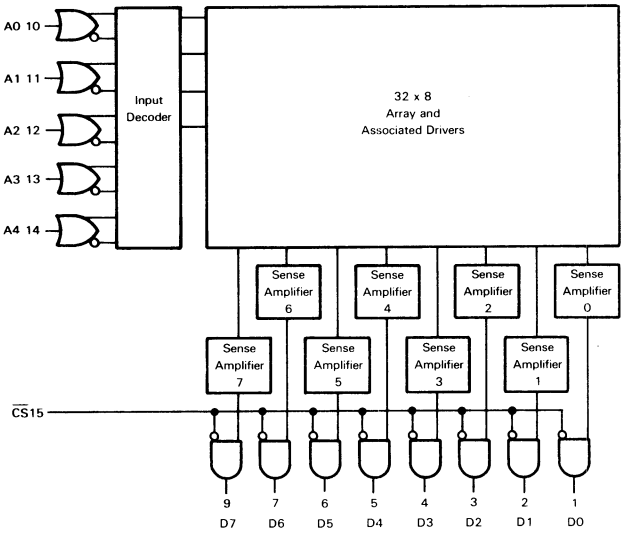
100001215

32 X 8-Bit ROM

PIN CONFIGURATION



BLOCK DIAGRAM



- Typical Address Acces Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 kΩ Input Pulldown Resistors on all inputs
- Power Dissipation (520 mW typ @ 25°C)
- Decreases with Increasing Temperature

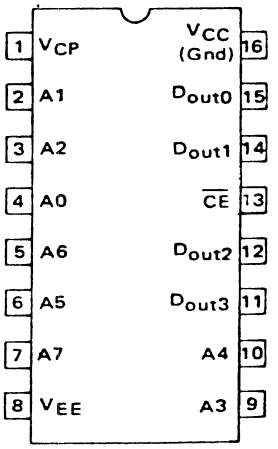
The 100001215 is a 256-bit read only memory organized as 32 words by 8 bits. The words are selected by five binary address lines; full word decoding is incorporated on the chip. The chip enable input causes all eight outputs to go to a low state when it is high. Address to output access time in 15 ns typical.

NOTE: *This is an ECL device.*

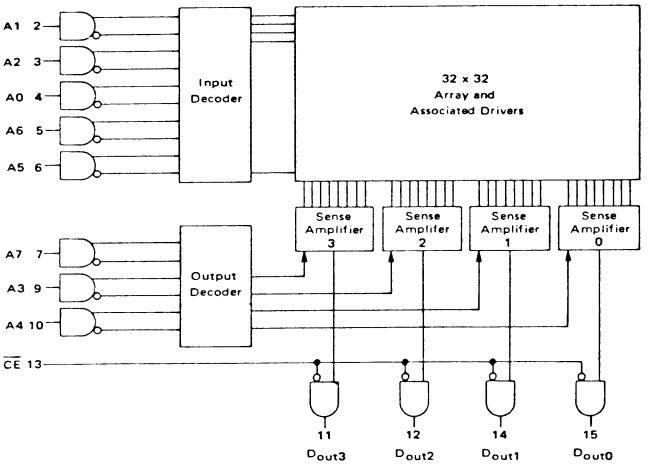
100001216

1024-Bit PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It has a single negative logic chip enable. When the chip is disabled ($\overline{CE}$ = high), all ouutputs are forced to a low logic 0 (low).

NOTE: *This is an ECL device.*

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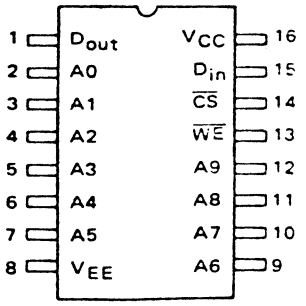
100001217

1024 X 1-Bit RAM

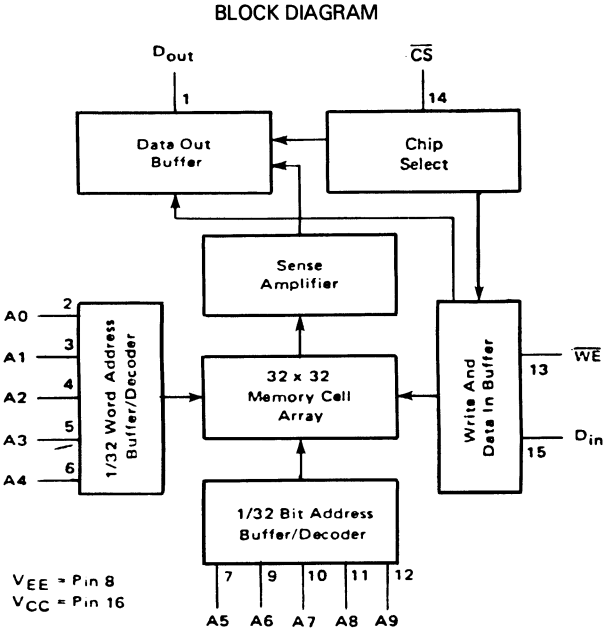
PIN CONFIGURATION



PIN DESIGNATION

CS	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
WE	Write Enable Input

BLOCK DIAGRAM



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

This 1024-bit random access memory is organized as 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) which is decoded on the chip. The chip has a separate data in line, a non-inverting data output, and an active-low chip select. The typical address access time is 20 ns.

NOTE: *This is an ECL device.*

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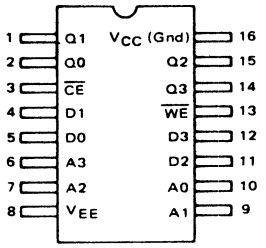
100001218

16 x 4-Bit Register File (RAM)

PIN CONFIGURATION

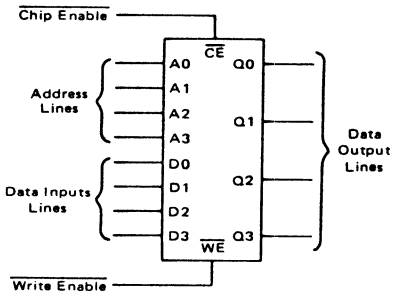


TRUTH TABLE

MODE	INPUT			OUTPUT
	CE	WE	D	Q
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

PIN DESIGNATION



V_{CC} = Gnd
V_{EE} = -5.2 Vdc

This register file is a 64-bit read only memory organized as a 16 x 4 array. It includes fully decoded inputs and an chip enable.

The Write Enable input, when low, allows data to be entered; when high, it disables the data inputs. The Chip Enable input, when low, allows full functional operation of the device; when high, all outputs go to a low logic state.

The device has input pulldown resistors and open emitter outputs.

NOTE: *This is an ECL device.*

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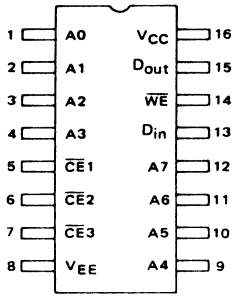
100001219

256 x 1-Bit RAM

PIN CONFIGURATION

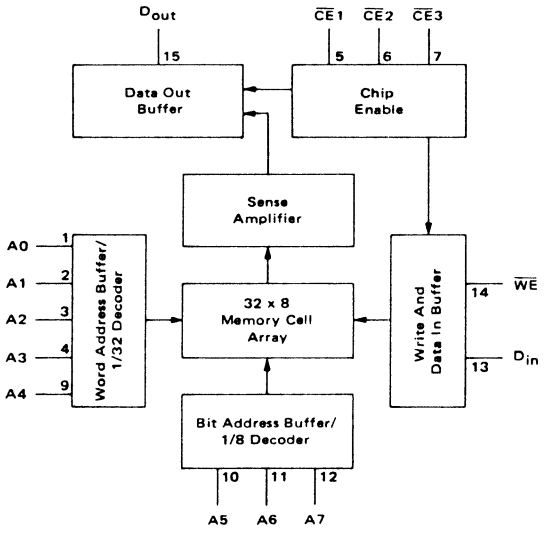


TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

BLOCK DIAGRAM



This 256-bit random access memory is organized as 256 one-bit words. An 8-bit address (A0-A7) selects the stored data. The memory includes three active-low chip enable inputs.

When all the chip enable inputs (CE1'-CE3') are low, the operation of the memory is controlled by the WE' input. If WE' is low, the memory is in write mode. In this mode, the Dout output is low and the data present at the data input (pin 13) is stored at the selected address. If WE' is high, the memory is in the read mode and the data at the selected memory location is presented at the data output (pin 15).

Open emitter outputs permit full wire ORing to data buses, with Q low when the chip is disabled.

NOTE: *The 100001219 is an ECL device.*

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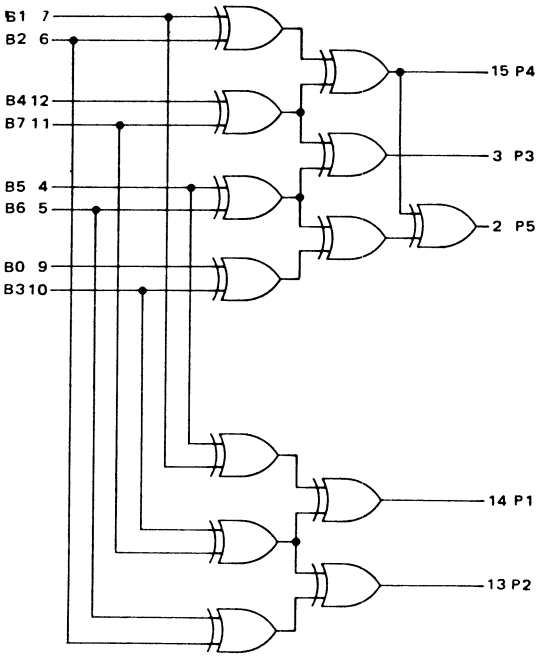
100001221

Error Dectection/Correction Circuit

BLOCK DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

NOTE: *This is an ECL device.*

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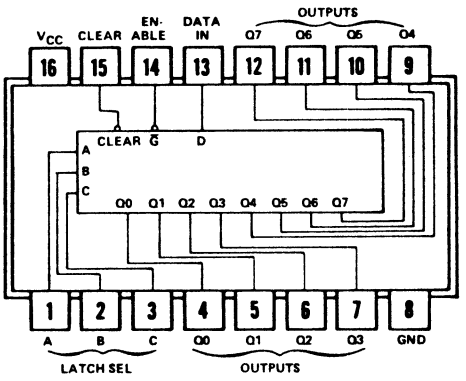
100001222

8-Bit Addressable Latch

PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H ≡ high level, L ≡ low level
D ≡ the level at the data input
Q_{i0} ≡ the level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

Besides storing data in its eight addressable latches, the 100001222 can also function as a 1-of-8 decoder or demultiplexer with active-high outputs. The clear and enable inputs control the modes of operation of the device (see function table). In the addressable latch mode, data is written into the addressed latch and all unaddressed latches remain unchanged. In memory mode, the latches are unaffected by the data or the address inputs. The enable should be held high while the address lines are changing to ensure that data in the latches does not change. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the corresponding D input with all other outputs being low. In clear mode, all outputs are low.

NOTE *The 100001222 is a low power Schottky device.*

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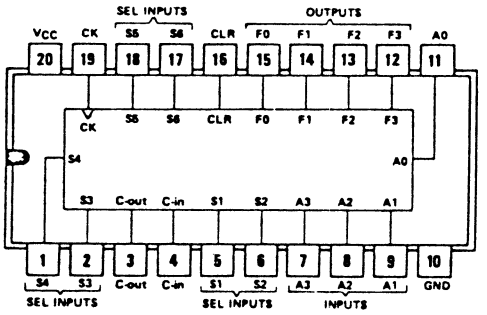
100001223

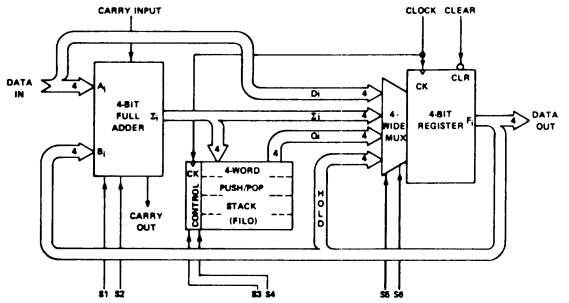
4-Bit-Slice Expandable Control Element

PIN CONFIGURATION



positive logic: See function table.

BLOCK DIAGRAM



REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i ≡ 3, 2, 1, 0
Ai ≡ Data inputs
QiA ≡ Push-pop stack word A output (internal)
QiA0 ≡ the level of Qi before the indicated inputs conditions were established.
Fi ≡ Device outputs
Fi0 ≡ the level of Fi before the indicated input conditions were established.
Σi ≡ Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

μlink operations show previous data location after clock transition.

ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

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100001223 (CONT.)

The 100001223 is a 4-bit slice control device consisting of an output register, push-pop stack, and a full adder. It has the capability to generate or select the source of the next function of microprogram address.

The 4-bit, edge-triggered register maintains a constant output during each clock cycle. The two source select lines (S5, S6) select one of the following inputs to this register: the current output of the register, an operand or address stored in the push-pop stack, the outputs of a four-function full adder, or a direct data-in address port. At any time the register's output can be set to zero using the clear input.

The 4-word push-pop stack can nest up to four levels of program or return addresses. In load mode, the output of the full adder is loaded into the first (top) word of the stack and no push operation occurs. In push mode, the data also is loaded into the first word, but the previous first three words are pushed one word down on the stack. In pop mode, the words in the stack move up one location on each clock transition. In this mode, the contents of the fourth (bottom) word are not lost. After three transitions of the clock, all the words in the stack are filled with the contents of the fourth register.

The adder is controlled by the select inputs (S1,S2) to perform one of the following functions:

- Incrementing A or B, decrementing B
- Unconditional jumps or relative offsets
- Retun to zero or one
- No change
- Since the function select lines of the register inputs, push-pop stack, and adder are independent, multiple functions can be selected to occur on the same clock transition.

NOTE *The 100001223 is a Schottky device.*

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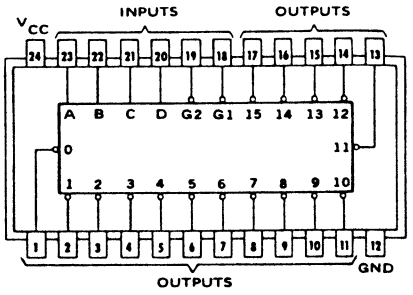
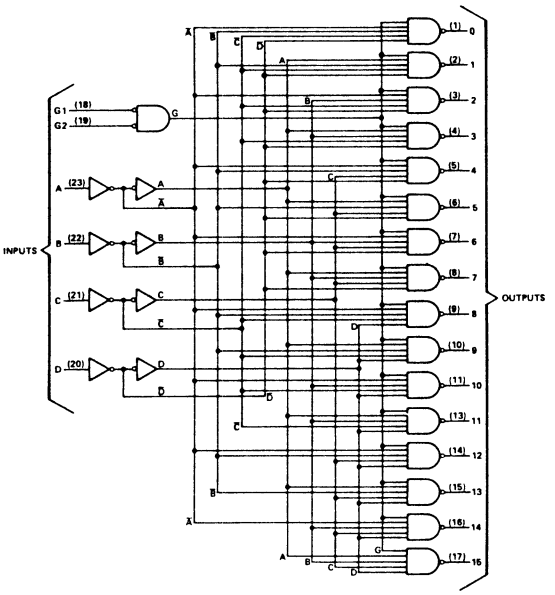
100001224

4-Line-to-16-Line Decoder/Demultiplexer With Open-Collector Outputs

PIN CONFIGURATION



BLOCK DIAGRAM



The 100001224 decodes four inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs (G1,G2) are low. It performs a demultiplexing operation by passing data from one of the strobe inputs to the outputs addressed by the input lines with the other strobe input is low. All outputs are high when either strobe is high.

FUNCTION TABLE

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

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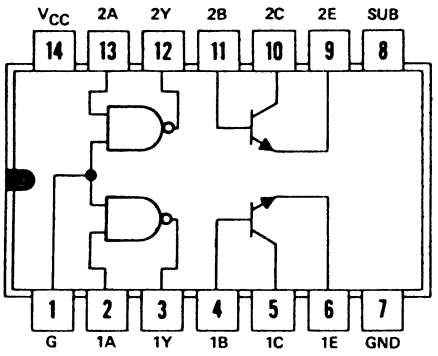
100001225

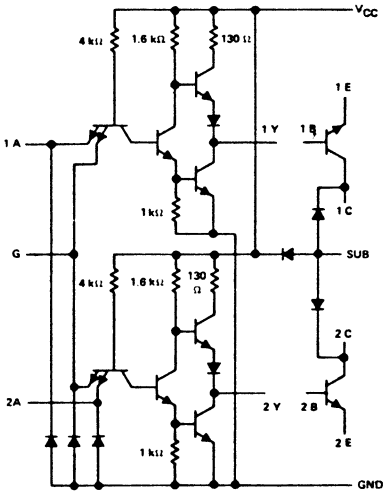
Dual Peripheral Positive-AND Driver

PIN CONFIGURATION



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

LOGIC DIAGRAM



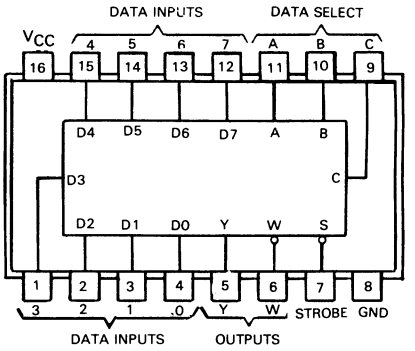
Resistor values shown are nominal

The 100001225 consists of two AND drivers and two uncommitted, high-current, high-voltage, n-p-n transistors.

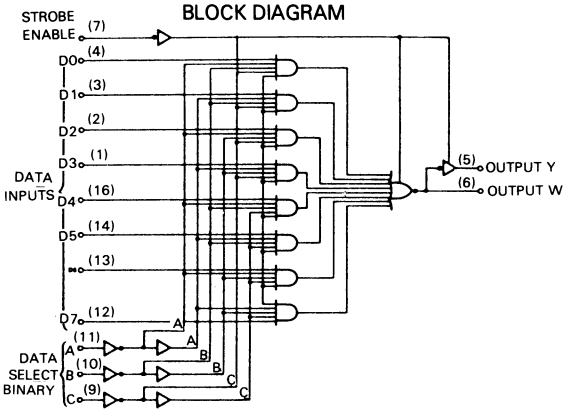
100001226

Data Selector/Multiplexer with Tri-State Outputs

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

The 100001226 selects one-of-eight inputs and features strobe-controlled tri-state outputs. The device is enabled when the strobe is low. When the strobe input is high, both outputs are in a high-impedance state and can neither drive nor load the bus significantly. When the strobe is low, the outputs operate as standard TTL totem-pole outputs.

NOTE *The 100001226 is a low power Schottky device.*

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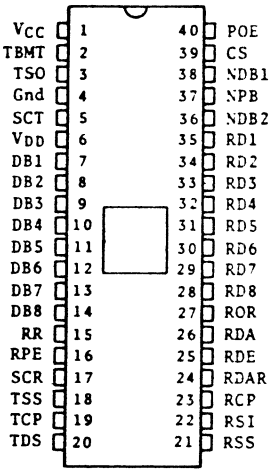
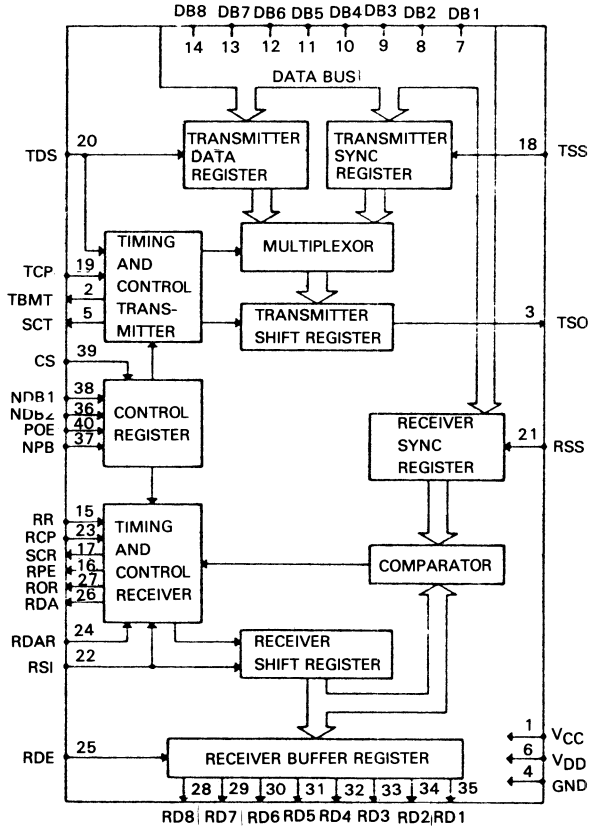
100001227

Universal Synchronous Receiver/Transmitter

PIN CONFIGURATION



BLOCK DIAGRAM



The USR/T performs all the receiving and transmitting functions associated with synchronous data communications. It can operate in full or half duplex mode, receiving and transmitting simultaneously at different baud rates. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmed by the external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals.

The 100001227 has tri-state outputs.

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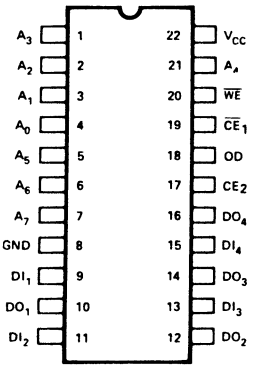
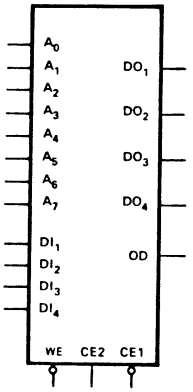
100001228

256 x 4-Bit Static RAM

PIN CONFIGURATION



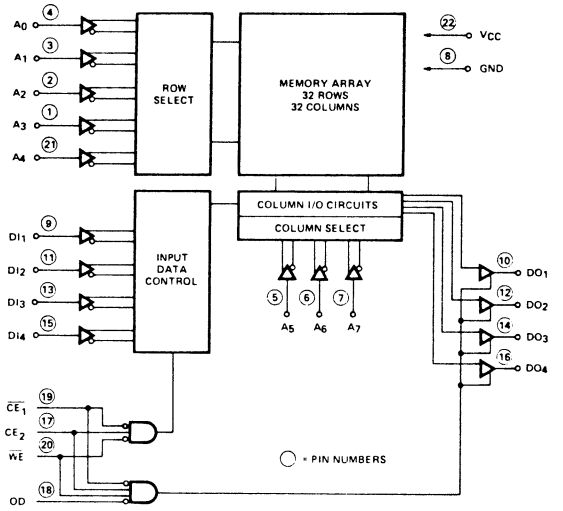
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	$\overline{CE}_2$	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



The 100001228 is a 1024-bit random access memory organized as 256 words by 4 bits. It uses DC (static) circuitry. Data is read out nondestructively and non-inverted.

It has two chip enables and tri-state outputs.

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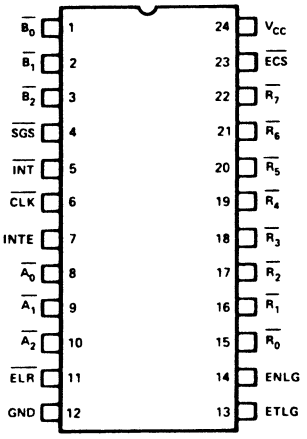
100001229

Priority Interrupt Control Unit

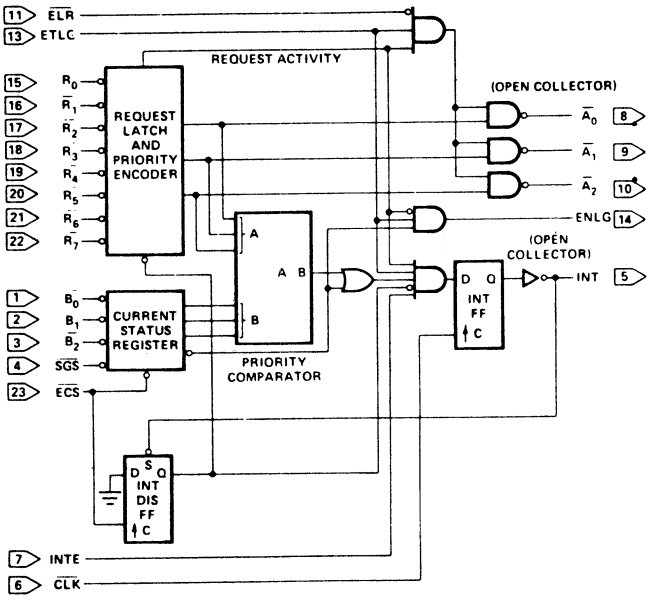
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



The 100001229 accepts eight requesting levels, determines the highest priority, compares this priority to a software controller current status register, and issues an interrupt to the system along with vector information to identify the service routine. It has open-collector outputs so that it can be easily expanded.

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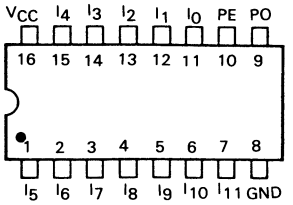
100001230

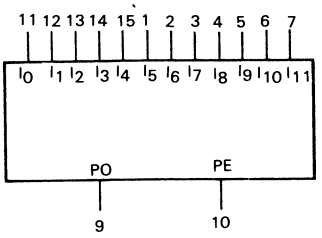
Twelve-Input Parity Checker/Generator

PIN CONFIGURATION



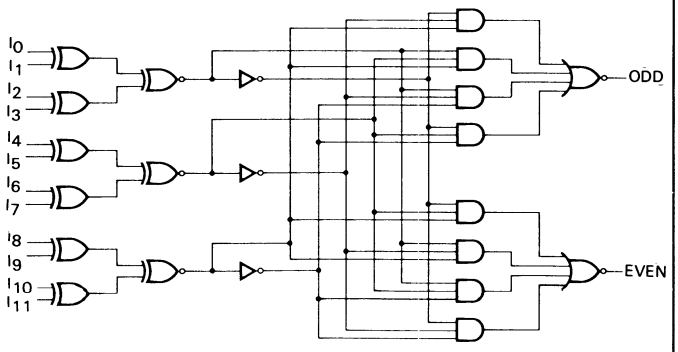
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



DEFINITION OF FUNCTIONAL TERMS

I_0 through I_{11} The twelve inputs to the parity tree.

ODD The ODD parity output of the device. When an ODD number of I inputs are at a HIGH level, the ODD output will be HIGH.

EVEN The EVEN parity output of the device. When an EVEN number of I inputs are at a HIGH level, the EVEN output will be HIGH.

LOGIC EQUATIONS

Odd Output = $I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$

Even Output = $\overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$

TRUTH TABLE

NUMBER OF I INPUTS		OUTPUT	
LOW	HIGH	ODD	EVEN
0	12	L	H
1	11	H	L
2	10	L	H
3	9	H	L
4	8	L	H
5	7	H	L
6	6	L	H
7	5	H	L
8	4	L	H
9	3	H	L
10	2	L	H
11	1	H	L
12	0	L	H

H = HIGH
L = LOW
X = Don't Care

The 100001230 is a high-speed 12-input device for generating and checking odd or even parity.

NOTE *The 100001230 is a Schottky device.*

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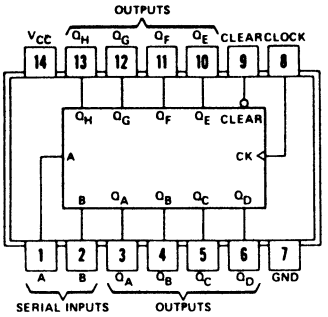
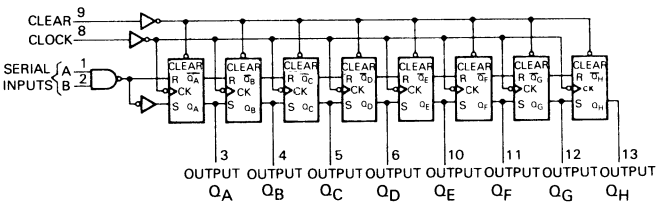
100001231

8-Bit Parallel-Out Serial Shift Register

PIN CONFIGURATION



BLOCK DIAGRAM



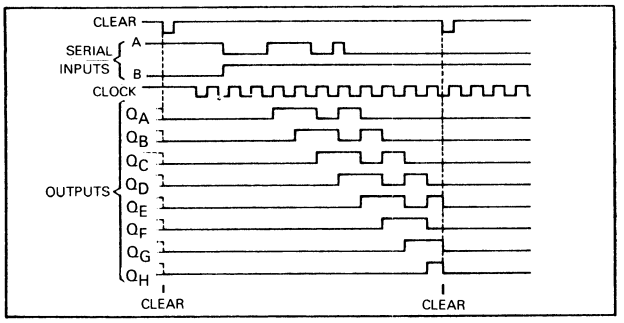
TRUTH TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

positive logic: High input to clear resets all four outputs low

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



The 100001231 is a 8-bit shift register which features gated serial inputs, asynchronous clear, and totem-pole outputs. A low on either (both) of the serial gated inputs (A,B) inhibits the entry of new data and resets the first flip-flop to low on the next clock pulse. A high input enables the other input which will determine the state of the first flip-flop. Clocking occurs on the low-to-high transition of the clock.

NOTE *The 100001231 is a low power Schottky device.*

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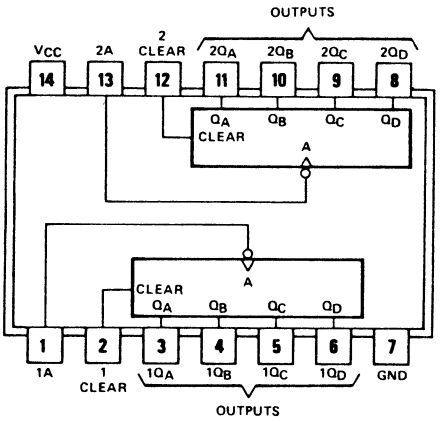
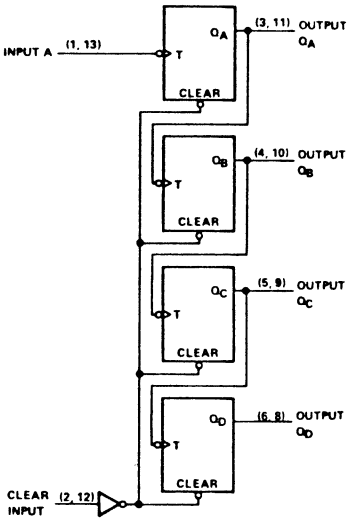
100001232

Dual 4-Bit Binary Counter

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

The 100001232 consists of eight master-slave flip-flops and additional gating to implement two independent 4-bit counter. Each counter has a direct clear and a clock input.

NOTE *The 100001231 is a low power Schottky device.*

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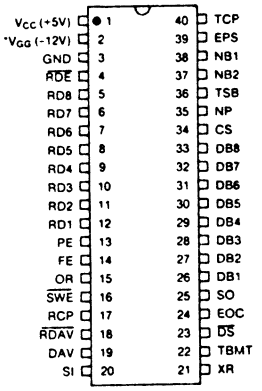
100001234

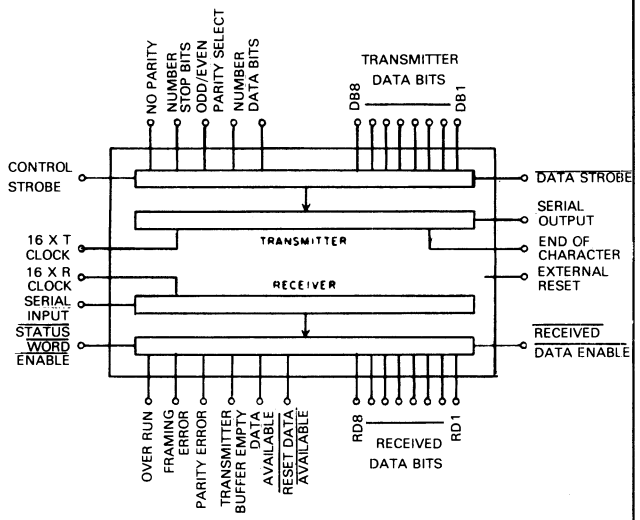
Universal Asynchronous Receiver/Transmitter

PIN CONFIGURATION
(TOP VIEW)

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



This is a universal asynchronous receiver-transmitter (UART) with complete serial-to-parallel and parallel-to-serial interface. The maximum serial data rate in KHz is 30, and the supply voltage is 5. This device is TTL compatible.

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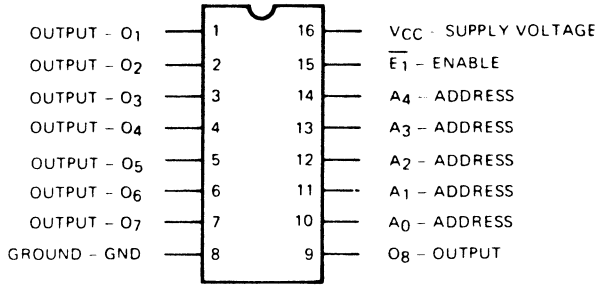
100001239 through 100001245

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

These 256-bit programmable read only memories are organized as 32 words by 8 bits. They include on-chip address decoding, a chip enable input ($\overline{E1}$), and three-state ouputs.

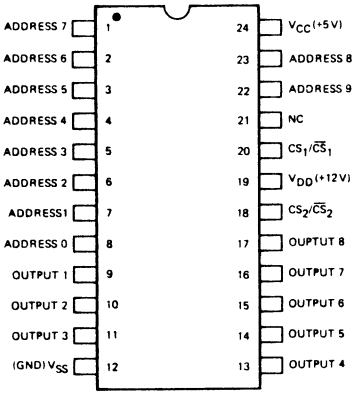
Each memory is addressed with inputs A0 through A4 which select one of 32 words. To enable the ouputs for a readout, enable $\overline{E1}$ must be low. If the enable is high, the outputs are held off permitting wire-ORing of the three-state outputs of several packages.

NOTE *100001239 through 100001245 are Schottky devices.*

100001246

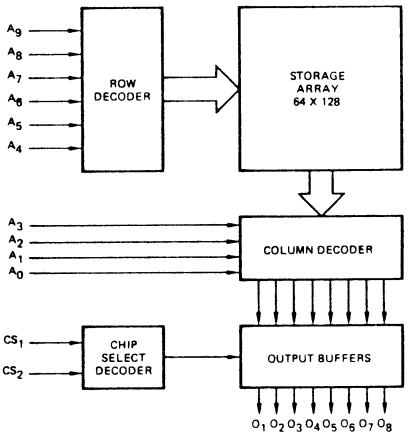
1024 x 8-Bit ROM

PIN CONFIGURATION



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM



The 100001246 is a 8192-bit read only memory organized as 1024 words by 8 bits. Two chip select inputs are logically ANDed together to provide control of the tri-state output buffers. This memory is static and requires no clock signal.

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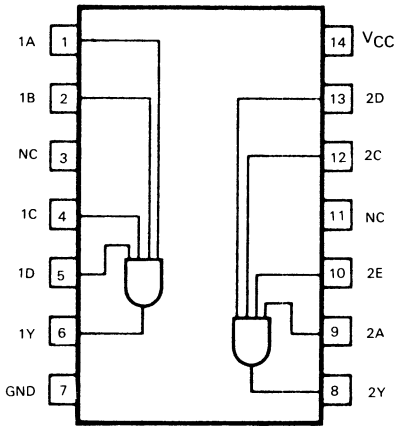
100001247

Dual 4-Input AND Gate

PIN CONFIGURATION



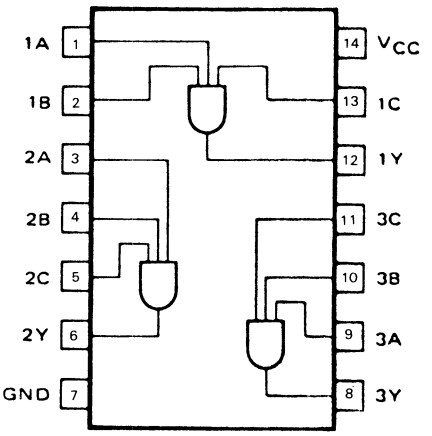
Y = ABCD

NOTE *The 100001247 is a low power Schottky device.*

100001248

Triple 3-Input AND Gate

PIN CONFIGURATION



Y = ABC

NOTE *The 100001248 is a low power Schottky device.*

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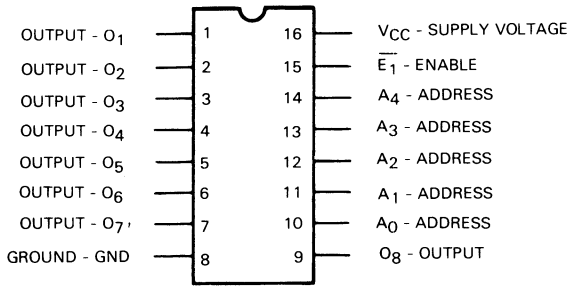
100001249

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable input ($\overline{E1}$), and three-state outputs.

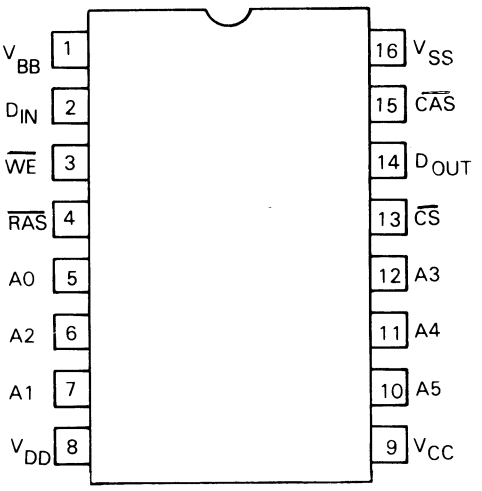
The memory is addressed with inputs A0 through A4 which select one of 32 words. To enable the ouputs for a readout, enable $\overline{E1}$ must be low. If the enable is high, the outputs are held off permitting wire ORing of the three-state outputs of several packages.

NOTE *The 100001249 is a Schottky device.*

100001250

4096 x 1 Bit NMOS RAM

PIN CONFIGURATION



Y = $\overline{AB}$

A0 - A5	Address Inputs
$\overline{CAS}$	Column Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
VBB	Power (-5V)
VCC	Power (+5V)
VDD	Power (+12V)
VSS	Power Ground

This device contains 4096 (4096 x 1) addressable storage cells and the necessary circuitry to address, write, read, and refresh each cell without pattern dependence.

The 12 address bits required to decode 1 of the 4096 cell locations are multiplexed onto the 6 address bits (A0-A5) and latched into the on-chip address latches by externally applying two negative going TTL-Level clocks ($\overline{RAS}$ and $\overline{CAS}$). The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits into the chip. Chip Select ($\overline{CS}$) is latched into the part along with the column address.

All inputs are TTL compatible, and the outputs are tri-state, TTL compatible.

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100001250 (cont.)

Data is written while RAS is active. The latter falling edge of CAS or write strobes data into the on-chip data latch.

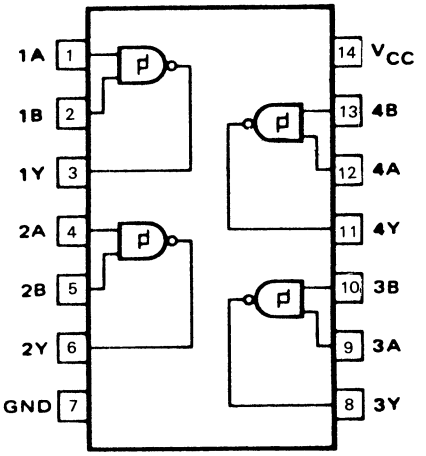
Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low).

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within 2 ms time interval.

100001251

Quad 2-Input NAND Schmitt Trigger

PIN CONFIGURATION



NOTE *The 100001251 is a low power Schottky device.*

$$Y = \overline{AB}$$

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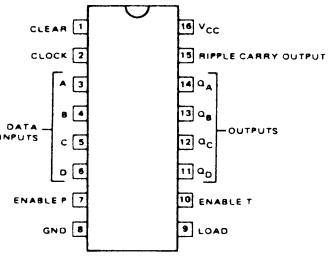
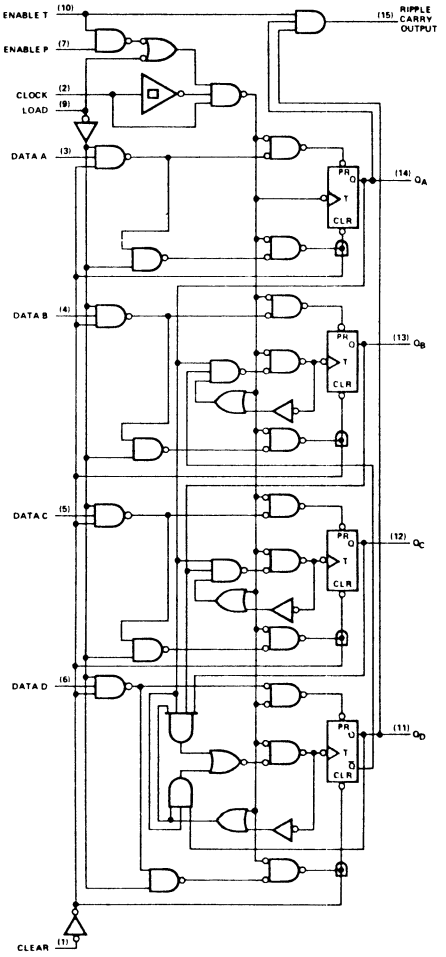
100001252

Synchronous 4-Bit Decade Counter With Direct Clear

PIN CONFIGURATION



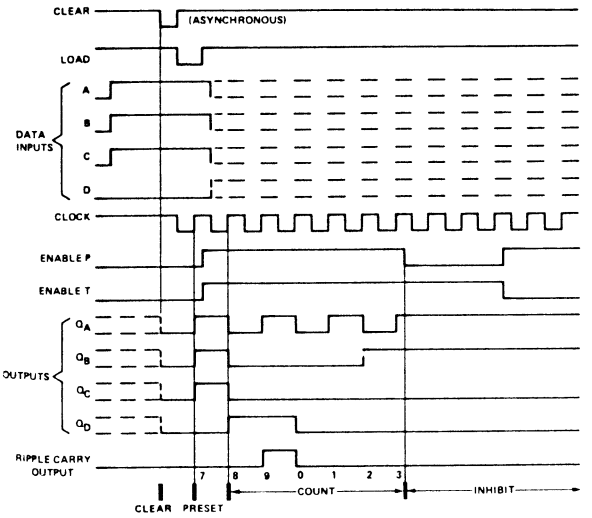
BLOCK DIAGRAM



TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



The 100001252 is a presettable decade counter which features an internal carry look-ahead. A buffered clock inputs triggers all four flip-flops on the low-to-high transition.

Since presetting the outputs is synchronous, a low on the load input disables the counter and causes the outputs to agree with the setup data after the next clock. A low on the clear input sets the outputs to low regardless of the levels of the clock, load or enable inputs.

The carry look-ahead circuitry allows these counters to be cascaded using the two count enable inputs and the ripple carry output. Both count enable inputs (P,T) must be high to count. The T input is fed forward to enable the ripple carry output to produce a high pulse which lasts almost as long as the QA output is high. This pulse can be used to enable successive cascaded stages.

Changes on the enable P, enable T, load, or clear inputs have no effect until clocking occurs.

NOTE *The 100001252 is a low power Schottky device.*

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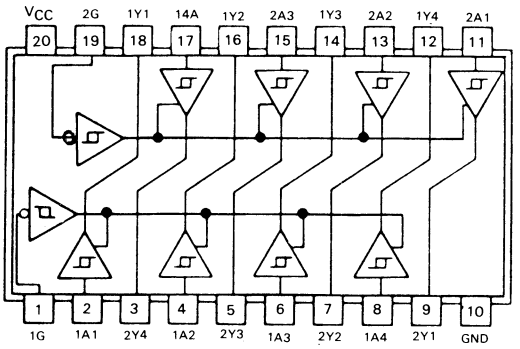
100001253

Octal Buffer And Line Driver

PIN CONFIGURATION



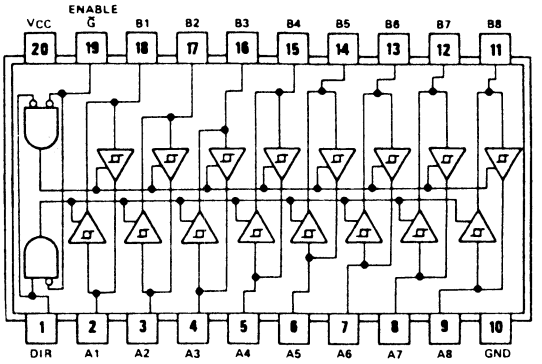
This device has tri-state outputs to drive bus lines or buffer memory address registers. It features selectable combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

NOTE *The 100001253 is a low power Schottky device.*

100001254

Octal Bus Transceiver

PIN CONFIGURATION



This device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input $\overline{(G)}$ can be used to disable the device so that the busses are effectively isolated. It has tri-state output.

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

NOTE *The 100001254 is a low power Schottky device.*

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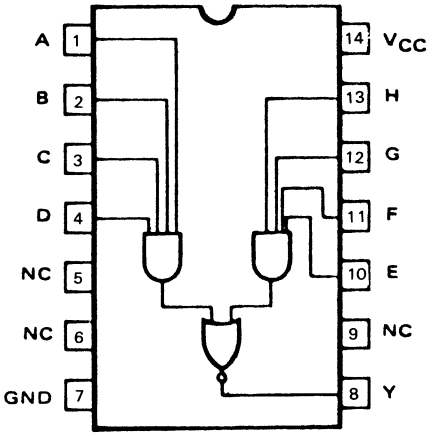
100001255

2-Wide 4-Input AND-OR-INVERT Gate

PIN CONFIGURATION



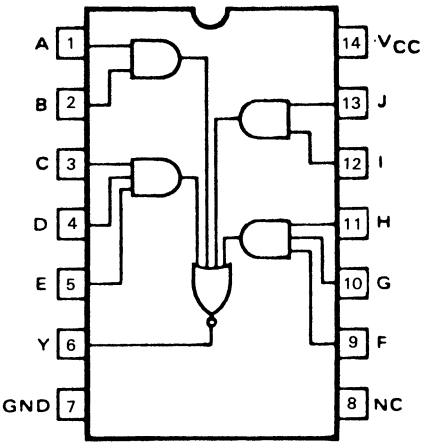
positive logic:
$y = (\overline{ABCD}) + (\overline{EFGH})$

NOTE *The 100001255 is a low power Schottky device.*

100001256

4-Wide 2-Input AND-OR-INVERT Gate

PIN CONFIGURATION



positive logic:
$y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$
NC - No internal connection

NOTE *The 100001256 is a low power Schottky device.*

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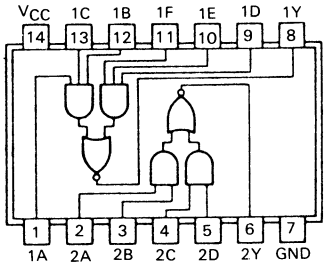
100001257

Dual 2-Wide 2-Input AND-OR-INVERT Gate

PIN CONFIGURATION



positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

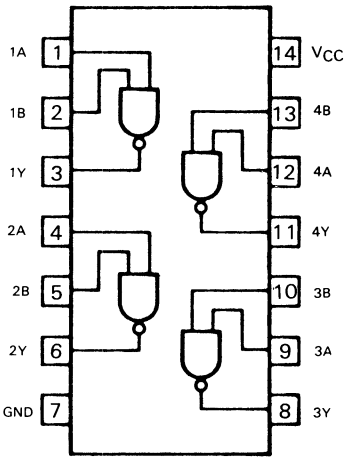
$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

NOTE *The 100001257 is a low power Schottky device.*

100001258

Quad 2-Input NAND Buffer w/Open Collector Outputs

PIN CONFIGURATION



$Y = \overline{AB}$

NOTE *The 100001258 is a low power Schottky device.*

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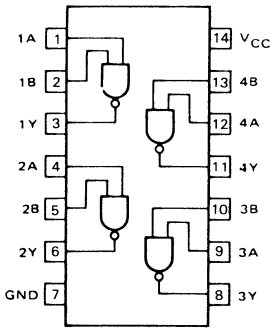
100001259

Quad 2-Input NAND Buffer

PIN CONFIGURATION



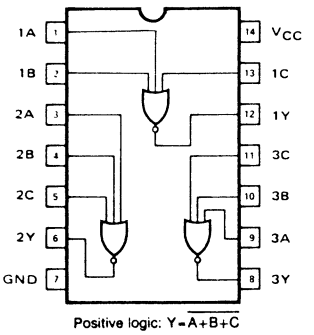
Positive logic: $y = \overline{AB}$

NOTE *The 100001259 is a low power Schottky device.*

100001260

Triple 3-Input NOR Gate

PIN CONFIGURATION



Positive logic: $Y = \overline{A+B+C}$

NOTE *The 100001260 is a low power Schottky device.*

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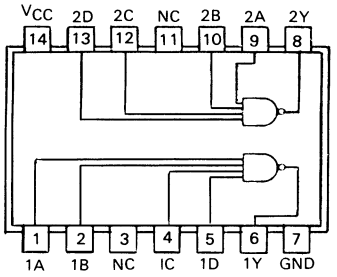
100001261

Dual 4-Input NAND Gate

PIN CONFIGURATION



positive logic:
$Y = \overline{ABCD}$

NOTE *The 100001261 is a low power Schottky device.*

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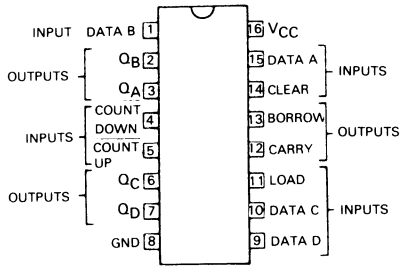
100001262

Synchronous Decade Up/Down Dual Clock Counter, BCD with Clear

PIN CONFIGURATION

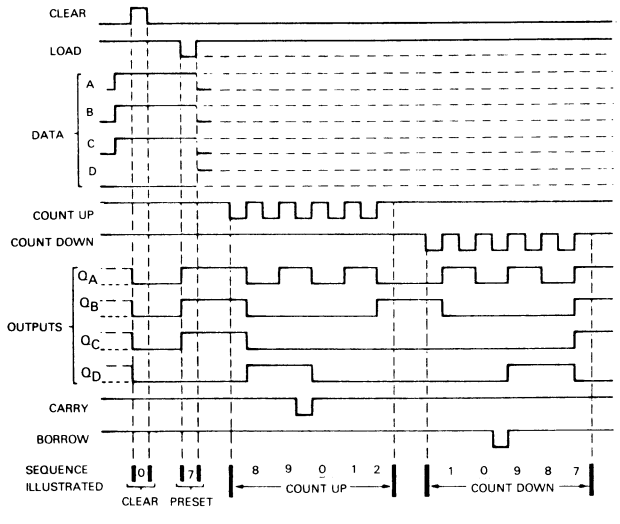


logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:

A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high

The 100001262 is a synchronous up/down counter containing four master-slave flip-flops. The outputs of the flip-flops are triggered by a low-to-high transition of either count input. Counting occurs when one count input is pulsed and the other is held high. The direction of the counting is determined by the count input which is pulsed. Each output can be preset to the a certain value by entering that value on the corresponding input when the load input is low. When the clear input is high, all the outputs are forced low.

Carry and borrow outputs are available for cascading the counting operations. When the counter underflows, the borrow output produces a pulse equal in width to the count-down input. Likewise, when the counter overflows, the carry output produces a pulse equal in width to the count-up input.

NOTE *The 100001262 is a low power Schottky device.*

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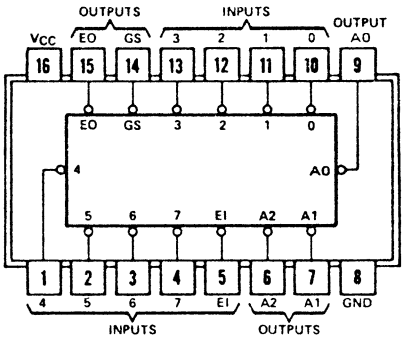
100001263

8-Line-to-3-Line Octal Priority Encoder

PIN CONFIGURATION

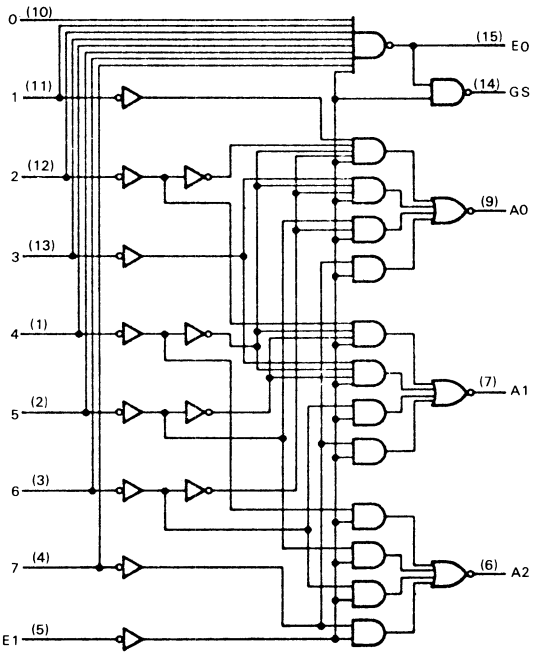


FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

BLOCK DIAGRAM



This encoder features priority decoding of the inputs to ensure that only the highest-order data line is encoded. It encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) allows octal expansion without the need for external circuitry. Data inputs and outputs are active at the low logic level.

NOTE *The 100001263 is a low power Schottky device.*

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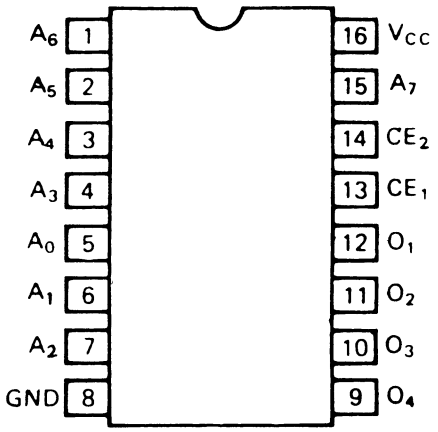
100001264

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



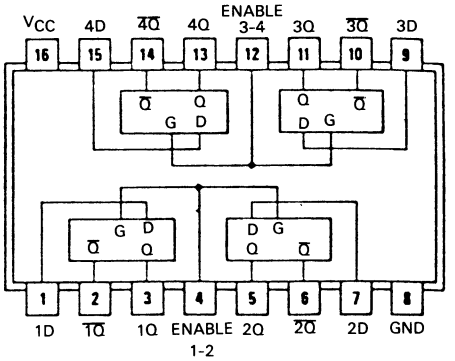
This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001264 is a Schottky device.*

100001265

4-Bit Bistable Latch

PIN CONFIGURATION



1-2

FUNCTION TABLE

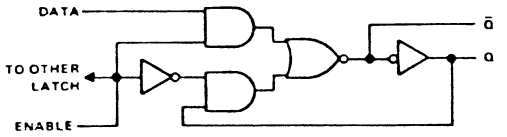
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

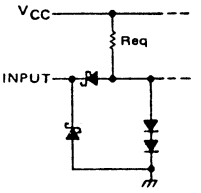
H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G.

BLOCK DIAGRAM

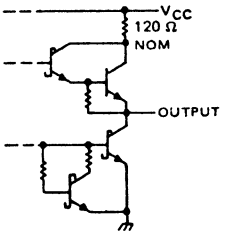
(each latch)



EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



Data: Req = 17 kΩ
Enable: Req = 4.2 kΩ

Information present at a data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

NOTE *The 100001265 is a low power Schottky device.*

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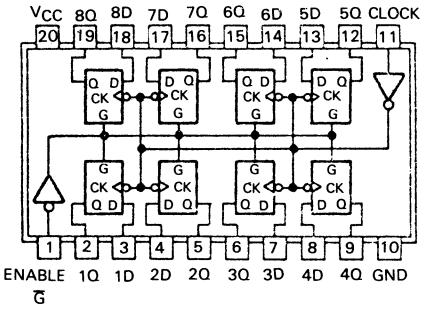
100001266

Octal D-Type Flip-Flops With Enable

PIN CONFIGURATION

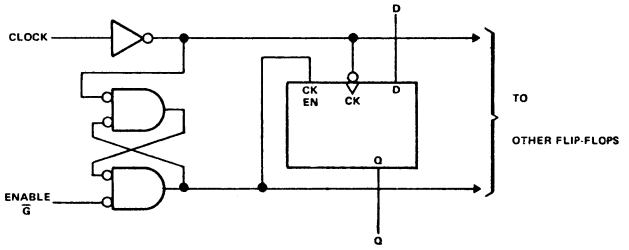


FUNCTION TABLE

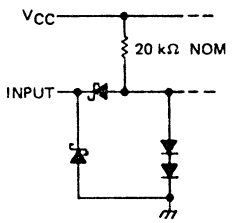
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
$\overline{G}$	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

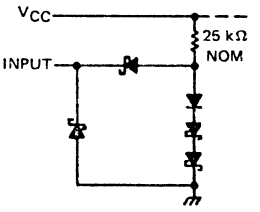
BLOCK DIAGRAM



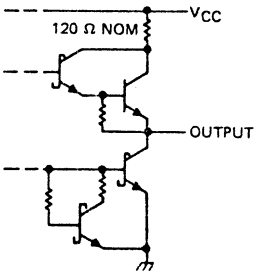
EQUIVALENT OF CLOCK OR ENABLE INPUT



EQUIVALENT OF DATA INPUT



TYPICAL OF ALL OUTPUTS



The 100001266 consists of eight edge-triggered D-type flip-flops with a common enable input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive going edge of the clock pulse if the enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

NOTE *The 100001266 is a low power Schottky device.*

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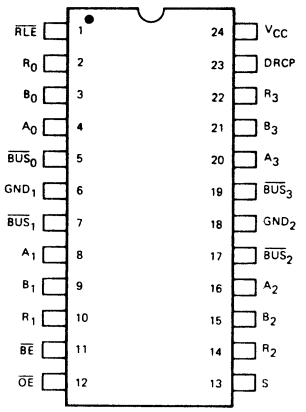
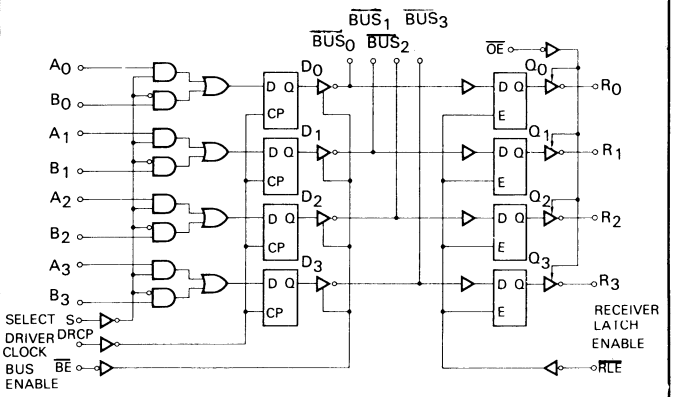
100001267

Quad Tri-State Bus Transceiver With Interface Logic

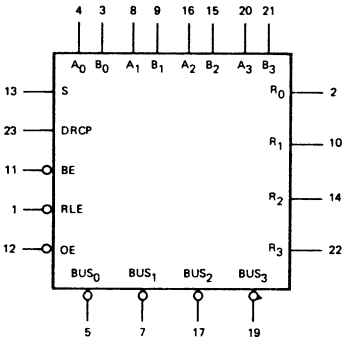
LOGIC DIAGRAM



Note: Pin 1 is marked for orientation.



LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

The 100001267 consists of four D-type edge-triggered flip-flops each with a 2-input multiplexer. The flip-flop outputs are connected to four tri-state bus drivers. Each bus driver is connected to the input of a receiver. The receiver outputs are connected to four D-type latches with tri-state outputs.

The bus driver is disabled when the bus enable ($\overline{BE}$) is high since the outputs are forced to a high-impedance state.

The input register consists of the four D-type flip-flops with the 2-input multiplexers. These multiplexers are controlled by the common select input (S). When S is low, the Ai data is stored in the register and when S is high, the Bi data is stored. The data is entered into the driver register on the low-to-high transition of the common clock (DRCP).

Data from the A or B inputs is inverted at the bus output, and data at the bus input is inverted at the receiver output, which results in noninverted data from the driver input to the receiver output. The receiver latches are controlled by the receiver latch enable input ($\overline{RLE}$). When this input is low, the receiver outputs follow the bus inputs. When it is high, the latch retains the present data regardless of the bus input. The tri-state latch outputs are controlled by the $\overline{OE}$ input. When $\overline{OE}$ is high, the receiver outputs are in the high-impedance state.

NOTE *The 100001267 is a low power Schottky device.*

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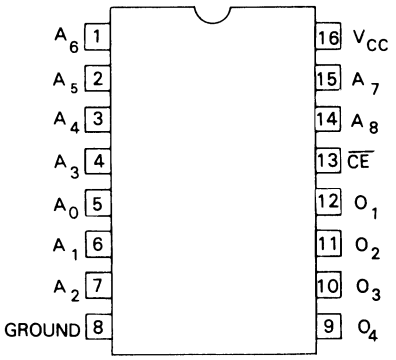
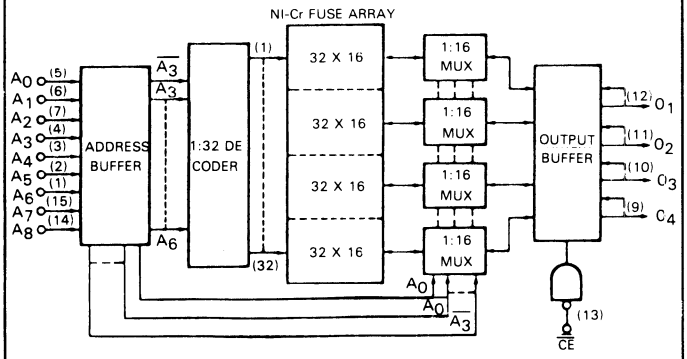
100001268 through 100001337

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector

NOTE *100001268 through 100001299 are Schottky devices.*

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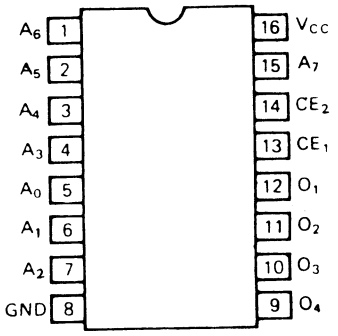
100001338 through 100001353

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They include on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *100001338 through 100001353 are Schottky devices.*

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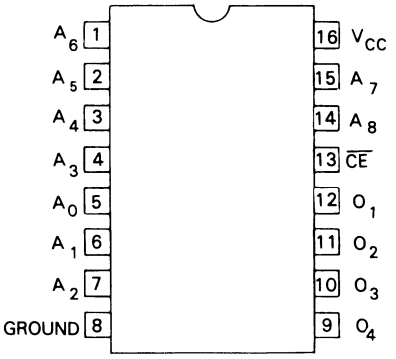
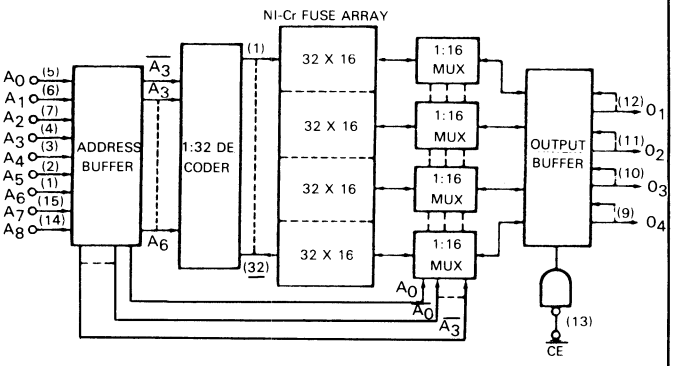
100001354

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *The 100001354 is a Schottky device.*

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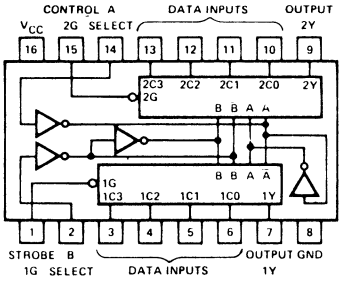
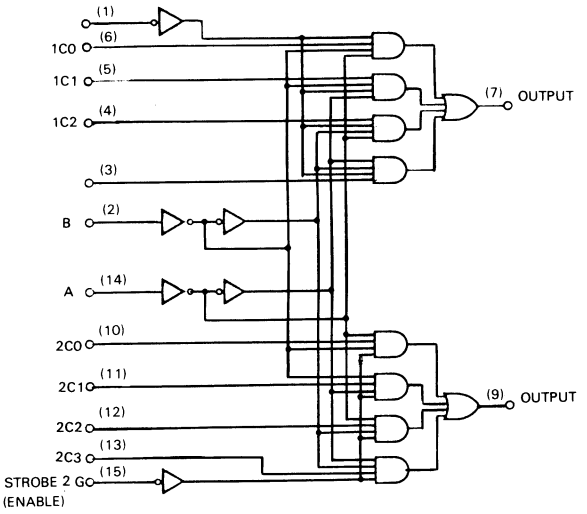
100001355

Dual 4-Line To 1-Line Data Selector/Multiplexer

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

The 100001355 data selector/multiplexor contains inverters and drivers which supply complementary, decoding data selection to its AND-OR gates. There are independent control inputs for each of the two 4-line sections.

The tri-states outputs allow the 100001355 to drive the data lines of bus-oriented systems. When all of the common outputs but one are disabled (in a high impedance state), the remaining output is enabled (in low impedance state) to drive the bus line high or low.

NOTE *The 100001355 is a Schottky device.*

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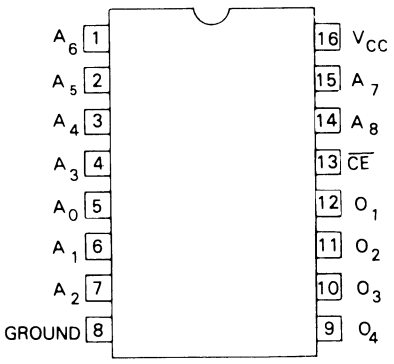
100001356

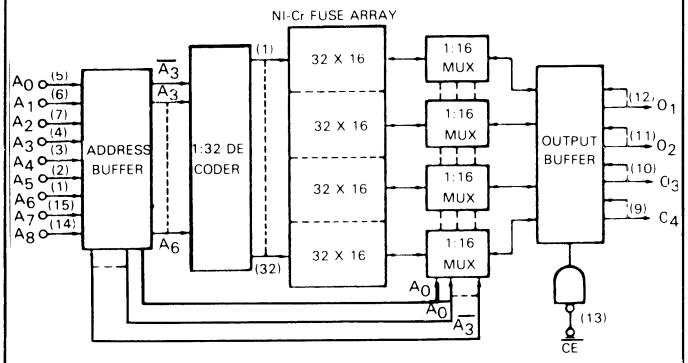
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the programming pin.

BLOCK DIAGRAM



This 2048-bit programmable read only memory is organized as 512 words by 4 bits. It includes on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

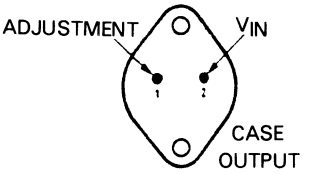
NOTE: *The 100001356 is a Schottky device*

100001357

Adjustable +1.2 - 37V, 1.5A Voltage Regulator.

PIN CONFIGURATION

(To-3 Steel)
Metal Can Package LOW PROFILE



(BOTTOM VIEW)

The voltage can be adjusted down to 1.2 volts from a 37 volt output range.

The device is guaranteed capable of 1.5 amp output current and has a line regulation of 0.01%/V. Load regulation is 0.1% 80dB ripple rejection.

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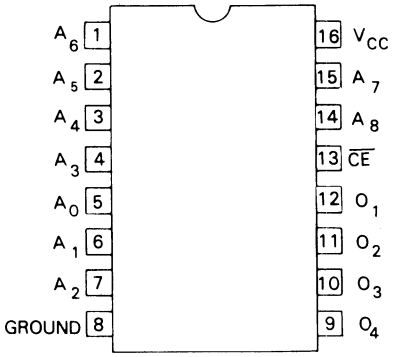
100001358

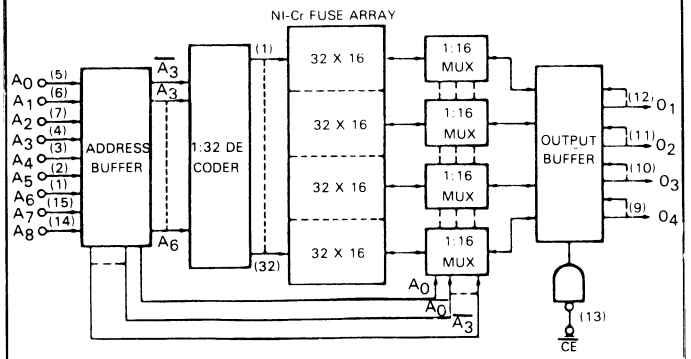
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



This 2048-bit programmable read only memory is organized as 512 words by 4 bits. It includes on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *The 100001358 is a Schottky device.*

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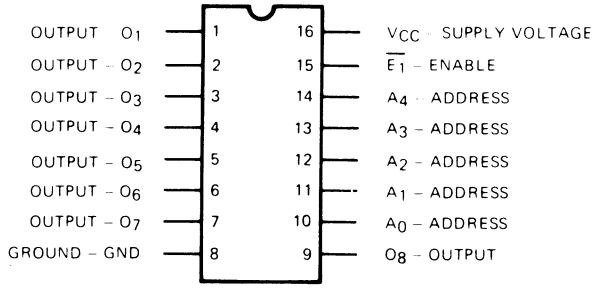
100001359

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

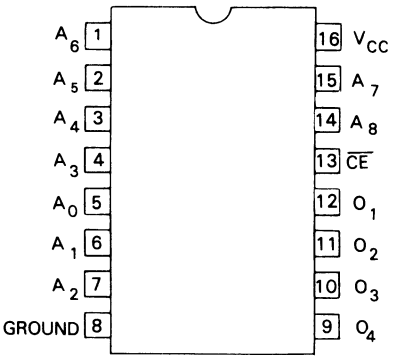
This 256-bit programmable read only memory is organized as 32 words by 8-bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and tri-state outputs.

NOTE *The 100001359 is a Schottky device.*

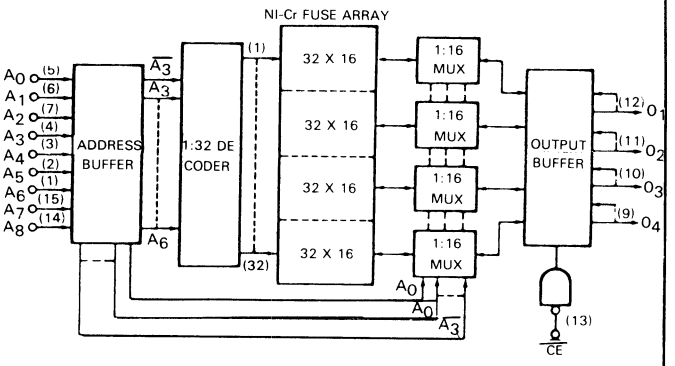
100001360

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *The 100001360 is a Schottky device.*

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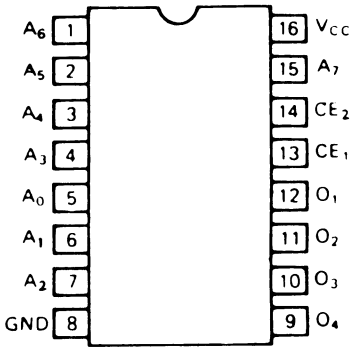
100001361

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



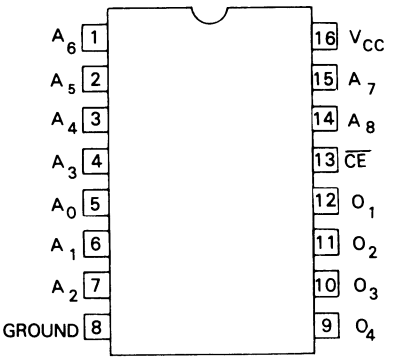
This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001361 is a Schottky device.*

100001362

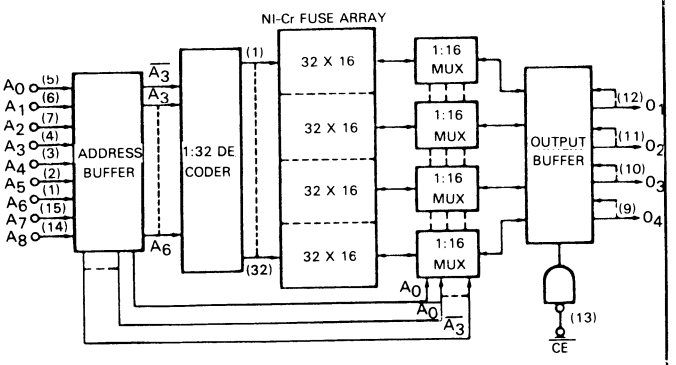
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the programming pin.

BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *The 100001362 is a Schottky device.*

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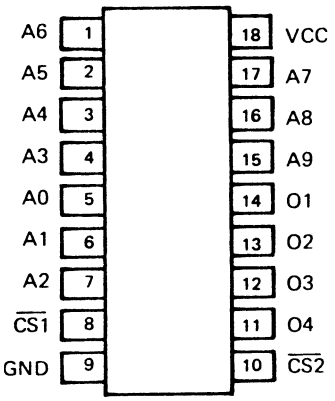
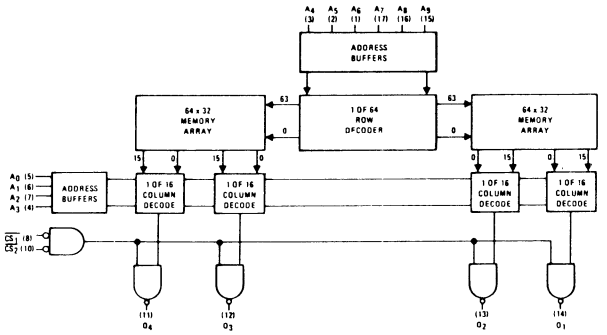
100001363

1024 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



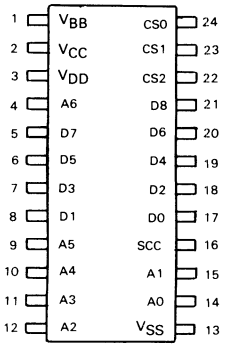
This 4096-bit programmable read only memory is organized as 1024 words by 4 bits.

NOTE *The 100001363 is a Schottky device.*

100001364 through 100001367

Column Select Character Generator

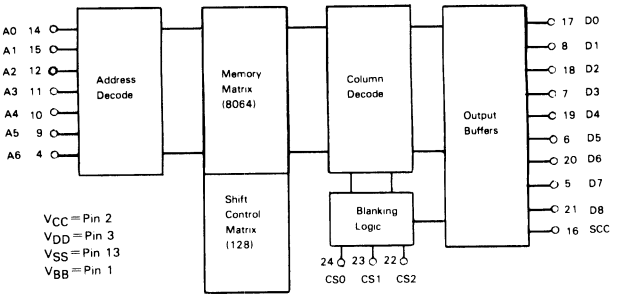
PIN CONFIGURATION



TRUTH TABLE

CS2	CS1	CS0	OUTPUT
0	0	0	0
0	0	1	C1
0	1	0	C2
0	1	1	C3
1	0	0	C4
1	0	1	C5
1	1	0	C6
1	1	1	C7

BLOCK DIAGRAM



These devices are mask-programmable 8192-bit vertical scan (column select) character generators. They contain 128 characters in a 7 x 9 matrix. A shift Control Command (SCC) bit can be programmed so that a high logic level will appear at the SCC output, in addition to the coding at D0-D8, to indicate that a character is to be shifted.

Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7 x 9 matrix. A 7-bit address code (A0-A6) is used to select one of the 128 characters programmed in the memory. To output a character addressed by A0-A6, a column select code (CS0-CS2) is sequentially applied (see truth table). Each column is read at outputs D0-D8).

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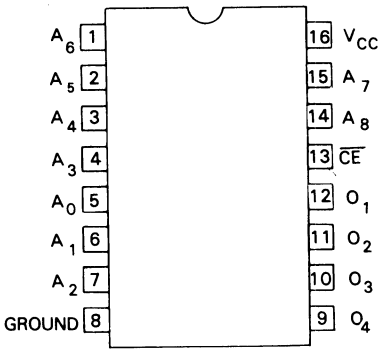
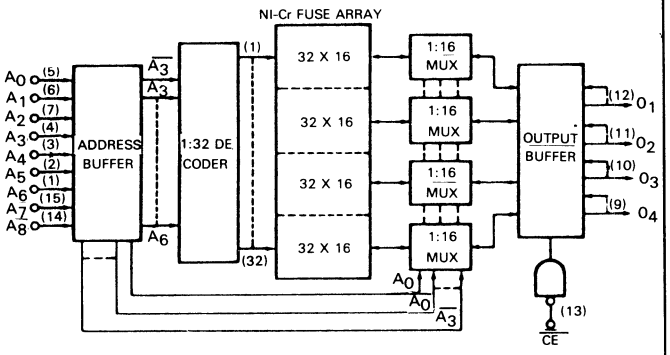
100001369 through 100001398

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



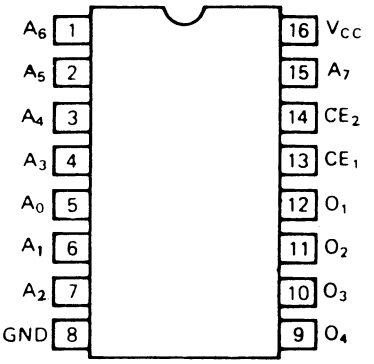
These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *100001369 through 100001398 are Schottky devices.*

100001399 through 100001402

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001399 is a Schottky device.*

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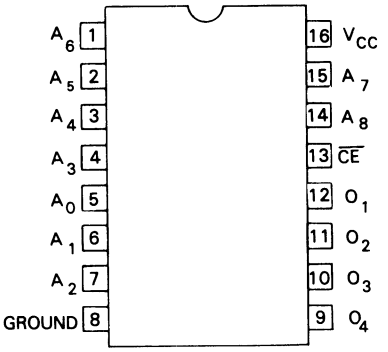
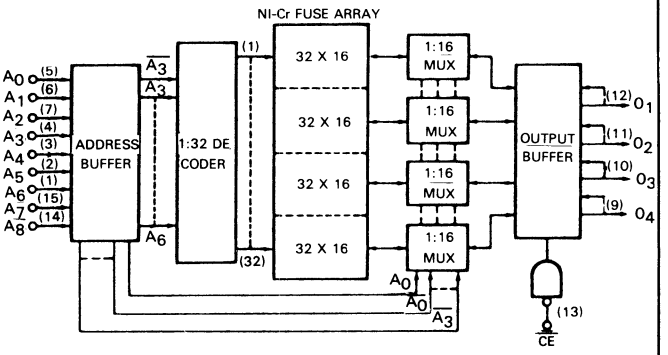
100001403

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *The 100001403 is a Schottky device.*

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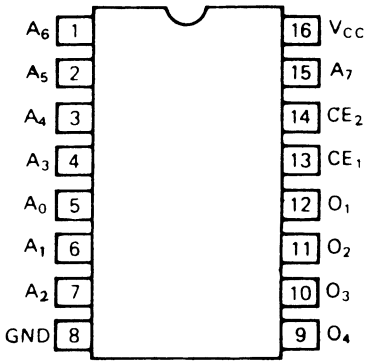
100001404 and 100001405

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



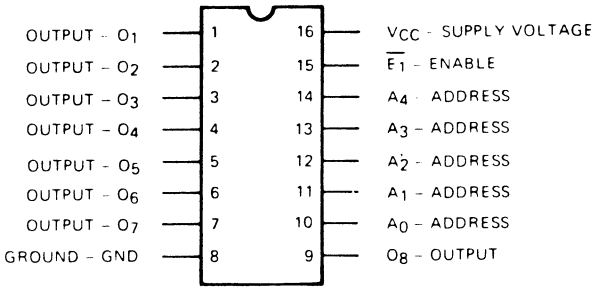
These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They include on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001404 and 100001045 are Schottky devices.*

100001406 through 100001409

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

These 256-bit programmable read only memories are organized as 32 words by 8 bits. They include on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

NOTE *100001406 through 100001409 are Schottky devices.*

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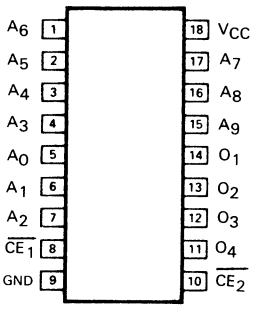
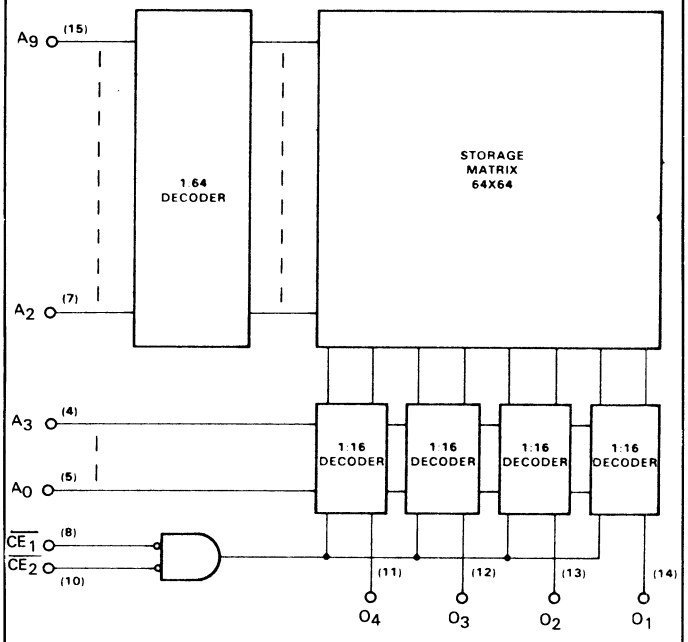
100001410

1024 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



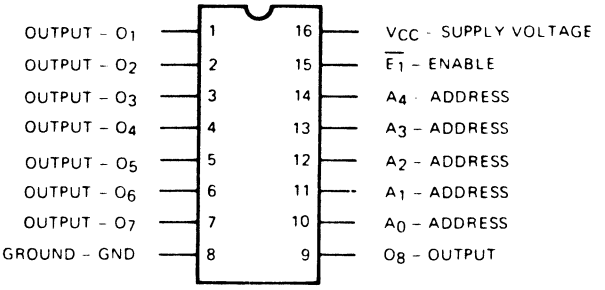
This 4096-bit bipolar programmable read only memory is organized as 1024 words by 4 bits. It includes on-chip decoding, 2 chip enable inputs, and open collector outputs. The maximum address access time is 60 ns.

NOTE *The 100001410 is a Schottky device.*

100001411

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable input ($\overline{E1}$), and three-state outputs.

NOTE *The 100001411 is a Schottky device.*

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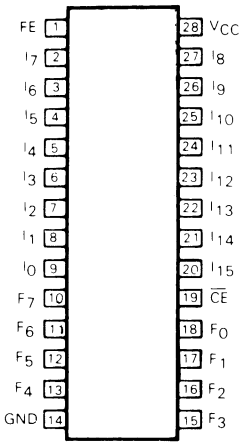
100001412

Bipolar Programmable Logic Array

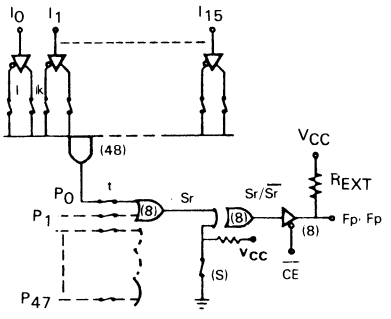
PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	F_p^*
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

FPLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

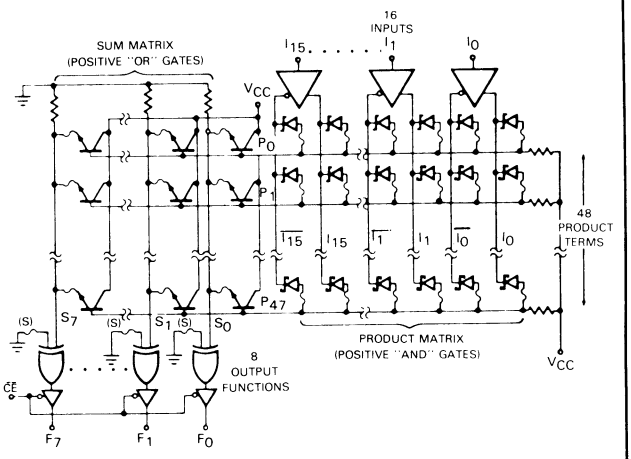
Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

LOGIC DIAGRAM



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

This device features a chip-enable control, an output inhibit, and tri-state outputs.

NOTE *The 100001412 is a Schottky device.*

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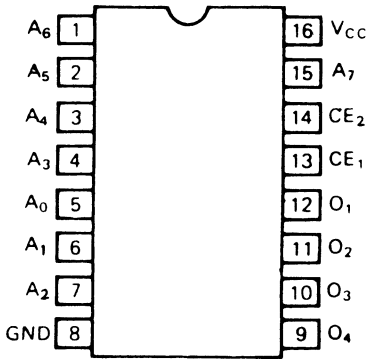
100001413 and 100001414

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



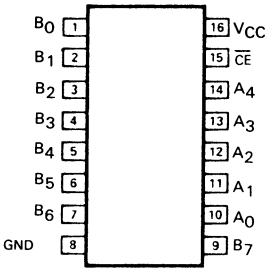
These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They include on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *100001413 and 100001414 are Schottky devices.*

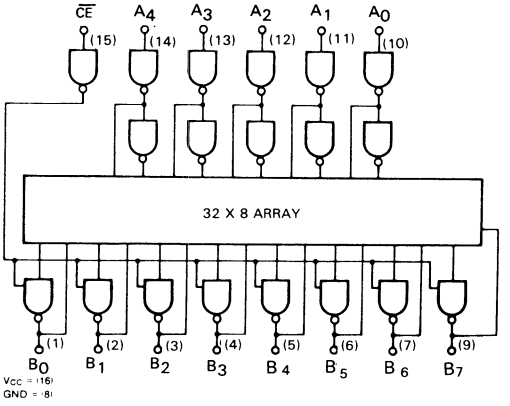
100001415

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



LOGIC DIAGRAM



This 256-bit bipolar programmable read only memory is organized as 32 words by 8 bits. It includes on-chip decoding, a chip enable, and open collector outputs.

NOTE *The 100001415 is a Schottky device.*

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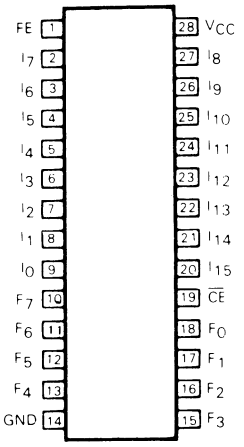
100001416

Bipolar Programmable Logic Array

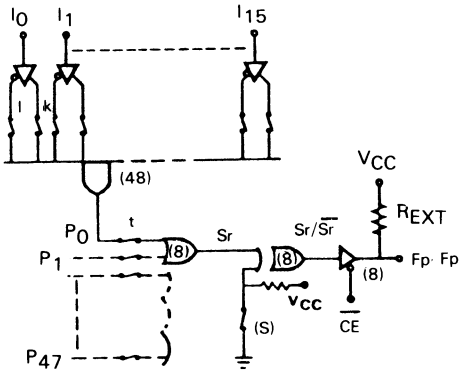
PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$F\dot{p}$
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

FPLA EQUIVALENT LOGIC PATH



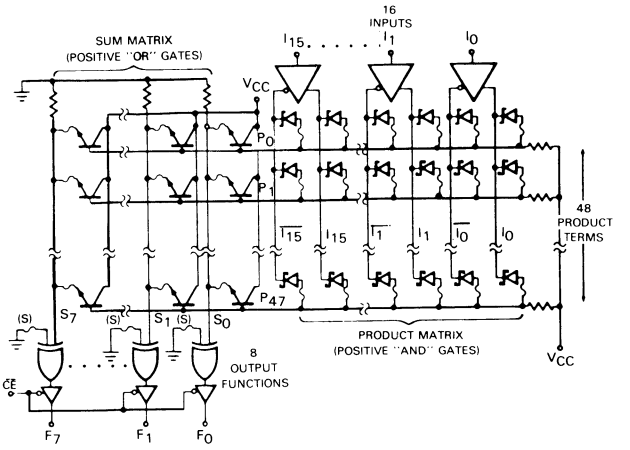
Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^{\bullet} = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S)

LOGIC DIAGRAM



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

This device features a chip-enable control, an output inhibit, and tri-state outputs.

NOTE *The 100001416 is a Schottky device.*

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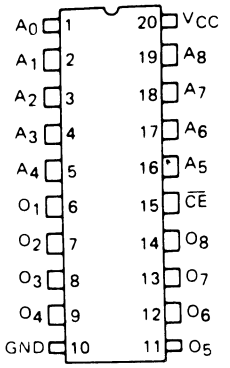
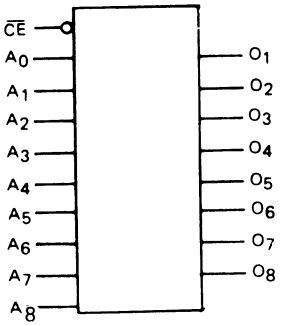
100001417 through 100001426

512 x 8-Bit Bipolar PROM

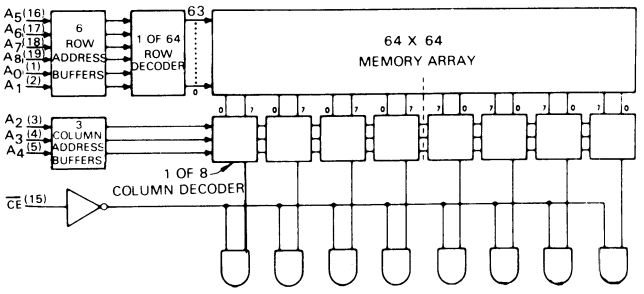
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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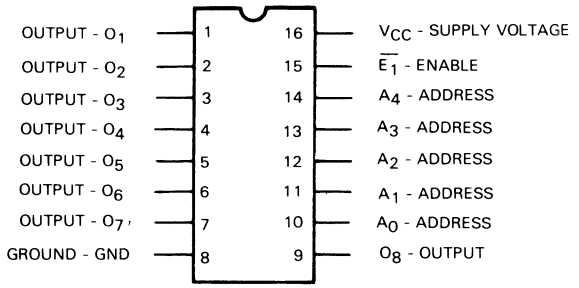
100001427 through 1000001430

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION

PIN CONFIGURATION



Low = Enable

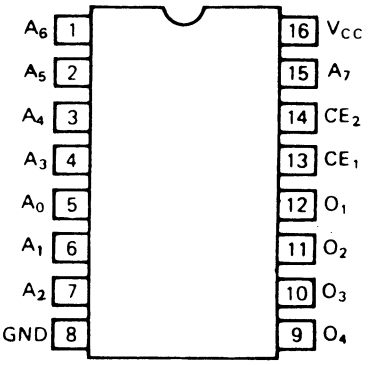
These 256-bit programmable read only memories are organized as 32 words by 8 bits. They include on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

NOTE *100001417 through 100001430 are Schottky devices.*

100001431 through 100001436

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They include on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *100001431 through 100001436 are Schottky devices.*

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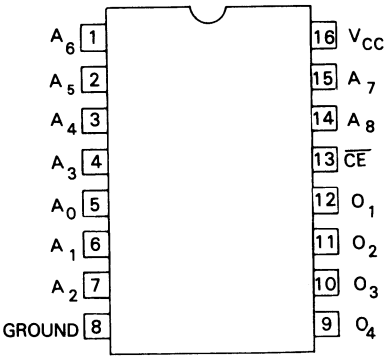
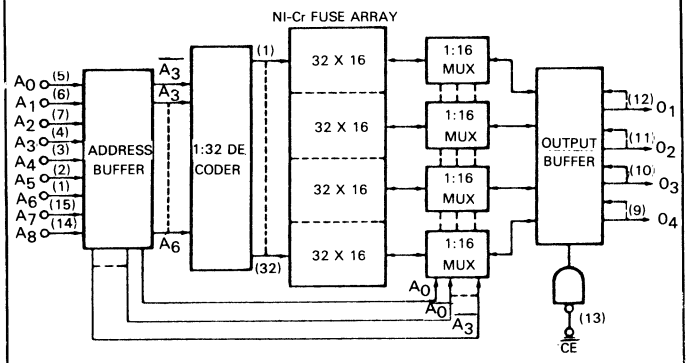
100001437 through 100001460

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



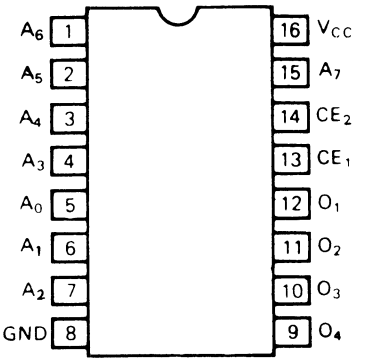
These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE *100001437 through 100001460 are Schottky devices.*

100001461 through 100001465

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



These 1024-bit programmable read only memories are organized as 256 words by 4 bits. They include on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *100001461 through 100001465 are Schottky devices.*

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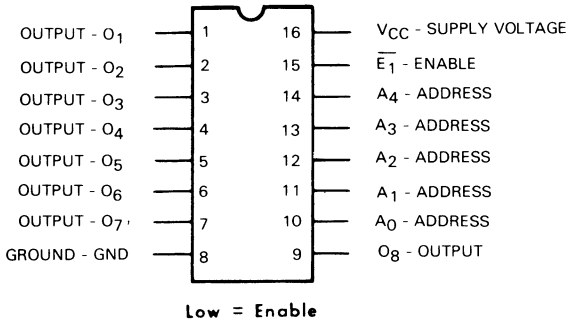
100001467 and 1000001468

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

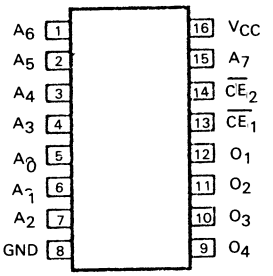
The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

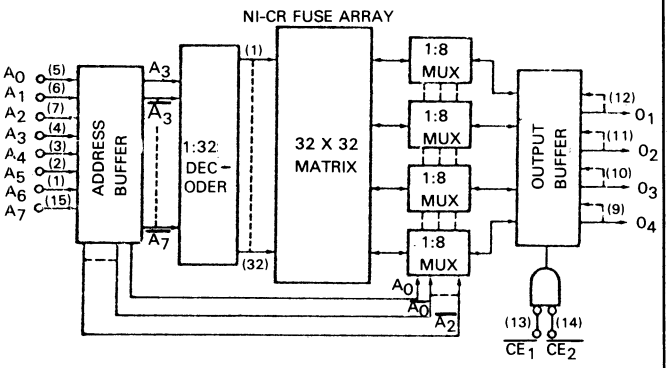
100001469

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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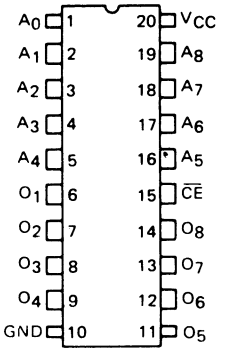
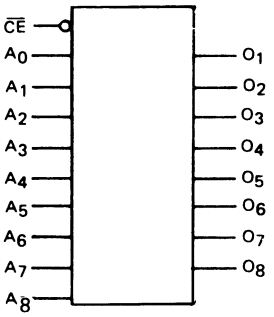
100001470 through 100001473

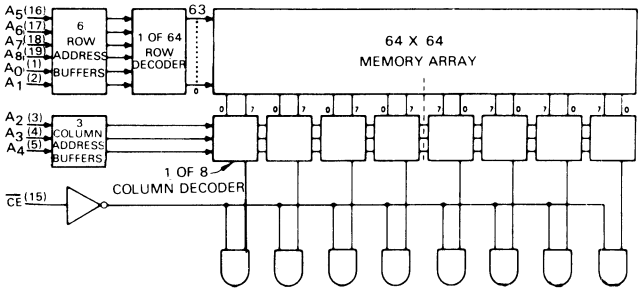
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



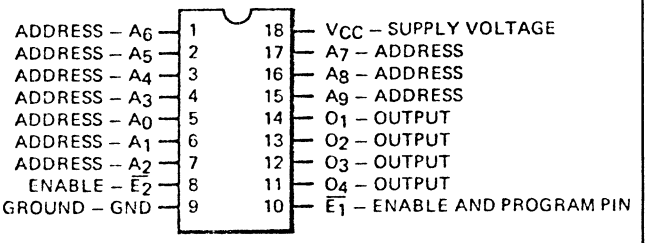
This device is a fully decoded high speed Schottky TTL 4096-Bit PROM in a 512 word by 8 bit format with tri-state output.

NOTE: *This is a Schottky device.*

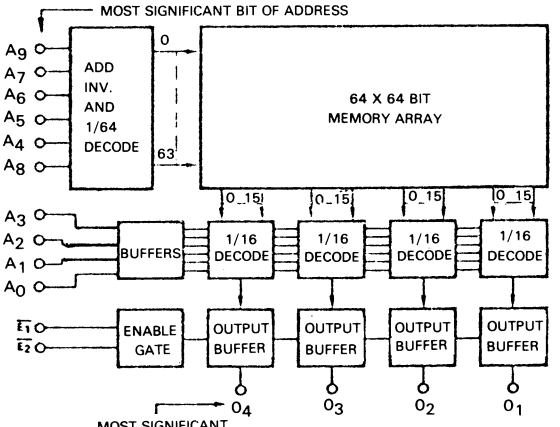
100001474 through 100001493

1024 x 4-Bit PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ and $\overline{E_2}$ must be LOW.



VCC = 18
GND = 9

This 4096-bit programmable read only memory is organized as 1024 words by 4 bits. It includes on-chip address decoding, two chip enables ($\overline{E1}$, $\overline{E2}$) and open collector outputs.

The memory is addressed with inputs A0 through A9, which select one of 1024 words. A word is read out on the outputs O1 through O4. Both enables $\overline{E1}$ and $\overline{E2}$ must be low to read. If either enable is high, the outputs are held off, permitting wire ORing of open collector outputs of several packages.

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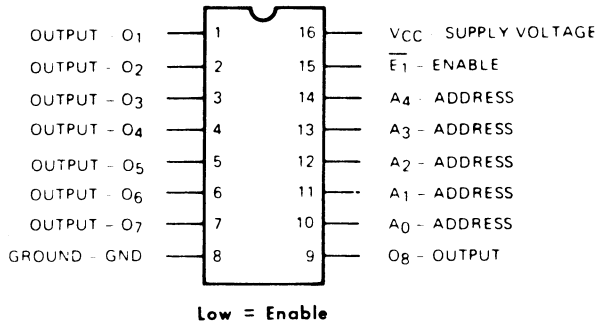
100001494

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E_1}$), and tri-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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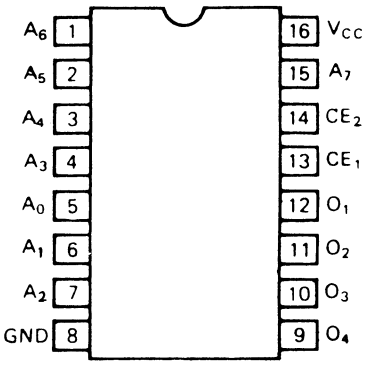
100001495

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



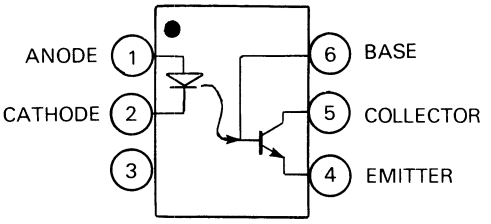
This 1024-bit programmable read only memory is organized as 256 words by 4 bits. It includes on-chip address decoding, two chip enable inputs (CE1, CE2), and uncommitted collector outputs.

NOTE *The 100001495 is a Schottky device.*

100001496

Phototransistor Optically Coupled Isolator

PIN CONFIGURATION



This device is an NPN silicon planar phototransistor optically coupled to a gallium arsenide diode.

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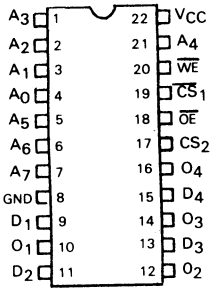
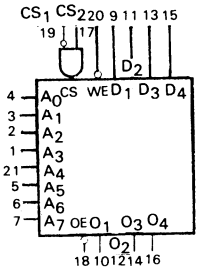
100001497

256 x 4-Bit Bipolar RAM

PIN CONFIGURATION



LOGIC SYMBOL



VCC = Pin 22
GND = Pin 8

The 100001497 is a fully decoded 1024-bit random access memory organized as 256 words by 4 bits. It features three-state outputs and two chip select inputs. A word is addressed by the 8-bit address A0 through A7.

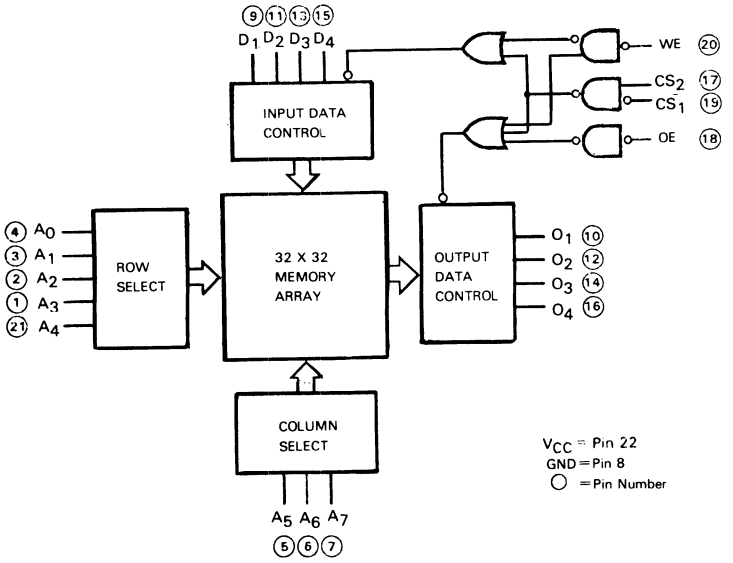
The read and write operations are controlled by the state of the active low Write Enable (WE). When WE is low and the chip is selected, the data at Din is written into the addressed location. When WE is high and the chip is selected, the data in the addressed location is read out at Dout.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS_1}$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11,13, 15	93422 3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW), HIGH Z = High Impedance.

LOGIC DIAGRAM



VCC = Pin 22
GND = Pin 8
○ = Pin Number

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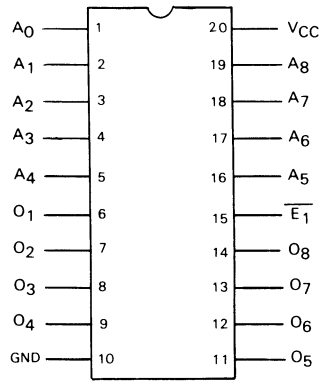
100001498

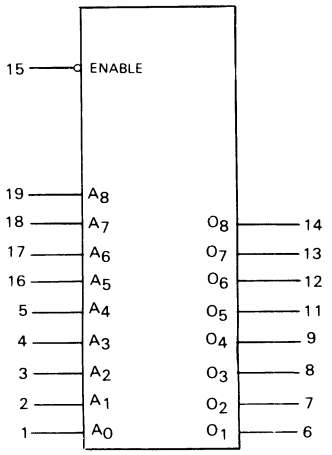
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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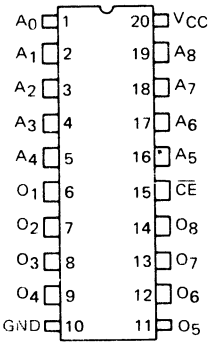
100001499 and 100001500

512 x 8-Bit Bipolar PROM

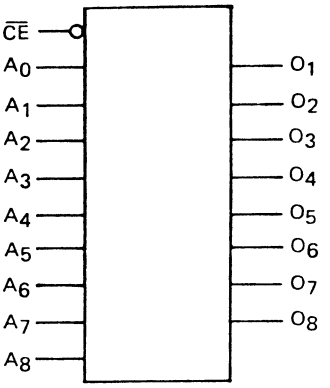
PIN CONFIGURATION



PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

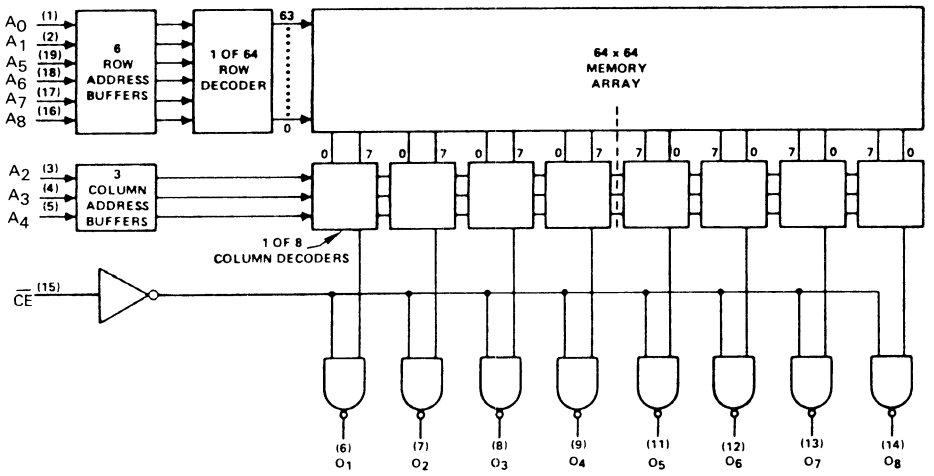
LOGIC SYMBOL



These fully decoded 4096-bit programmable read only memories are organized as 512 words by 8 bits. The 100001499 has open collector outputs and the 100001500 has tri-state outputs. They also have an active-low chip enable input $\overline{CE}$.

NOTE *The 100001499 and 100001500 are Schottky devices.*

LOGIC DIAGRAM



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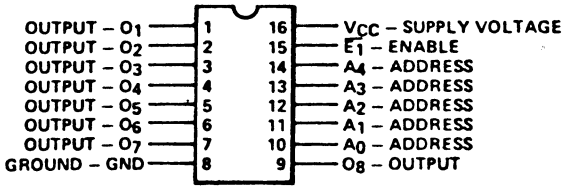
100001501

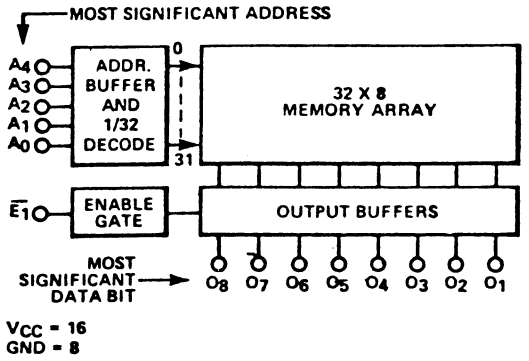
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

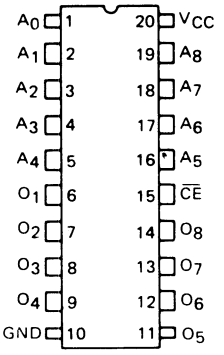
The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 0_1 through A_8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

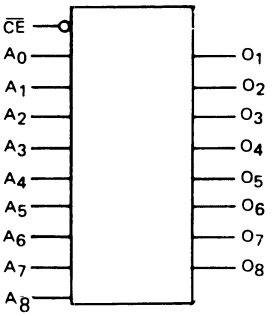
NOTE: *This is a Schottky device.*

100001502 through 100001505

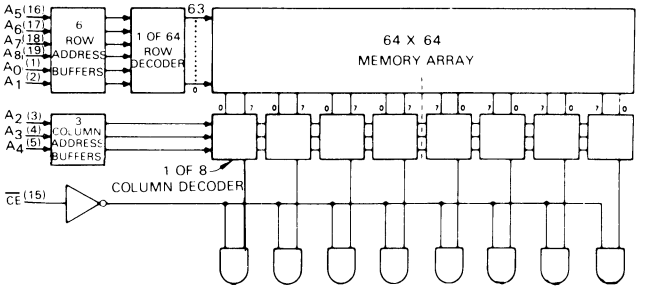
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

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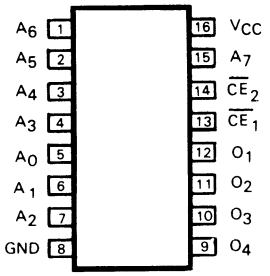
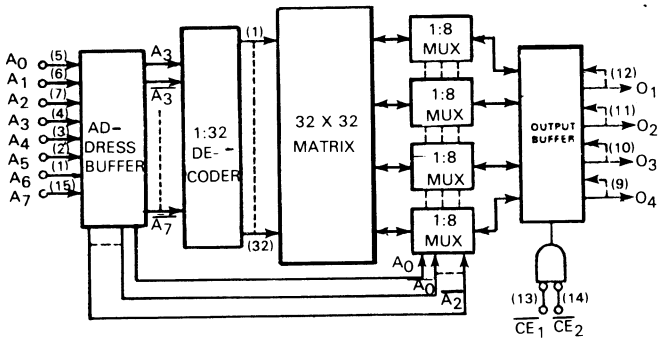
100001506 through 100001511

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

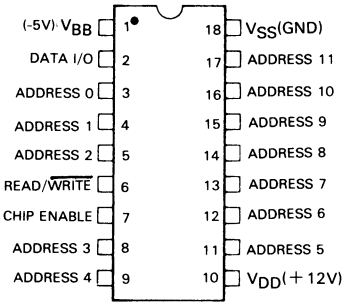
$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs, and must be asserted together while low to enable the chip.

NOTE: *This is a Schottky device.*

100001512

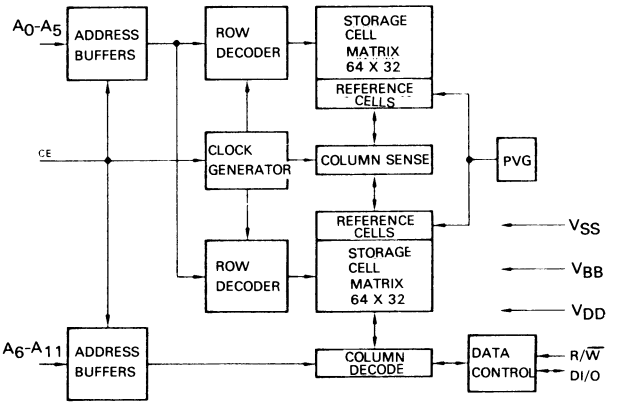
4096-Bit Dynamic RAM

PIN CONFIGURATION



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM



The 100001512 random access memory is organized as 4096 words by 1 bit. When the chip enable (CE) goes low, the memory is internally precharged and then assumes its low power standby mode. The operating cycles are initiated when CE goes high. The read cycle is non-destructive. The data in and data out signals are bused together as a common I/O signal line.

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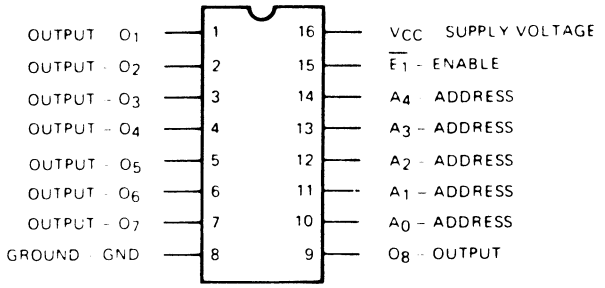
100001513 and 1000001514

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Low = Enable

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E_1}$), and tri-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 throughA8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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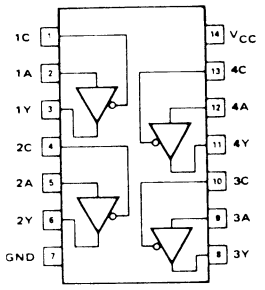
100001515

Quad Bus Buffer Gate With Tri-State Output

PIN CONFIGURATION



TRUTH TABLE

Inputs		Output
C	A	Y
L	L	L
L	H	H
H	X	(Z)

L = Low Voltage Level
H = High Voltage Level
X = Don't care
(Z) = High impedance (off)

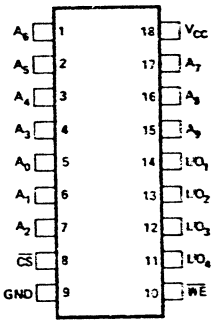
$$Y = A\overline{C}$$

NOTE *The 10001515 is a low power Schottky device.*

100001516

1024 X 4 Bit Static RAM

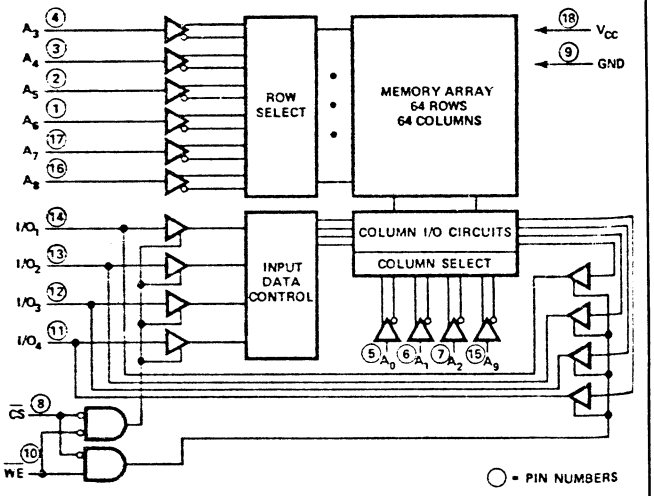
PIN CONFIGURATION



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

BLOCK DIAGRAM



The 100001516 is directly TTL compatible: All inputs and outputs. It is also a 4096-Bit Static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon Gate MOS Technology. It uses fully DC stable (static circuitry throughout-in both and decoding-and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

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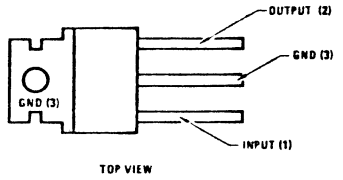
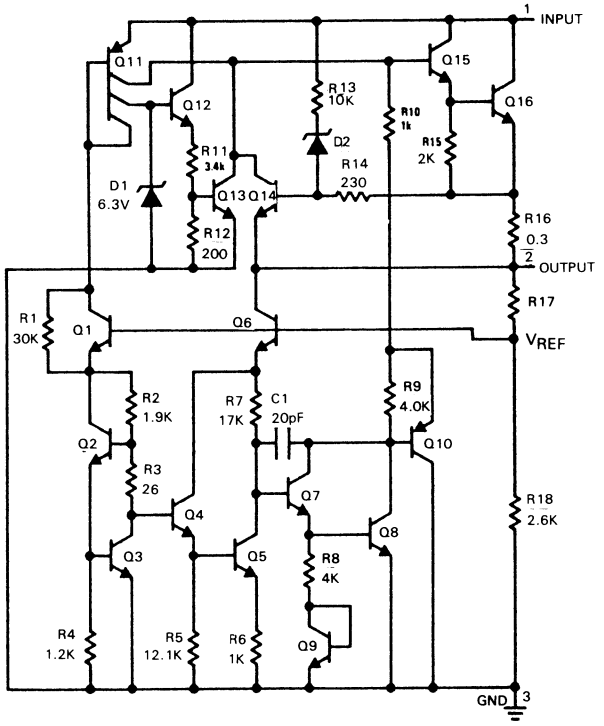
100001517

+5V, 1.5A, 3% Fixed Voltage Regulator

PIN CONFIGURATION



LOGIC DIAGRAM

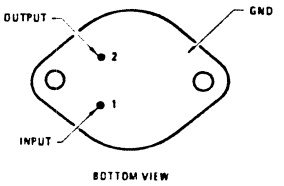


The 100001517 is a three terminal fixed voltage regulator with a 5 volt output. It includes a current limiter and an internal thermal overload protection circuit.

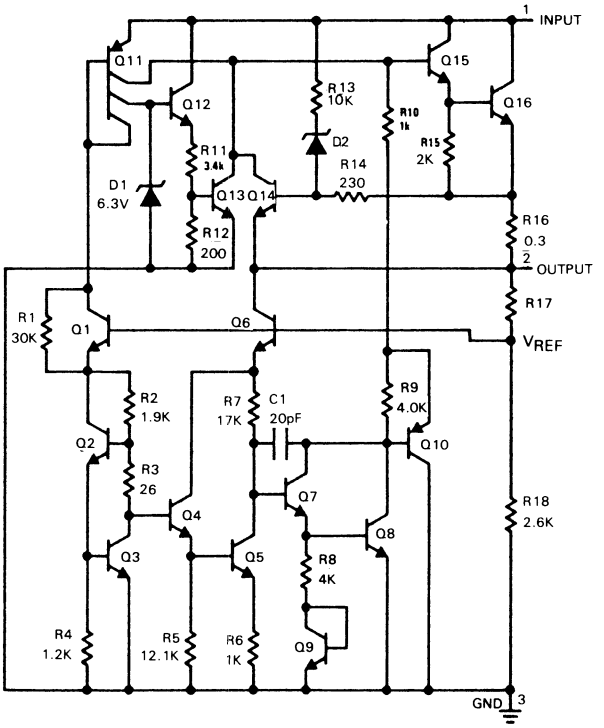
100001518

+24V, 1.5A, 3% Fixed Voltage Regulator

PIN CONFIGURATION



LOGIC DIAGRAM



The 100001518 is a three terminal fixed voltage regulator with a 24 volt output. It includes a current limiter and an internal overload protection circuit.

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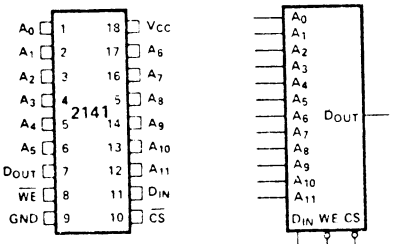
100001519

4096 x 1-Bit Static Ram

PIN CONFIGURATION



LOGIC SYMBOL

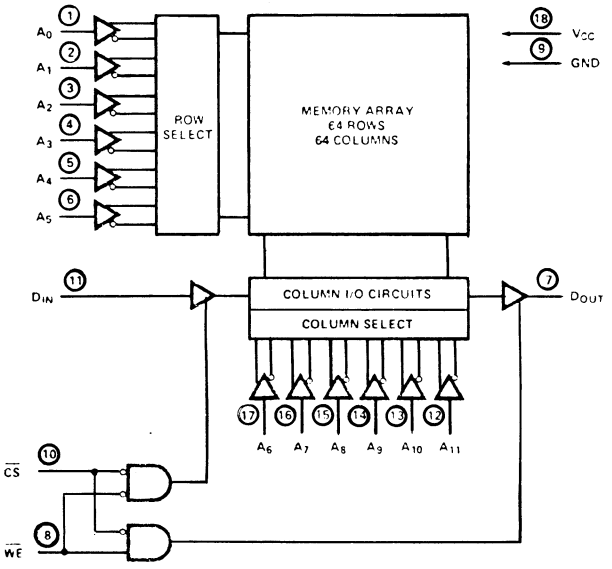
PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



This device is a 4096-bit Static Random Access Memory as 4096 words by 1-bit. CS controls the power-down feature. In less than a cycle time after CS goes high - deselecting the device - the part automatically reduces it's power requirements and remains in this low standby mode as CS remains high.

The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

This device is TTL compatible.

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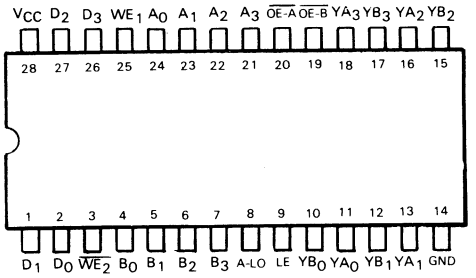
100001520

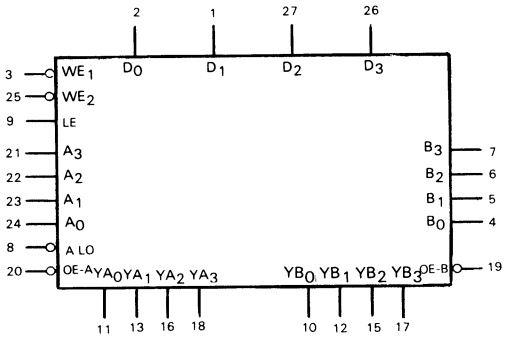
16 x 4-Bit Two-Port RAM

PIN CONFIGURATION



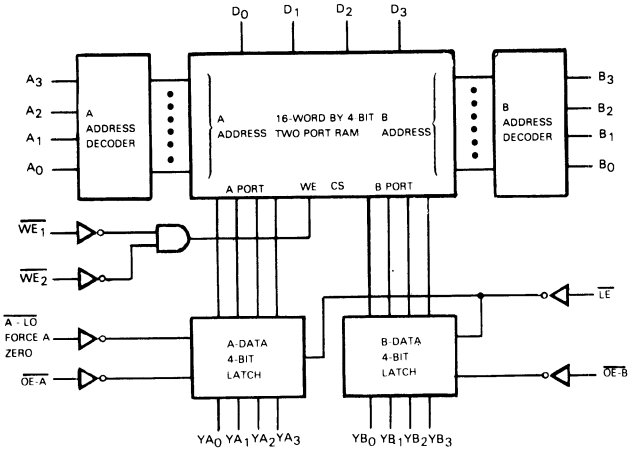
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LOGIC DIAGRAM



DEFINITION OF TERMS

D_0, D_1, D_2, D_3 Data Inputs. New data is written into the RAM through these inputs.

A_0, A_1, A_2, A_3 The A-address Inputs. The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0, B_1, B_2, B_3 The B-address inputs. The four-bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0, YA_1, YA_2, YA_3 The four A-Data Latch Outputs.

YB_0, YB_1, YB_2, YB_3 The four B-Data Latch Outputs.

$\overline{WE}_1, \overline{WE}_2$ Write Enables. When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

$\overline{OE}$-A A-port Output Enable. When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH, the YA_i outputs are in the high-impedance (off) state.

$\overline{OE}$-B B-port Output Enable. When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH, the YB_i outputs are in the high-impedance (off) state.

LE Latch Enable. The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs.

$\overline{A\text{-}LO}$ Force A Zero. This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed.

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100001520 (CONT.)

The 100001520 is a 64-bit, two port random access memory organized as 16 words by 4 bits. Any two words can be read from the two output ports simultaneously. Each port has a four-bit latch which is controlled by the latch enable (LE). The memory has two write enable inputs ($\overline{WE1}$, $\overline{WE2}$). $\overline{WE1}$ and LE can be wired together to make the operation of the memory appear edge-triggered.

A 4-bit A-address field and a 4-bit B address field address any of the 16 memory words for the A-output port or B-output port, respectively. The D inputs are used to load data into the device.

The device features tri-state outputs so that several devices can be cascaded. The A-output port or the B-output port, respectively, is in the high-impedance state when the $\overline{OE}$-A' input or $\overline{OE}$-B' input is high.

The write enable inputs control writing data into the memory. When both these enables are low, data is written into the word selected by the B-address field. When either enable is high, no data is written into the memory. The outputs follow the data inputs during writing.

NOTE *The 100001520 is a low power Schottky device.*

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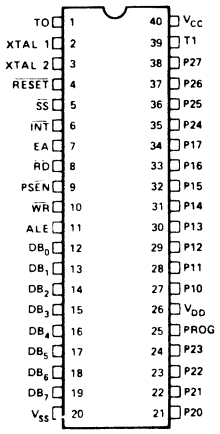
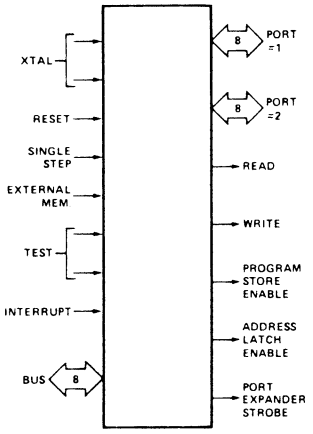
100001523

8-Bit Microcomputer

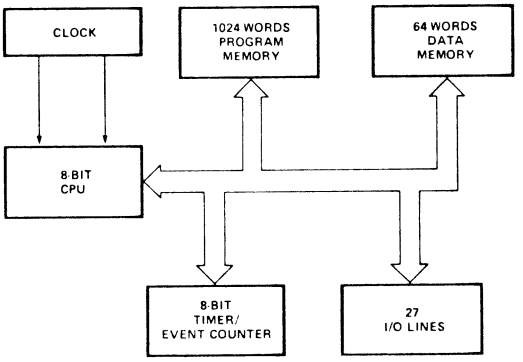
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



The 100001523 contains a 1K x 8 ROM program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to an oscillator and clock circuits.

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming. Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

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100001523 (CONT.)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
		Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH})
		Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

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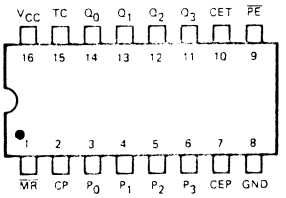
100001524

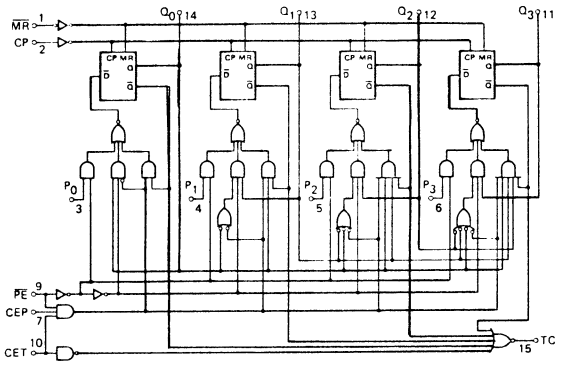
Four-Bit Binary Counter

PIN CONFIGURATION

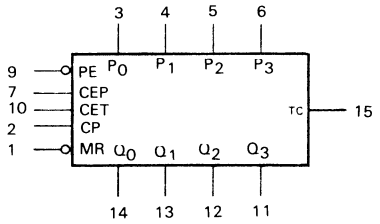


Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS									OUTPUTS			
CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
X	L	X	X	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	H	X	X	X	X	COUNT			

H = HIGH
L = LOW
X = Don't Care

NC = No Change
D_i may be either HIGH or LOW
↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

CET	Q_0	Q_1	Q_2	Q_3	TC
H	H	H	H	H	H
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L

The 100001524 is a synchronous 4-bit binary counter. When the parallel enable ($\overline{PE}$) is low, the data on the P0-P3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is high and both count enables (CEP,CET) are also high, counting occurs on the positive transition of the clock. The terminal count output (TC) is high when CET is high and the counter is in its terminal count state. The counter also has a master reset input ($\overline{MR}$), which, when low, forces the Q outputs low independently of all other inputs.

NOTE *The 100001524 is a Schottky device.*

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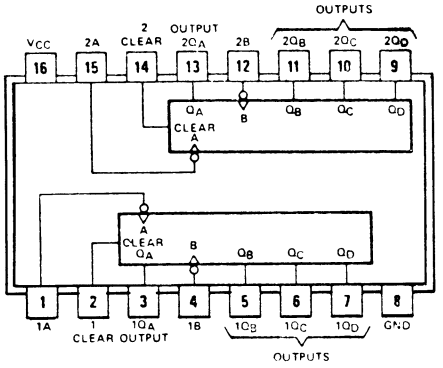
100001525

Dual 4-Bit Decade And Binary Counters

PIN CONFIGURATION



FUNCTION TABLES

BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

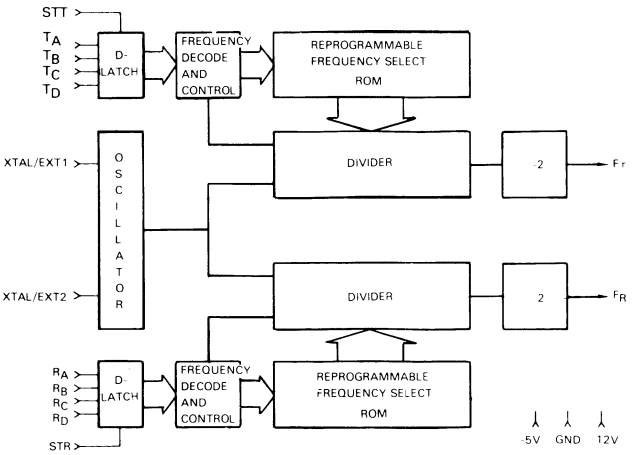
NOTE *The 100001525 is a low power Schottky device.*

100001526

Baud Rate Generator
Programmable Divider

PIN CONFIGURATION

BLOCK DIAGRAM



This is a ROM controlled divider. It has:

- On chip crystal oscillator or external frequency input
- Choice of 2 x 16 output frequencies
- 16 asynchronous/synchronous baud rates
- Direct UART/USRT compatibility
- Full duplex communication capability
- Re-programmable ROM allows generation of other frequencies
- TTL, MOS compatibility
- On chip pull-up resistor
- 0.01% accuracy
- 50% duty cycle

NOTE: *This is a Schottky device*

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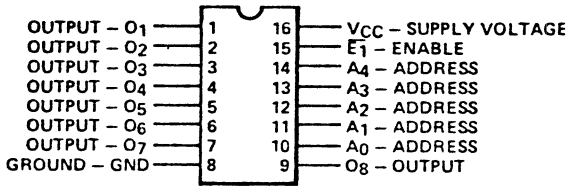
100001527

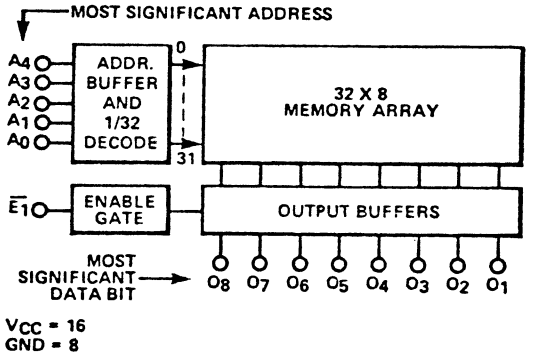
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE: *This is a Schottky device.*

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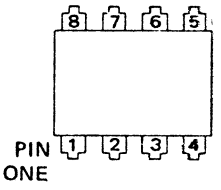
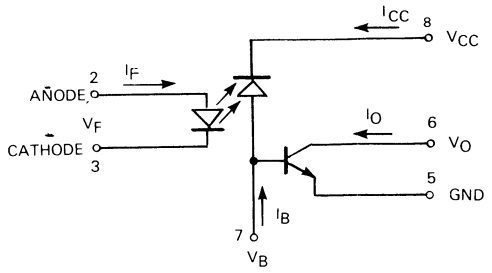
100001528

High Speed Optically Coupled Isolators

PIN CONFIGURATION





This device uses GaAsP light emitting diodes optically coupled to a photo-sensitive circuit. It provides 3000 Vdc isolation between the input and the output. It has open collector ouput, and is TTL compatible.

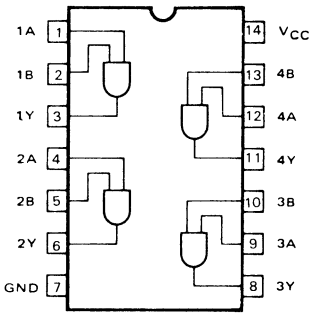
100001528 features:

- 2 MHz BANDWIDTH
- HIGH COMMON MODE TRANSIENT IMMUNITY: 1000V/μs
- HIGH SPEED: 1 Mbit/s

100001529

Quad 2-Input AND Gate w/Open Collector Outputs

PIN CONFIGURATION



Positive logic: Y = AB

NOTE *The 100001529 is a Schottky device.*

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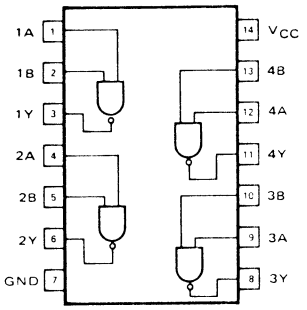
100001530

Quad 2-Input NAND Gate w/Open Collector Outputs

PIN CONFIGURATION



Positive logic: $Y = \overline{AB}$

NOTE *The 100001530 is a low power Schottky device.*

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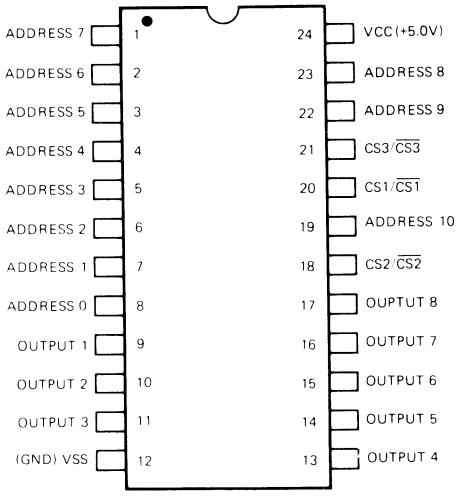
100001533 and 100001534

2048 X 8-Bit MOS PROM

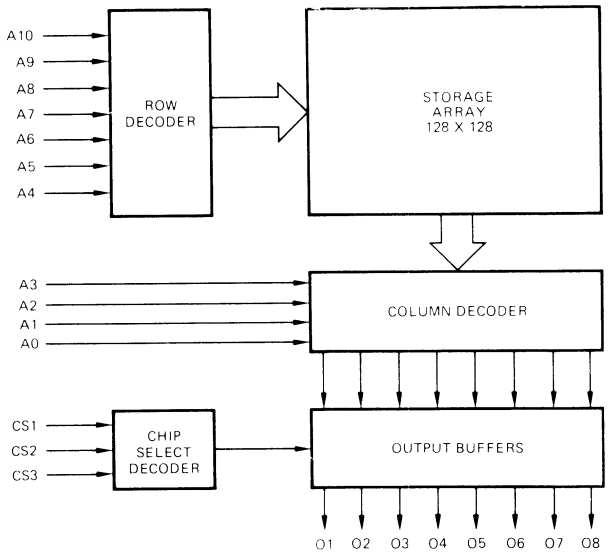
PIN CONFIGURATION



Top View

Pin 1 is marked for orientation.

BLOCK DIAGRAM



Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity is specified, thus allowing the addressing of 8 memory chips without external gating. Also this device is TTL compatible and N-channel silicon gate MOS technology is used.

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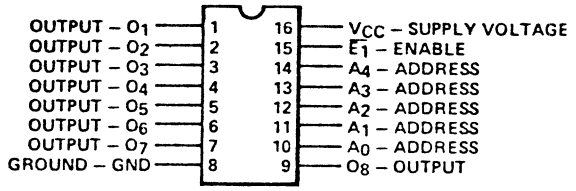
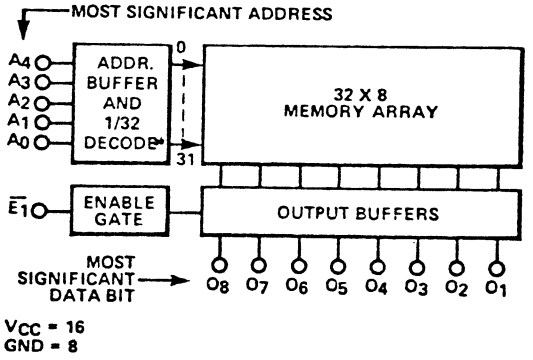
100001535 through 1000001538

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$) and three-state outputs.

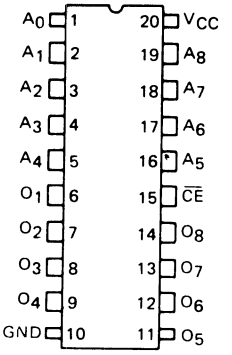
The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

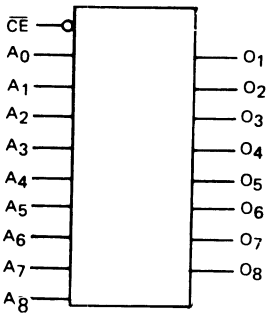
NOTE *100001535 through 100001538 are Schottky devices.*

100001539 through 100001544

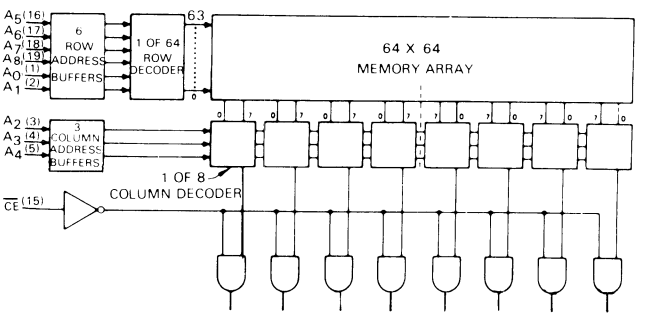
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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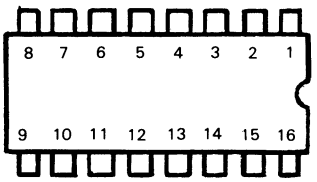
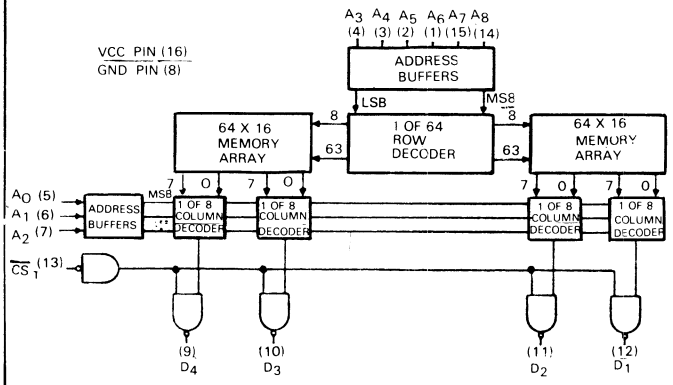
100001545

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION





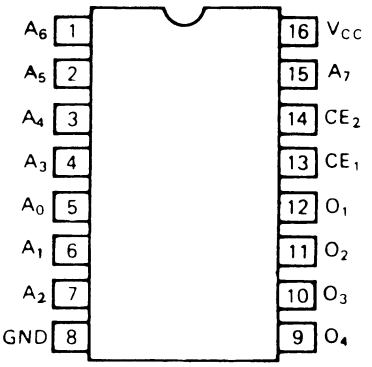
This 2048-bit programmable read only memory is organizd as 512 words by 4 bits. It includes on-chip address decoding and open-collector outputs.

NOTE *The 100001545 is Schottky device.*

100001546

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

NOTE *The 100001546 is a Schottky device.*

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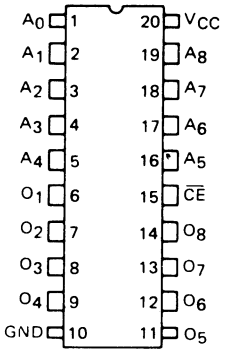
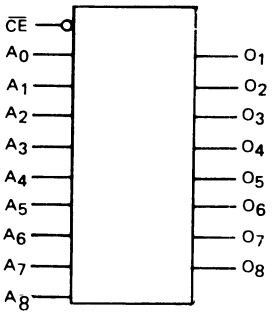
100001547 and 100001548

512 x 8-Bit Bipolar PROM

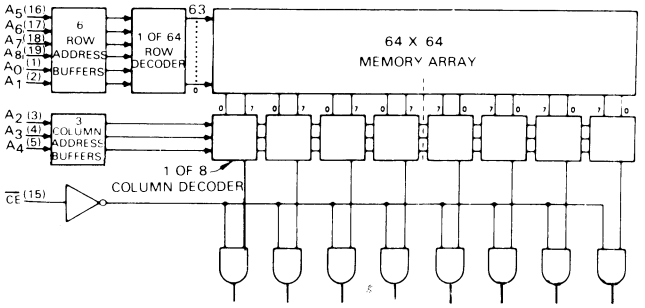
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



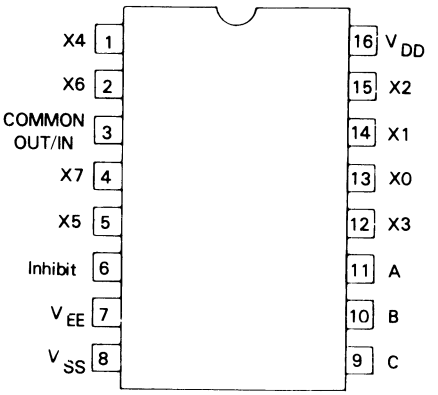
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

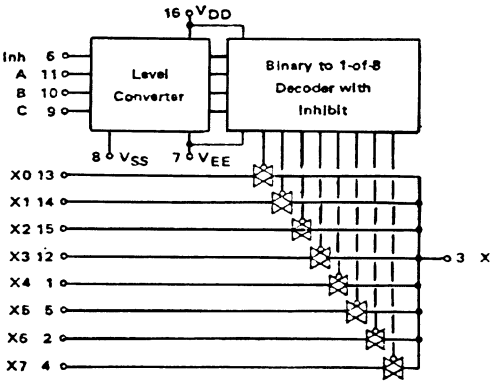
100001549

Analog Multiplexors/Demultiplexors

PIN CONFIGURATION



8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



TRUTH TABLE

Control Inputs		
Inhibit	Select C B A	On Switches MC15051
0	0 0 0	x 0
0	0 0 1	x 1
0	0 1 0	x 2
0	0 1 1	x 3
0	1 0 0	x 4
0	1 0 1	x 5
0	1 1 0	x 6
0	1 1 1	x 7
1	x x x	none

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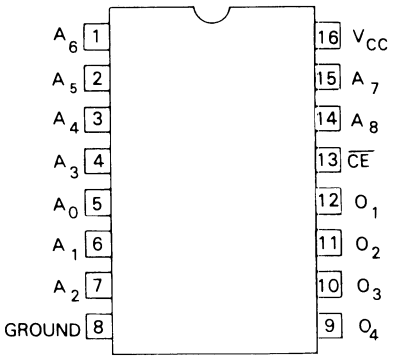
100001550 through 100001619

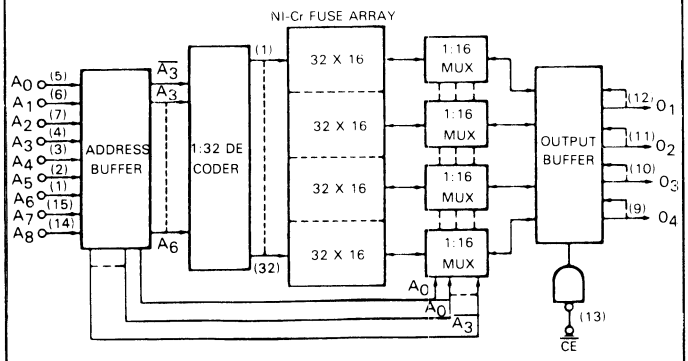
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



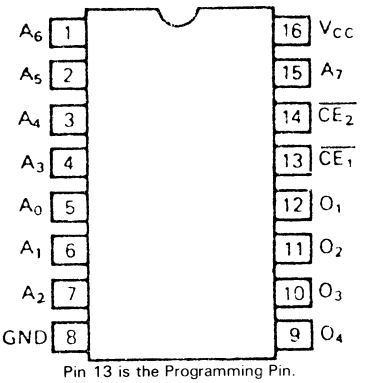
These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector

NOTE: *This is a Schottky device.*

100001620 through 100001634

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided. The device is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low.

NOTE: *This is a Schottky device.*

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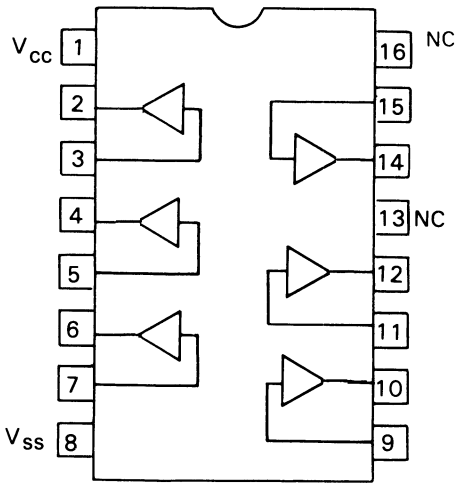
100001635

Hex Buffers

PIN CONFIGURATION



Y = A

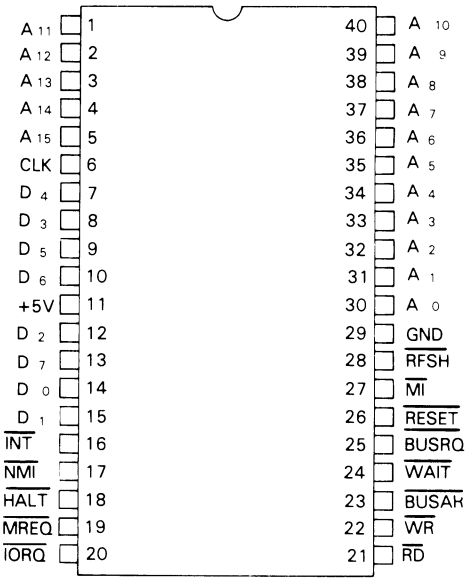
This is a complimentary MOS device.

Note that pin 16 is not connected internally on this device; consequently, connections to this pin will not affect circuit operation.

100001636

8 Bit CPU Chip

PIN CONFIGURATION



A_0-A_{15} (Address Bus)	Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D_0-D_7 (Data Bus)	Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M_1}$ (Machine Cycle one)	Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{MREQ}$ (Memory Request)	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$ (Input/ Output Request)	Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

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100001636 (cont.)

$\overline{RD}$ (Memory Read) — Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) — Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) — Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) — Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) — Input, active low. $\overline{WAIT}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) — Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt) — Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the CPU to restart to location 0066_H.

$\overline{RESET}$ — Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

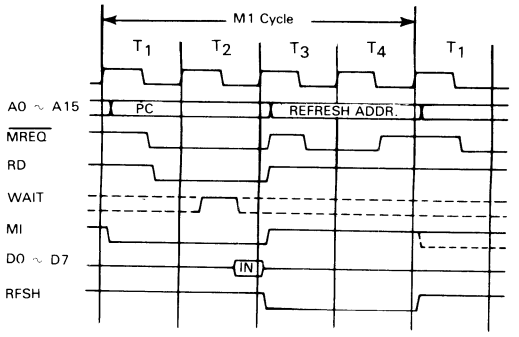
$\overline{BUSRQ}$ (Bus Request) — Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) — Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



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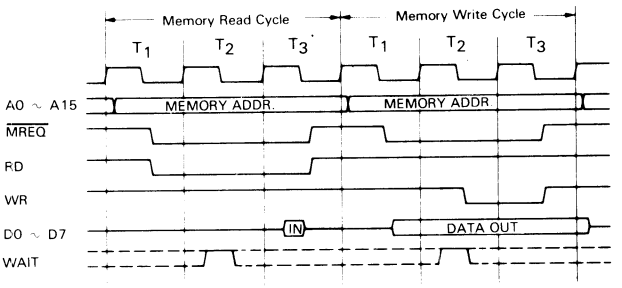
100001636 (cont.)

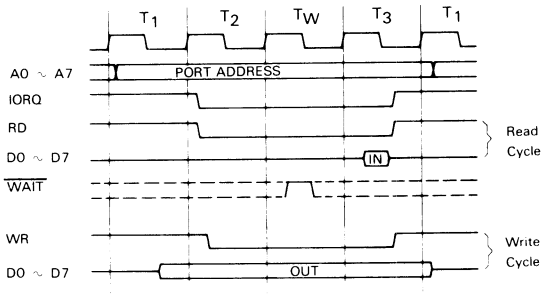
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



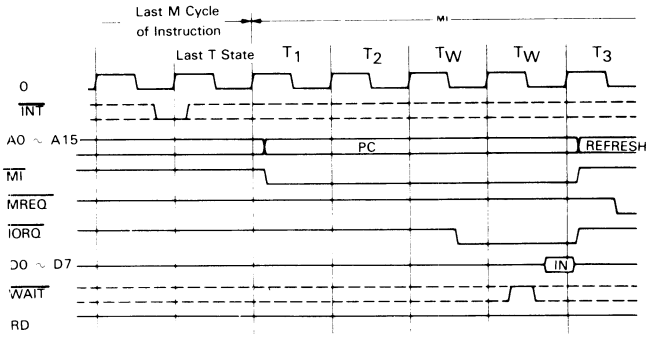
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the peripheral controllers, can be easily implemented.



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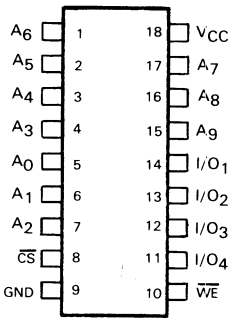
100001641

1024 x 4-Bit Static Ram

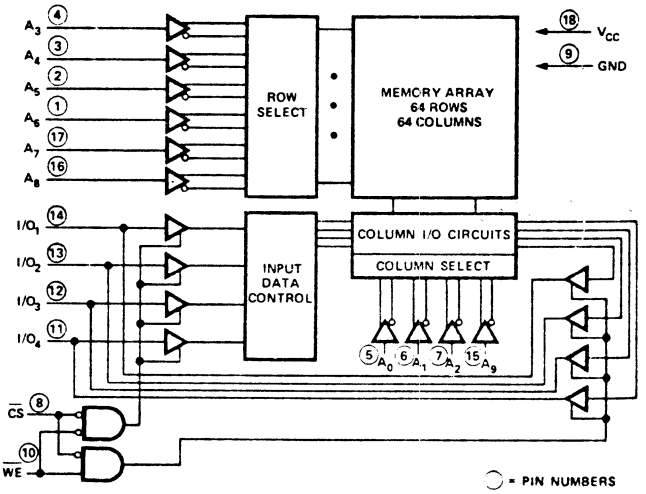
PIN CONFIGURATION



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

BLOCK DIAGRAM

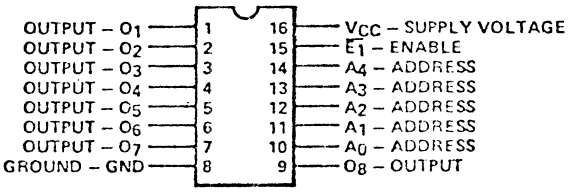


1. A READ occurs during the overlap of a low **$\overline{CS}$** and a high **$\overline{WE}$**.
2. A write occurs during the overlap of a low **$\overline{CS}$** and a low **$\overline{WE}$**.
3. **$\overline{WE}$** is high for a read cycle.
4. If the **$\overline{CS}$** low transition occurs simultaneously with the **$\overline{WE}$** low transition, the output buffers remain in a high impedance state.
5. **$\overline{WE}$** must be high during all address transitions.

100001643

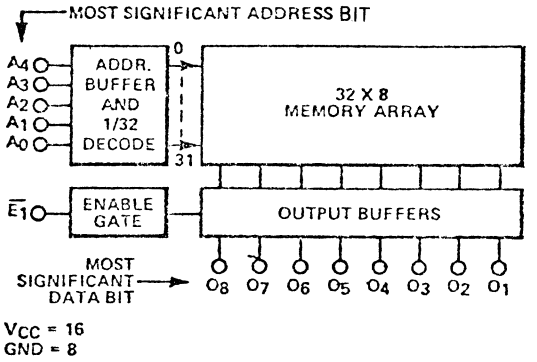
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable (E1), and three-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable E1 must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE: *This is a Schottky device.*

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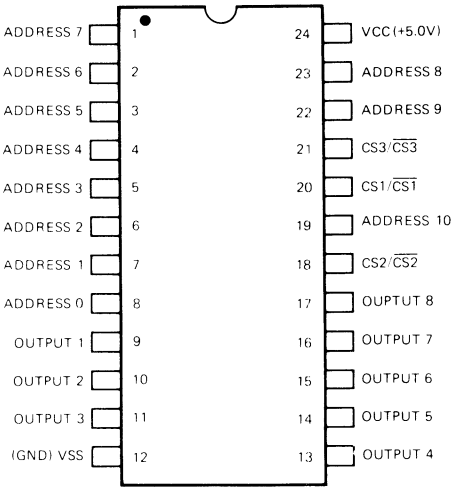
100001644 through 100001646

2048 X 8-Bit MOS PROM

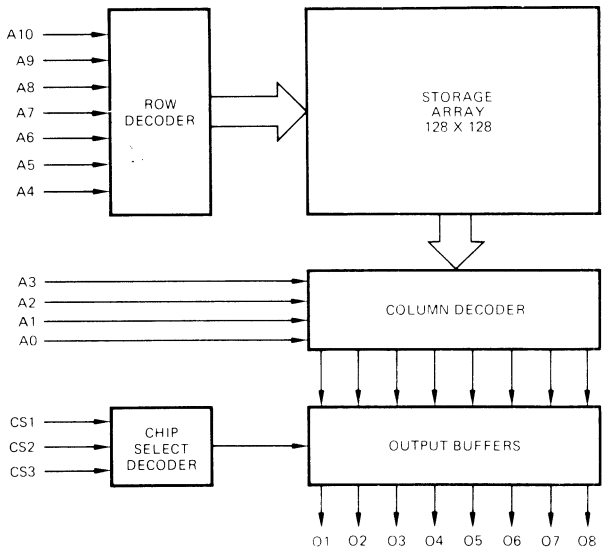
PIN CONFIGURATION



Top View

Pin 1 is marked for orientation.

BLOCK DIAGRAM

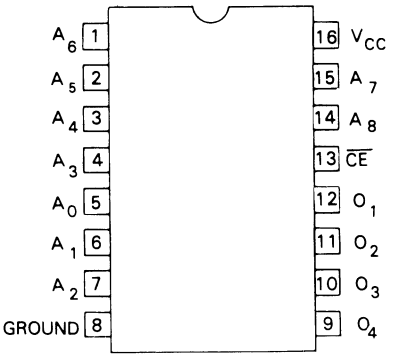


Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity is specified, thus allowing the addressing of 8 memory chips without external gating. Also this device is TTL compatible and N-channel silicon gate MOS technology is used.

100001647 through 100001676

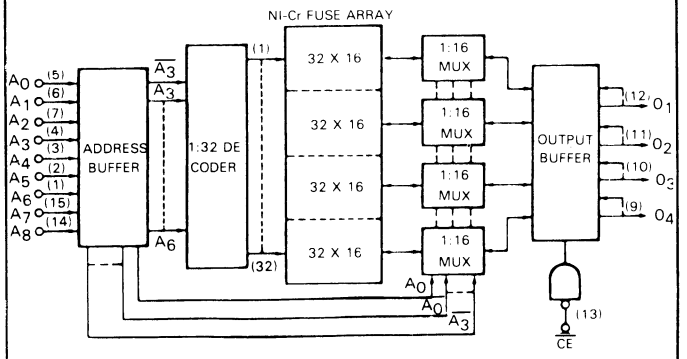
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector outputs.

NOTE: *This is a Schottky device.*

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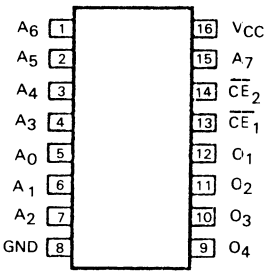
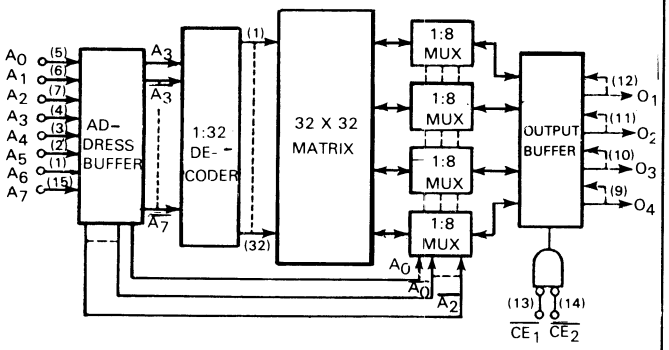
100001677 through 100001680

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

NOTE: *This is a Schottky device.*

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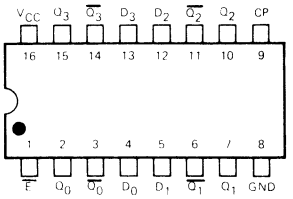
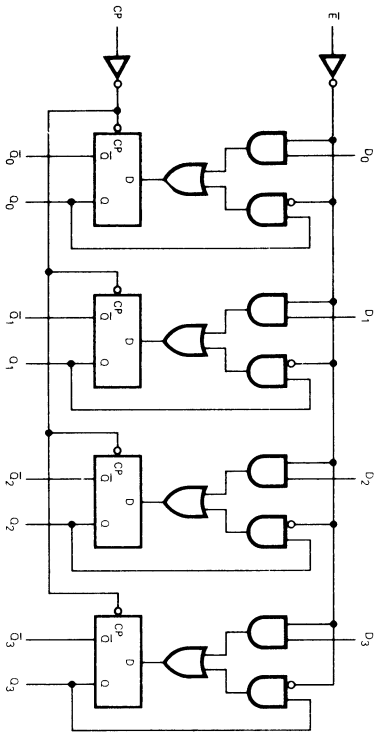
100001681

Quad D-Type Flip Flop with Enable

PIN CONFIGURATION



BLOCK DIAGRAM



Inputs			Outputs	
$\bar{E}$	D_i	CP	Q_i	$\bar{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

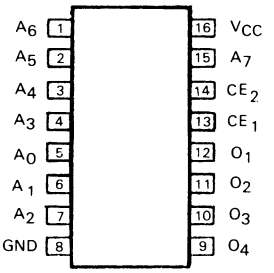
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition

NOTE *The 100001681 is a low power Schottky device.*

100001682

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



This integrated circuit is a high-speed, electrically programmable, fully decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

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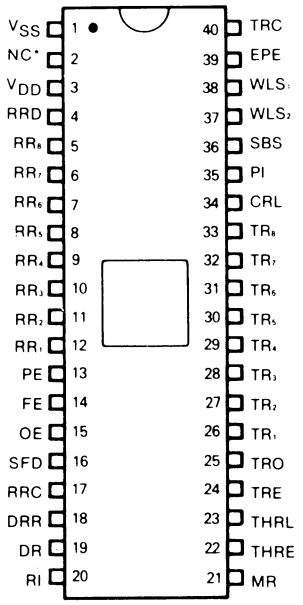
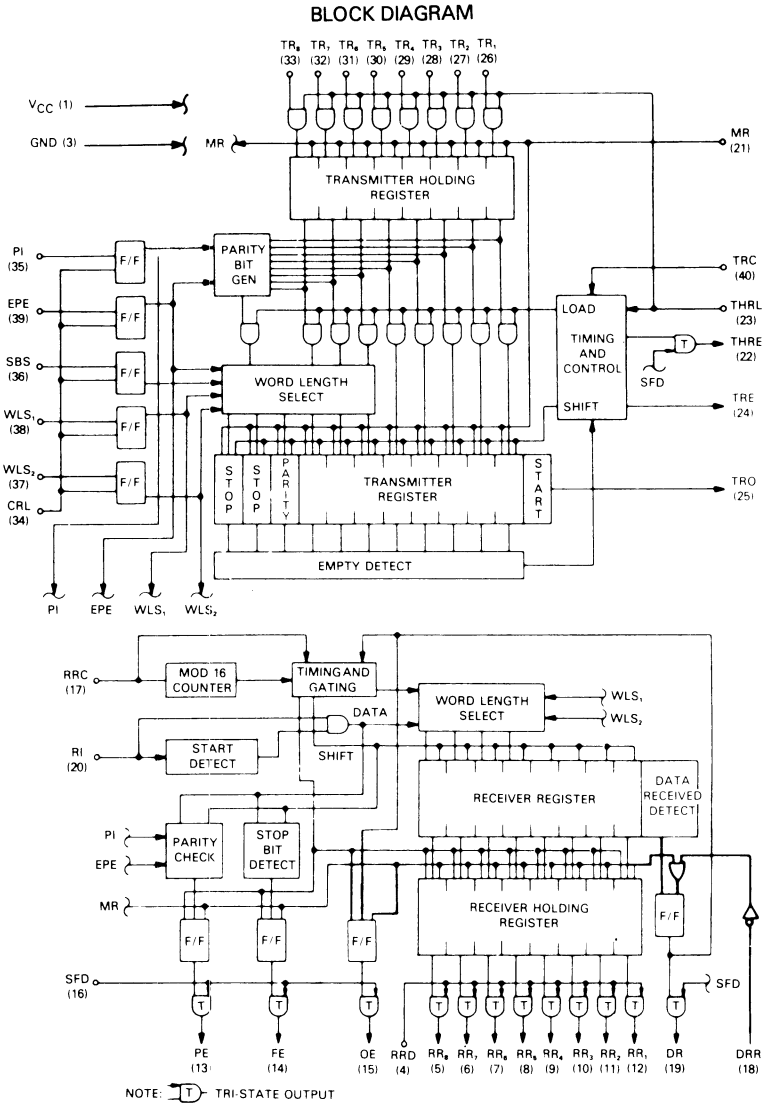
100001684

Asynchronous Receiver/Transmitter

PIN CONFIGURATION



BLOCK DIAGRAM



The Asynchronous Receiver/Transmitter is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data analog with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic.

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100001684 (cont.)

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 volts supply
2		NC	No Connection (Open)
3	GROUND	GND	Ground = OV
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8 RR_1 data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR_1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, appied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage, V_{OL}.

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100001684 (cont.)

PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.
36	STOP BIT (S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.
37-38	WORD LENGTH SELECT	WLS_2 WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER CLOCK	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

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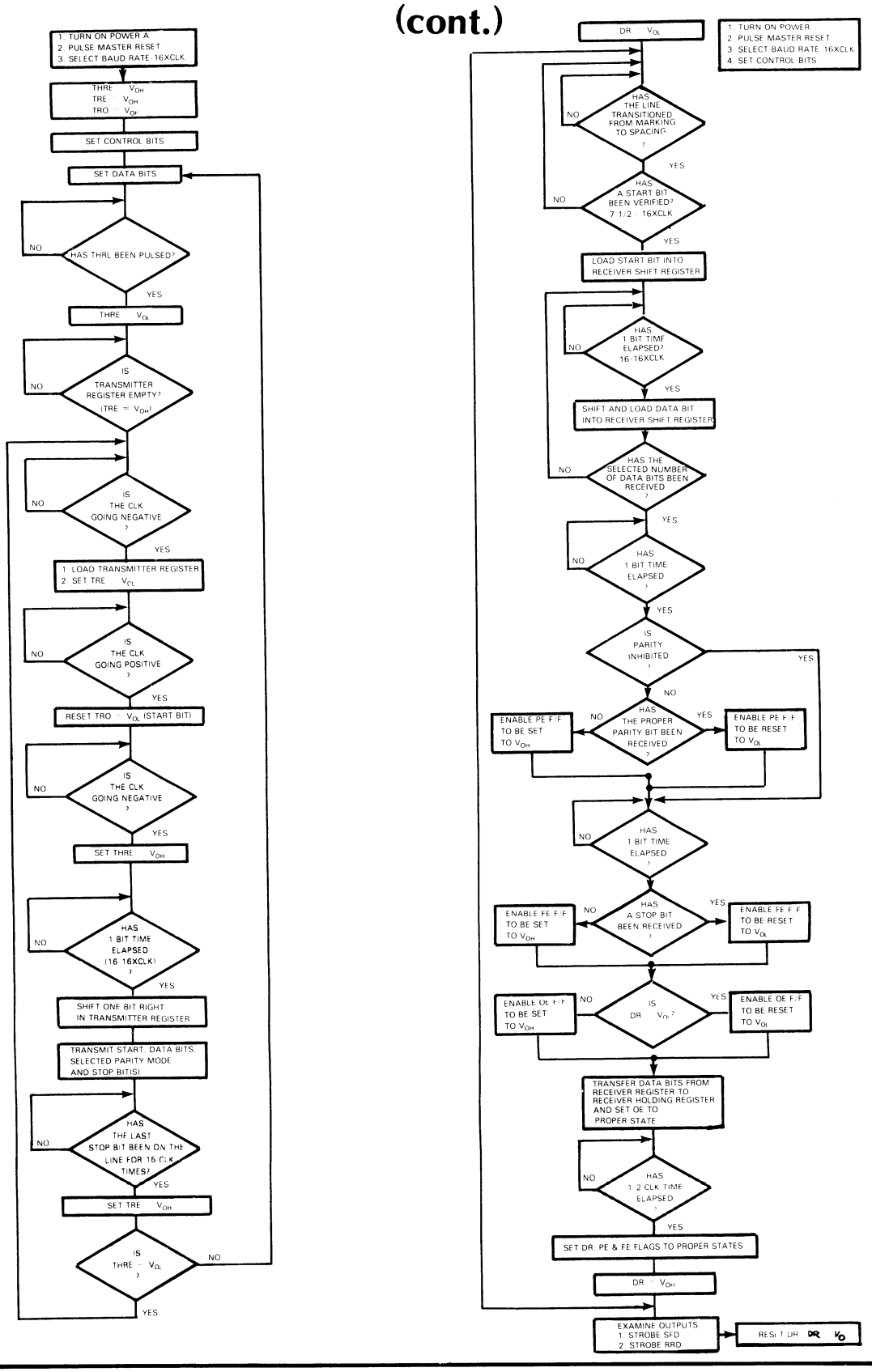
100001684 (cont.)



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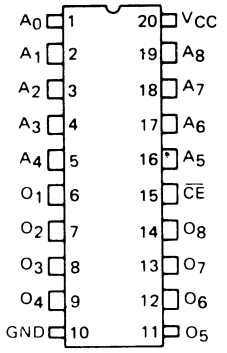
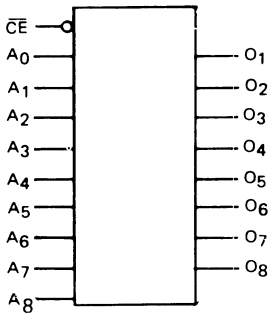
100001685

512 x 8-Bit Bipolar PROM

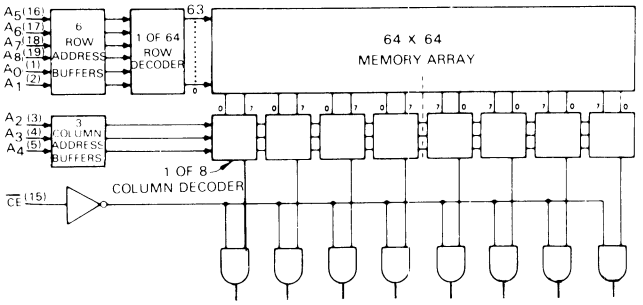
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



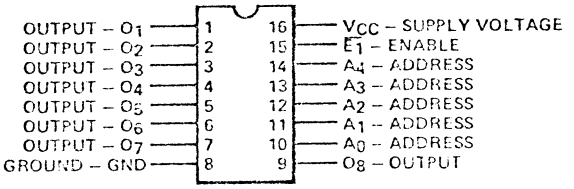
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

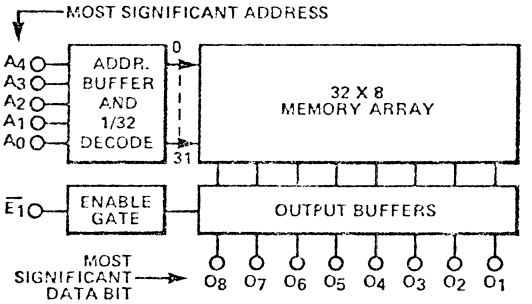
100001686

32 X 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory has open collector outputs and low input current PNP inputs.

The device enabled when $\overline{E}_1$ is low.

NOTE: *This is a Schottky device.*

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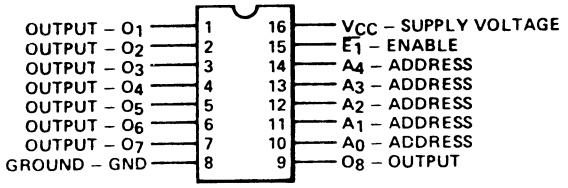
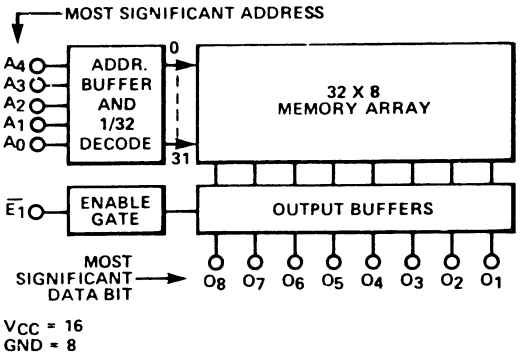
100001687

32 x 8-Bit PROM

PIN CONFIGURATION



BLOCK DIAGRAM



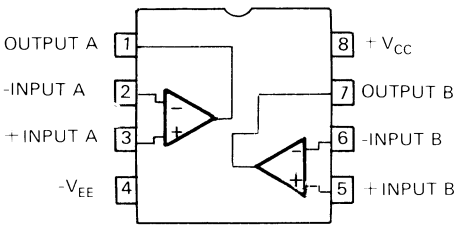
This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE *This is a Schottky device.*

100001688

Dual BIFET Operational Amplifier



This is a Junction-field effect transistor input (BIFET) dual operational amplifier. It has a typical slew rate of 13 V/μ s, an offset voltage of 15.0 mV at 25°C.

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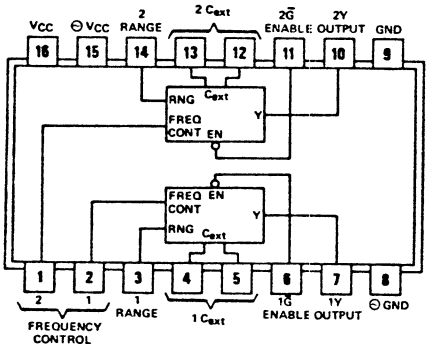
100001698

Dual Voltage Controlled Oscillator

PIN CONFIGURATION



logic: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

This device features two independent voltage controlled oscillators (VCO). The input frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency from 0.12 hertz to 85 megahertz. The output frequency can be approximated as follows:

$f_0 = 5 \times 10^{-4}$

C_{EXT}

where f_0 = output frequency in hertz

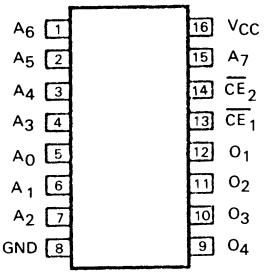
C_{EXT} = external capacitance in farads.

NOTE: *This is a Schottky device.*

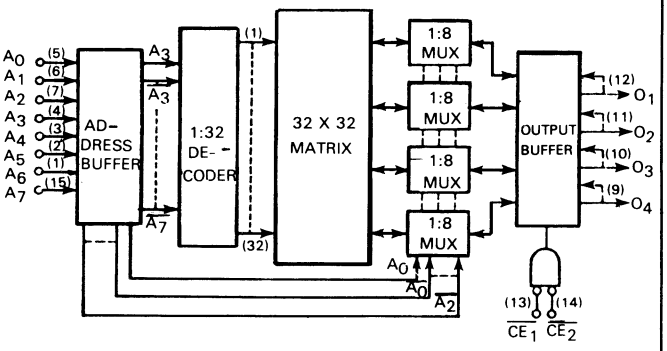
100001699

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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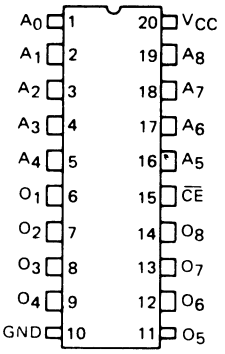
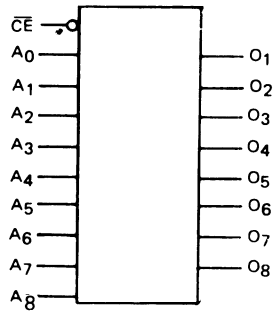
100001700

512 x 8-Bit Bipolar PROM

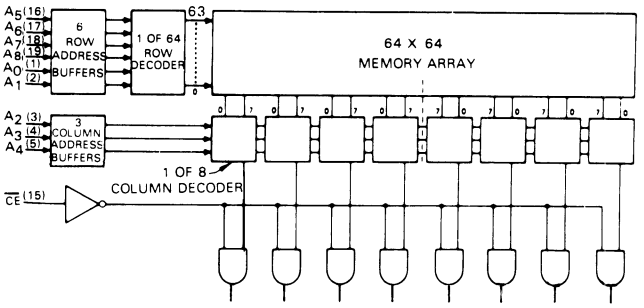
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



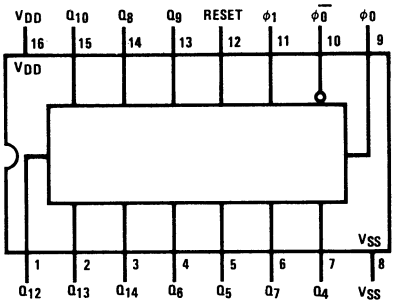
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001701

14 Stage Ripple Carry Binary Counter

PIN CONFIGURATION



This is a 14 stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. They are reset to the zero state by a logical "1" at the reset input independent of clocks.

This counter has low power TTL compatibility.

NOTE: *This is a CMOS device.*

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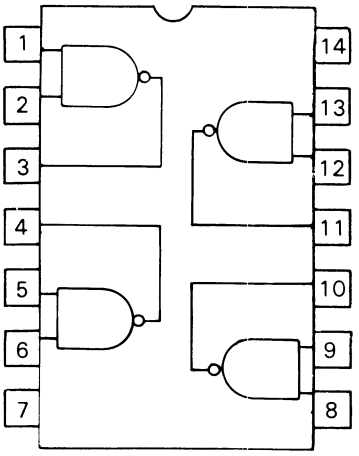
100001702

Quad 2-Input NAND Gate

PIN CONFIGURATION



V_{DD} = PIN 14
V_{SS} = PIN 7

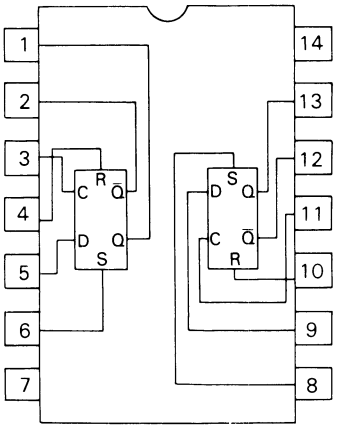
$Y = \overline{AB}$

This is a low power complimentary MOS device.

100001703

Dual Type D-Flip Flop

PIN CONFIGURATION



V_{SS} = PIN 7
V_{DD} = PIN 14

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\bar{Q}$	
⌐⌐	0	0	0	0	1	NO CHANGE
⌐⌐	1	0	0	1	0	
⌐⌐	X	0	0	Q	$\bar{Q}$	
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = DON'T CARE
+ = LEVEL CHANGE

This is a low power Complimentary MOS device.

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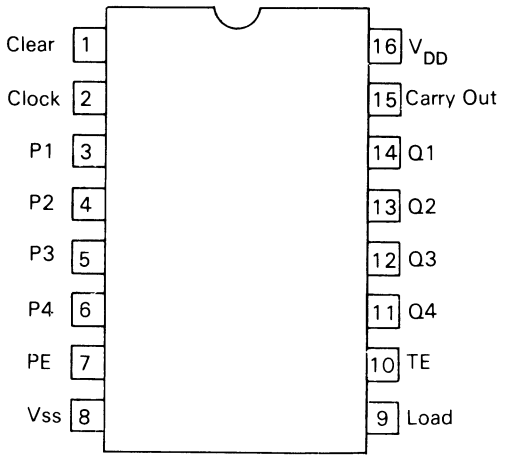
100001704

4-Bit Binary Counter (With Asynchronous Clear)

PIN CONFIGURATION



This counter is fully programmable; that is the outputs maybe preset to either level. As presetting is synchronous, settling up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, bad or enable inputs.

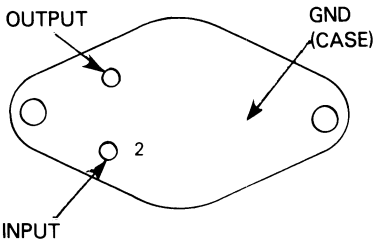
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing the function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE), must be high to count and enable input TE fed foward to enable the carry positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

NOTE: *This is a CMOS device.*

100001707

+5V, 5A 50W, 5% Voltage Regulators

PIN CONFIGURATION



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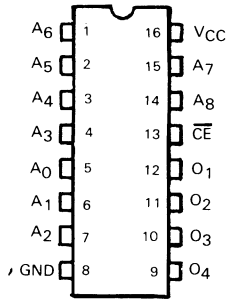
100001710

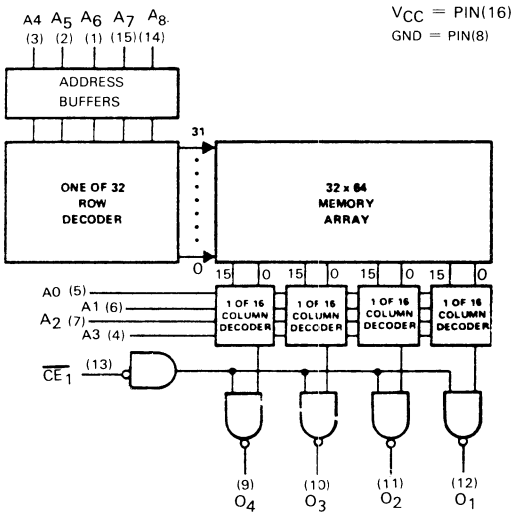
512 X 4 Prom

PIN CONFIGURATION



$A_0 - A_8$	Address Inputs
$\overline{CE}$	Chip Enable Input
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 2048-bit high speed field programmable read only memory has tri-state output.

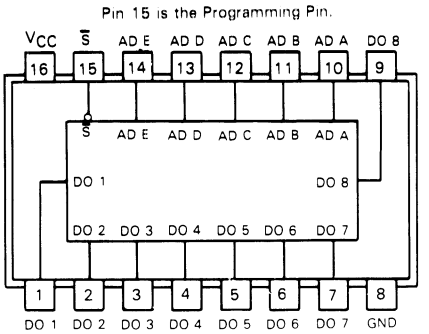
With a 45 ns maximum address access time, the prom is intended for ultra high speed logic systems.

NOTE: *This is a Schottky device.*

100001711

32 X 8 Bit PROM

PIN CONFIGURATION



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

NOTE: *This is a Schottky device.*

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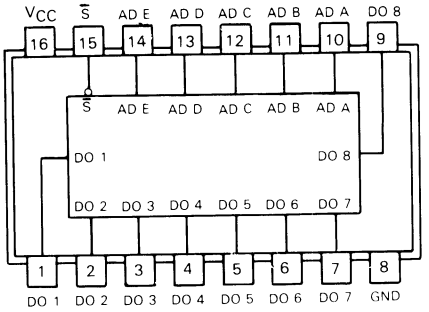
100001712

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



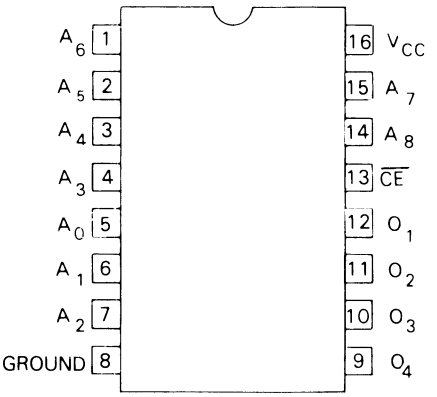
This 256-bit, high speed programmable read only memory has tri-state output. It is TTL compatible. $\overline{S}$ must be low to enable the chip.

NOTE: *This is a Schottky device.*

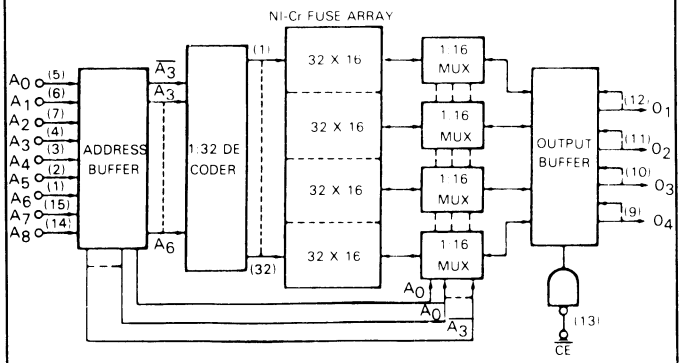
100001713

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory has tri-state output. It is TTI compatible. $\overline{CE}$ must be low to enable the device.

NOTE: *This is a Schottky device.*

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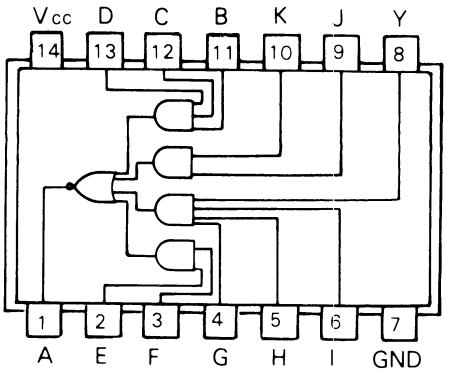
100001714

4-2-3-2 Input And Or Invert Gates
Open-Collector Output

PIN CONFIGURATION
(TOP VIEW)



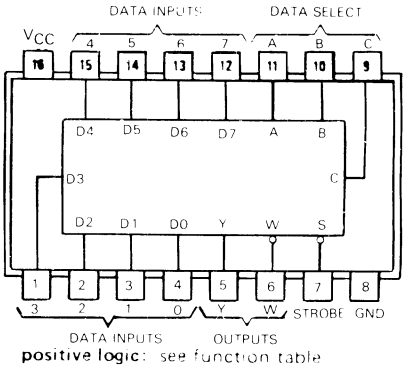
positive logic: $Y = \overline{ABCD + EF + GHI + JK}$

This device has open collector output and has transistor to transistor logic (TTL).

NOTE: *This is a Schottky device.*

100001715

1-of-8 Data Selector/Multiplexor

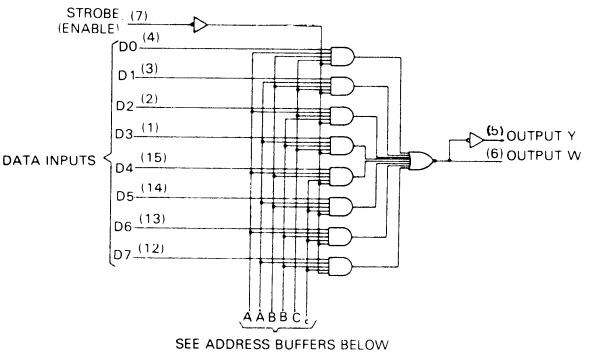


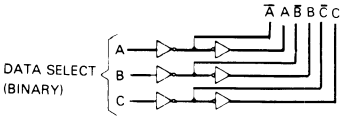
positive logic: see function table

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input





This device contains full on-chip binary decoding to select the desired data source. It has a strobe input which must be at a low logic level to enable this device.

NOTE: *This is a Schottky device.*

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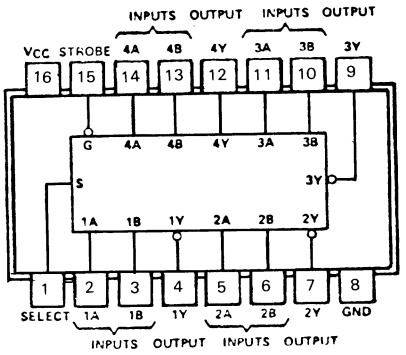
100001716

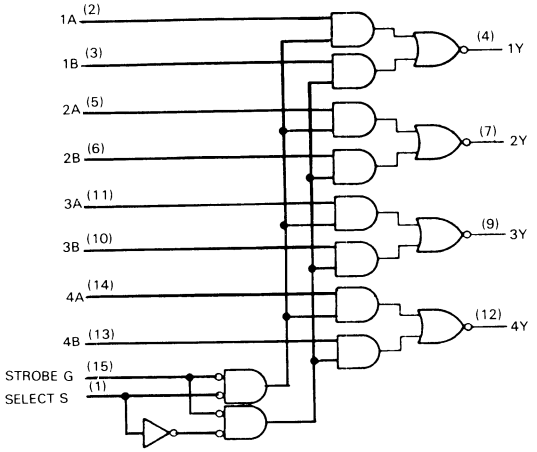
Quadruple 2-Line-To-1-Line Data Selector/Multiplexor with Inverted Outputs

PIN CONFIGURATION

(TOP VIEW)



BLOCK DIAGRAM



TRUTH TABLE

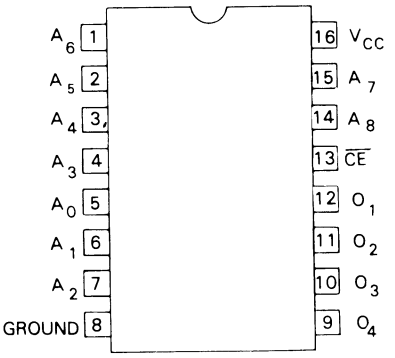
INPUTS				OUTPUTS
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

NOTE *The 100001716 is a Schottky device.*

100001717 through 100001730

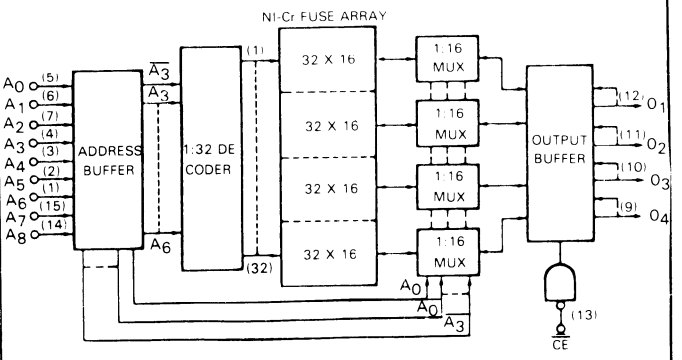
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the Programming Pin.

BLOCK DIAGRAM



These 2048-bit programmable read only memories are organized as 512 words by 4 bits. They include on-chip decoding, a chip enable input ($\overline{CE}$), and open collector

NOTE: *This is a Schottky device.*

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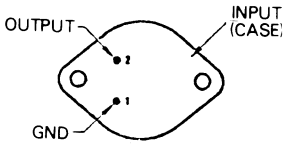
100001731

-5V, 1.5A, 15W, 5% Voltage Regulator

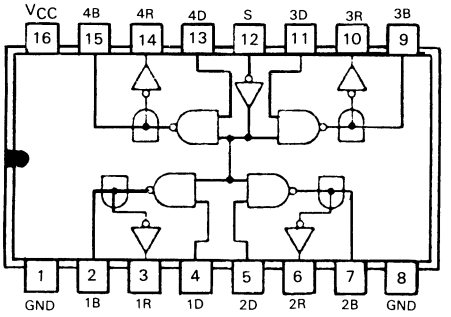
PIN CONFIGURATION



100001732

Quadruple Bus Tranceivers

PIN CONFIGURATION
(TOP VIEW)



FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

NOTE *The 10001732 is a Schottky device.*

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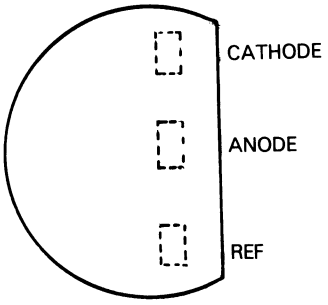
100001733

Adjustable Shunt Voltage Regulator +3 -30V

PIN CONFIGURATION

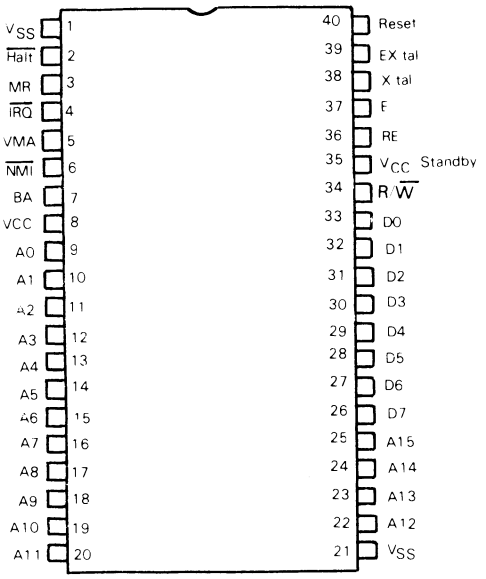


This is a three terminal adjustable regulator. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors.

100001734

8 Bit Microprocessor With Clock and RAM

PIN CONFIGURATION



This is a monolothic 8-bit microprocessor that contains all accumulators and registers, also an internal clock oscillator and driver on the same chip. In addition, it has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing Vcc standby, thus facilitating memory retention during a power-down situation.

- On-Chip Clock Circuit
- 128 X 8 Bit On-Chip RAM
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Addressing
- Interrupt Capability

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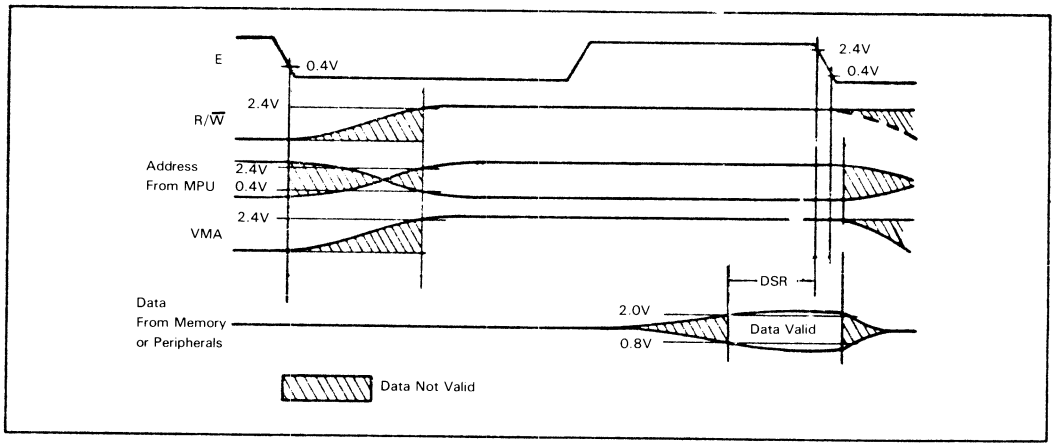
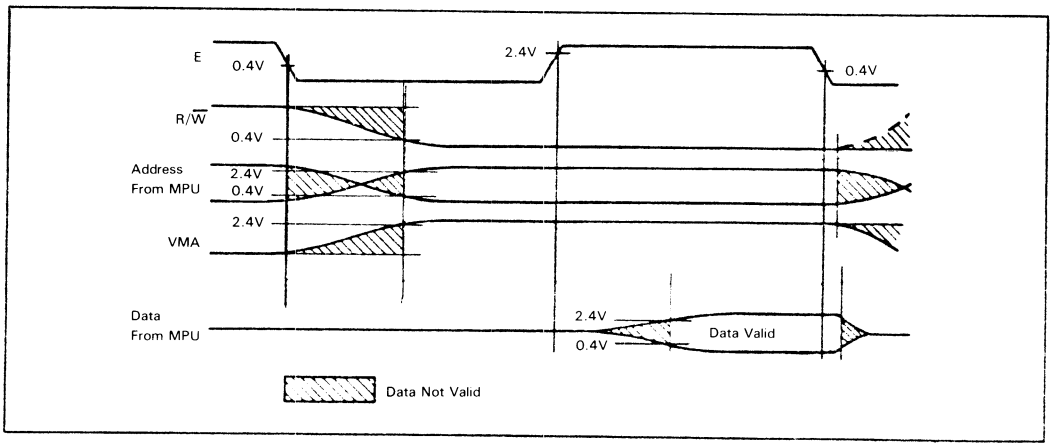
100001734 (cont.)

-READ DATA FROM MEMORY OR PERIPHERALS



-WRITE DATA IN MEMORY OR PERIPHERALS



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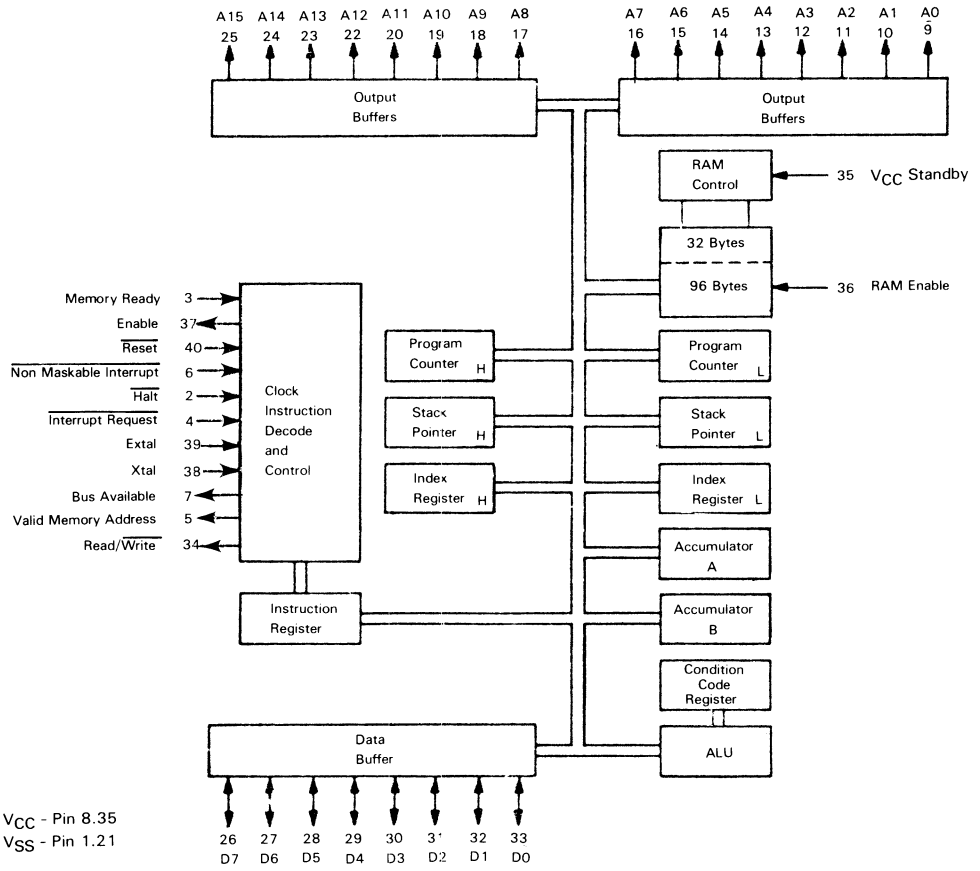
100001734 (Cont.)



The following is a summary of the device signals:

Address Bus (A0-A15) - Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 90 pF.

Data Bus (D0-D7) - Eight pins are used for the data bus. It is bidirectional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

Data Bus will be in the output mode when the internal RAM is accessed. This prohibits external data entering the MPU. It should be noted that the internal RAM is fully decoded from $0000 to $007F. External RAM at $0000 to $007F must be disabled when internal RAM is accessed.

$\overline{Halt}$ - When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high state. Valid Memory Address will be at a low state. The address bus will display the address of the next instruction.

Halt should be tied high if not used. This is good engineering design practice in general and necessary to insure proper operation of the part.

Read/$\overline{Write}$ (R/W) - This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). When the processor is halted, it will be in the logical one state. This ouput is capable of driving one standard TTL load and 90 pF.

Valid Memory Address (VMA) - This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

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100001734 (Cont.)

Bus Available (BA) - The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available (but not in a three-state condition). This will occur if the Halt line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit 1 = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Interrupt Request (IRQ) - This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The Halt line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while Halt is low.

Reset - This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the information in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ.

NOTE: If option 1 is chosen, Reset and RE pins can be tied together.

Reset, when brought low, must be held low at least three clock cycles. This allows the device adequate time to respond internally to the reset. This is independent of the 20 ms power-up reset that is required.

When Reset is released it MUST go through the low-to-high threshold without bouncing, oscillating, or otherwise causing an erroneous Reset (less than three clock cycles). This may cause improper MPU operation until the next valid Reset.

Non-Maskable Interrupt (NMI) - A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on NMI.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

Inputs IRQ and NMI are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

NMI should be tied high if not used. This is good engineering design practice in general and necessary to insure proper operation of the part.

Figure 12 is a flowchart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

RAM Enable (RE) - A TTL-compatible RAM enable input controls the on-chip RAM. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during a power-down situation. RAM enable must be low three cycles before VCC goes below 4.75 V during power-down.

RE should be tied to the correct high or low state if not used. This is good engineering design practice in general and necessary to insure proper operation of the part.

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100001734 (Cont.)

EXtal and Xtal - The device has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal. (AT cut.) A divide-by-four circuit has been added to the device so that a 4 MHz crystal may be used in lieu of a 1 MHz crystal for a more cost-effective system. Pin 39 of the device may be driven externally by a TTL input signal if a separate clock is required. Pin 38 is to be left open in this mode.

Memory Ready (MR) - MR is a TTL compatible input control signal which allows stretching of E. When MR is high, E will be in normal operation. When MR is low, E may be stretched integral multiples of half periods, thus allowing interface to slow memories.

Enable (E) - This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL compatible clock. This clock may be conditioned by a Memory Ready Signal.

VCC Standby - This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed.

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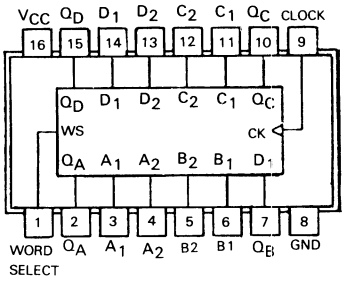
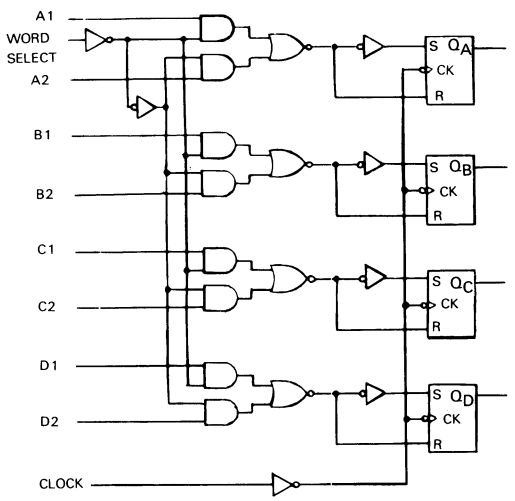
100001735

Quadruple 2-Input Multiplexer With Storage

PIN CONFIGURATION



BLOCK DIAGRAM



Dynamic input activated by a transition from a high level to a low level.

FUNCTION TABLE

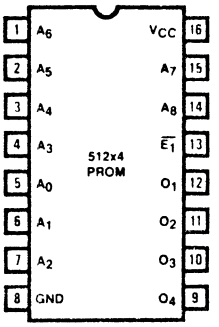
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

NOTE *The 100001735 is a low power Schottky device.*

100001742

512 X 4 PROM

PIN CONFIGURATION



This 2048-bit programmable read only memory has open collector outputs. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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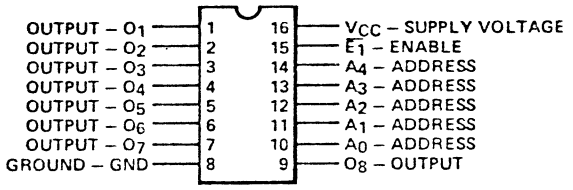
100001746

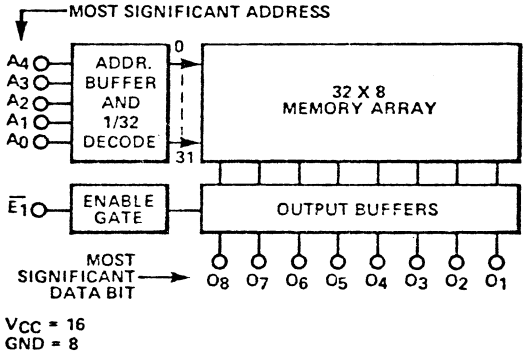
it Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

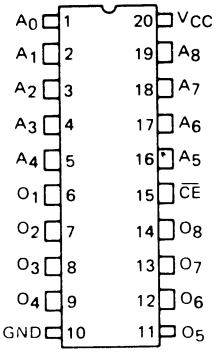
The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

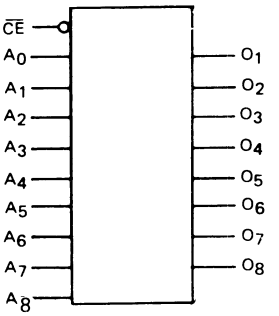
NOTE *The 100001746 is a Schottky device.*

100001747 and 100001748

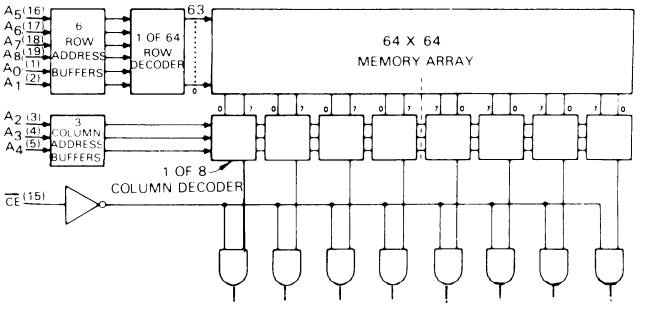
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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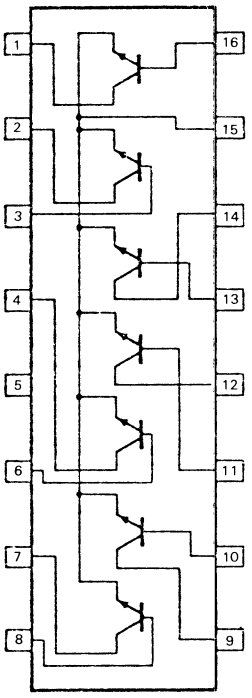
100001749

Seven Transistor Array

PIN CONFIGURATION

N PACKAGE



This device consists of seven high current silicon n-p-n transistors on a common monolithic substrate.

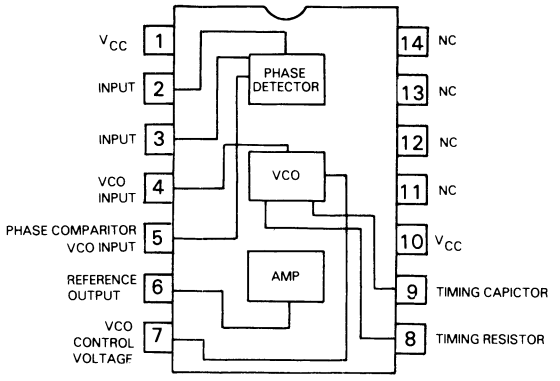
It is connected in a common-emitter configuration.

NOTE: *The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (pin 5) should be maintained at either d.c. or signal (a.c.) ground.*

100001750

Voltage Controlled Oscillator

PIN CONFIGURATION



This is a general purpose phase locked loop containing a stable, highly linear voltage controlled oscillator for low distortion demodulation. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. It is specified for operation over the 0°C to 70°C temperature range and has TTL and DTL compatible phase detector input and square wave output.

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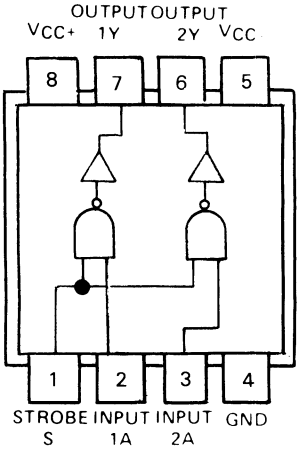
100001751

Dual Line Driver

PIN CONFIGURATION

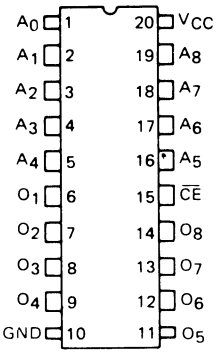


$Y = \overline{AS}$

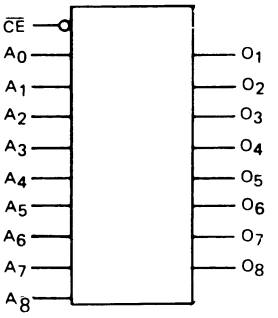
100001752 through 100001768

512 x 8-Bit Bipolar PROM

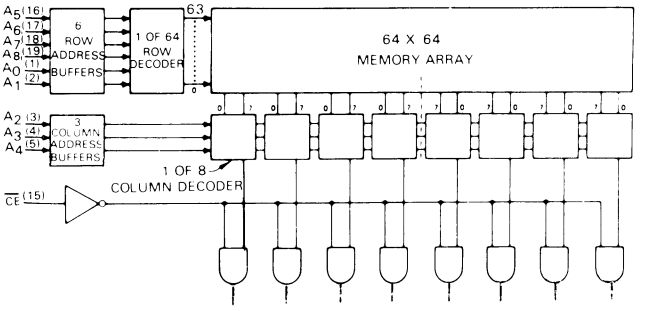
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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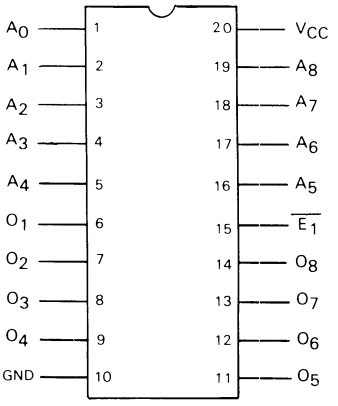
100001766 through 100001768

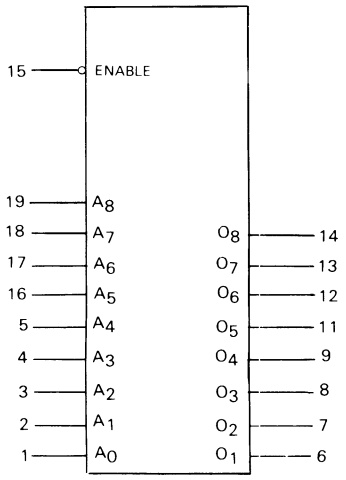
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



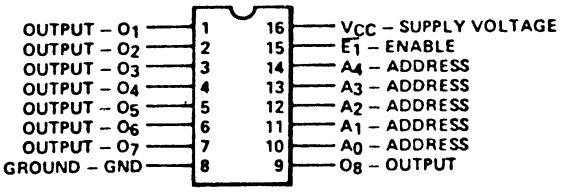
This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

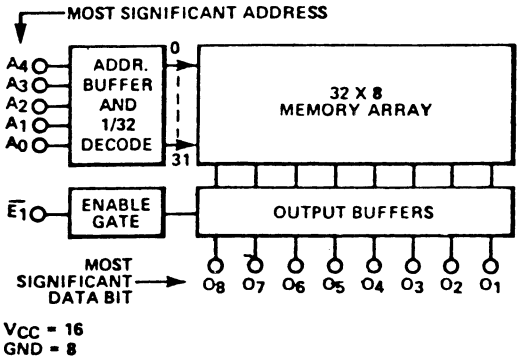
100001769

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 0_1 through A_8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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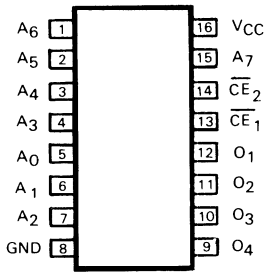
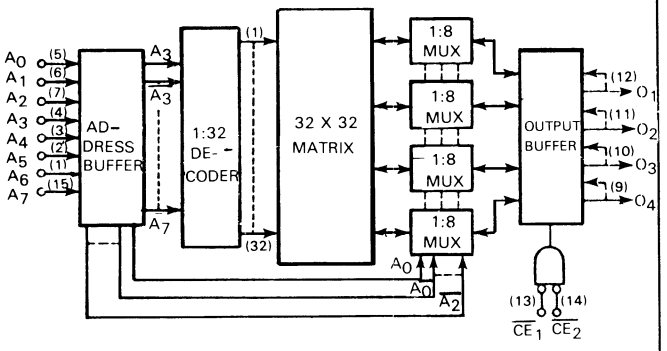
100001770

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

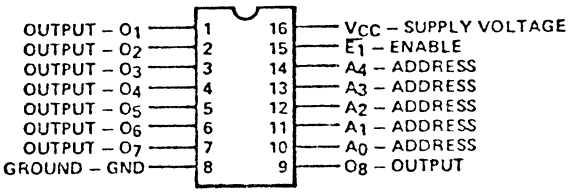
$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

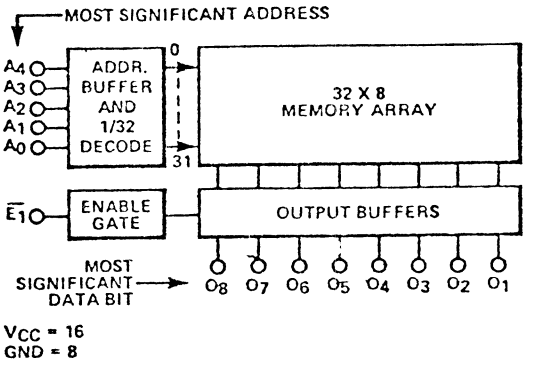
100001771

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{(E_1)}$, and tri-state outputs.

The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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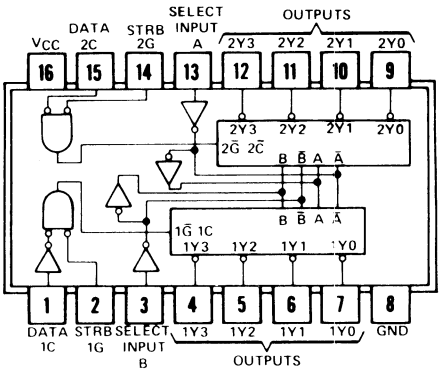
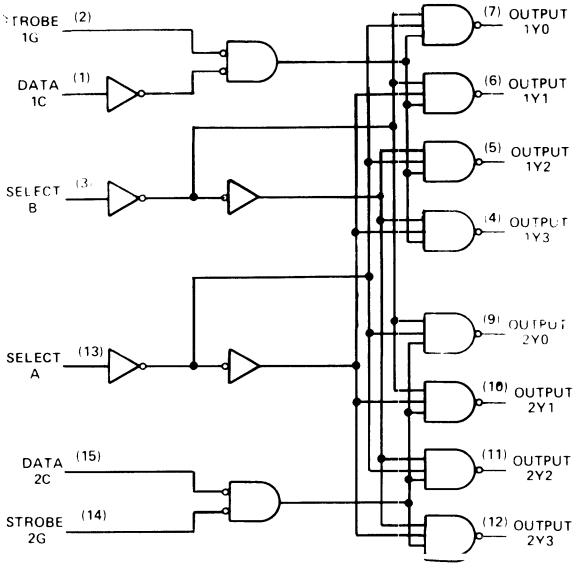
100001775

Dual 2-Line-To-4-Line Decoder /Demultiplexer Open Collector Outputs

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

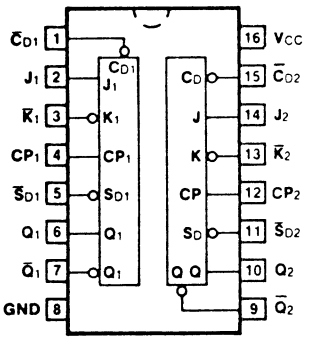
†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

NOTE *The 100001775 is a low power Schottky device*

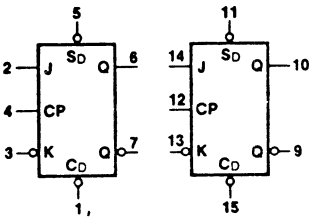
100001777

Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops With Preset And Clear

PIN CONFIGURATION



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

TRUTH TABLE

INPUTS		OUTPUTS	
@ t_n		@ $t_n + 1$	
J	K	Q	Q
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

The 100001777 has two high speed independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform.

NOTE: *This is a low power Schottky device.*

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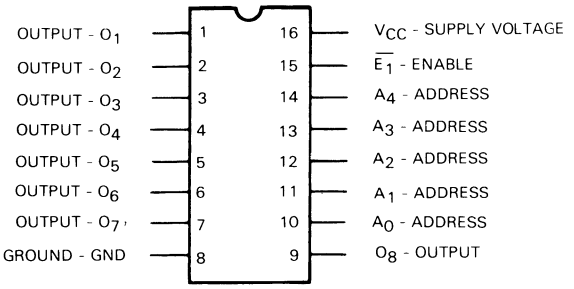
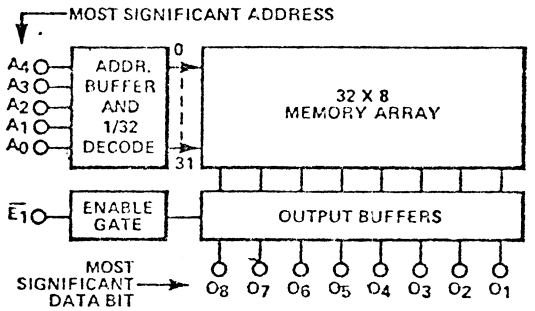
100001778 and 100001779

32 x 8-Bit PROM



BLOCK DIAGRAM



VCC = 16
GND = 8

This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable input ($\overline{E1}$), and three-state outputs.

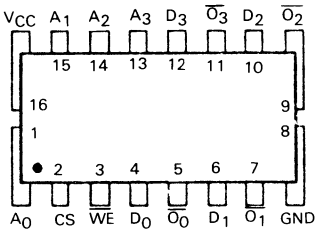
The memory is addressed with inputs A0 through A4 which select one of 32 words. To enable the ouputs for a readout, enable $\overline{E1}$ must be low. If the enable is high, the outputs are held off permitting wire ORing of the three-state outputs of several packages.

NOTE: *This is a Schottky device.*

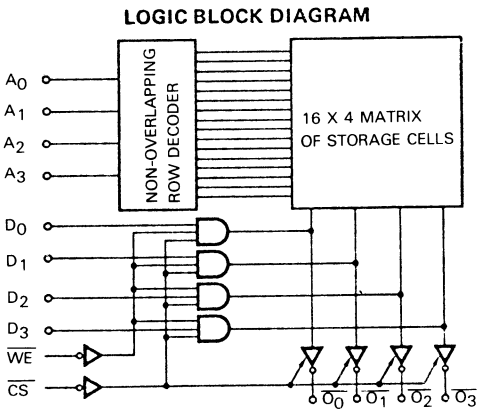
100001781

16 x 4 Bit RAM

PIN CONFIGURATION



LOGIC BLOCK DIAGRAM



This 64-bit random access memory is organized as a 16 word by 4-bit array. $\overline{CS}$ is the active low chip select. The active low write line is $\overline{WE}$ when the device is selected.

NOTE: *This is a Schottky device.*

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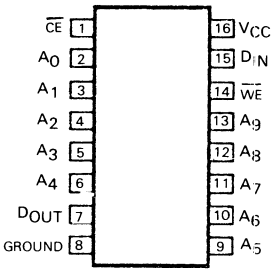
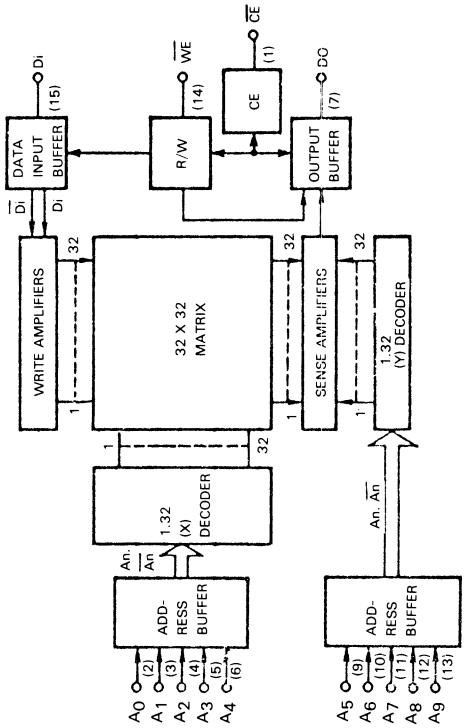
100001783

1024x1 Bit Static RAM

PIN CONFIGURATION



BLOCK DIAGRAM



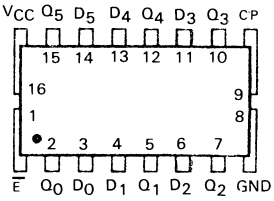
This 1024-bit, fully decoded random access memory is compatible with DTL and TTL logic families. It has tri-state output.

With $\overline{WE}$ and $\overline{CS}$ held low, the data at D in is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ is held low.

100001784

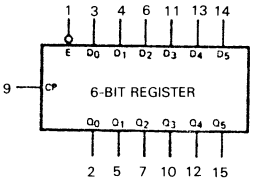
6-Bit Storage Register

PIN CONFIGURATION

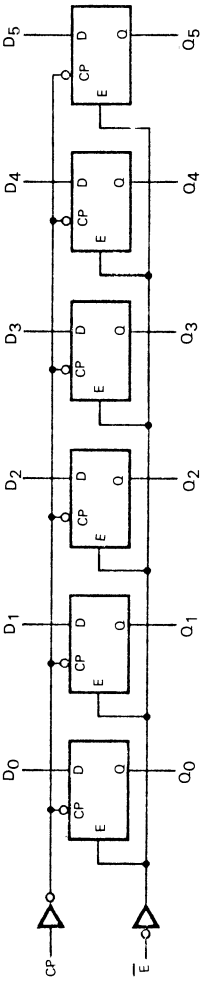


The chip is enabled when $\overline{E}$ is low.

LOGIC SYMBOL



BLOCK DIAGRAM



NOTE: *The 100001784 is a Schottky device.*

This is a 6-bit high speed Schottky register with a buffered common register enable.

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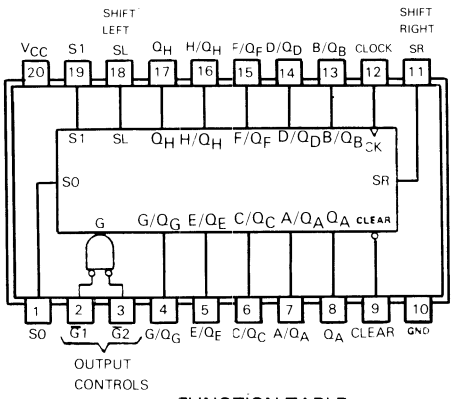
100001785

8-Bit Universal Shift/Storage Registers

PIN CONFIGURATION

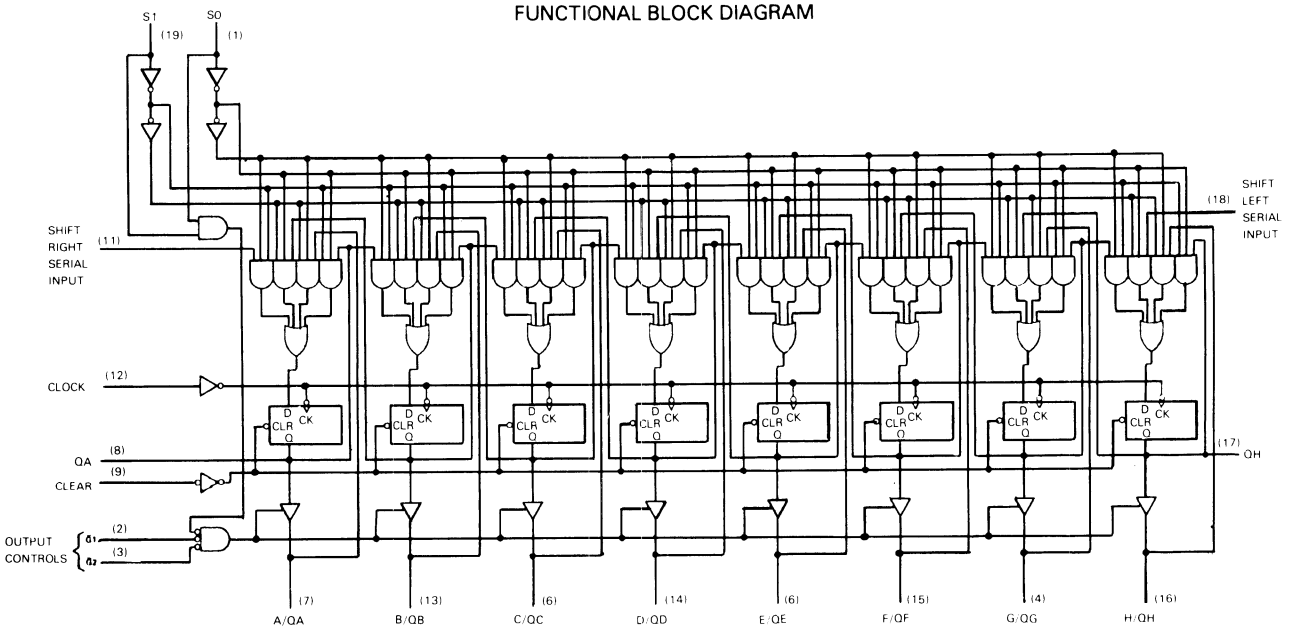


FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

FUNCTIONAL BLOCK DIAGRAM



These Schottky 8-bit universal registers feature multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20 pin package. The tri-state outputs drive bus lines directly.

NOTE: *This is a Schottky device.*

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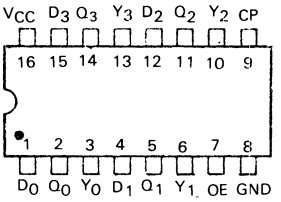
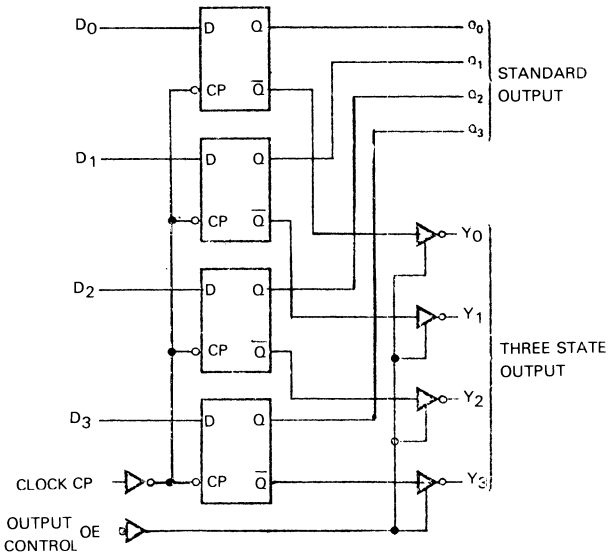
100001786

Quad D Register with Standard and Three State Ouputs

PIN CONFIGURATION





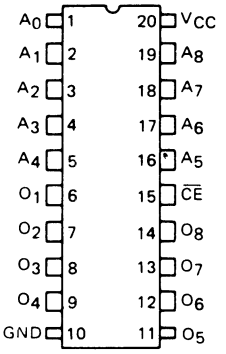
This 4-bit, high speed Schottky register consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW to HIGH transition of the clock.

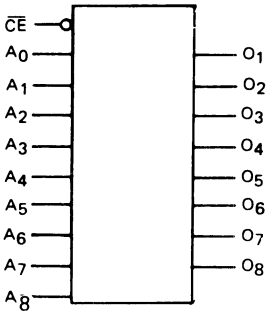
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" **(OE)** input is LOW. When the **OE** input is high, the Y outputs are in the high-impedance state.

100001788 through 100001792

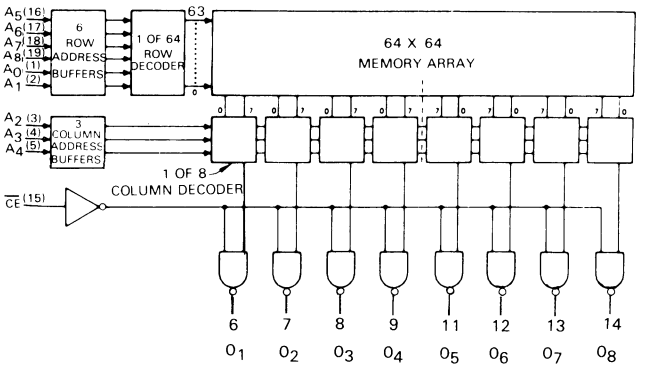
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

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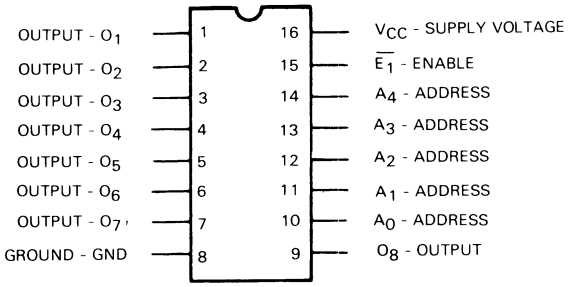
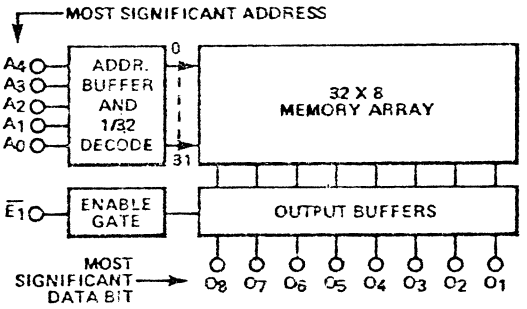
100001794 and 100001795

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE *100001794 and 100001795 are Schottky devices.*

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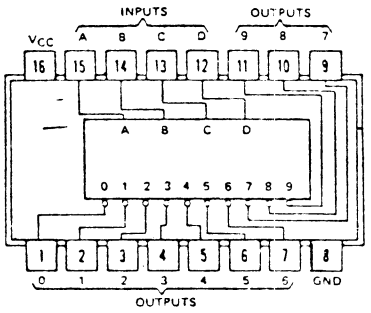
100001802

4-Line to 10-Line Decode
BCD to Decimal

PIN CONFIGURATION
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

NO.	BCD INPUT				EXCESS-3 INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	H	H	H

This is a multipurpose decoder. For any valid input combination, one- and only one - output is low.

For all invalid input combinations, all outputs are high.

The device accepts four BCD inputs and provides 10 mutually exclusive outputs.

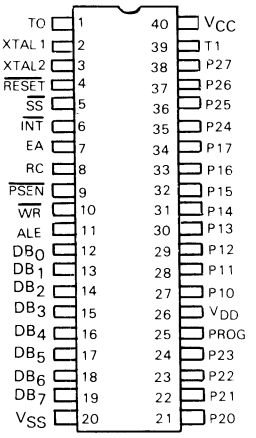
It is TTL and CMOS compatible.

NOTE *The 100001802 is a low power Schottky device*

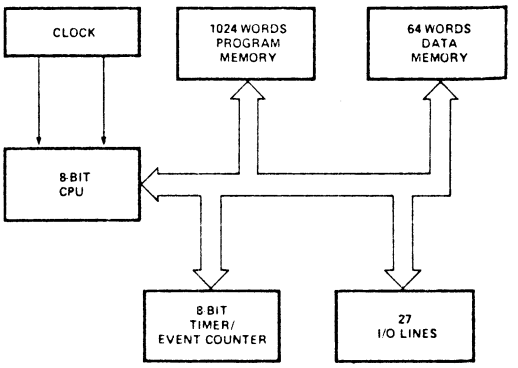
100001803

User Programmable/Erasable EPROM

PIN CONFIGURATION



BLOCK DIAGRAM



This device is a 8-bit parallel computer fabricated on a single silicon chip using an N-channel silicon gate MOS process.

It contains a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to onboard oscillator and clock circuits.

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100001803 (cont.)

RD	8	Output strobe activated during a BUS read Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{\text{RESET}}$	4	Input which is used to initialize the processor. (Non TTL VIH)
$\overline{\text{WR}}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{\text{PSEN}}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL VIH)
XTAL2	3	Other side of crystal input.
VSS	20	Circuit GND potential
VDD	26	+5V during operation.
VCC	40	Main power supply; +5V during operation.
PROG	25	N.C.
P10-P17	27-34	8-bit quasi-bidirectional port.
Port 1		
P20-P27	21-24	8-bit quasi-bidirectional port.
Port 2	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{\text{RD}}$, $\overline{\text{WR}}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{\text{PSEN}}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.
TO	1	Input pin testable using the conditional transfer instructions JTO and JNTO. TO can be designated as a clock output using ENTO CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{\text{INT}}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

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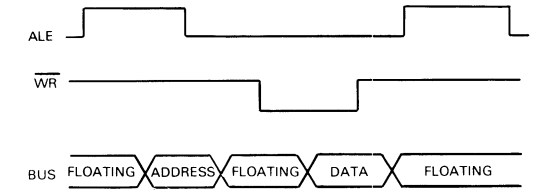
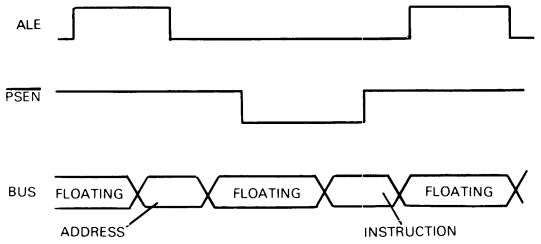
100001803 (cont.)

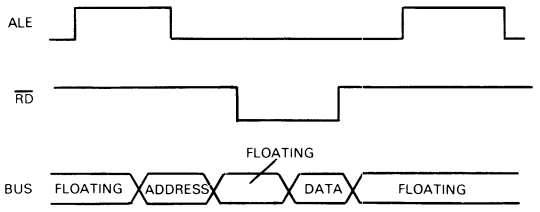
Write to External Data Memory



Instruction Fetch From External Program Memory



Read From External Data Memory

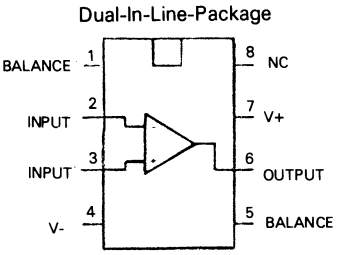


100001804

JFET OP AMP

PIN CONFIGURATION

Dual-In-Line-Package



TOP VIEW

This device incorporates high voltage JFETs on the same chip with standard bipolar transistors. It has low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. Input voltage range is ± 20.

It has:

- High slew rate
- Wide bond width
- Fast settling time
- Low voltage and current noise
- Low I/F noise corner

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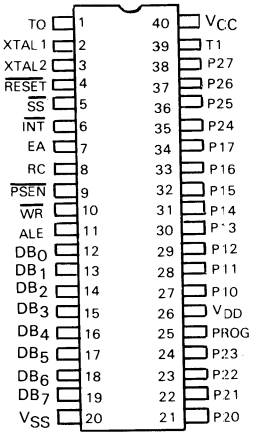
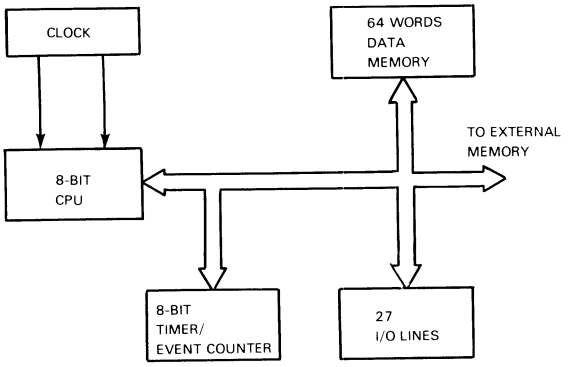
100001807

8-Bit Microcomputer

PIN CONFIGURATION



BLOCK DIAGRAM



This device is a 8-bit parallel computer fabricated on a single silicon chip using an N-channel silicon gate MOS process.

It contains a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to onboard oscillator and clock circuits.

This microprocessor is an efficient controller as well as an arithmetic processor handling capability as well as facilities for both binary and BCD arithmetic.

(cont.)

VSS	20	Circuit GND potential
VDD	26	+5V during operation.
VCC	40	Main power supply; +5V during operation.
PROG	25	N.C.
P10-P17	27-34	8-bit quasi-bidirectional port.
Port 1		
P20-P27	21-24	8-bit quasi-bidirectional port.
Port 2	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JTO and JNTO. TO can be designated as a clock output using ENTO CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

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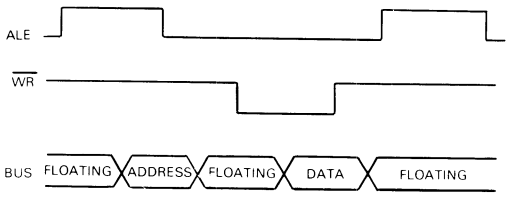
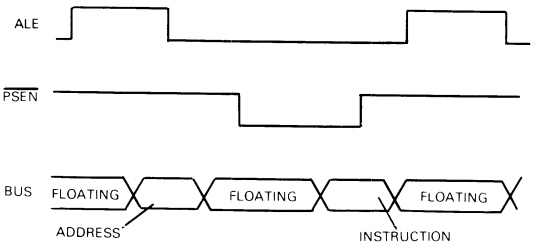
100001807 (cont.)

RD	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{\text{RESET}}$	4	Input which is used to initialize the processor. (Non TTL VIH)
$\overline{\text{WR}}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{\text{PSEN}}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL VIH)
XTAL2	3	Other side of crystal input.

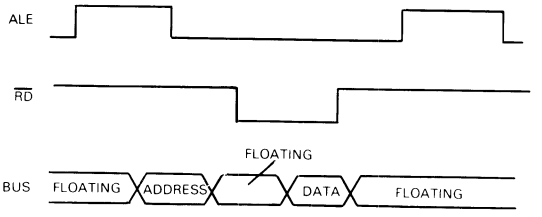
Write to External Data Memory



Instruction Fetch From External Program Memory



Read From External Data Memory



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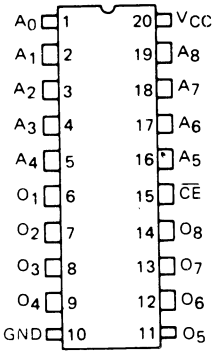
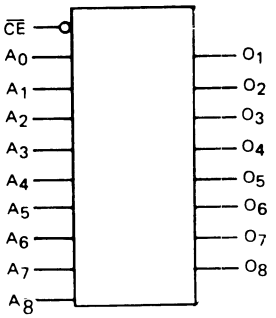
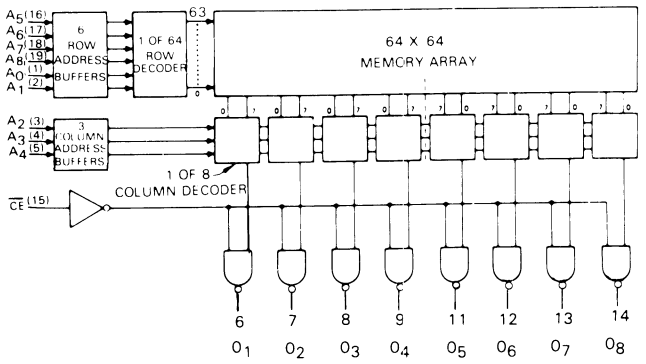
100001808

512 x 8-Bit Bipolar PROM

PIN CONFIGURATION







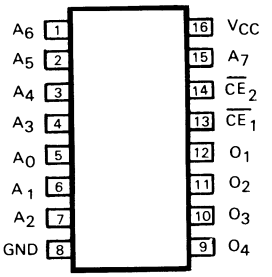
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

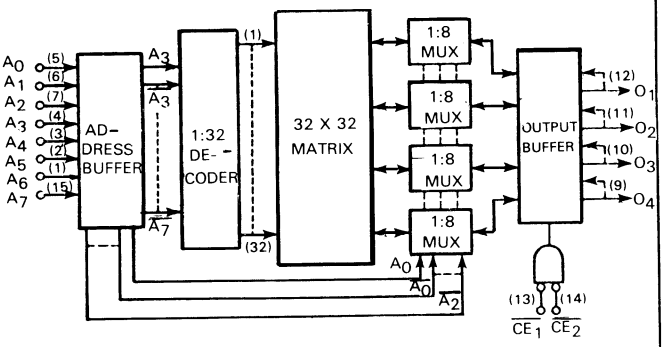
NOTE: *This is a Schottky device.*

100001809

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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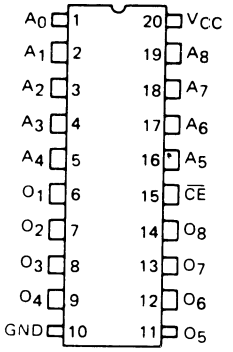
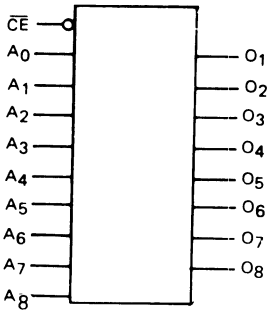
100001810

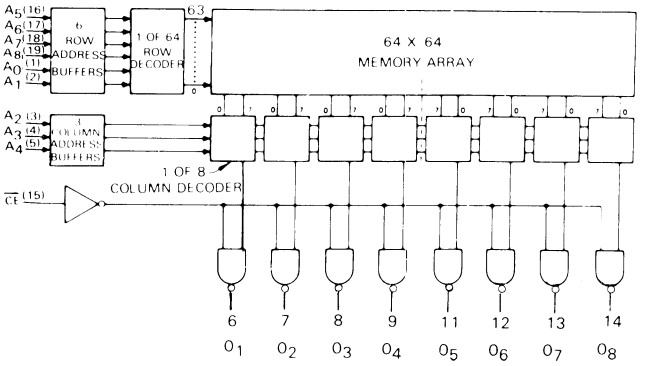
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





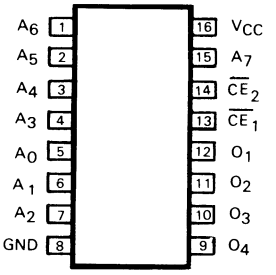
BLOCK DIAGRAM

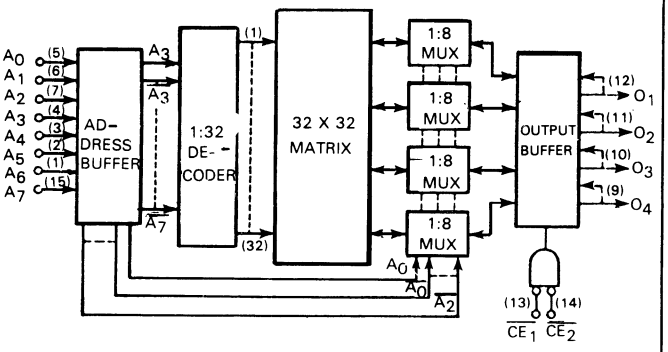


100001811

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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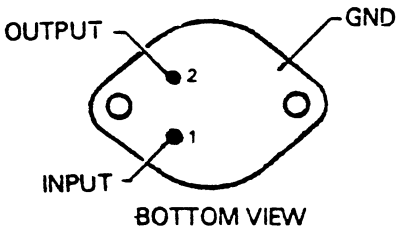
100001812

+12V, 3 Amp, 5% Regulator

PIN CONFIGURATION

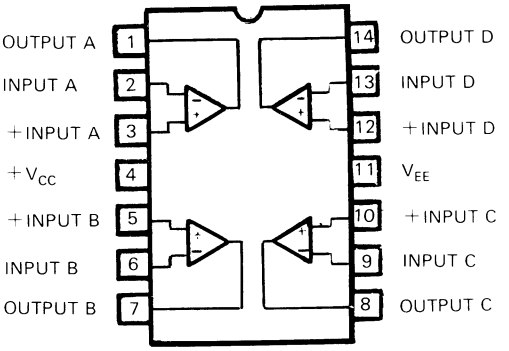


BOTTOM VIEW

100001814

Quad JFET-Input Operational Amplifier

Connection Diagram



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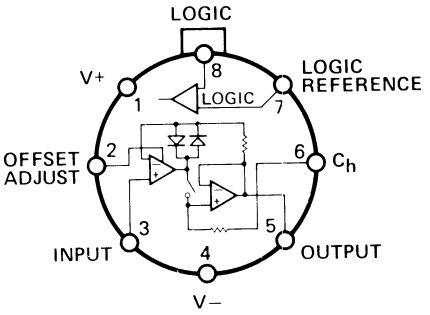
100001815

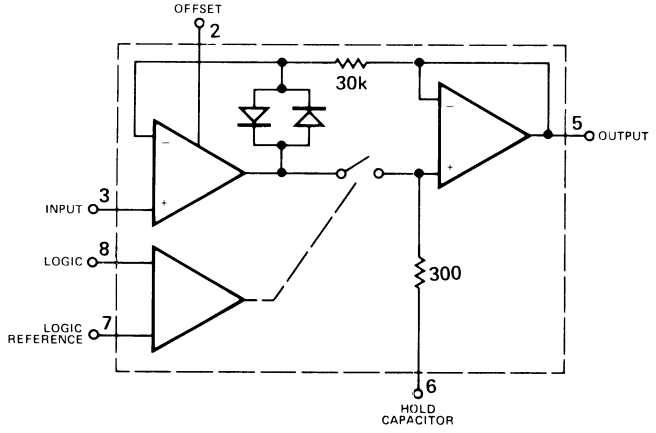
Sample And Hold

PIN CONFIGURATION

Top View



BLOCK DIAGRAM



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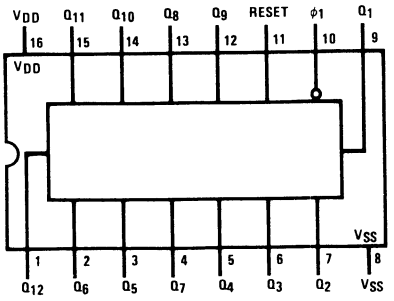
100001816

12-Bit Binary Counter

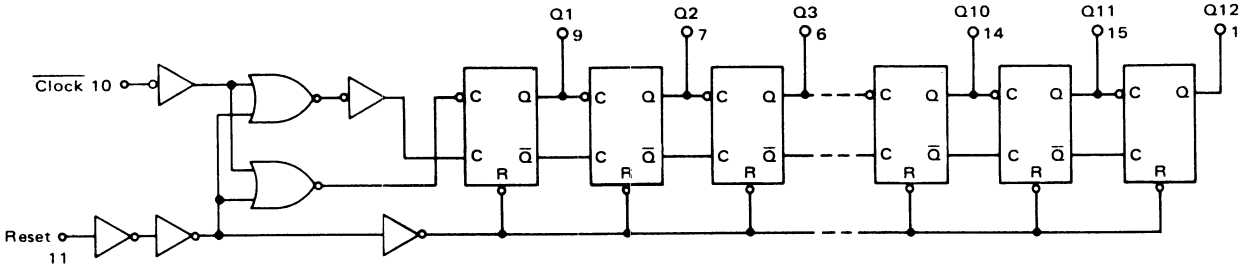
PIN CONFIGURATION



CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

BLOCK DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

This 12 stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. It is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. 13 MHz is a typically counting rate @ V_{DD} = 15V. It is TTL compatible.

NOTE: *The 100001816 is a CMOS device.*

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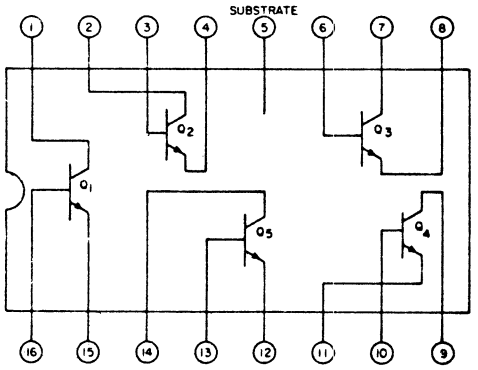
100001817

General Purpose N-P-N Transistor Array

PIN CONFIGURATION



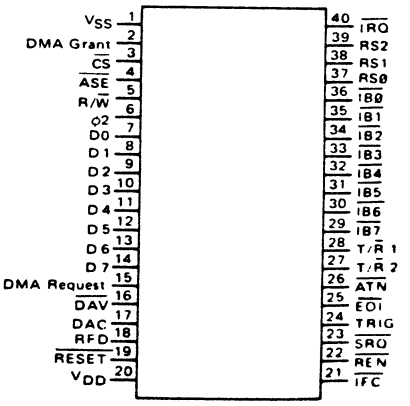
The 100001817 is an array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e., 1mA) for applications in which offset parameters are of special importance.

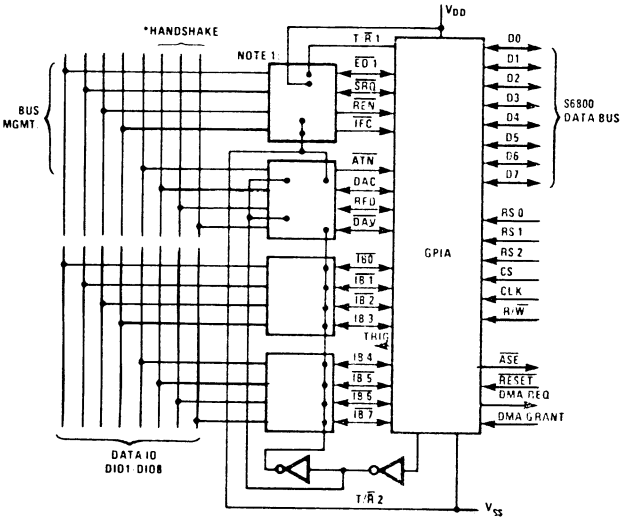
NOTE: *The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (pin 5) should be maintained at either d.c. or signal (a.c.) ground.*

100001819

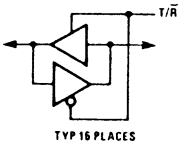
General Purpose Interface Adapter

PIN CONFIGURATION





NOTE 1:



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100001819 (cont.)

This device provides the means to interface between the IEEE488 standard instrument bus and the S6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

It will automatically handle all the handshake protocol needed on the instrument bus.

The IEEE488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communications to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive data concurrently.

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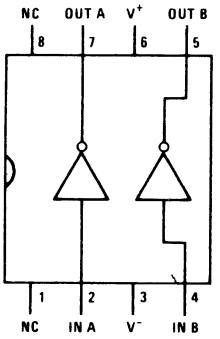
100001821

Two Phase MOS Clock Driver

Dual-In-Line Package

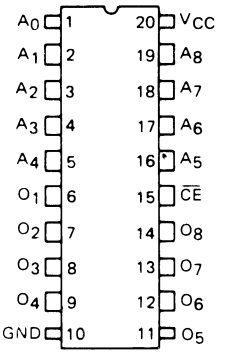


This is a monolothic high speed two phase MOS clock driver and interface circuit. The circuit design provides both high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels.

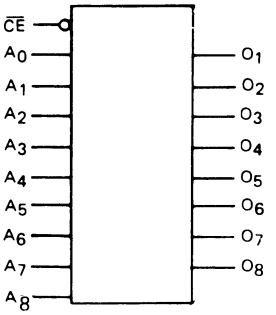
100001825 and 100001826

512 x 8-Bit Bipolar PROM

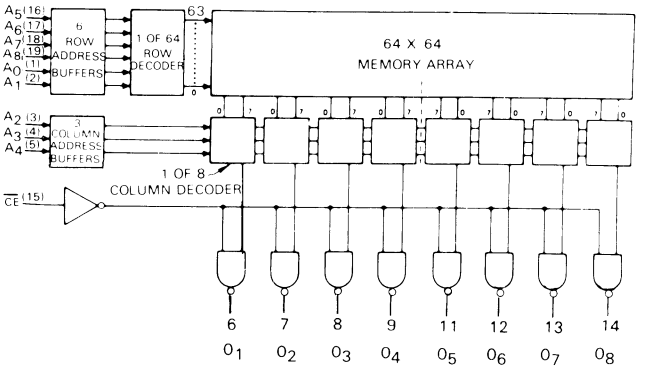
PIN CONFIGURATION



Pin 15 is the programming pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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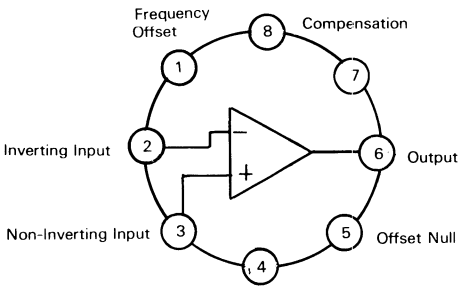
100001827

High Speed, Fast Settling Operational Amplifier.

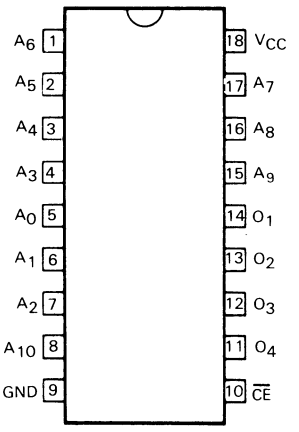
PIN CONFIGURATION
(TOP VIEW)



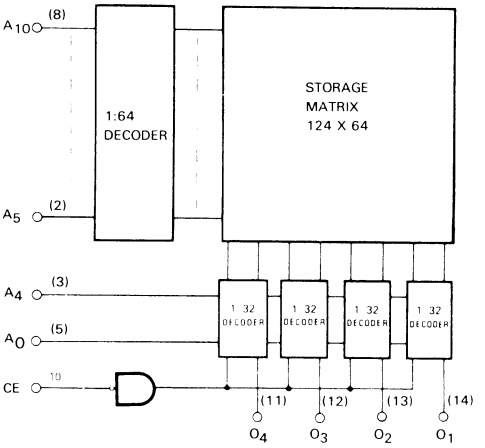
100001828

2048 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 8192-bit bipolar field programmable memory has tri-state output. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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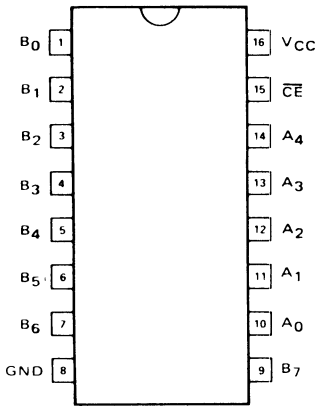
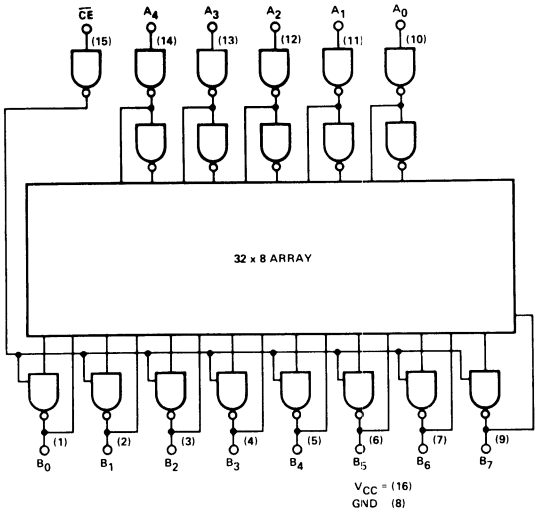
100001829

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



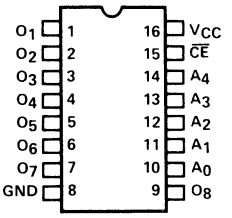
This 256-bit bipolar read only memory has tri-state outputs. It is TTL compatible. This chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001830

32 X 8 Bit PROM

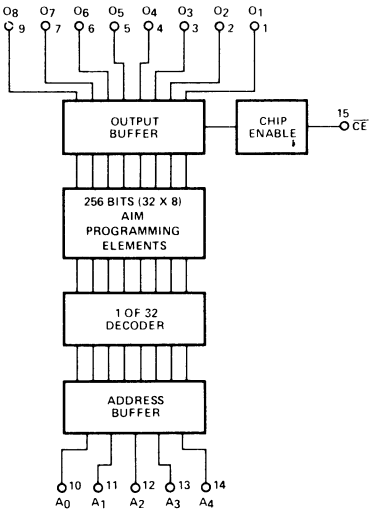
PIN CONFIGURATION



TOP VIEW

Pin 15 is the Programming Pin.

BLOCK DIAGRAM



TRUTH TABLE

ADDRESS INPUTS A_0–A_4	$\overline{CE}$	ANY OUTPUT O_1–O_8
Any one of 32 possible addresses.	L	H–if the bit uniquely associated with this output and address has been electrically programmed. L–if it has not been programmed.
Any one of 32 possible addresses.	H	All outputs are forced to a high impedance state regardless of the address.

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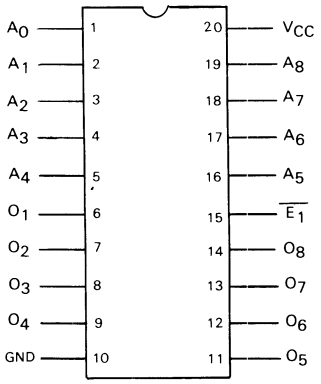
100001831 through 100001838

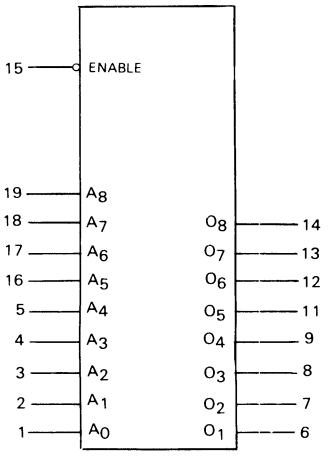
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



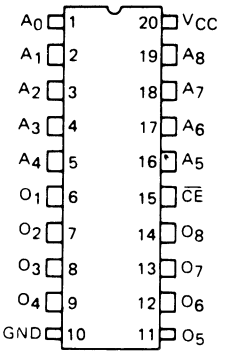
This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

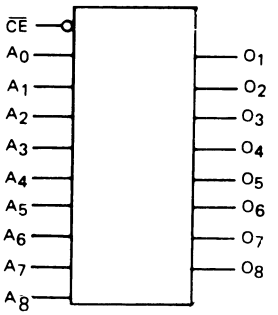
100001839 and 100001840

512 x 8-Bit Bipolar PROM

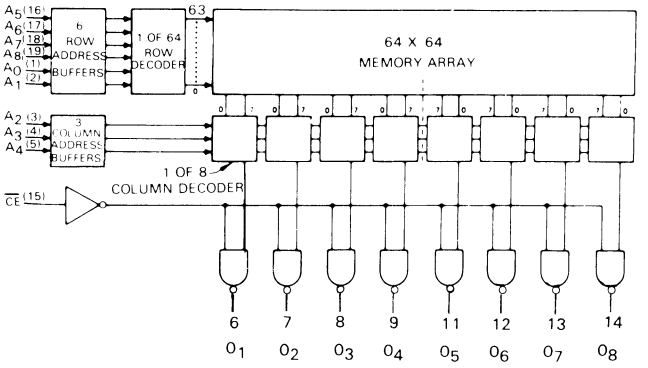
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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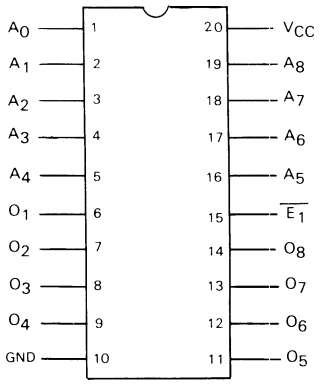
100001841 and 100001842

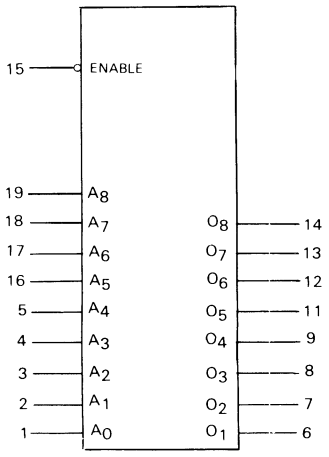
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



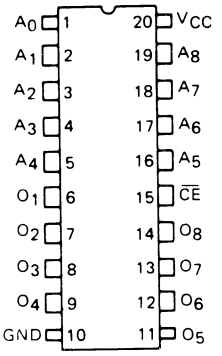
This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

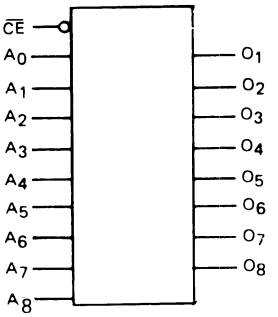
NOTE: *This is a Schottky device.*

100001843 and 100001844

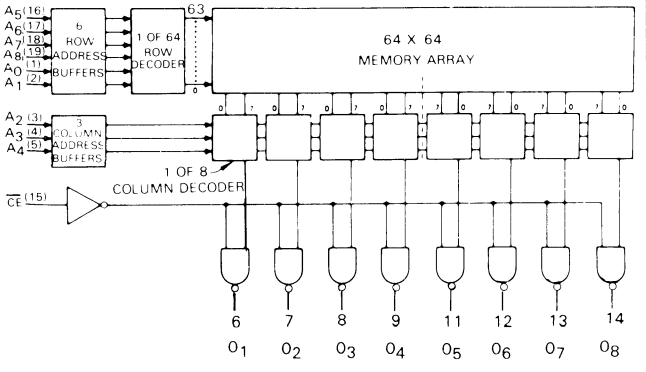
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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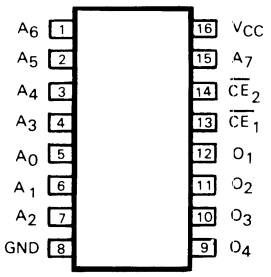
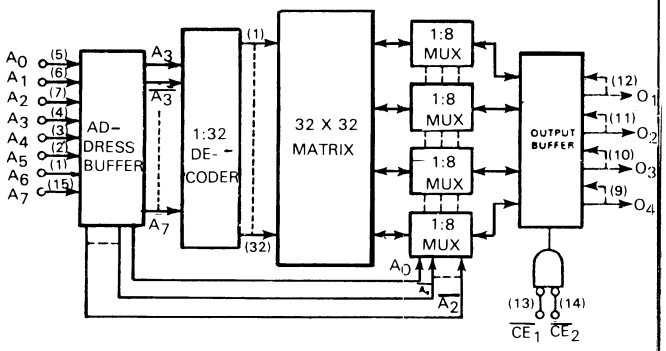
100001845

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This integrated circuit is a high speed electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

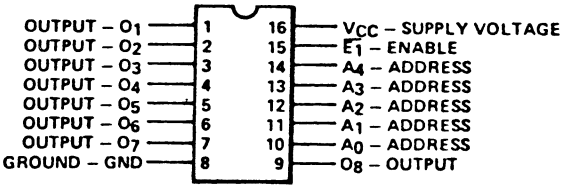
The same address inputs are used for both programming and reading.

NOTE: *This is a Schottky device.*

100001846 through 100001849

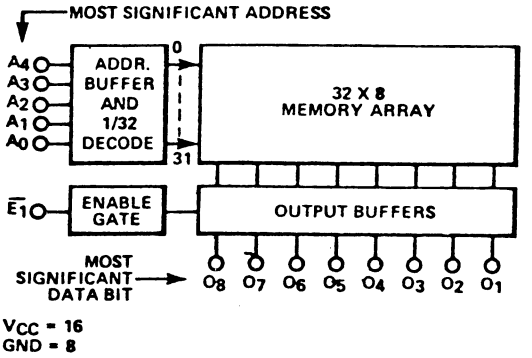
32 x 8-Bit Bipolar ROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

BLOCK DIAGRAM



This 256-bit bipolar programmable read only memory has open collector output.

The chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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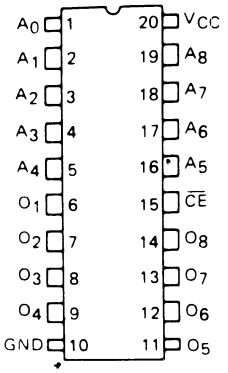
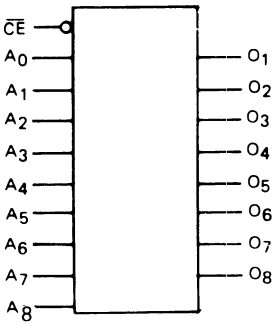
100001850 through 100001852

512 x 8-Bit Bipolar PROM

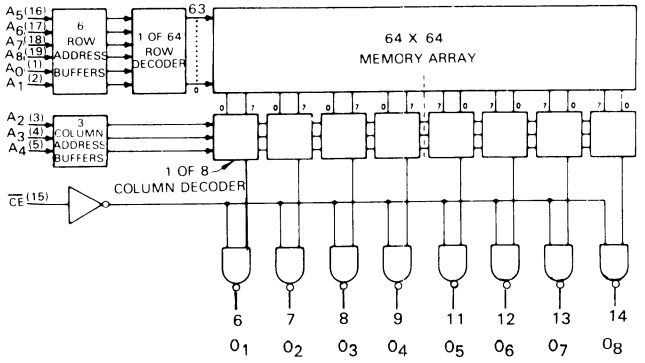
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



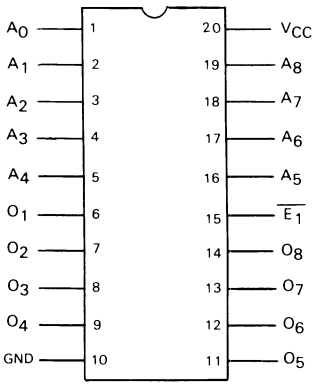
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001853

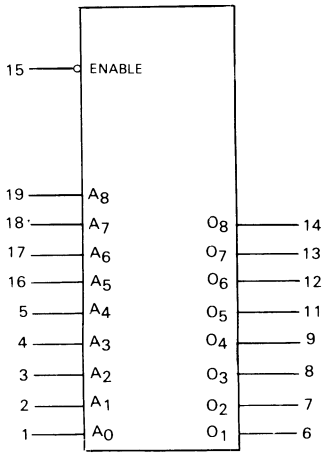
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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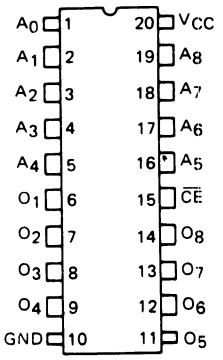
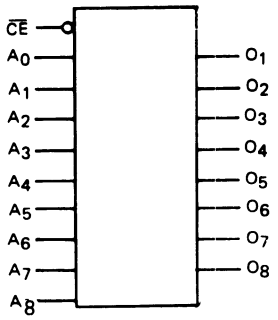
100001854 through 100001857

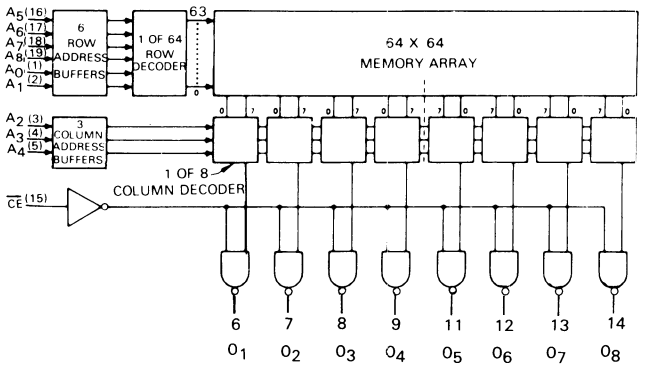
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



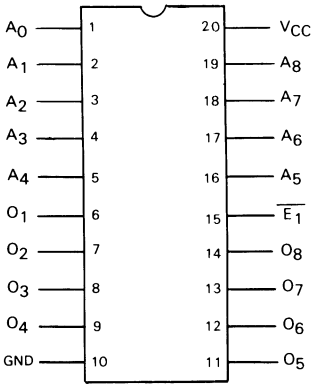
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001858 and 100001859

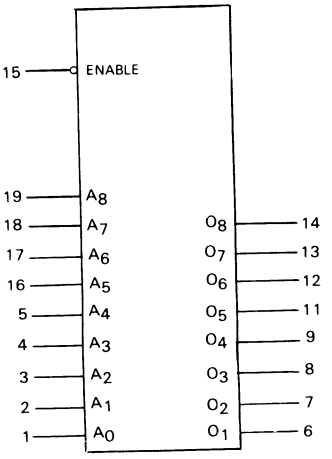
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

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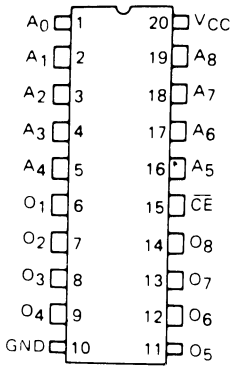
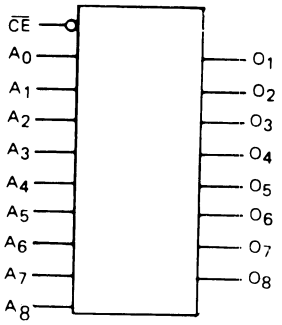
100001860

512 x 8-Bit Bipolar PROM

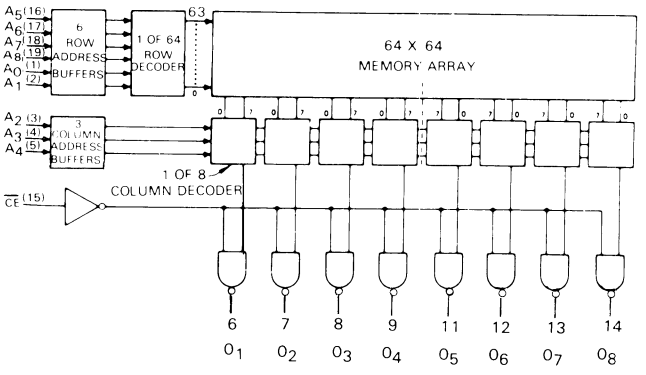
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



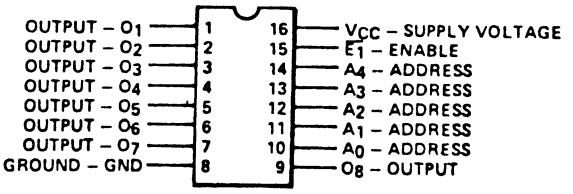
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001861 and 100001862

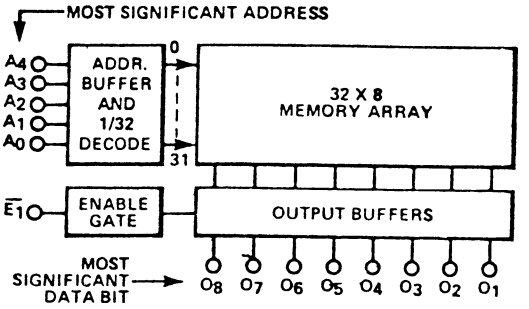
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and three-state outputs.

The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE: *This is a Schottky device.*

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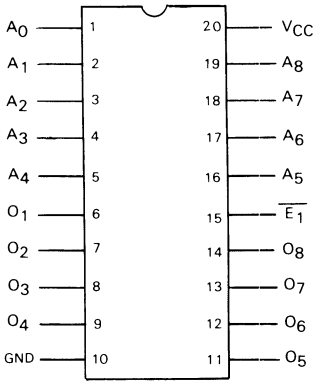
100001863

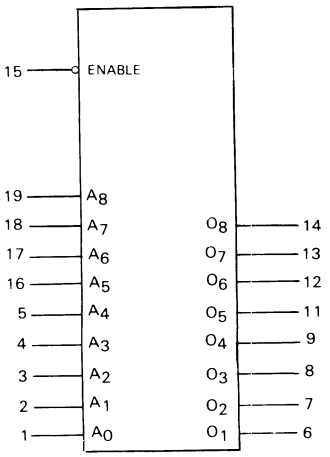
512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.

LOGIC SYMBOL



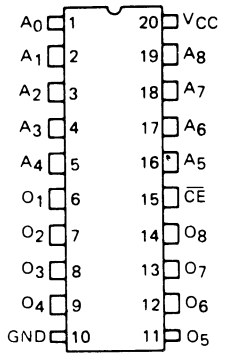
This 4096-bit programmable read only memory has open collector output. It is TTL compatible. This chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

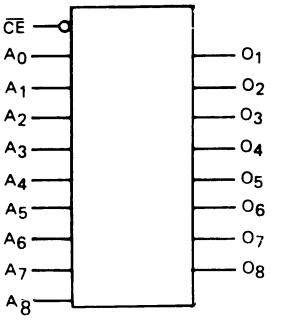
100001864 through 100001866

512 x 8-Bit Bipolar PROM

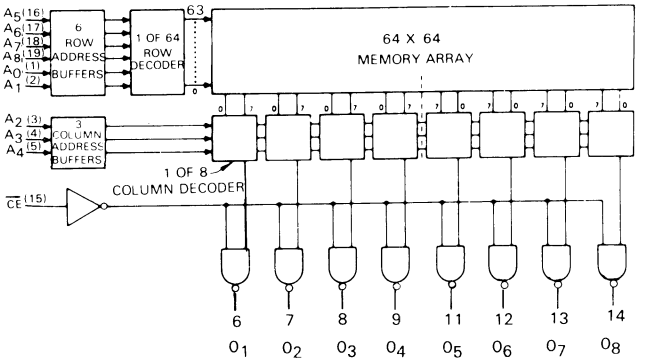
PIN CONFIGURATION



Pin 15 is the programming pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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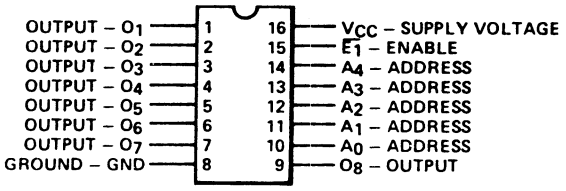
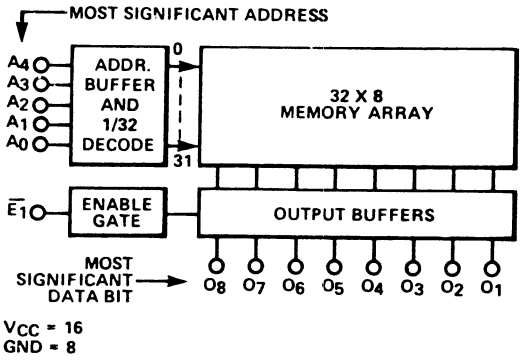
100001867

32 x 8-Bit PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable ($\overline{E1}$), and three-state outputs.

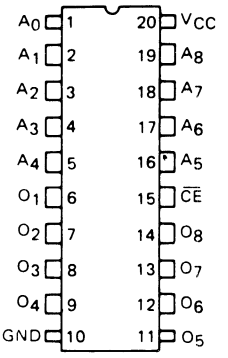
The memory is addressed with inputs A0 through A4, which select one of 32 words. A word is read out on the outputs 01 through A8. The enable $\overline{E1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the three-state outputs of several packages.

NOTE *This is a Schottky device.*

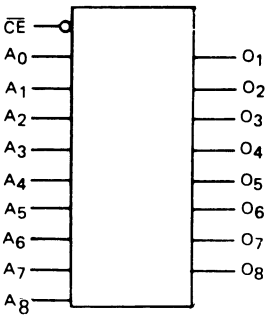
100001868

512 x 8-Bit Bipolar PROM

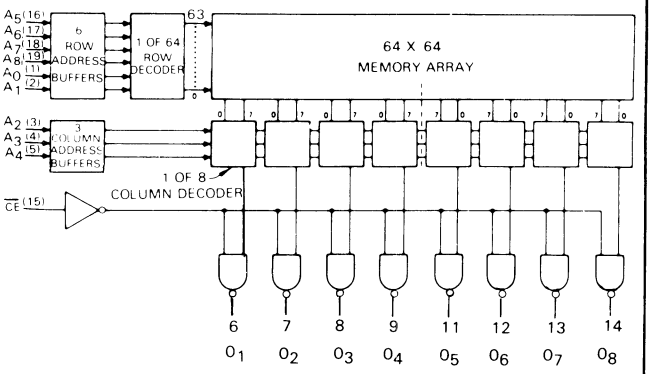
PIN CONFIGURATION



Pin 15 is the programming pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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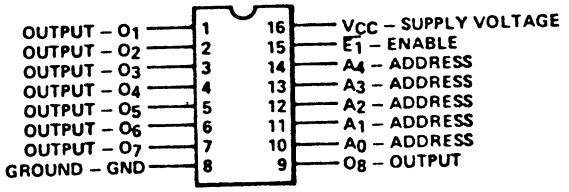
100001869 through 100001872

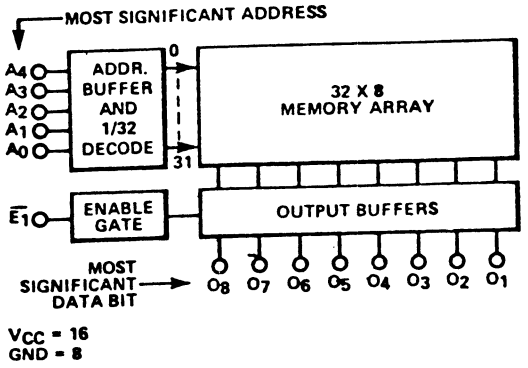
32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



To enable the device, $\overline{E_1}$ must be LOW.

BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 0_1 through A_8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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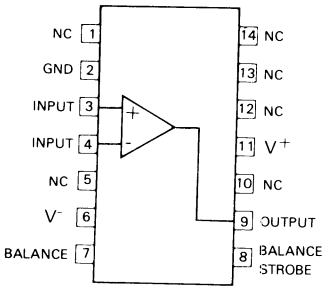
100001875

Voltage Comparator

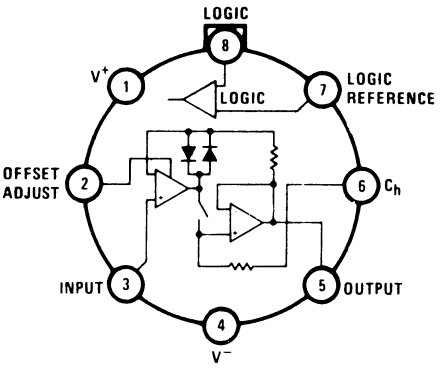
PIN CONFIGURATION



100001876

Monolothic Sample and Hold Circuit

PIN CONFIGURATION



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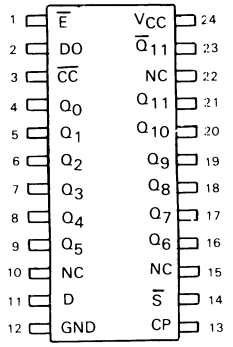
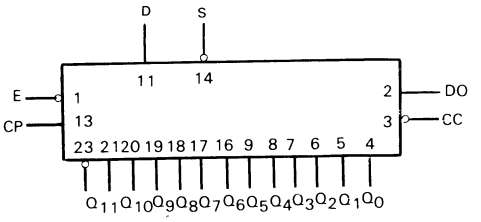
100001879

Twelve-Bit Successive Approximation Register

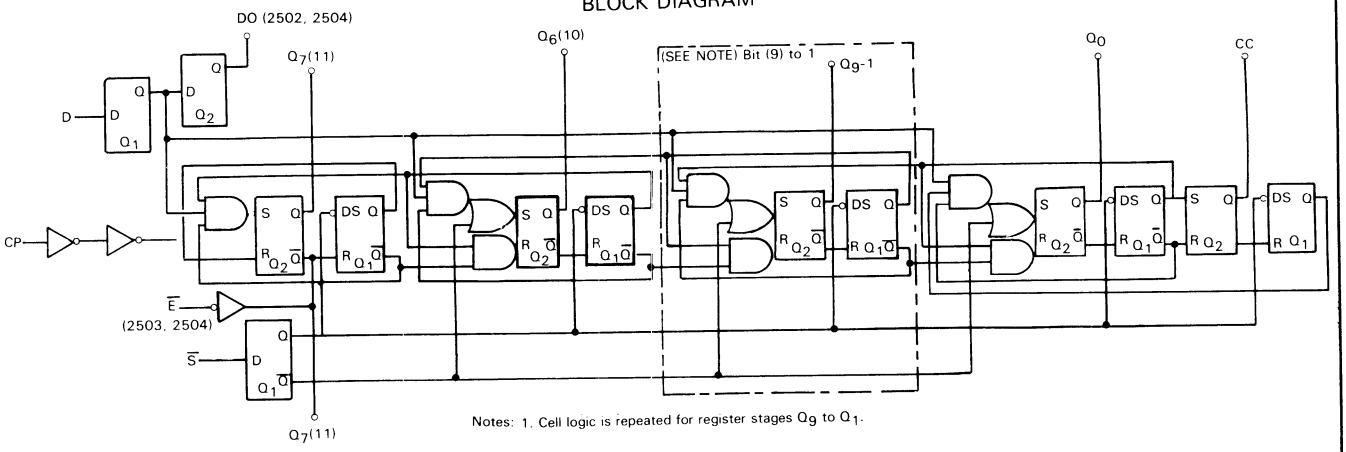
PIN CONFIGURATION



LOGIC DIAGRAM



BLOCK DIAGRAM



Notes: 1. Cell logic is repeated for register stages Q_9 to Q_1.

This is a 12-bit TTL Successive Approximation Register. The register contains all the digital control and storage necessary for successive approximation analog-to-digital conversion. It can also be used in digital systems as the control and storage element in recursive digital routines.

The register consists of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally, the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit, the next less significant bit is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state Q(11) LOW, and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q(11) register bit and the Q(10) register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH

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100001879 (cont.)

transition data enters the Q(10) register bit and Q(9) is set to LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion, the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the Q(11) bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used, the E input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

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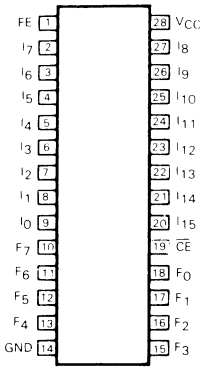
100001900

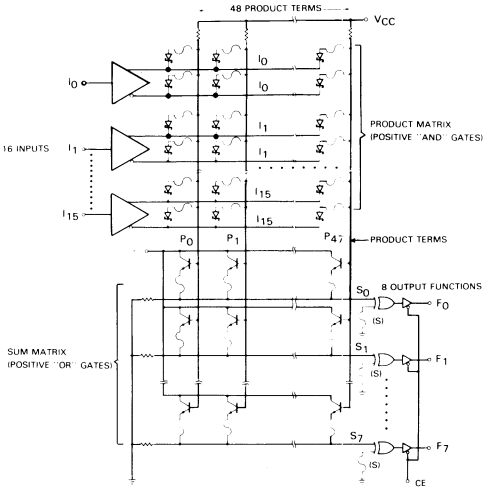
Bipolar Programmable Logic Array

PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	Fp
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

This device features a chip-enable control, an output inhibit, and tri-state outputs.

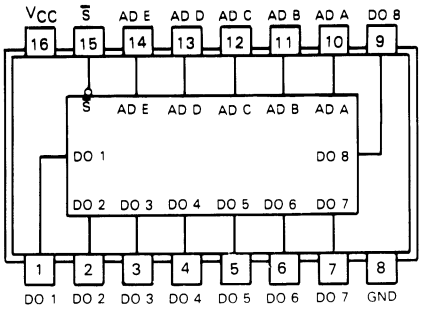
NOTE: *This is a Schottky device.*

100001901

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

NOTE: *This is a Schottky device.*

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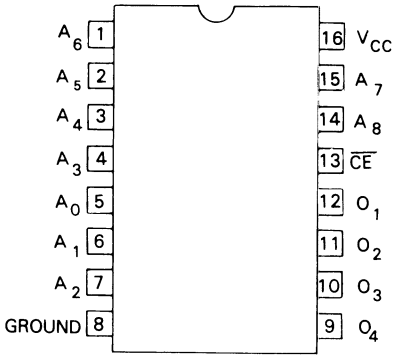
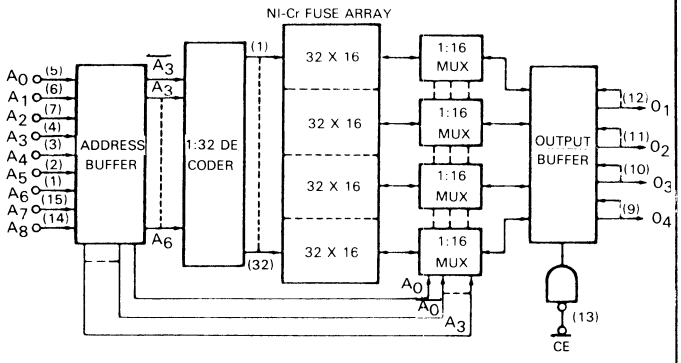
100001902 through 100001913

512 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM

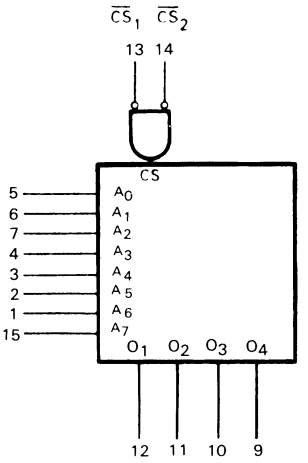


This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

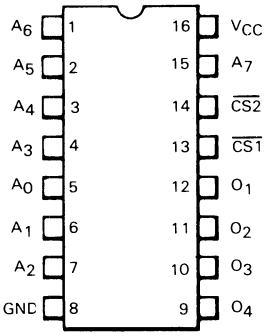
100001914 through 100001919

256 x 4-Bit Bipolar PROM

LOGIC SYMBOL



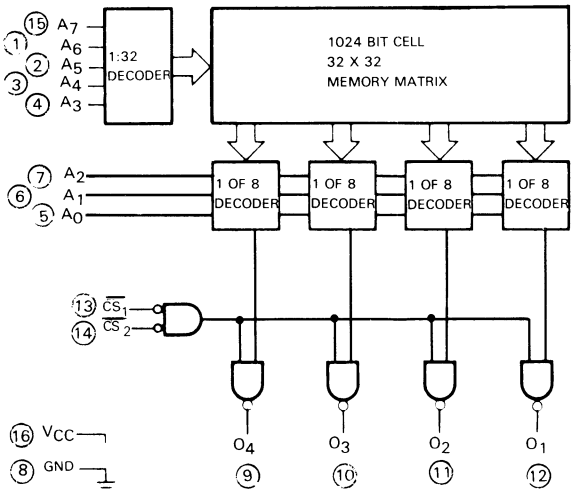
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

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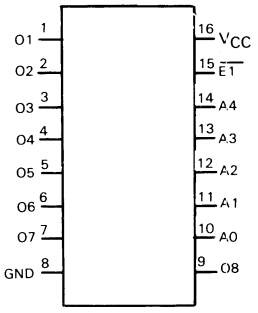
100001920 and 100001921

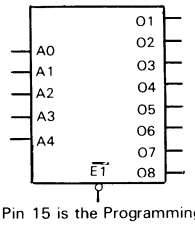
32 X 8 Bit PROM

Dual-In-Line Package



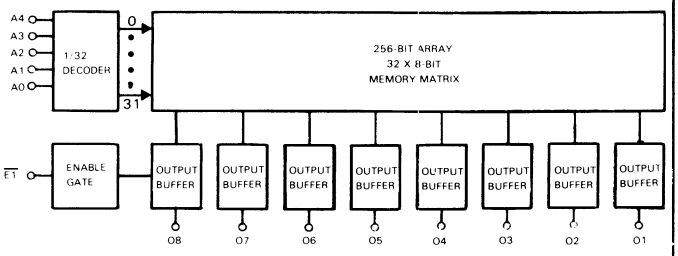
TOP VIEW

LOGIC SYMBOL



Pin 15 is the Programming Pin

BLOCK DIAGRAM



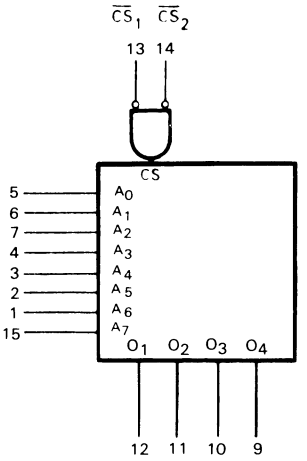
This 256-bit programmable read only memory is organized as 32 x 8-bits. It has tri-state output. The chip is enabled when $\overline{E_1}$ is low.

NOTE: *This is a Schottky device.*

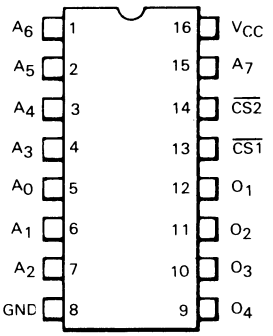
100001922 through 100001932

256 x 4-Bit Bipolar PROM

LOGIC SYMBOL



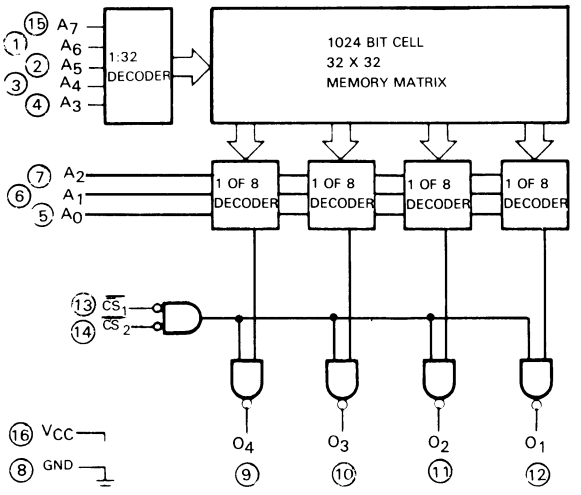
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS_1}, \overline{CS_2}$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

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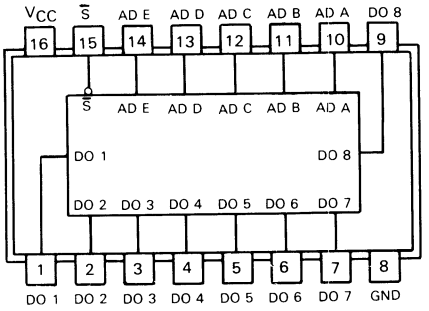
100001933 through 100001946

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



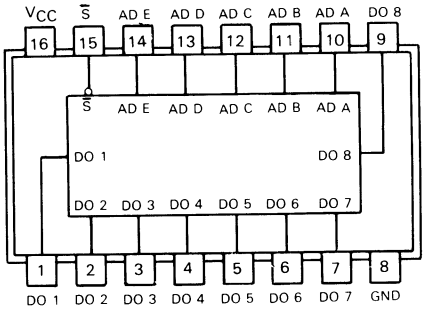
This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

100001947 through 100001950

32 X 8 Bit PROM Open Collector Output

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory has open collector output. $\overline{S}$ must be low to enable the chip.

NOTE: *This is a Schottky device.*

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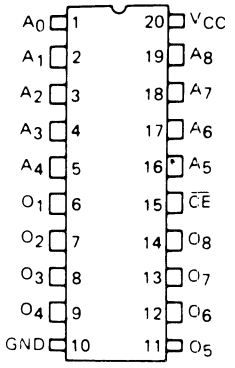
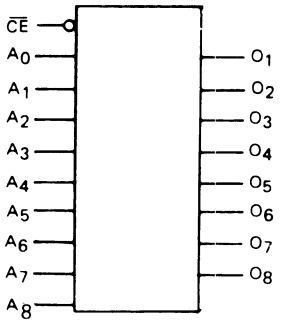
100001951 and 100001952

512 x 8-Bit Bipolar PROM

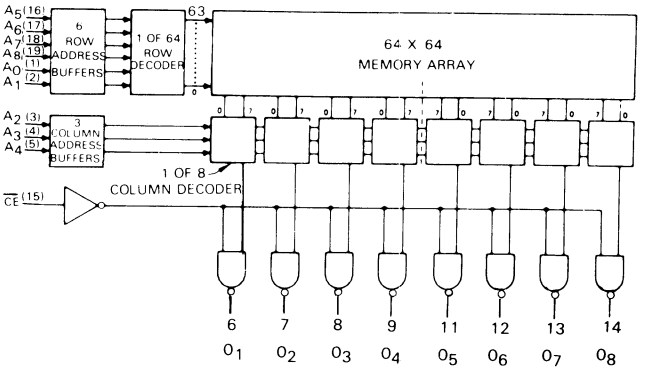
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



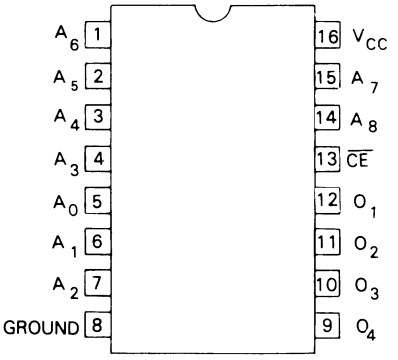
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100001953 through 100001965

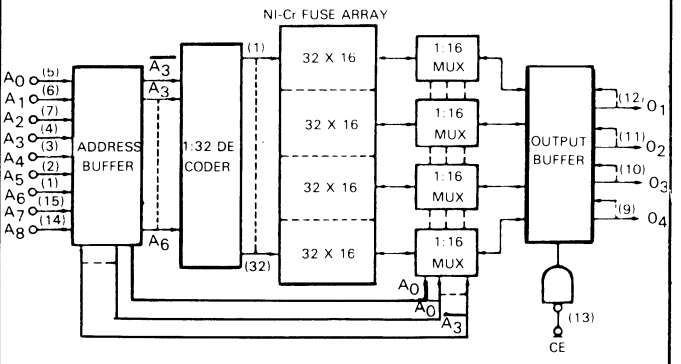
512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



Pin 13 is the programming pin.

BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

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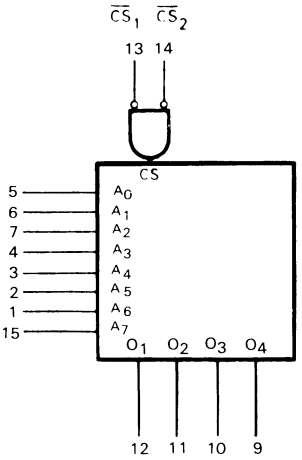
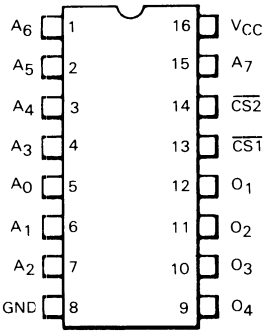
100001966 through 100001987

256 x 4-Bit PROM

LOGIC SYMBOL



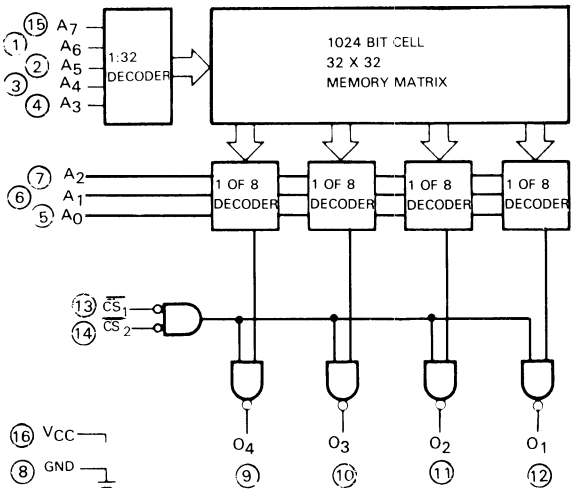
PIN CONFIGURATION



PIN NAMES

A_0 - A_7	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs (Active LOW)
O_1 - O_4	Data Outputs

BLOCK DIAGRAM



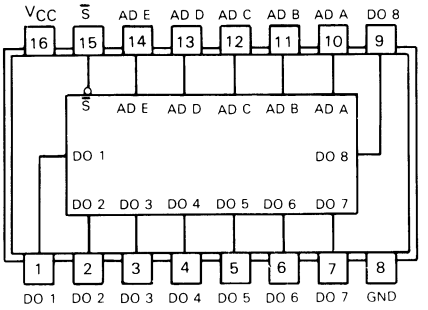
This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

100001988 through 100001993

32 x 8-Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

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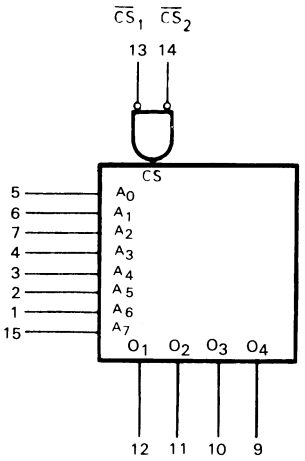
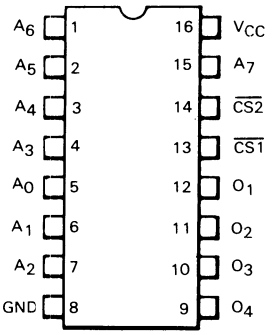
100001994 through 100001996

256 x 4-Bit PROM

LOGIC SYMBOL



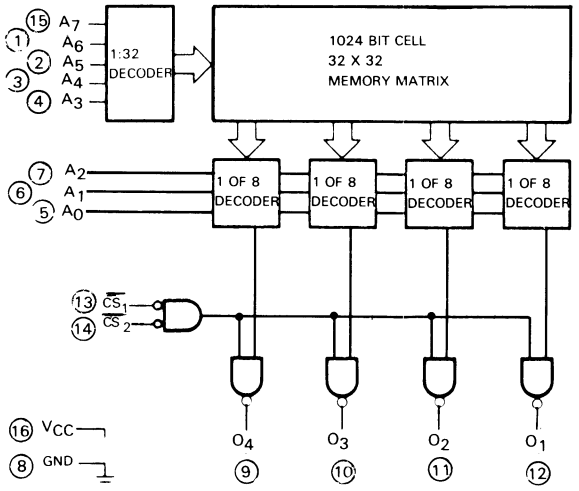
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

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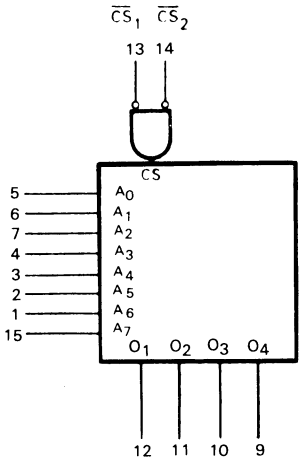
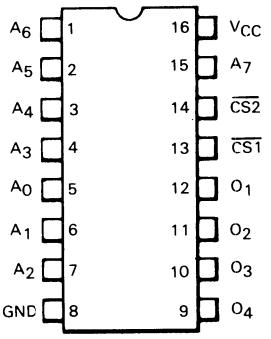
100002000 and 100002001

256 x 4-Bit PROM

LOGIC SYMBOL



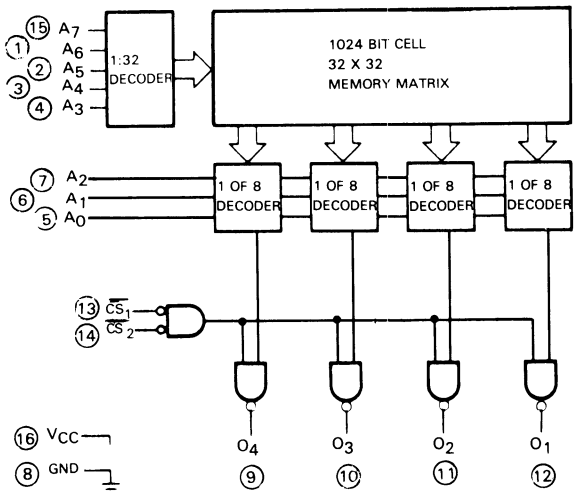
PIN CONFIGURATION



PIN NAMES

A_0 - A_7	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs (Active LOW)
O_1 - O_4	Data Outputs

BLOCK DIAGRAM



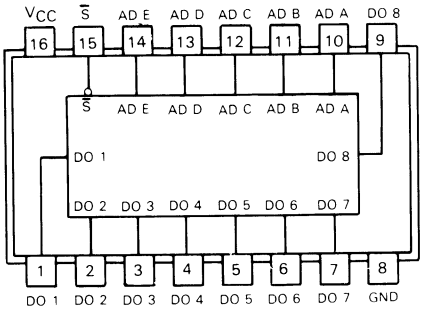
This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

100002002 and 100002003

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

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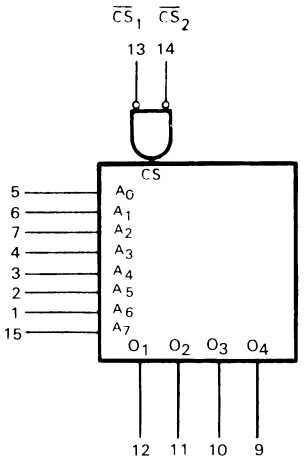
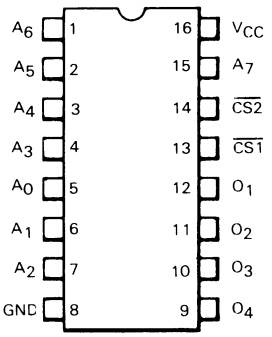
100002004 through 100002011

256 x 4 Prom Tri-State Output

LOGIC SYMBOL



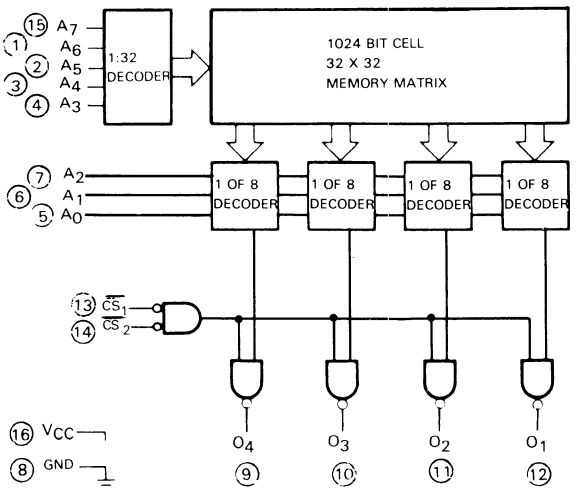
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



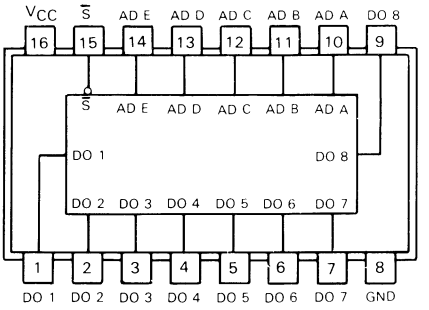
This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

100002012 and 100002013

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

NOTE: *This is a Schottky device.*

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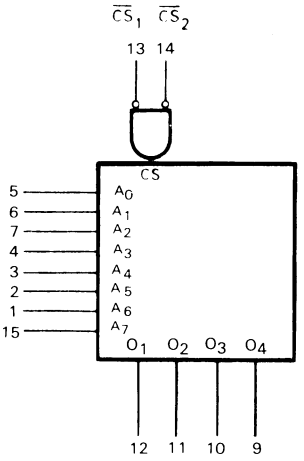
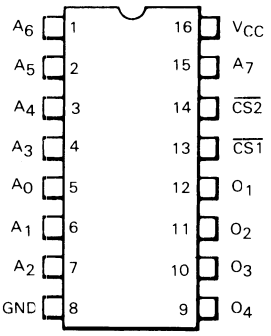
100002014

256 x 4 Prom Tri-State Output

LOGIC SYMBOL



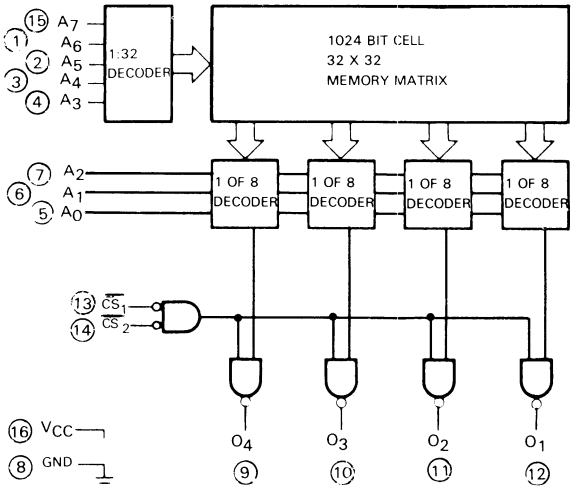
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 \quad O_4$	Data Outputs

BLOCK DIAGRAM



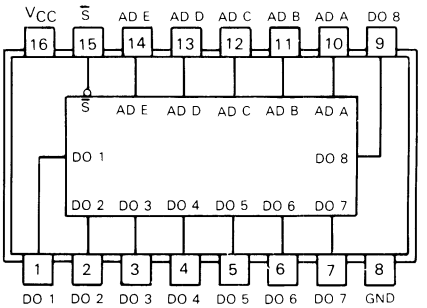
This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

100002015 and 100002016

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

NOTE: *This is a Schottky device.*

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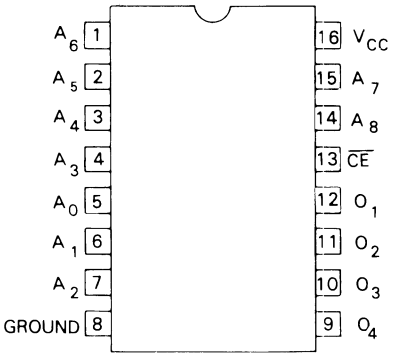
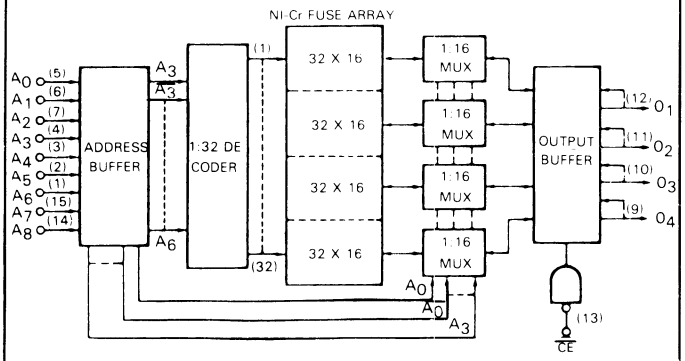
100002017

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory has tri-state output.

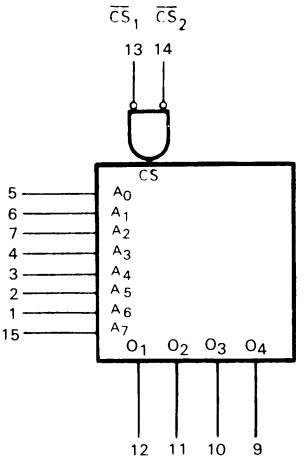
This chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

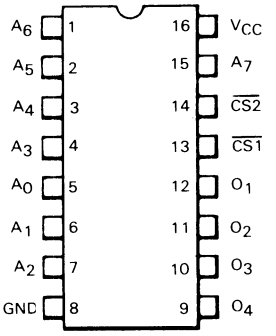
100002018 through 100002029

256 x 4 Prom Tri-State Output

LOGIC SYMBOL



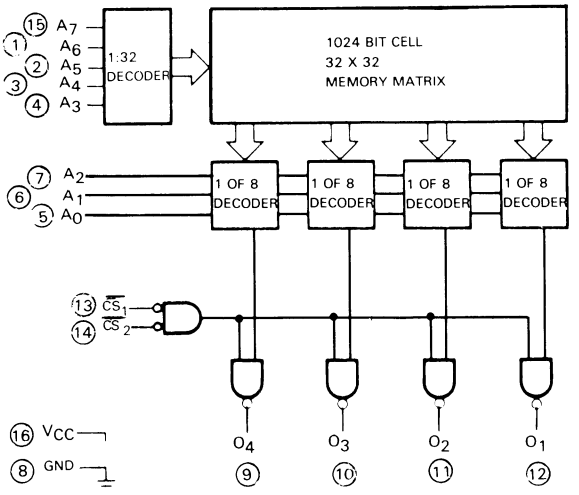
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

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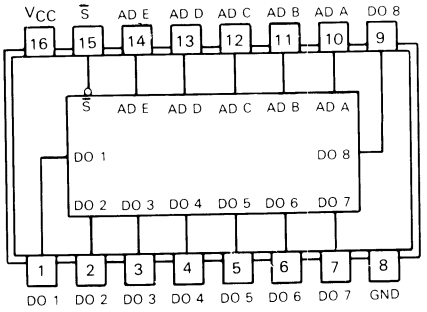
100002030

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

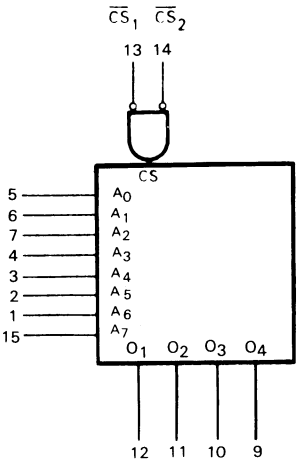


This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

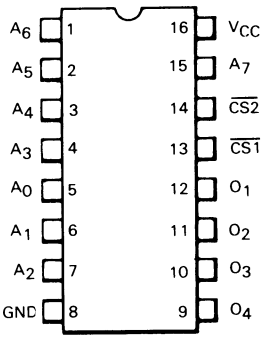
100002031 through 100002034

256 x 4 Prom Tri-State Output

LOGIC SYMBOL



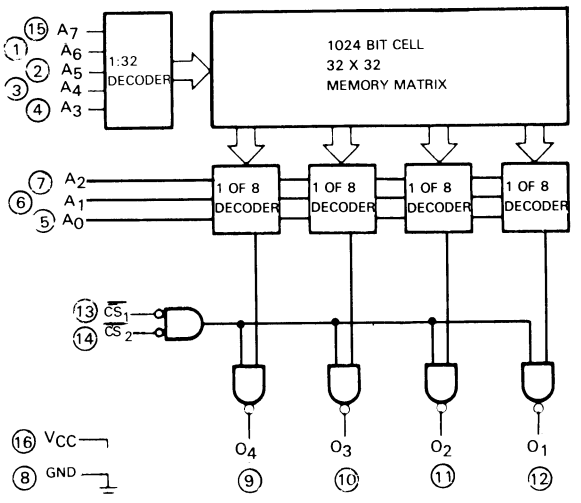
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

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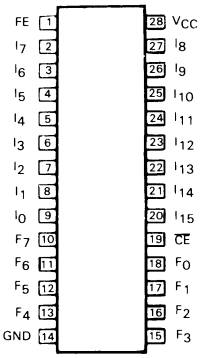
100002035 and 100002036

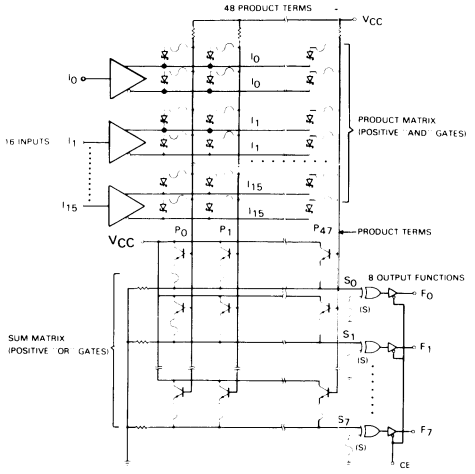
Bipolar Programmable Logic Array

PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	Fp
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

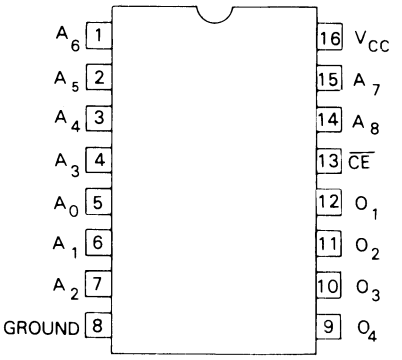
This device features a chip-enabled control, and output inhibit, and tri-state outputs. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

NOTE *This is a Schottky device.*

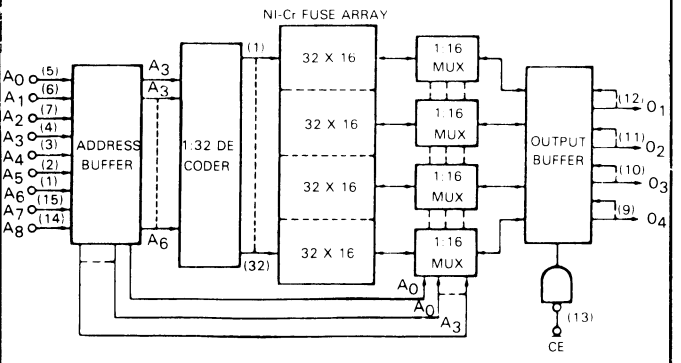
100002037 through 100002046

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low. It is TTL compatible.

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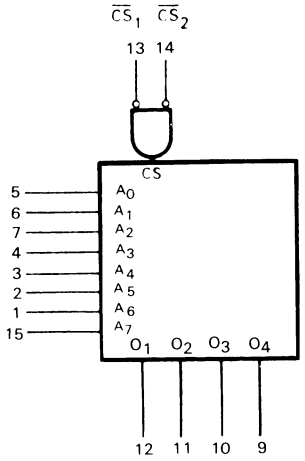
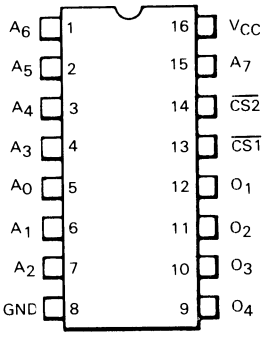
100002047 through 100002050

256x4-Bit PROM

LOGIC SYMBOL



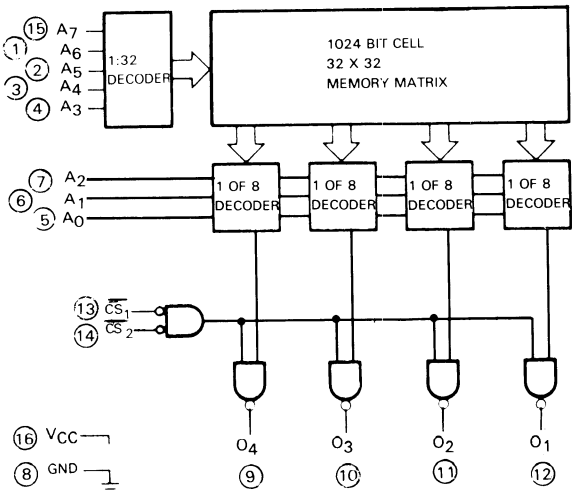
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

BLOCK DIAGRAM

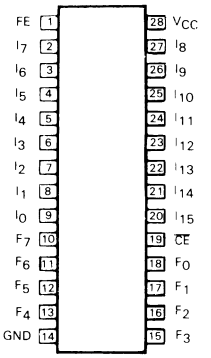


This 1024-bit field programmable read only memory has tri-state output. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

100002051 through 100002053

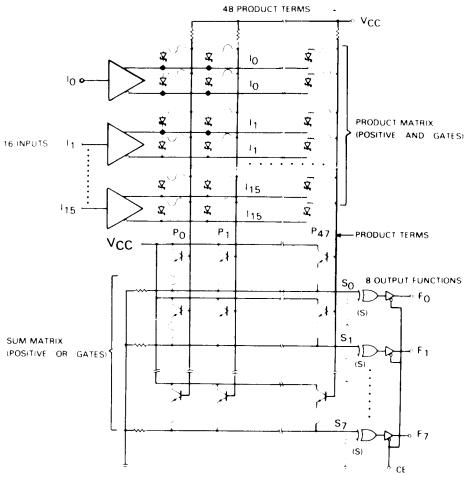
Bipolar Programmable Logic Array

PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? I(Pn)	Fp	$F_{\bar{p}}$
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

This device features a chip-enable control, an output inhibit, and tri-state outputs.

NOTE: *This is a Schottky device.*

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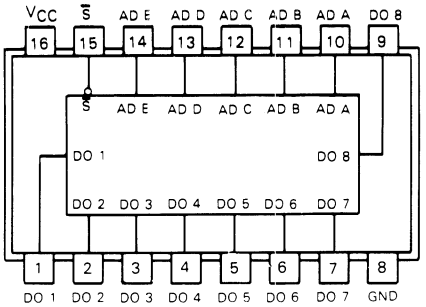
100002054

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

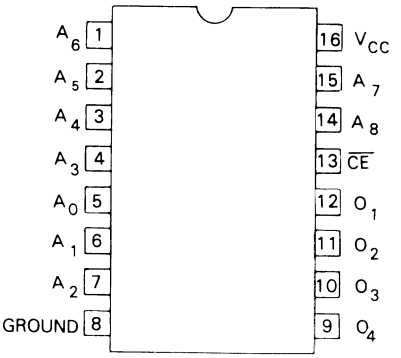


This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

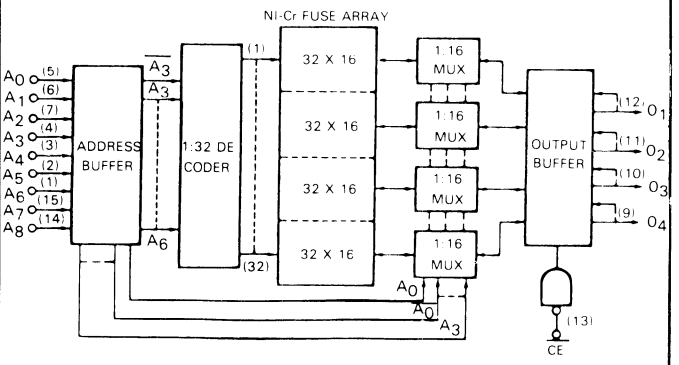
100002055

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory is a Schottky device with tri-state output. The chip is enabled when $\overline{CE}$ is low.

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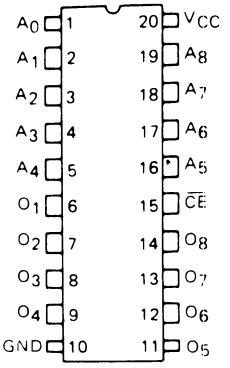
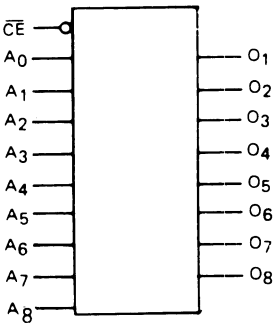
100002056 through 100002062

512 x 8-Bit Bipolar PROM

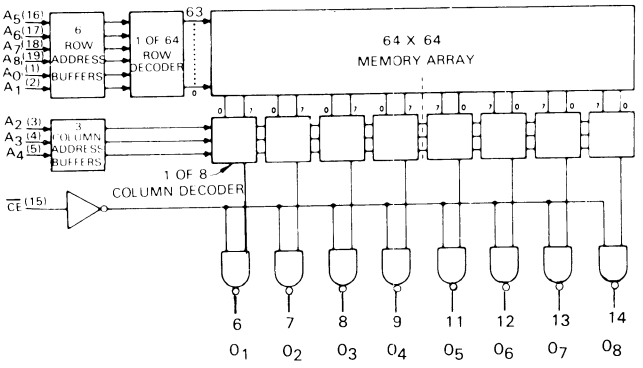
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



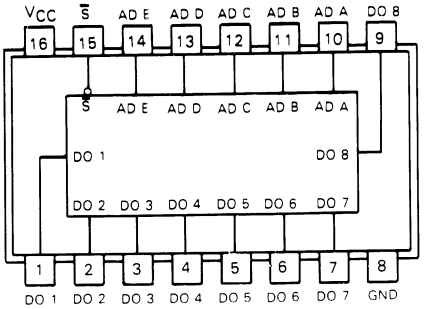
This device is a fully decoded high speed Schottky TTL 4096-Bit PROM in a 512 word by 8 bit format with tri-state output.

100002063 through 100002074

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.



This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

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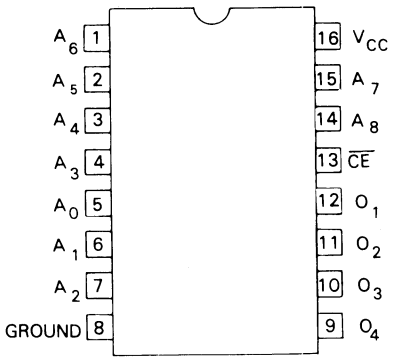
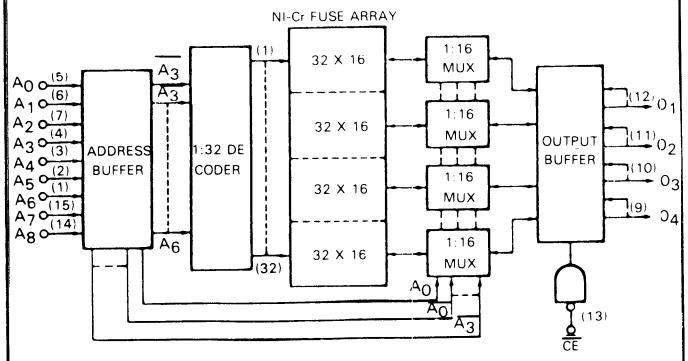
100002075 through 100002081

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



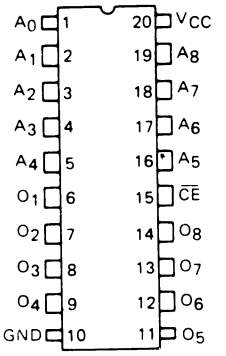
This 2048-bit bipolar programmable read only memory has tri-state output. It is fully TTL compatible. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

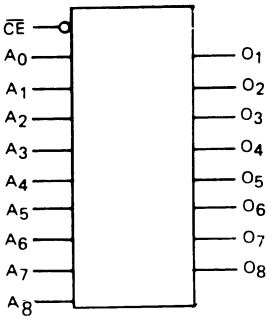
100002082 through 100002087

512 x 8-Bit Bipolar PROM

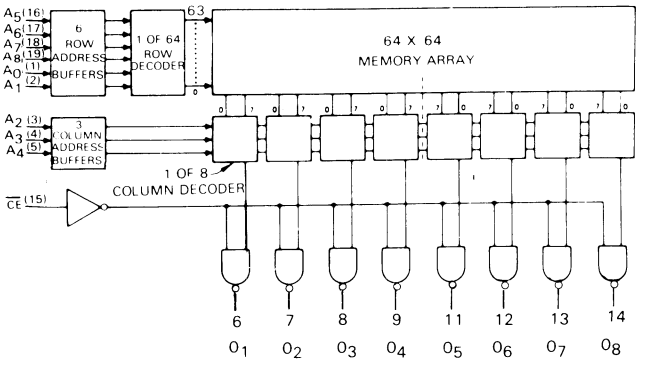
PIN CONFIGURATION



Pin 15 is the programming pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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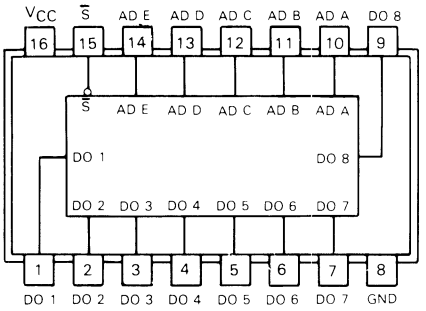
100002088 through 100002091

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

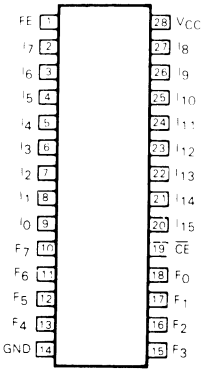


This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

100002092 through 100002095

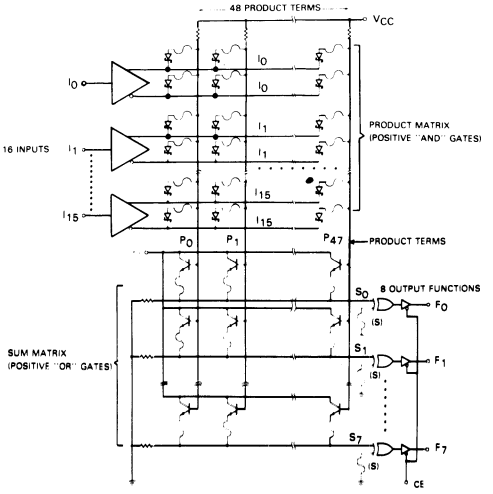
Bipolar Programmable Logic Array

PIN CONFIGURATION



TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? I(Pn)	Fp	$\overline{Fp}$
Disabled	X	1	X	Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1



This logic array contains 48 product terms (AND terms) and 8 sum terms (OR terms). Each OR term controls an output function. The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms.

This device features a chip-enable control, an output inhibit, and tri-state outputs.

NOTE: *This is a Schottky device.*

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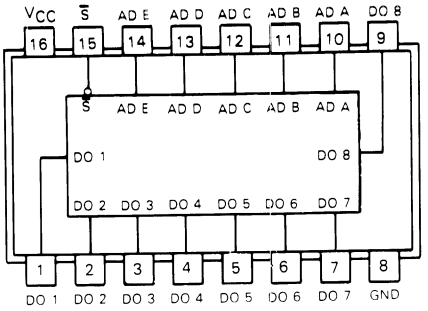
100002096 through 100002099

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

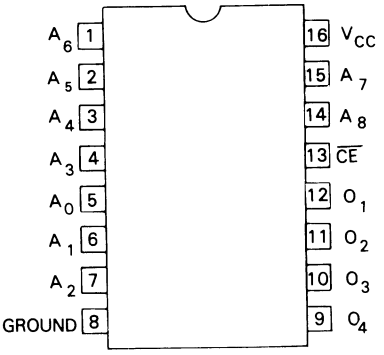


This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

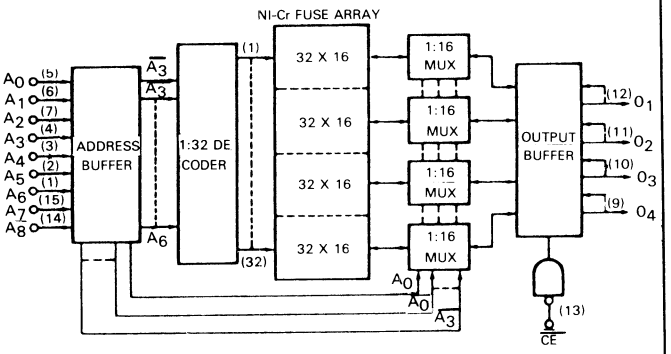
100002100

512 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory has tri-state output. It is fully TTL compatible.

The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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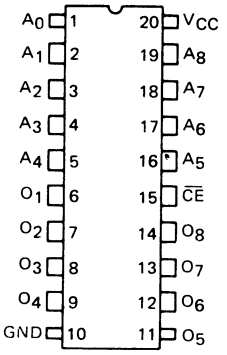
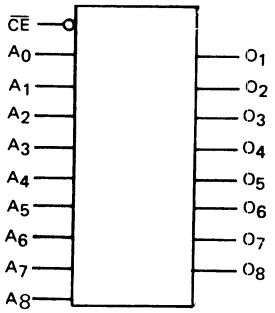
100002107

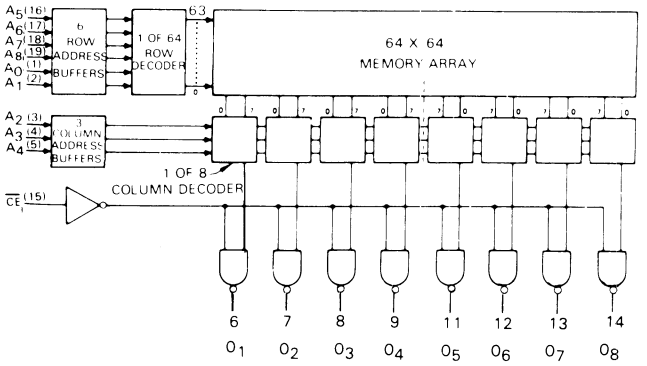
Bipolar PROM

PIN CONFIGURATION





BLOCK DIAGRAM



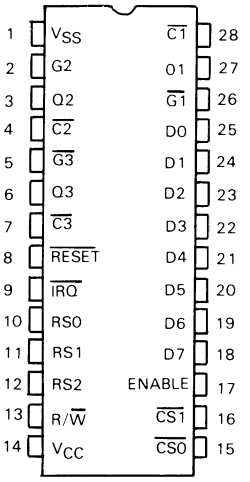
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

100002108

Programmable Timer

PIN CONFIGURATION



TRUTH TABLE

Register Select Inputs			Operations	
RS2	RS1	RS0	R/W=0	R/W=1
0	0	0	CR20=0 WRITE CONTROL REGISTER #3 CR20=1 WRITE CONTROL REGISTER #1	NO OPERATION
0	0	1	WRITE CONTROL REGISTER #2	READ STATUS REGISTER
0	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #1 COUNTER
0	1	1	WRITE TIMER #1 LATCHES	READ LSB BUFFER REGISTER
1	0	0	WRITE MSB BUFFER REGISTER	READ TIMER #2 COUNTER
1	0	1	WRITE TIMER #2 LATCHES	READ LSB BUFFER REGISTER
1	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #2 COUNTER
1	1	1	WRITE TIMER #3 LATCHES	READ LSB BUFFER REGISTER

This is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

It has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals.

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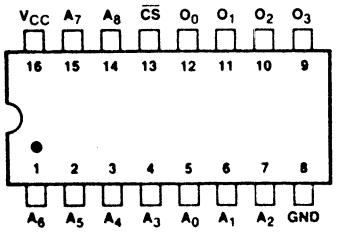
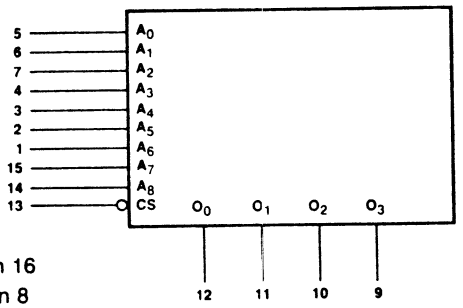
100002109

512 x 4 PROM
with Open Collector Outputs

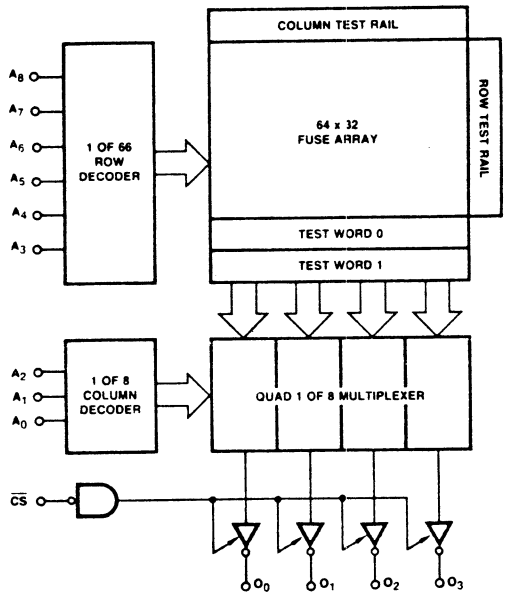
PIN CONFIGURATION





V_{CC} = Pin 16
GND = Pin 8

BLOCK DIAGRAM



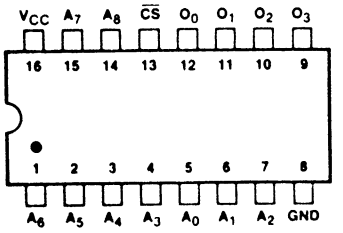
This 2048-bit programmable read only memory is TTL compatible, and has open collector output. The chip is enabled when $\overline{CS}$ is low.

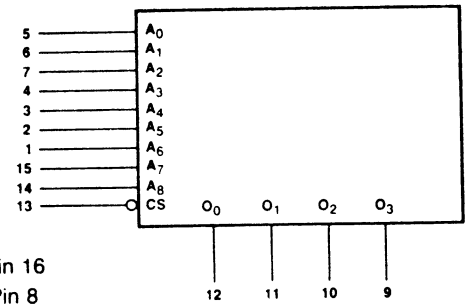
NOTE: *This is a Schottky device.*

100002110

512 x 4 PROM
with Tri-State Outputs

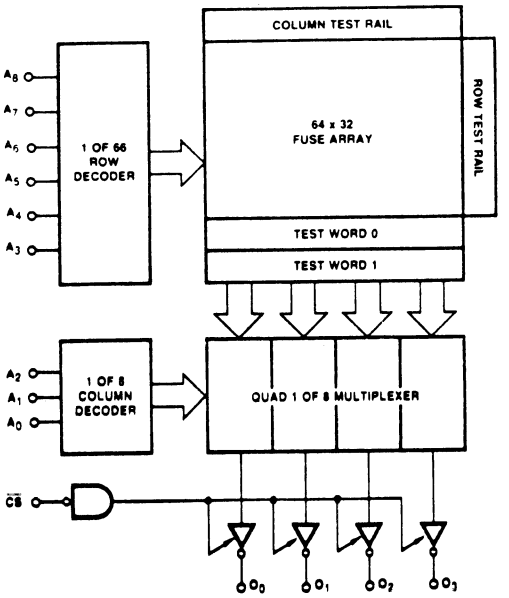
PIN CONFIGURATION





V_{CC} = Pin 16
GND = Pin 8

BLOCK DIAGRAM



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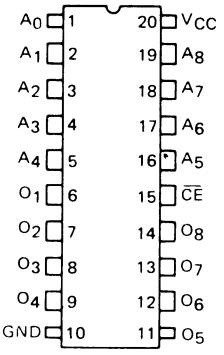
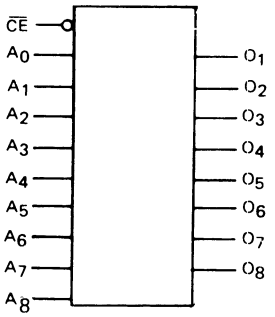
100002111 through 100002120

512 x 8-Bit PROM

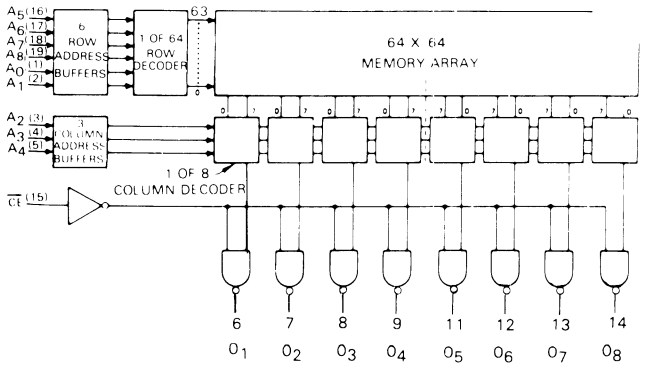
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



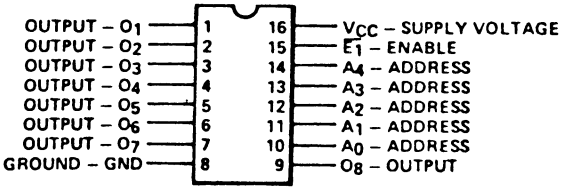
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

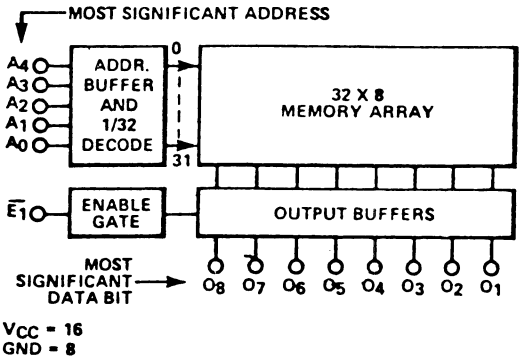
100002121 through 100002123

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 0_1 through A_8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

NOTE: *This is a Schottky device.*

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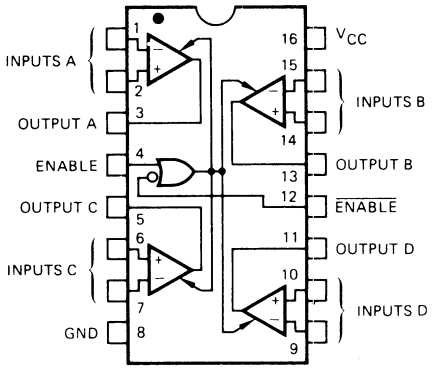
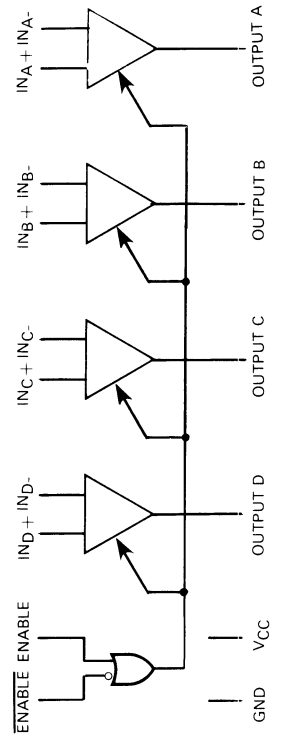
100002125

Quad High Speed Differential Line Driver

PIN CONFIGURATION





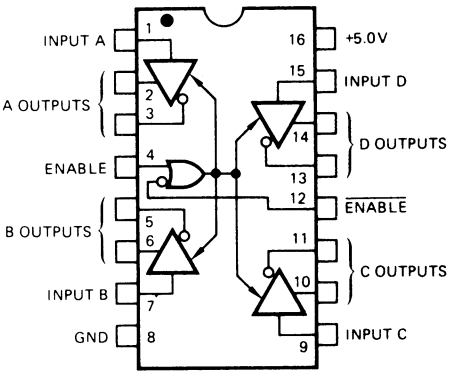
The 100002125 is a quad differential line driver, designed for digital data transmission over balanced lines. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

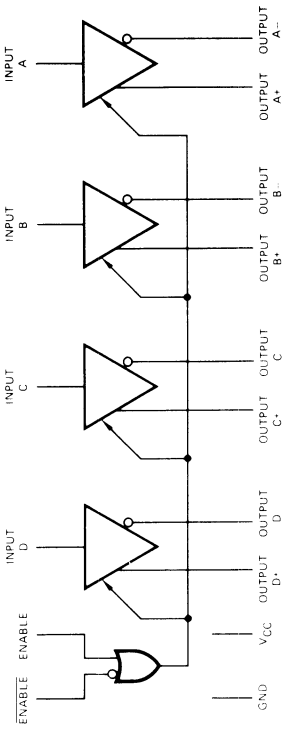
NOTE: *This is a low power Schottky device.*

100002126

Quad Differential Line Receivers

PIN CONFIGURATION





The 100002126 is a quad line receiver. The device features an input sensitivity of 200 mV over the input voltage range of 15 volts, also the 2126 has an input sensitivity of 500 mV over the input voltage range of 15 volts.

NOTE: *This is a low power Schottky device.*

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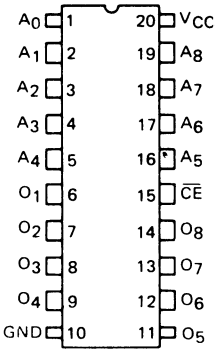
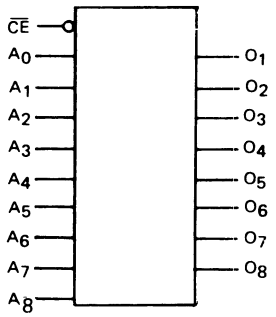
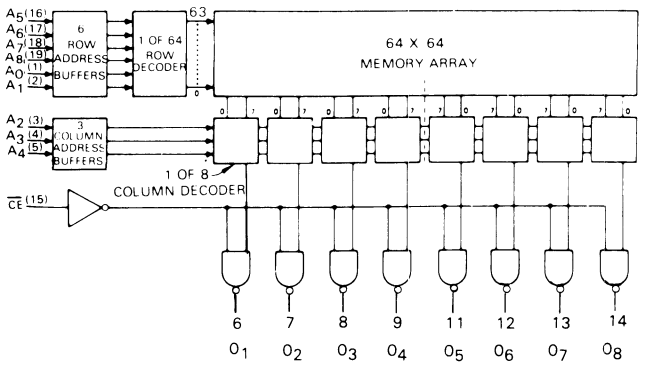
100002127 through 100002132

512 x 8-Bit PROM

PIN CONFIGURATION







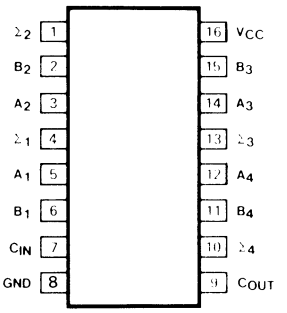
This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

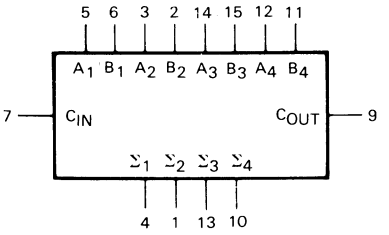
NOTE: *This is a Schottky device.*

100002133

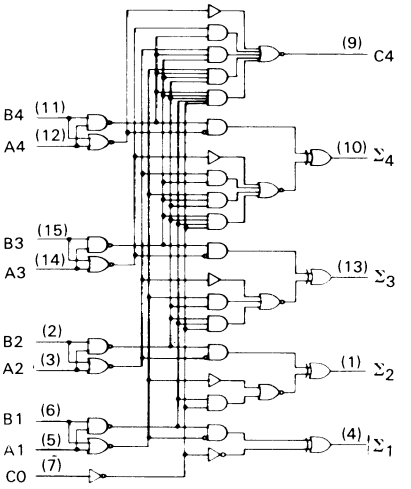
4-Bit Binary Full Adder (With Fast Carry)

PIN CONFIGURATION





V_{CC} = Pin 16
GND = Pin 8



This high speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words and a carry input. It generates the binary sum outputs and the carry output from the most significant bit. It operates with either active HIGH or active LOW operands. (postive or negative logic).

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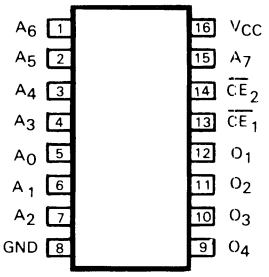
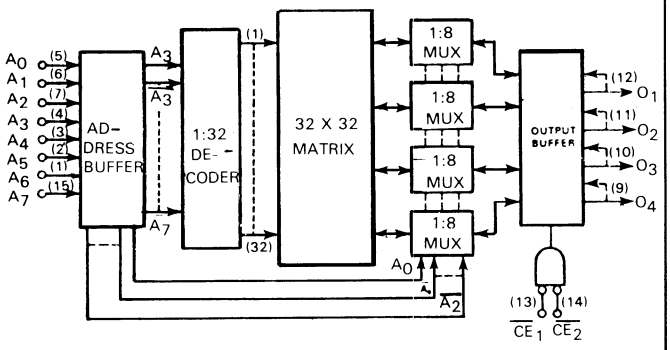
100002140

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

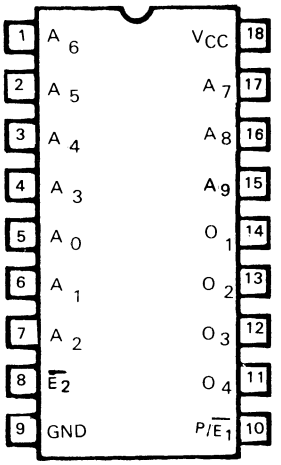
NOTE: *This is a Schottky device.*

100002144

1024 x 4-Bit PROM

PIN CONFIGURATION

Pin 10 is the Programming Pin.



This 4096-bit programmable read only memory has tri-state output. P/$\overline{E_1}$ and $\overline{E_2}$ must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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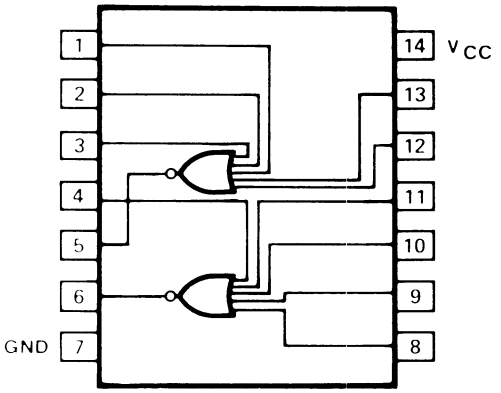
100002145

Dual 5-Input NOR Gate

PIN CONFIGURATION



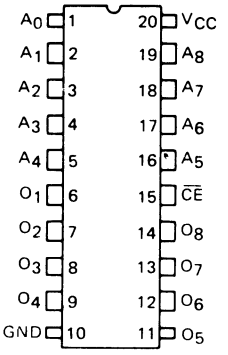
NOTE: *This is a low power Schottky device.*

$$Y = \overline{A + B + C + D + E}$$

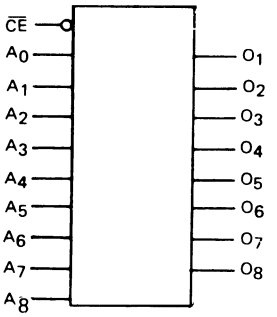
100002146

512 x 8-Bit Bipolar PROM

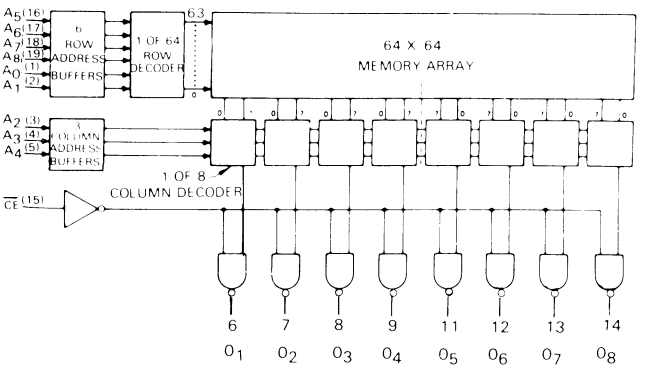
PIN CONFIGURATION



Pin 15 is the Programming Pin.



BLOCK DIAGRAM



This 4096-bit programmable read only memory device has tri-state output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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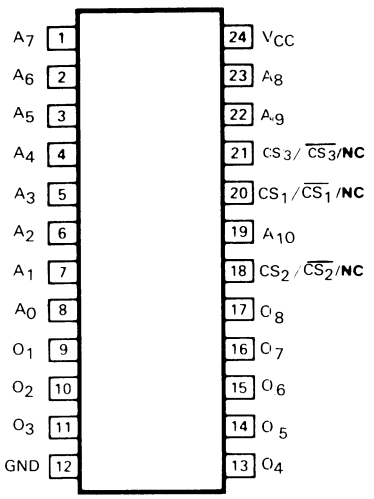
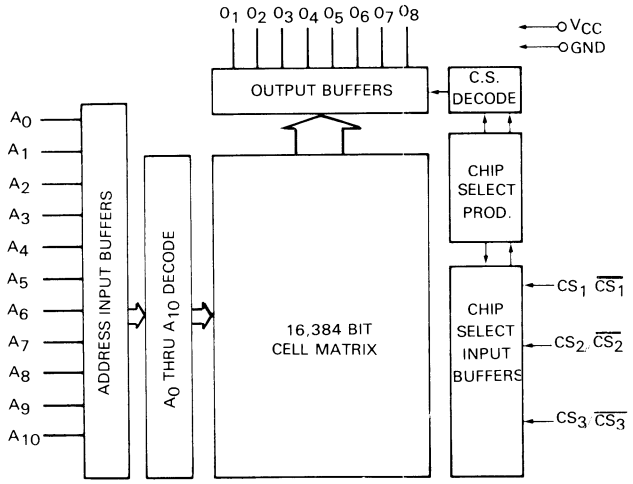
100002148 through 100002151

2048 x 8-Bit Static ROM

PIN CONFIGURATION





This 16384-bit static, NMOS mask programmed, read only memory is organized as 2048 x 8 bits per word.

Three programmable chip select input signals are provided to control output buffers. Each chip select polarity may be specified by the customer, thus allowing the addressing of 8 memory chips without external gating.

The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with other tri-state components.

This device requires no clock signals of any kind. It is TTL compatible.

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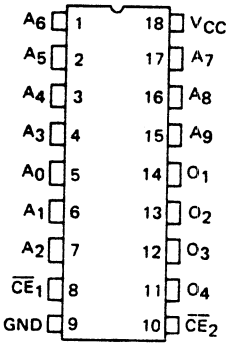
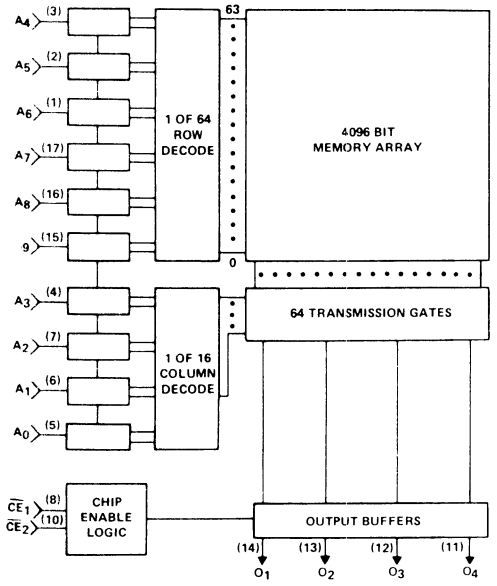
100002152

1Kx4 Programmable ROM

PIN CONFIGURATION



BLOCK DIAGRAM



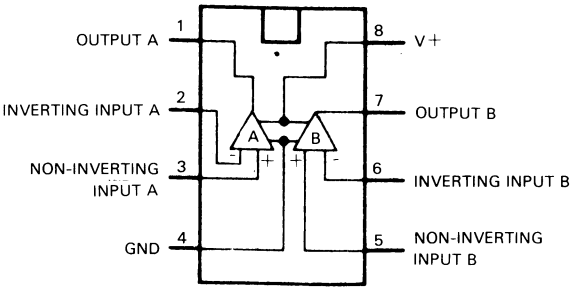
This device is a fully decoded, high speed, TTL field programmable ROM with 4096-bits in a 1K x 4 word format. It has tri-state output.

The chip is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low.

NOTE: *This is a Schottky device.*

100002154

Low Power Low Offset Voltage Dual Comparator



This device has output voltage which is compatible with TTL, DTL, ECL, MOS and CMOS logic systems.

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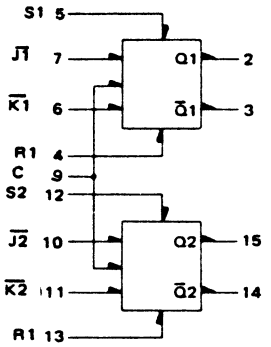
100002155

ECL Dual J-$\overline{K}$ Flip-Flop



CLOCK J-K TRUTH TABLE*

$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	Q_n
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transistion of clock for $\overline{J}$ $\overline{K}$ input condition present.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

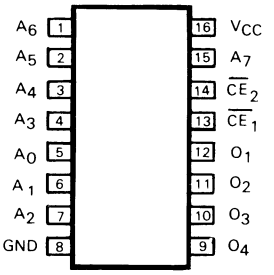
The 100002155 is an ECL dual J-K master-slave, dc coupled flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

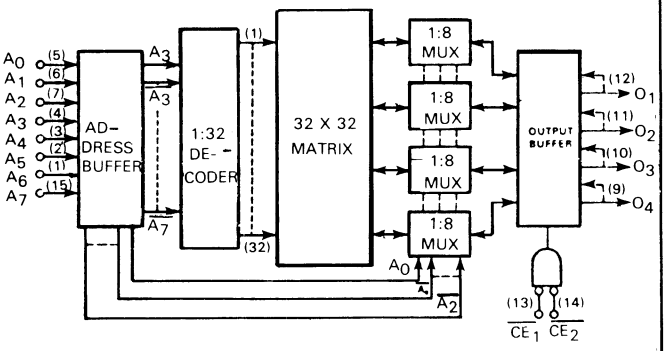
NOTE: *This is an ECL device*

100002158 and 100002159

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION





This 1024-bit bipolar read only memory is organized as 256 words by 4 bits. It features on-chip decoding, tri-state outputs, and a maximum access time of 50 ns.

$\overline{CE_1}$ and $\overline{CE_2}$ are chip enable inputs and must be asserted together to enable the chip.

NOTE: *This is a Schottky device.*

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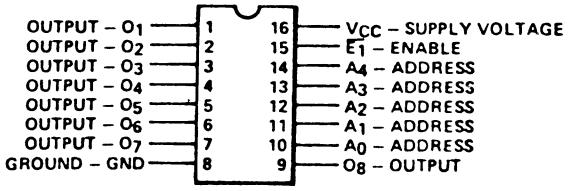
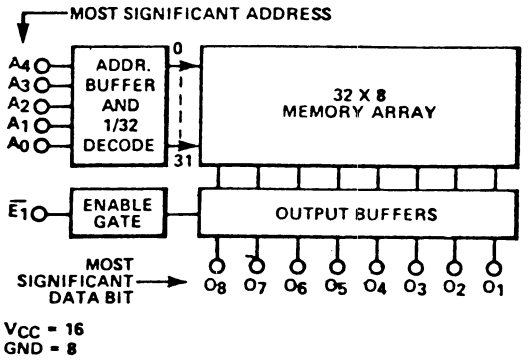
100002160 through 100002163

32 x 8-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



This 256-bit programmable read only memory is organized as 32 words by 8 bits. It includes on-chip address decoding, a chip enable $\overline{E_1}$, and tri-state outputs.

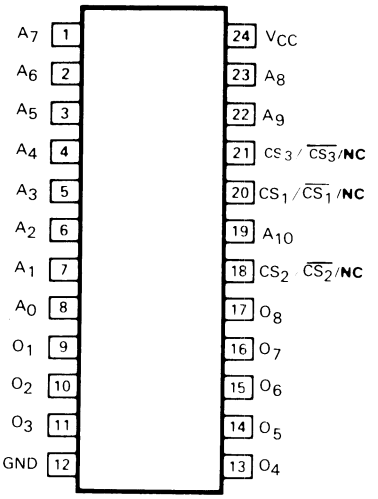
The memory is addressed with inputs A_0 through A_4, which select one of 32 words. A word is read out on the outputs 0_1 through A_8. The enable $\overline{E_1}$ must be low to read. If it is high the outputs are held off, permitting wire ORing of the tri-state outputs of several packages.

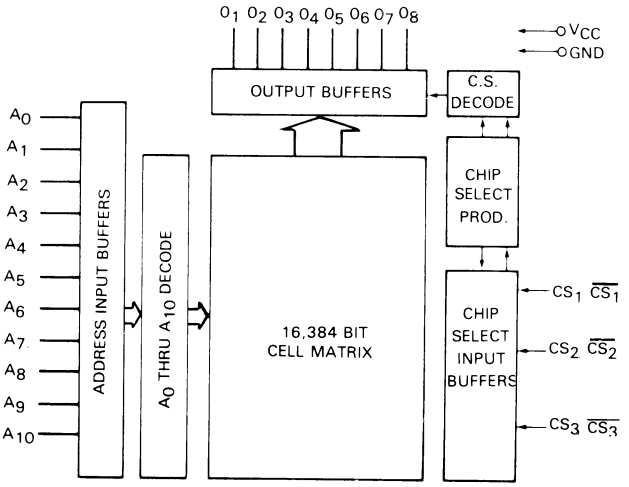
NOTE: *This is a Schottky device.*

100002164 through 100002166

2048 x 8-Bit Static ROM

PIN CONFIGURATION





This 16384-bit static, NMOS mask programmed, read only memory is organized as 2048 x 8 bits per word.

Three programmable chip select input signals are provided to control output buffers. Each chip select polarity may be specified by the customer, thus allowing the addressing of 8 memory chips without external gating.

The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with other tri-state components.

This device requires no clock signals of any kind. It is TTL compatible.

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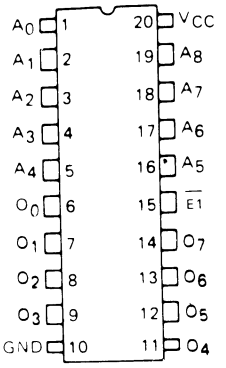
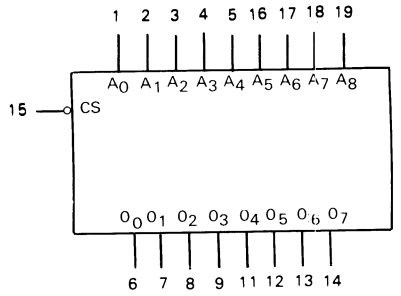
100002167 and 100002168

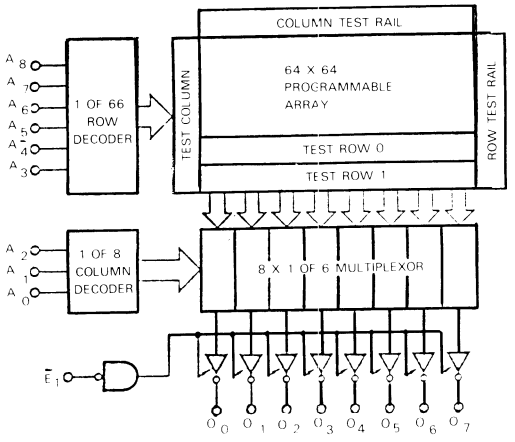
4096-Bit Generic Series Bipolar PROM

PIN CONFIGURATION



Pin 15 is the Programming Pin.





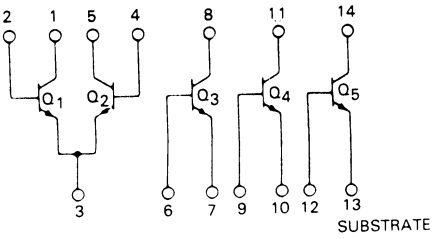
This 4096-bit bipolar programmable read only memory is organized as 512 words by 8 bits. It has open collector output and is a TTL device.

The chip is enabled when $\overline{E_1}$ is low.

100002169

High Voltage N-P-N Transistor Array

PIN CONFIGURATION



This device consists of five transistors with two of the transistors connected to form a differentially connected pair. This type is recommended for low-power applications in the DC through VHF range. It is in a 12 lead, T0-5 can and has 750 mW.

NOTE: *The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (pin 5) should be maintained at either d.c. or signal (a.c.) ground.*

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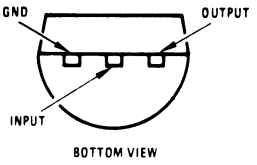
100002170

-12V, 1.5A, 15W Voltage Regulator

PIN CONFIGURATION



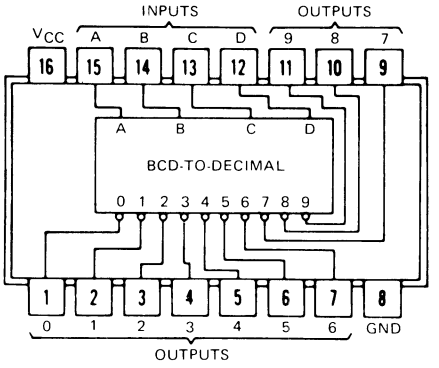
This device has:

- Preset output voltage error of less than +5% overload, line and temperature.
- Internal short-circuit, thermal and safe operating area protection.
- Easy adjustability to higher output voltages.
- Maximum line regulation less than 0.07% V_{OUT}/V.
- Maximum load regulation less than 0.07% V_{OUT}/mA.

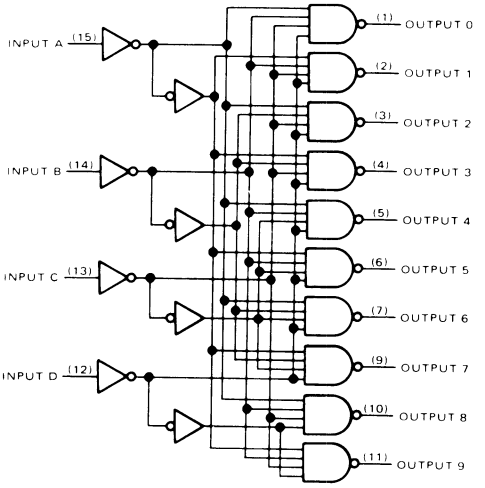
100002171

BCD-to-Decimal Decoder/Driver

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

This is a binary code digital-to-decimal decoder with open collector output.

NOTE: *It is a low power Schottky device.*

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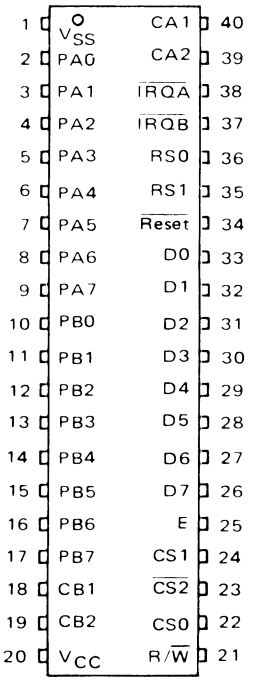
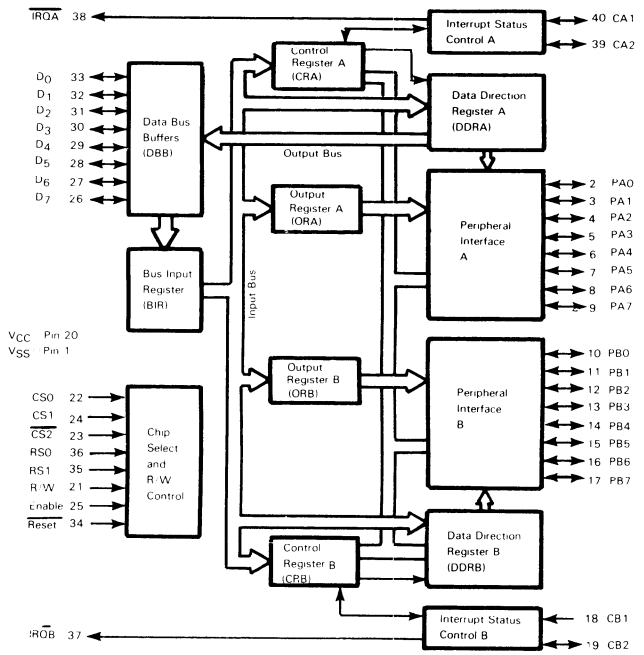
100002175

Peripheral Interface Adapter





This peripheral interface adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-bit bidirectional data bus for communication with the MPU
- Two bidirectional 8-bit buses for interface to peripherals
- Two programmable control registers
- Two programmable data direction registers
- Four individually controlled interrupt input lines; two usable as peripheral control outputs
- Handshake control logic for input and output peripheral operation
- High impedance 3-state and direct transistor drive peripheral lines
- Program controlled interrupt and interrupt disable capability
- CMOS drive capability on Side A peripheral lines
- Two TTL drive capability on all A and B side buffers
- TTL compatible
- Static operation

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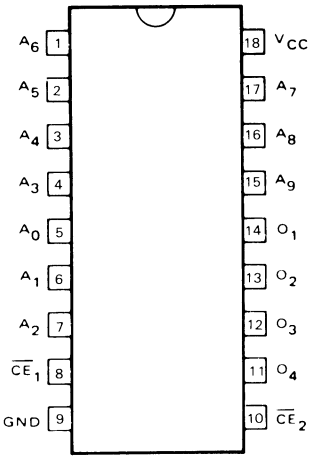
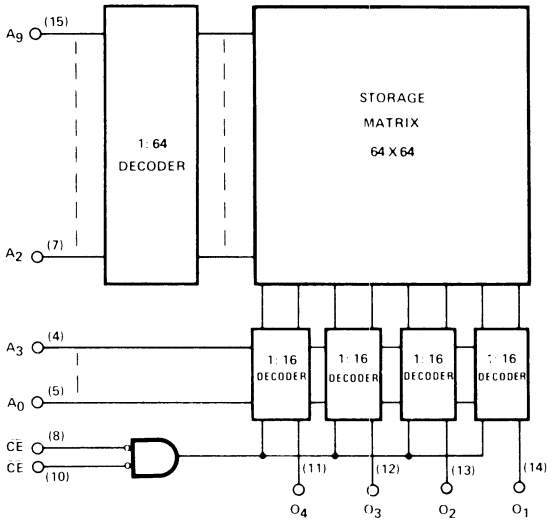
100002178

1024 x 4-Bit Bipolar PROM

PIN CONFIGURATION



BLOCK DIAGRAM



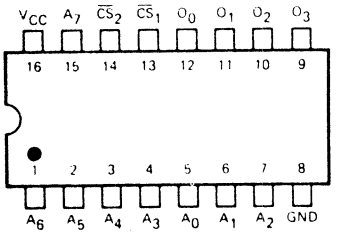
This 4096-bit bipolar programmable read only memory has tri-state output. The chip is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low.

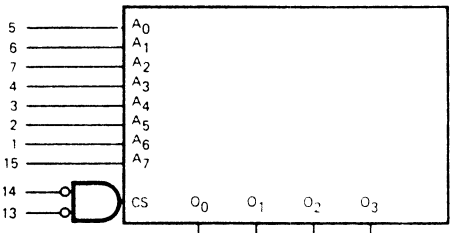
NOTE: *This is a Schottky device.*

100002179

256 x 4-bit PROM

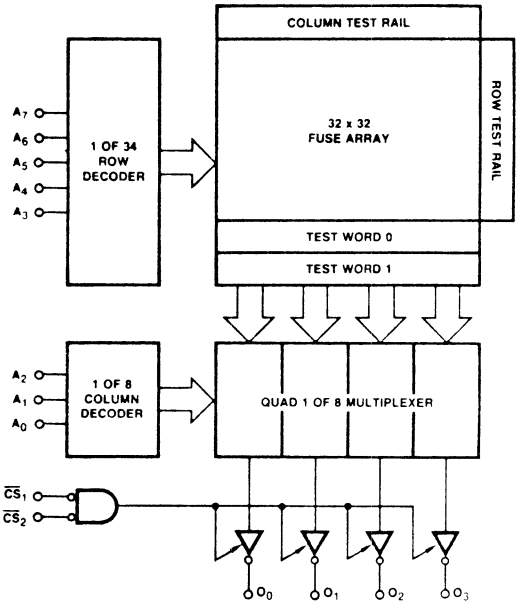
PIN CONFIGURATION





VCC = Pin 16
GND = Pin 8

BLOCK DIAGRAM



This 1024-bit programmable read only memory has tri-state output. The chip is enabled when $\overline{E_1}$ and $\overline{E_2}$ are low.

NOTE: *This is a Schottky device.*

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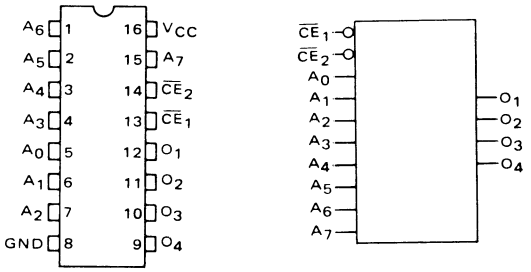
100002180

256 x 4-bit Field PROM

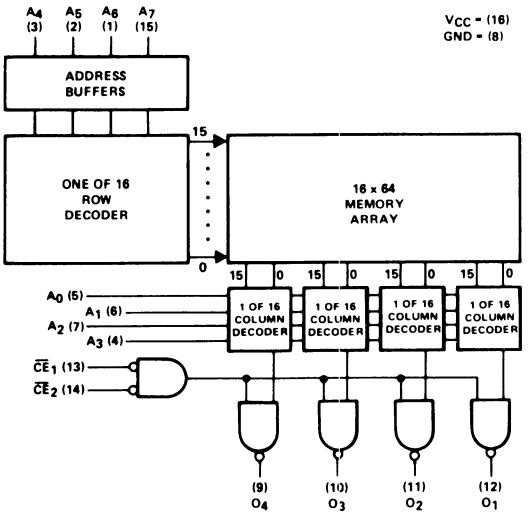
PIN CONFIGURATION



PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs

BLOCK DIAGRAM



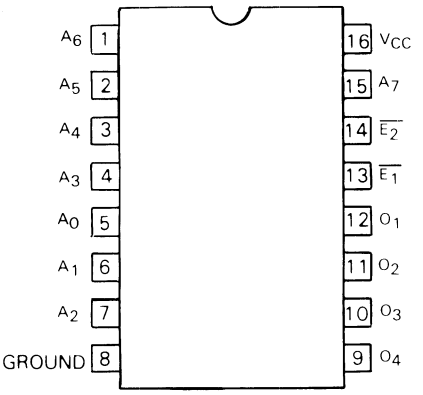
This 1024-bit field programmable read only memory is a fully decoded, high speed TTL device with tri-state output. The chip is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low.

NOTE: *This is a Schottky device.*

100002181

256 x 4-bit PROM

PIN CONFIGURATION



V_{CC} = PIN 16
GND = PIN 8

This 1024-bit programmable read only memory has open collector output and full Schottky clamping. The chip is enabled when $\overline{E_1}$ and $\overline{E_2}$ are low.

NOTE: *This is a Schottky device.*

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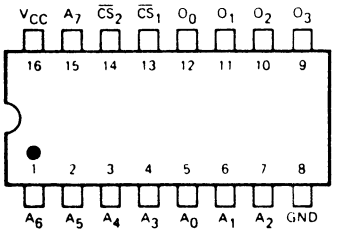
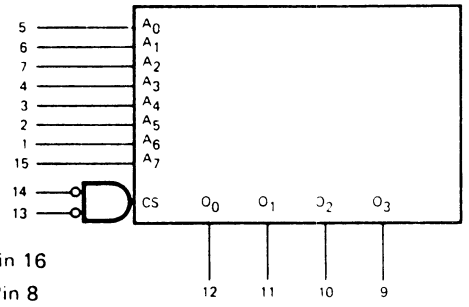
100002182

256 x 4-Bit PROM

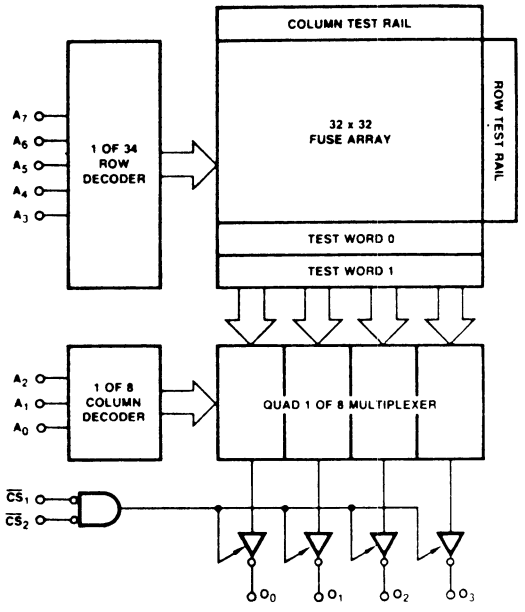
PIN CONFIGURATION





V_{CC} = Pin 16
GND = Pin 8

BLOCK DIAGRAM



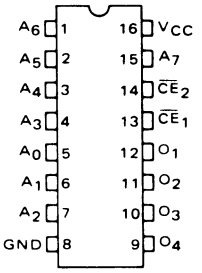
This 1024-bit field programmable read only memory has tri-state outputs. The chip is enabled when $\overline{CS_1}$ and $\overline{CS_2}$ are low.

NOTE: *This is a Schottky device.*

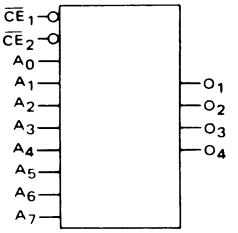
100002183

256 x 4-Bit Bipolar PROM

PIN CONFIGURATION



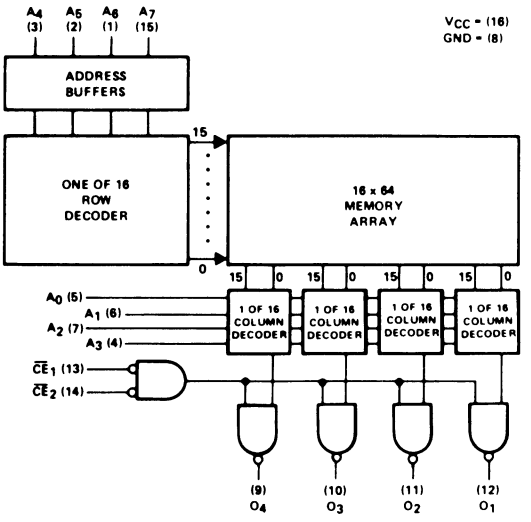
LOGIC SYMBOL



PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE_1}, \overline{CE_2}$	Chip Enable Inputs

BLOCK DIAGRAM



This 1024-bit field programmable read only memory is arranged in 256-bit by 4 words. It has open collector output and is TTL compatible. The chip is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low.

NOTE: *This is a Schottky device.*

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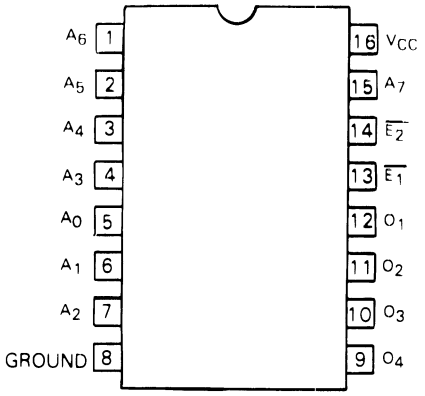
100002184

256 x 4-bit PROM

PIN CONFIGURATION



V_{CC} = PIN 16
GND = PIN 8

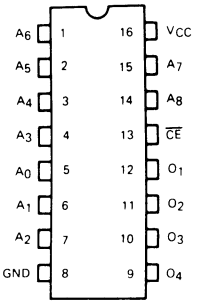
This 1024-bit programmable read only memory has open collector output and full Schottky clamping. The chip is enabled when $\overline{E_1}$ and $\overline{E_2}$ are low.

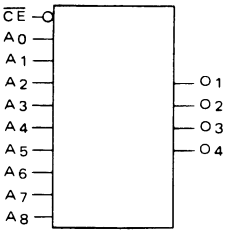
NOTE: *This is a Schottky device.*

100002190 through 100002194

512 x 4-Bit PROM

PIN CONFIGURATION

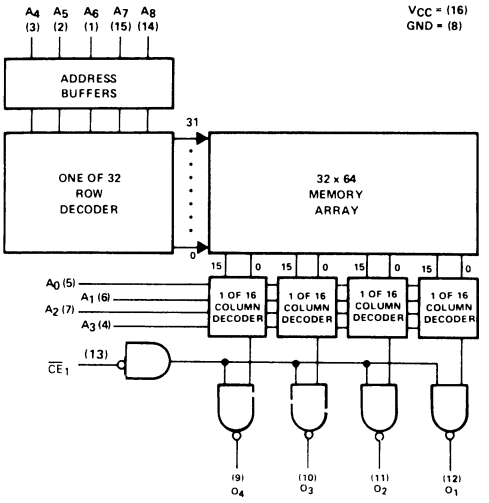




PIN NAMES

A0 – A8	Address Inputs
$\overline{CE}$	Chip Enable Input
O1 – O4	Data Outputs

BLOCK DIAGRAM



This 2048-bit bipolar programmable read only memory has open collector output. The chip is enabled when $\overline{CE}$ is low.

NOTE: *This is a Schottky device.*

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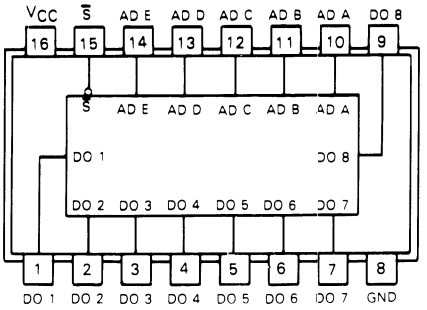
100002195 and 100002196

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

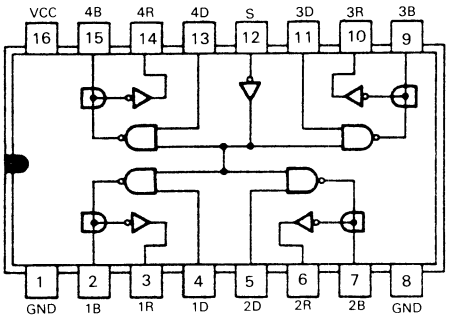


This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

100002199

Quad Bus Tranceiver

PIN CONFIGURATION



Positive logic: $B = \overline{\overline{DS}}$, $R = \overline{B}$
Each bus terminal, B, is a driver output and a receiver input.

FUNCTION TABLE (TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

FUNCTION TABLE (RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H high level L low level X irrelevant

The 10002199 is designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver output is of the open-collector type, and is designed to handle loads of up to 100 milliamperes (50 ohms to 5 volts). The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

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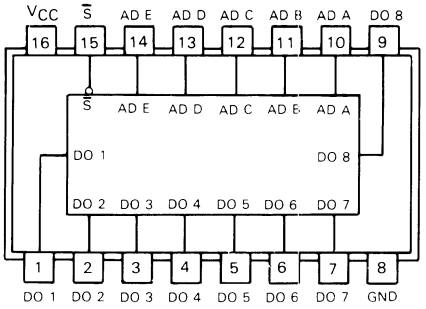
100002375

32 X 8 Bit PROM

PIN CONFIGURATION

Pin 15 is the Programming Pin.

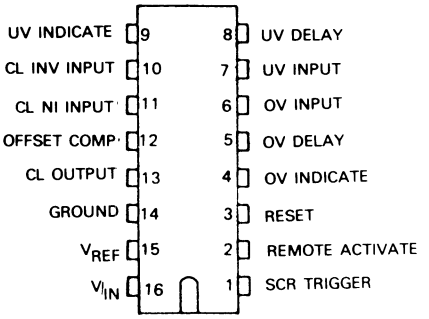


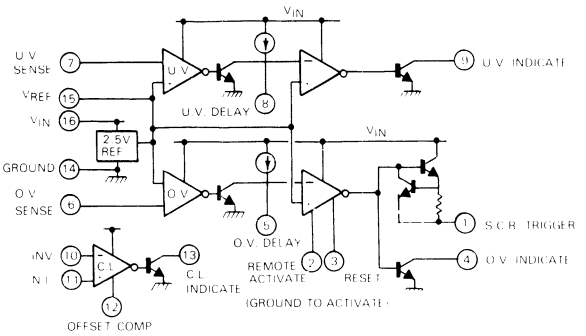
This 256-bit programmable read only memory is a Schottky device with tri-state output. $\overline{S}$ must be low to enable it.

100002377

Power Supply Output Supervisory Circuit

PIN CONFIGURATION





This monolithic integrated circuit has:

- overr-voltage, under-voltage, and current sensing circuits
- 1% accuracy reference voltage
- SCR crowbar drive of 200 mA
- Programmable time delays
- Open collector output which can be used independently or wire-ORed together
- Remote activation capability
- Total standby current less than 10mA

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101000001 through 101000224

PART NO.	REV	DESCRIPTION
101000001	00	XISTOR 2N3724
101000002	01	DIODE FDH600/WG1377
101000003	00	XISTOR 2N4125
101000004	00	XISTOR 2N4441
101000006	00	XISTOR 2N4922
101000013	00	XISTOR MK20
101000015	00	XISTOR 2N3725
101000016	00	XISTOR 2N4123
101000017	00	DIODE 1N5231
101000018	00	XISTOR 2N4918
101000019	00	XISTOR 2N5302
101000021	00	XISTOR 2N3715
101000022	00	DIODE 1N4997
101000023	00	DIODE BRIDGE MDA 962-1
101000024	00	DIODE MDA 950-1
101000026	00	DIODE 1N3879R
101000027	00	DIODE 1N5231 20%
101000028	00	DIODE 1N5240
101000031	00	DIODE ZENER 1N5248B 18V 5%
101000032	00	DIODE 1N5228B
101000036	00	XISTOR 2N5301 SEE 101000019
101000038	00	XISTOR TRIAC T2300B/T2301B
101000039	00	XISTOR SC245B TRIAC
101000040	00	FUSR7723393
101000045	00	XISTOR MPS 3646, 2N3646, SE3646
101000046	00	XISTOR TZ8065
101000048	00	DIODE 1N5252B
101000049	00	DIODE 1N5243B
101000050	00	DIODE CD332864/.5N5/.1ZS1 1%
101000051	00	XISTOR MPS3640
101000052	00	XISTOR 2N4403
101000058	00	DIODE 1N5250B 20V 1%
101000059	00	XISTOR 2N3789/2N3791
101000061	00	XISTOR 2N4919
101000062	02	OBSOLETE REPLACED BY 101000240
101000063	00	XISTOR 2N4399 PNP PWR
101000064	00	XISTOR D43C5 PNP
101000065	00	DIODE 1N3899R 20AMP
101000066	00	DIODE MDA 970-1FW BRIDGE
101000067	00	DIODE ZENER 1N5234B 6.2V
101000068	00	DIODE MDA 962A-1
101000069	00	DIODE 1N5235B/1N754A GLASS
101000070	00	XISTOR 2N4400
101000071	00	DIODE ZENER 1N5251B 22V 5%
101000072	00	DIODE 1N5252B/.5M24ZSE 2%
101000073	00	XISTOR TIP 34
101000074	00	XISTOR TIP 36 PNP
101000075	00	DIODE 1N4001
101000076	00	DIODE LED 209 OBSOLETE SEE 101000208
101000077	00	XISTOR TIP 31 NPN
101000078	00	REPLACED WITH 101000074
101000079	00	XISTOR TRIAC T2800B
101000080	00	DIODE 1N3908R
101000081	00	DIODE 1N5348B
101000082	00	XISTOR GED 45C5
101000083	00	XISTOR 2N4398
101000084	00	DIODE 1N3909R
101000085	01	DIODE 1N3469
101000086	00	DIODE ZENER 1N5248 18V 10%
101000087	00	DIODE ZENER 1N5348 11V
101000088	00	XISTOR 2N2646
101000089	00	DIODE 1N5241B
101000090	00	DIODE 1N5223B
101000091	00	RECT BRDG MOTOROLA MDA 990-1
101000092	00	DIODE 1N4003
101000093	00	DIODE 5245
101000094	00	XISTOR MPS A13
101000095	00	XISTOR 40662 TRIAC
101000096	00	XISTOR OBSOLETE SEE 062
101000097	00	XISTOR CN3566
101000098	00	XISTOR 2N6005
101000099	00	XISTOR 2N6010
101000100	00	DIODE 1N5349
101000101	00	MDA 980-1 BRIDGE RECTIFIER
101000102	00	DIODE 1N3889R
101000103	00	DIODE 1N5231B ZENER
101000104	00	XISTOR TIP 30
101000105	00	XISTOR TIP 29
101000106	00	XISTOR TIP 35
101000107	00	DIODE 40108
101000108	00	DIODE 1N4448
101000109	00	XISTOR TIP 36B
101000110	00	DIODE 1N5242
101000111	00	XISTOR TIP 42A W/INSUL H/W
101000112	01	DIODE 1N5341
101000113	00	DIODE (SEE 101000002)
101000114	00	DIODE CD4148
101000115	00	XISTOR TEXAS INST TIP33
101000116	00	DIODE DUPLICATE (SEE 101000133)
101000117	00	XISTOR HA2-2955A-5 (SEE 100000244)
101000118	00	XISTOR HA1-2625-5 (SEE 100000243)
101000120	00	DIODE 1N4004
101000121	00	RECTIFIER SILICON MR 1205FL
101000122	00	XISTOR 2N6164
101000123	00	XISTOR TIP29A
101000124	00	XISTOR TIP 31A
101000125	00	DIODE 1N5347
101000126	00	DIODE 1N5355

PART NO.	REV	DESCRIPTION
101000127	02	XISTOR PHOTO NPN PLANAR SILICON
101000128	00	XISTOR TIP 36A
101000129	00	XISTOR TRIAC T2400D
101000130	00	XISTOR TRIAC T2300D/T2301D
101000131	00	DIODE 1N3880
101000132	02	DIODE NETWORK 4-CD8(148)
101000133	00	RECT MR 1215SL 80A SILICON RECT
101000134	00	DIODE ZENER 7.5V 1% .5M7.5ZS1
101000135	00	DIODE MR831 MOTOROLA
101000136	00	DIODE 1N5236B
101000137	00	XISTOR TIP 141
101000138	00	XISTOR TIP 146
101000139	00	DIODE 1N4735
101000140	00	XISTOR 2N4393
101000141	00	DIODE ZENER 1N5239B
101000142	00	DIODE RECTIFIER 1N4933 MOTOROLA
101000143	00	DIODE ZENER 1N5347B 10V 5W +5-5%
101000144	00	DIODE ZENER 1N5238B 8.7V 5%
101000145	00	DIODE 1N5259
101000146	00	DIODE 1N4947
101000147	00	DIODE 1N5438B
101000148	00	DIODE 1N4934
101000149	00	DIODE ZENER IN4754
101000150	00	DIODE ZENER IN5229B
101000151	00	DIODE MLED500
101000152	00	TRIAC SC245D
101000153	00	XISTOR TIP35A
101000154	00	XISTOR KE4393-18 TYPE FET
101000155	00	XISTOR 2N4059
101000156	00	DIODE LED RT ANGLE (HP#5082-4415)
101000157	00	XISTOR TIP 48
101000158	00	XISTOR MPS A-42
101000159	00	XISTOR MPS A-92
101000160	00	XISTOR 2N4888
101000161	00	DIODE IN4007 1000V
101000162	00	DIODE IN5223
101000163	00	DIODE ZENER 1N5342B
101000164	00	XISTOR MJE 1100
101000165	00	TRIAC T6411D
101000166	00	XISTOR PWR PNP EP1281
101000167	00	XISTOR PWR NPN EP1278
101000168	00	XISTOR D45H4 PNP
101000169	00	XISTOR TA8327 PNP
101000170	00	XISTOR NJE 2955 PNP
101000171	00	XISTOR RCA 31 NPN
101000172	00	XISTOR D44C5 NPN
101000173	00	XISTOR 2N6122 NPN
101000174	00	XISTOR 2N6125 NPN
101000175	00	XISTOR D45H7 PNP
101000176	00	XISTOR 2N6133 PNP
101000177	00	DIODE IN5343B ZENER
101000178	00	XISTOR 2N6126 PNP/TIP 42B/42C
101000179	00	XISTOR D44H7 NPN
101000180	00	XISTOR 2N5883 PNP
101000181	00	XISTOR 2N3772 PNP
101000182	00	XISTOR EP1285 NPN
101000183	00	XISTOR 2N6129 NPN
101000184	00	XISTOR 2N5987 PNP
101000185	00	DIODE ZENER 1N5221B
101000186	00	DIODE ZENER 1N5222B
101000187	00	DIODE ZENER 1N5223B
101000188	00	DIODE ZENER 1N5224B
101000189	00	DIODE ZENER 1N5226B
101000190	00	DIODE ZENER 1N5227B
101000191	00	DIODE ZENER 1N5230B
101000192	00	DIODE ZENER 1N5232B
101000193	00	DIODE ZENER 1N5233B
101000194	00	DIODE ZENER 1N5237B
101000195	00	DIODE ZENER 1N5240B
101000196	00	DIODE ZENER 1N5242B
101000197	00	DIODE ZENER 1N5244B
101000198	00	DIODE ZENER 1N5245B
101000199	00	XISTOR TIP 41B NPN PWR
101000200	00	XISTOR RCA 41B NPN POWER
101000201	00	?ISTOR 2N6131 UPN POWER
101000202	00	XISTOR RCA 42A PNP POWER
101000203	00	XISTOR 2N 3640
101000204	00	XISTOR BF 338
101000205	00	XISTOR BDY 95
101000206	00	XISTOR PHOTO OP640
101000207	00	DIODE ZENER 9<IV 5W +5% IN5346B
101000208	00	DIODE TIL209A (LED) LT ADMTG
101000209	00	XISTOR 2N3906 00658-01
101000210	00	XISTOR 2N3904 00658-02
101000211	01	ORS REPLACED BY 101000421
101000212	00	XISTOR 2N4442 00658-04
101000213	00	XISTOR TD-101 NPN 100082
101000214	00	XISTOR 2N2219 NPN 100125
101000215	00	XISTOR 2N3053 PNP 100158
101000216	00	XISTOR 2N3055 NPN 100159
101000217	00	XISTOR 2N4037 PNP 100160
101000218	00	XISTOR MPS-U51 NPN 100083
101000219	00	XISTOR 2N3771 NPN 100173
101000220	00	DIODE 1N914 100091
101000221	00	DIODE 1N752 100118
101000222	00	DIODE 1N4736A 100161
101000223	00	DIODE 1N3208 100174
101000224	00	DIODE IN5221 USE 101-185 100121

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101000225 through 101000421

PART NO.	REV	DESCRIPTION
101000225	00	DIODE SCR RCA40654
101000226	00	DIODE RECT BRAKE ASSY
101000227	00	XISTOR MJE 2955
101000228	00	XISTOR MJE 3055
101000229	00	DIODE SZ 3V1/2 W1N52
101000230	00	XISTOR 2N3643
101000231	00	XISTOR 2N5189
101000232	00	XISTOR 2N4916
101000233	00	XISTOR 2N3644
101000234	00	DIODE A14F
101000235	00	XISTOR MPS-U01
101000236	00	XISTOR MPS-U51 SELECTED
101000237	00	DIODE RECT
101000238	00	XISTOR TTY
101000239	00	XISTOR TTY
101000240	01	XISTOR DG5022-240
101000241	00	XISTOR MDA 980-2 BRIDGE
101000242	00	DIODE 5082-2811/2303
101000243	00	TRIAC 2N6165
101000244	00	XISTOR HAMMER DRIVE
101000245	00	XISTOR SPECIAL
101000246	00	XISTOR 2N3253
101000247	00	XISTOR 2N2904
101000248	00	XISTOR 2N2369A
101000249	00	XISTOR 2N2894
101000250	00	SEE 101000216
101000251	00	XISTOR 2N1595
101000252	00	XISTOR 2N1597
101000253	00	XISTOR 2N683
101000254	00	XISTOR 2N5574/5C50D
101000255	00	DIODE SPECIAL SELECT
101000256	00	DIODE SEE 100000092
101000257	00	DIODE 1N752A
101000258	00	DIODE 1N757A
101000259	00	DIODE 1N965
101000260	00	DIODE 1N1192
101000261	00	XISTOR 2N4249
101000262	00	XISTOR 2N3565
101000263	00	DIODE 3A200
101000264	00	(USE 101-103)
101000265	00	DIODE TYPE 125
101000266	00	DIODE 1N2069A
101000267	00	DIODE IN4748A
101000268	00	DIODE
101000269	00	XISTOR 2N5190
101000270	00	XISTOR 2N3868,2N5153,2N6190
101000271	00	DIODE TRIAC
101000272	00	XISTOR 2N2219A
101000273	00	XISTOR 2N3740
101000274	00	DIODE IN823 SEL 6.2V 1%
101000275	00	XISTOR MD2905A
101000276	00	XISTOR MD2219A
101000277	00	DIODE 8 ASSY COMMON ANODE
101000278	00	DIODE 8 ASSY COMMON CATHODE
101000279	00	XISTOR MD2369
101000280	00	XISTOR 2N5683
101000281	00	XISTOR 2N5685
101000282	00	XISTORLTIP-145
101000283	00	XISTOR TIP-140
101000284	00	DIODE RECTIFIER
101000285	00	DIODE SILICON SIGNAL
101000286	00	DIODE PHOTOVOLTAIC
101000287	00	XISTOR PWR 2N5884
101000288	00	DIODE MDA-970 USE 101-66
101000289	00	REPLACED WITH 101000241
101000290	00	XISTOR MJE1103
101000291	00	XISTOR PHOTO SPECIAL
101000292	00	DIODE MDA-952-1
101000293	00	XISTOR MM4001
101000294	00	XISTOR MM3009
101000295	00	XISTOR SEE 101-298
101000296	00	XISTOR PN4258A PBP
101000297	00	XISTOR MPS 2369
101000298	00	XISTOR SPECIAL
101000299	00	XISTOR 2N4091
101000300	00	DIODE LED TIL 220
101000301	00	DIODE, IN3062,TID778,FDN700
101000302	EE00	DIODE IN3317
101000303	EE00	DIODE IN3305
101000304	00	XISTOR OUTLINE READOUT ASSY CTG DISK
101000305	00	XISTOR 2N2905A
101000306	00	OBSOLETE, DO NOT USE
101000307	00	DIODE MDA990-2
101000308	00	TRIAC 200V T27 10B
101000309	00	XISTOR 2N3810
101000310	00	XISTOR 2N2920
101000311	00	DIODE IN5352B
101000312	00	DIODE IN5362B
101000313	00	DIODE IN823
101000314	00	OBSOLETE ,REPLACED BY 101000400
101000315	00	XISTOR TIP 31B
101000316	00	XISTOR 2N6050 PNP
101000317	00	XISTOR 2N6057 NPN
101000318	00	XISTOR MJE 2090
101000319	00	XISTOR TIP 32A
101000320	00	XISTOR MJE 2100
101000321	00	DIODE ZENER IN5350A
101000322	00	MOX TS3-65
101000323	00	XISTOR 2N6030
101000324	00	XISTOR 2N5630
101000325	00	XISTOR PN2907A PNP
101000326	01	DIODE A114M, IN4937
101000327	01	DIODE SCR 2N3896
101000328	EE00	PHOTO SENSOR SILICON S1010GE6PL
101000329	00	XISTOR TIP30A
101000330	00	DIODE LED, RED MV5054-3 5082-4655
101000331	00	XISTER 2N5573
101000332	00	XISTOR TIP 32B
101000333	00	DIODE 1N4998
101000334	00	DIODE LED DSPL TIL-313
101000335	00	DIODE 1N1184A
101000336	00	DIODE MR 1121
101000337	01	XISTOR MJ410 RCA410
101000338	00	XISTOR MJE 5191
101000339	00	XISTOR MJE 5194
101000340	00	DIODE IN5148A
101000341	00	DIODE HOT CARRIER, PAIR 5082-2804
101000342	00	XISTOR 2N4033 PNP SWITCHING
101000343	00	XISTOR 2N3019 NPN LOW PWR
101000344	00	XISTOR PWR MJ4502 TO-3 CASE
101000345	00	XISTOR PWR MJ802 TO-3 CASE
101000346	00	XISTOR MPS A55
101000347	00	XISTOR MPS A05
101000348	00	XISTOR TRIAC T6420M
101000349	00	DIODE HOT CARRIER A2S807 5082-2800
101000350	00	XISTOR 2N5771-18 PNP
101000351	00	DIODE MR752
101000352	00	XISTOR 2N4392 FET
101000353	00	XISTOR MPS A06
101000354	00	XISTOR MPS A56
101000355	00	DIODE BRIDGE
101000356	EE00	SEE 123001038
101000357	EE00	DIODE 5082-2835 SCHOTTKY
101000358	EE00	XISTOR TP115 PNP
101000359	EE00	XISTOR TIP 120 NPN
101000360	00	DIODE 1N5359A
101000361	00	DIODE 1N4005
101000362	00	DIODE 1N5254B ZENER
101000363	02	DIODE A5C663
101000364	00	DIODE BRG RECT FULL WAVE SGL PHASE
101000365	EE00	DIODE MR860
101000366	00	OBSOLETE, REPLACED BY 101000369
101000367	00	XISTOR 2N5038
101000368	00	DIODE ZENER 1N5338B 5.1V
101000369	00	XISTOR PWR 2N5671
101000370	00	DIODE IN3900
101000371	00	XISTOR 2N4124 NPN SILICON
101000372	00	XISTOR MD708B DUAL NPN
101000373	00	DIODE 1N5395
101000374	00	DIODE 2N6386 NPN
101000375	00	RECT 1N6098 PWR SCHOTTKY
101000376	00	RECT 2N6504
101000377	02	DIODE 5082-4658 LED
101000378	00	RECT HOT CARRIER PWR IN6096
101000379	00	DIODE IN5817
101000380	00	REGULATOR A8W (6052) 48S137368
101000381	00	XISTOR TIP110 60V 2A NPN
101000382	01	MJ425/2N6545
101000383	00	RECT BRIDGE SILICONE B610-60 6A 600V
101000384	00	DIODE ZENER 4.7V 1% (500MW)
101000385	00	DIODE 6A SWITCH UES1302
101000386	EE00	DIODE SILICON TRIAC 8A ISOLAB
101000387	00	XISTOR PNP SILICON DARLINGTON ECLIPSE
101000388	00	DIODE MOTOROLA IN 5200 SER SEL TO 1%
101000389	EE00	DIODE ZENER IN5240 10V 1% SELECTED
101000390	00	XISTOR 2N4391 N CHAN SWITCHING FET
101000391	00	RECT FAST RECOVERY 3AMP 200V
101000392	00	DIODE 1N3913R 30A
101000393	00	DIODE 30AMP 50V FAST RECOVERY REC PKG
101000394	00	DIODE 1N2993B ZENER 10W 43V +5-5%
101000395	00	XISTER 2N6032
101000396	00	RECT HALF-WAVE IN TO-3PKG COM CATHODE
101000397	00	DIODE MR 756 6A/600V PIV 400A IFSM
101000398	00	DIODE 400V FAST RECOVERY IN3883
101000399	00	XISTOR,D40D4
101000400	00	DIODE,SCHOTTY DO-5 40AMP 30V IN6097
101000401	00	XISTOR MJ3029 LCCRT 48-137596
101000402	00	XISTOR MJ3761 LCCRT 48-137596
101000403	00	XISTOR FLY BACK SWITCHING
101000404	00	DIODE TRANSIENT ABSORB P6KE6.8A
101000405	00	XISTOR DARLINGTON PWR 2N6058
101000406	00	OPTICAL SWITCH HOME SENSOR
101000407	00	DIODE SCHOTTKG 30AMP 40V TO 3
101000408	00	DIODE SCHOTTKG 3AMP IN5820 DGC CMPTR
101000409	00	DIODE FULL WAVE BRIDGE 4A 600V MN P/S
101000410	00	XISTOR NPN SILICON PWR
101000411	00	DIODE HIGH VOLT 3KV PIV HX30PD
101000412	EE00	DIODE H617 HX200LP
101000413	00	XISTOR TO-3 PWR MJ-2955
101000414	00	DIODE BRIDGE MDA 3506 DGC P/S
101000415	01	XISTOR HI VOLT INDTR SWITCHING
101000416	00	XISTOR SERIES SWITCH
101000417	00	DIODE 800V FAST RECOVERY CS/20
101000418	00	XISTOR NPN D40E7
101000420	00	DIODE FAST RECOVERY MR821
101000421	00	DIODE ZENER 16V 1/2W 5% IN5246B

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101000422 through 102000118

PART NO.	REV	DESCRIPTION
101000422	EE00	DIODE ZENER 1% 28V IN5362
101000423	00	RECT IN3890
101000424	00	RECT BRIDGE I.R. 250JBIL
101000425	01	XISTOR SWITCHING HI VOLTAGE
101000426	00	XISTOR TIP 33C
101000427	00	DIODE 1/2W 14V 1% ZENER
101000428	00	XISTOR SCR MCR202 DGC-JR
101000429	EE00	DIODE LED GREEN 5082-4955
101000430	00	DIODE BRIDGE MDA350R
101000431	EE00	DIODE DUAL 15A 200NS PIV 50V TO3 CATH
101000432	EE00	XISTOR LOW PWR NPN 2N5550
101000433	EE00	XISTOR DARLING PWR MOTOROLA MJ11015
101000434	EE00	XISTOR NPN DARLINGTON PWR MJ11016
101000435	EE00	XISTOR PWR MOTOROLA 2N5339
101000436	EE00	XISTOR PWR MOTOROLA 2N6193
101000437	EE00	XISTOR PWR TIP41C
101000438	EE00	DIODE ZENER 1N4743B
101000439	EE00	DIODE CURRENT REGULATOR IN5314
101000440	00	XISTOR PWR MM5007
101000441	00	XISTOR PWR 2N5339
101000442	00	DIAC ST2
101000443	00	XISTOR TIP152
101000444	00	DIODE ZENER 36V 5W IN5365B
101000445	EE00	DIODE ZENER 17V 5% DGC-JR
101000446	00	INDICATOR HI-AMBIENT LED GRN TSTEQ
101000447	00	INDICATOR HI-AMBIENT LED RED TSTEQ
101000448	00	INDICATOR HI-AMBIENT LED YEL TSTEQ
101000449	00	DIODE 15A 400V IN3212
101000450	00	DIODE IN4948 FAST RECOVERY 1000V
101000451	EE00	DIODE ZENER TRANSIENT SUPPRESSOR 5V
101000452	EE00	DIODE ZENER TRANSIENT SUPPRESSOR 15V
101000453	00	RECTIFIER SCR 600V 10A S2R00M
101000454	00	RECTIFIER FAST RECOVERY MR831
101000455	00	DIODE IN5393
101000460	00	RECTIFIER SILICON CTL C156A-92RM10
101000461	00	DIODE ZENER IN4729A
101000462	00	XISTOR SWITCHMODE NPN 400V 8A
101000463	00	DIODE 800V D2201N , S8M
101000464	00	DIODE DUAL PKG P714X
101000465	02	TRANSDUCER OPTICAL AEW01-CV
101000466	EE00	RECTIFIER FAST REC 200V 6A 200NS
101000468	EE00	XISTOR PWR NPN 100V TIP31C
101000472	EE00	RECTIFIER FAST RECOVERY IN3890R
101000473	00	DIODE ARRAY 16X0/20 13010
101000475	EE00	RECTIFIER PWR IN1186A
101000476	EE00	RECTIFIER PWR IN1186AR
101000478	00	DIODE DUAL IN TO3 FASY RECOVERY
101000479	EE00	DIODE SCR C147A
101000480	EE00	DIODE SCR C230F2,C230F3
101000482	00	MPSA43
101000483	00	MPSU60
101000484	00	SR3142
101000485	00	MR820
101000486	00	MR502
101000487	00	MR852
101000488	00	IN4002 10369
101000489	00	1N4454 10160
101000490	00	1N5415 13054
101000491	00	1N4736A 10329
101000492	00	1N5807 10424-01
101000493	00	1N4733 10103-05
101000495	00	XISTOR TIP 125 13007
101000496	00	XISTOR 2N4401 13013
101000497	00	XISTOR 2N5320 10443-01
101000498	00	XISTOR 2N5322 10444-01
101000499	00	XISTOR 2N6103 10445-01
101000500	00	XISTOR PN3644 13070
101000501	00	XISTOR MPS5162
101000502	00	XISTOR TIP 47
101000503	00	XISTOR GEC 122F
101000504	00	XISTOR 2N4126
101000505	EE00	SOLID STATE LED LAMP (GREEN)
101000506	EE00	SOLID STATE LED LAMP (YELLOW)
101000508	EE00	DIODE SWITCHING SILICON IN4607
101000509	EE00	XISTOR PWR NPN TIP51
101000510	00	DIODE ZENER IN5257B 33V 5% 1/2W
101000511	EE00	XISTOR 2N5031 NPN SILICON RF SM SGL
101000512	EE00	XISTOR 2N5875 PNP 10A
102000001	00	RES 2.70 OHM 1/4W 5%
102000002	00	RES 3.00 OHM 1/4W 5%
102000003	00	RES 3.30 OHM 1/4W 5%
102000004	00	RES 3.60 OHM 1/4W 5%
102000005	00	RES 3.90 OHM 1/4W 5%
102000006	00	RES 4.30 OHM 1/4W 5%
102000007	00	RES 4.70 OHM 1/4W 5%
102000008	00	RES 5.10 OHM 1/4W 5%
102000009	00	RES 5.60 OHM 1/4W 5%
102000010	00	RES 6.20 OHM 1/4W 5%
102000011	00	RES 6.80 OHM 1/4W 5%
102000012	00	RES 7.50 OHM 1/4W 5%
102000013	00	RES 8.20 OHM 1/4W 5%
102000014	00	RES 9.10 OHM 1/4W 5%
102000015	00	RES 10.00 OHM 1/4W 5%
102000016	00	RES 11.00 OHM 1/4W 5%
102000017	00	RES 12.00 OHM 1/4W 5%
102000018	00	RES 13.00 OHM 1/4W 5%
102000019	00	RES 15.00 OHM 1/4W 5%
102000020	00	RES 16.00 OHM 1/4W 5%

PART NO.	REV	DESCRIPTION
102000021	00	RES 18.00 OHM 1/4W 5%
102000022	00	RES 20.00 OHM 1/4W 5%
102000023	00	RES 22.00 OHM 1/4W 5%
102000024	00	RES 24.00 OHM 1/4W 5%
102000025	00	RES 27.00 OHM 1/4W 5%
102000026	00	RES 30.00 OHM 1/4W 5%
102000027	EE00	S (DUPLICATE PART, SEE 102000263)
102000028	00	RES (DUPLICATE PART,SEE 102000286)
102000029	00	RES 39.00 OHM 1/4W 5%
102000030	00	RES 43.00 OHM 1/4W 5%
102000031	00	RES 47.00 OHM 1/4W 5%
102000032	00	RES 51.00 OHM 1/4W 5%
102000033	00	RES 56.00 OHM 1/4W 5%
102000034	00	RES 62.00 OHM 1/4W 5%
102000035	00	RES 68.00 OHM 1/4W 5%
102000036	00	RES 75.00 OHM 1/4W 5%
102000037	00	RES 82.00 OHM 1/4W 5%
102000038	00	RES (DUPLICATE PART,SEE 102000253)
102000039	00	RES 100.00 OHM 1/4W 5%
102000040	00	RES 110.00 OHM 1/4W 5%
102000041	00	RES 120.00 OHM 1/4W 5%
102000042	00	RES 130.00 OHM 1/4W 5%
102000043	00	RES 150.00 OHM 1/4W 5%
102000044	00	RES 160.00 OHM 1/4W 5%
102000045	00	RES 180.00 OHM 1/4W 5%
102000046	00	RES 200.00 OHM 1/4W 5%
102000047	00	RES 220.00 OHM 1/4W 5%
102000048	00	RES 240.00 OHM 1/4W 5%
102000049	00	RES 270.00 OHM 1/4W 5%
102000050	00	RES 300.00 OHM 1/4W 5%
102000051	00	RES 330.00 OHM 1/4W 5%
102000052	00	RES 360.00 OHM 1/4W 5%
102000053	00	RES 390.00 OHM 1/4W 5%
102000054	00	RES 430.00 OHM 1/4W 5%
102000055	00	RES 470.00 OHM 1/4W 5%
102000056	00	RES 510.00 OHM 1/4W 5%
102000057	00	RES 560.00 OHM 1/4W 5%
102000058	00	RES 620.00 OHM 1/4W 5%
102000059	00	RES 680.00 OHM 1/4W 5%
102000060	00	RES 750.00 OHM 1/4W 5%
102000061	00	RES 820.00 OHM 1/4W 5%
102000062	00	RES 910.00 OHM 1/4W 5%
102000063	00	RES 1.00K OHM 1/4W 5%
102000064	00	RES 1.10K OHM 1/4W 5%
102000065	00	RES 1.20K OHM 1/4W 5%
102000066	00	RES 1.30K OHM 1/4W 5%
102000067	00	RES 1.50K OHM 1/4W 5%
102000068	00	RES 1.60K OHM 1/4W 5%
102000069	00	RES 1.80K OHM 1/4W 5%
102000070	00	RES 2.00K OHM 1/4W 5%
102000071	00	RES 2.20K OHM 1/4W 5%
102000072	00	RES 2.40K OHM 1/4W 5%
102000073	00	RES 2.70K OHM 1/4W 5%
102000074	00	RES 3.00K OHM 1/4W 5%
102000075	00	RES 3.30K OHM 1/4W 5%
102000076	00	RES 3.60K OHM 1/4W 5%
102000077	00	RES 4.30K OHM 1/4W 5%
102000078	00	RES 4.70K OHM 1/4W 5%
102000079	00	RES 5.10K OHM 1/4W 5%
102000080	00	RES 5.60K OHM 1/4W 5%
102000081	00	RES 6.20K OHM 1/4W 5%
102000082	00	RES 6.80K OHM 1/4W 5%
102000083	00	RES 7.50K OHM 1/4W 5%
102000084	00	RES 8.20K OHM 1/4W 5%
102000085	00	RES 9.10K OHM 1/4W 5%
102000086	00	RES 10.00K OHM 1/4W 5%
102000087	00	RES 11.00K OHM 1/4W 5%
102000088	00	RES 12.00K OHM 1/4W 5%
102000089	00	RES 13.00K OHM 1/4W 5%
102000090	00	RES 15.00K OHM 1/4W 5%
102000091	00	RES 16.00K OHM 1/4W 5%
102000092	00	RES 18.00K OHM 1/4W 5%
102000093	00	RES 20.00K OHM 1/4W 5%
102000094	00	RES 22.00K OHM 1/4W 5%
102000095	00	RES 24.00K OHM 1/4W 5%
102000096	00	RES 27.00K OHM 1/4W 5%
102000097	00	RES 30.00K OHM 1/4W 5%
102000098	00	RES 33.00K OHM 1/4W 5%
102000099	00	RES 36.00K OHM 1/4W 5%
102000100	00	RES 39.00K OHM 1/4W 5%
102000101	00	RES 43.00K OHM 1/4W 5%
102000102	00	RES 47.00K OHM 1/4W 5%
102000103	00	RES 51.00K OHM 1/4W 5%
102000104	00	RES 56.00K OHM 1/4W 5%
102000105	00	RES 62.00K OHM 1/4W 5%
102000106	00	RES 68.00K OHM 1/4W 5%
102000107	00	RES 75.00K OHM 1/4W 5%
102000108	00	RES 82.00K OHM 1/4W 5%
102000109	00	RES 91.00K OHM 1/4W 5%
102000110	00	RES 100.00K OHM 1/4W 5%
102000111	00	RES 110.00K OHM 1/4W 5%
102000112	00	RES 120.00K OHM 1/4W 5%
102000113	00	RES 130.00K OHM 1/4W 5%
102000114	00	RES 150.00K OHM 1/4W 5%
102000115	00	RES 160.00K OHM 1/4W 5%
102000116	00	RES 180.00K OHM 1/4W 5%
102000117	00	RES 200.00K OHM 1/4W 5%
102000118	00	RES 220.00K OHM 1/4W 5%

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102000119 through 102000316

PART NO.	REV	DESCRIPTION
102000119	00	RES 240.00K OHM 1/4W 5%
102000120	00	RES 270.00K OHM 1/4W 5%
102000121	00	RES 300.00K OHM 1/4W 5%
102000122	00	RES 330.00K OHM 1/4W 5%
102000123	00	RES 360.00K OHM 1/4W 5%
102000124	00	RES 390.00K OHM 1/4W 5%
102000125	00	RES 430.00K OHM 1/4W 5%
102000126	00	RES 470.00K OHM 1/4W 5%
102000127	00	RES 510.00K OHM 1/4W 5%
102000128	00	RES 560.00K OHM 1/4W 5%
102000129	00	RES 620.00K OHM 1/4W 5%
102000130	00	RES 680.00K OHM 1/4W 5%
102000131	00	RES 750.00K OHM 1/4W 5%
102000132	00	RES 820.00K OHM 1/4W 5%
102000133	00	RES 910.00K OHM 1/4W 5%
102000134	00	RES 1.00M OHM 1/4W 5%
102000135	00	RES 1.10M OHM 1/4W 5%
102000136	00	RES 1.20M OHM 1/4W 5%
102000137	00	RES 1.30M OHM 1/4W 5%
102000138	00	RES 1.50M OHM 1/4W 5%
102000139	00	RES 1.60M OHM 1/4W 5%
102000140	00	RES 1.80M OHM 1/4W 5%
102000141	00	RES 2.00M OHM 1/4W 5%
102000142	00	RES 2.20M OHM 1/4W 5%
102000143	00	RES 2.40M OHM 1/4W 5%
102000144	00	RES 2.70M OHM 1/4W 5%
102000145	00	RES 3.00M OHM 1/4W 5%
102000146	00	RES 3.30M OHM 1/4W 5%
102000147	00	RES 3.60M OHM 1/4W 5%
102000148	00	RES 3.90M OHM 1/4W 5%
102000149	00	RES 4.30M OHM 1/4W 5%
102000150	00	RES 4.70M OHM 1/4W 5%
102000151	00	RES 5.10M OHM 1/4W 5%
102000152	00	RES 5.60M OHM 1/4W 5%
102000153	00	RES 6.20M OHM 1/4W 5%
102000154	00	RES 6.80M OHM 1/4W 5%
102000155	00	RES 7.50M OHM 1/4W 5%
102000156	00	RES 8.20M OHM 1/4W 5%
102000157	00	RES 9.10M OHM 1/4W 5%
102000158	00	RES 10.00M OHM 1/4W 5%
102000159	00	RES 11.00M OHM 1/4W 5%
102000160	00	RES 12.00M OHM 1/4W 5%
102000161	00	RES 13.00M OHM 1/4W 5%
102000162	00	RES 15.00M OHM 1/4W 5%
102000163	00	RES 16.00M OHM 1/4W 5%
102000164	00	RES 18.00M OHM 1/4W 5%
102000165	00	RES 20.00M OHM 1/4W 5%
102000166	00	RES 22.00M OHM 1/4W 5%
102000167	00	RES 24.00M OHM 1/4W 5%
102000168	00	RES 27.00M OHM 1/4W 5%
102000169	00	RES 30.00M OHM 1/4W 5%
102000170	00	RES 33.00M OHM 1/4W 5%
102000171	00	RES 36.00M OHM 1/4W 5%
102000172	00	RES 39.00M OHM 1/4W 5%
102000173	00	RES 43.00M OHM 1/4W 5%
102000174	00	RES 47.00M OHM 1/4W 5%
102000175	00	RES 51.00M OHM 1/4W 5%
102000176	00	RES 56.00M OHM 1/4W 5%
102000177	00	RES 62.00M OHM 1/4W 5%
102000178	00	RES 68.00M OHM 1/4W 5%
102000179	00	RES 75.00M OHM 1/4W 5%
102000180	00	RES 82.00M OHM 1/4W 5%
102000181	00	RES 91.00M OHM 1/4W 5%
102000182	00	RES 100.00M OHM 1/4W 5%
102000183	00	RES 5.00 OHM 1/4W 5%
102000185	00	RES 150.00 OHM 1/10W 1%
102000186	01	RES 17.50 OHM 3W 1%
102000187	00	RES 22.50 OHM 3W 1%
102000188	01	RES .10 OHM 3W 1%
102000189	01	RES 1.00 OHM 3W 5%
102000190	00	RES 10.00K OHM 10W %
102000191	00	RES 180.00 OHM 2W 5%
102000192	01	RES 180.00 OHM 3W 5%
102000193	01	RES 330.00 OHM 3W 5%
102000194	01	RES 470.00 OHM 3W 5%
102000195	01	RES 600.00 OHM 3W 5%
102000196	00	RES 1.00 OHM 5W %
102000197	00	RES 4.00K OHM 10W %
102000198	00	RES 12.00K OHM 1/4W 5%
102000199	00	RES NETWORK SUBSTRATE
102000200	00	RES . OHM W % THMC
102000201	00	RES 3.90K OHM 1/4W 5%
102000202	00	RES 15.00 OHM W 1% NON IND
102000203	00	RES 12.50 OHM W 1% NON IND
102000204	00	RES 11.00 OHM W 1%
102000205	00	RES 14.00 OHM W 1%
102000206	01	RES 680.00 OHM 2W 5%
102000207	00	RES 95.30 OHM W 1%
102000208	00	RES 25.00 OHM W %
102000209	00	RES 470.00 OHM 1W 5%
102000210	00	RES 1.50K OHM 1/8W 1%
102000211	00	RES 1.65K OHM 1/8W 1%
102000212	00	RES 1.82K OHM 1/8W 1%
102000213	00	RES 2.00K OHM 1/8W 1%
102000214	00	RES 2.21K OHM 1/8W 1%
102000215	00	RES 15.00K OHM 1/8W 1%
102000216	00	RES 1.30K OHM 1/8W 1%
102000217	00	RES 200.00 OHM 1/8W 5%

PART NO.	REV	DESCRIPTION
102000218	00	RES 240.00 OHM 1/8W 5%
102000219	00	RES 330.00 OHM 1/8W 5%
102000220	00	RES 390.00 OHM 1/8W 5%
102000221	00	POT 2.00K OHM 1W 10%
102000222	00	POT 20.00K OHM 1W 10%
102000223	00	RES 11.00 OHM W 2%
102000224	00	RES 14.00 OHM 1%
102000225	00	THM 4" DISC 300 FNWL LA23W1
102000226	01	RES 95.30 OHM 1/2W 1%
102000227	01	RES 25.00 OHM 3W 5%
102000228	01	RES 8.00 OHM 4W 3%
102000229	01	RES 30.00 OHM 3W 1%
102000230	01	RES .20 OHM 10W 5%
102000231	00	RES .50 OHM 3W 5%
102000232	01	RES 4.00 OHM 5W 5%
102000233	00	RES 390.00 OHM 1/2W 5%
102000234	00	RES 10.00 OHM 1/2W 5%
102000235	00	POT 100.00 OHM 1/2W 10%
102000236	01	RES 390.00 OHM 3W 5%
102000237	00	RES 180.00 OHM 1W 5%
102000238	01	RES 11.00 OHM 4W 3%
102000239	01	RES 14.00 OHM 3W 1%
102000240	01	RES 53.60 OHM 3W 1%
102000241	00	RES 10.00K OHM 1/4W 1%
102000242	00	RES 3.32K OHM 1/4W 1%
102000243	00	RES 12.10K OHM 1/8W 1%
102000244	00	RES 5.62K OHM 1/8W 1%
102000245	00	THM 5.00K OHM W % THMC
102000246	01	RES 17.50 OHM 3W 1%
102000247	01	RES 75.00 OHM 3W 1%
102000248	01	RES 100.00 OHM 3W 1%
102000249	00	RES 10.00 OHM 1/4W 1%
102000250	00	RES 6.81K OHM 1/4W 1%
102000251	01	RES 1.50 OHM 3W 5% W.W.
102000252	00	RES 270.00 OHM 1W 5% CARBON
102000253	00	RES 91.00 OHM 1/4W 5% PIH/COR
102000254	00	RES 30.00 OHM 1/4W 5%
102000255	00	RES 91.00 OHM 1/2W 5%
102000256	00	RES 7.87K OHM 1/4W 1%
102000257	01	RES 38.00 OHM 3W 1% A-P WOU
102000258	00	RES 47.00 OHM 1/2W 5%
102000259	00	RES 3.60 OHM 1W 5% CARBON
102000260	01	RES 50.00 OHM 5W 5%
102000261	00	RES 130.00 OHM 1/4W 5% PIHER
102000262	00	RES 3.00 OHM 1W 5% CARBON
102000263	00	RES 33.00 OHM 1/4W 5% PIHER
102000264	00	RES 160.00 OHM 1/4W 5% PIHER 0
102000265	00	RES 27.00 OHM 1/2W 5% (1/2WR)
102000266	01	RES 150.00 OHM 3W 1% A-P WOU
102000267	00	RES 220.00 OHM 1/2W 5% CARBON
102000268	00	RES 30.00 OHM 1/2W 5%
102000269	00	RES 510.00 OHM 1/2W 5% CARBON
102000270	00	RES 7.50 OHM 2W 5% 0
102000271	00	RES 34.00 OHM 1/4W 1%
102000272	01	RES .05 OHM 5W 5% W/W
102000273	00	RES 470.00 OHM 1/2W 5%
102000274	00	RES 1.50 OHM 1/2W 5% CARBON
102000275	00	RES 1.50 OHM 20W
102000276	00	RES 15.00 OHM 12W
102000277	00	RES 50.00 OHM 20W
102000278	00	RES DUMMY
102000279	00	RES 120-00 OHM 1/2W 5% PIHER/CRNG C5M
102000280	00	RES 140.00 OHM 1/2W 2%
102000281	00	RES 5.10K OHM 2W 5% CARBON
102000282	00	RES 10.00K OHM 2W 5% CARBON
102000283	00	RES 1.00K OHM 1/2W 5%
102000284	00	POT 5.00K OHM
102000285	00	POT 500.00K OHM
102000286	00	RES 36.0 OHM 1/4W 5%
102000287	00	RES 39.00 OHM 1/4W 5% PIHER
102000288	00	POT 50.00K OHM 1W 10%
102000289	01	RES .10 OHM 10W 5%
102000290	00	RES 75.00 OHM 1W 5%
102000291	01	RES 0.50 OHM 10W 5%
102000292	00	RES 82.00 OHM 1/2W 5%
102000293	00	POT 500.00 OHM W %
102000294	00	POT 1.00K OHM 5%
102000295	00	POT 10.00K OHM 5%
102000296	00	RES 50.00 OHM 50W 5%
102000297	00	RES 150.00 OHM 1/8W 1%
102000298	00	RES 6.80K OHM 1/8W 1%
102000300	00	RES 6.80 OHM 1/2W 5%
102000301	00	RES 150.00 OHM 2W 5%
102000302	00	RES 12.00 OHM 5W 5%
102000303	00	POT 500.00 OHM 1W 10%
102000304	00	RES 1.00K OHM 1/4W 1%
102000305	00	POT 10.00K OHM 3/4W
102000306	00	POT 20.00K OHM 3/4W
102000307	00	POT 100.00K OHM 3/4W
102000308	00	NET RES NTWK300145-6K-6K
102000309	00	POT 1.00M OHM 1/2W 20%
102000310	00	RES 20.00K OHM 2W 5%
102000311	00	RES 51.00 OHM 1/2W 5% PIHER
102000312	00	RES 7.32K OHM 1/4W 1%
102000313	01	RES 100.00 OHM 3W 5%
102000314	01	RES 125.00 OHM 3W 5%
102000315	00	RES 330.00 OHM 1/2W 2%
102000316	00	RES 6.8K OHM 1/2W 5%

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102000317 through 102000513

PART NO.	REV	DESCRIPTION
102000317	01	RES 110.00 OHM 3W 5%
102000318	00	RES 14.70 OHM 1/8W 1%
102000320	00	RES 68.00 OHM 1/2W 5%
102000321	00	RES 3.01K OHM 1/8W 1%
102000322	00	RES 511.00 OHM 1/4W 1%
102000323	00	RES 1.47K OHM 1/8W 1%
102000324	00	RES 1.96K OHM 1/4W 1% METFILM
102000325	00	RES 3.24K OHM 1/4W 1% METFILM
102000326	00	RES 4.42K OHM 1/4W 1% METFILM
102000327	00	RES 4.99K OHM 1/4W 1% METFILM
102000328	00	RES 2222.00 OHM 1/10W .02%
102000329	00	RES 1778.00 OHM 1/10W .02%
102000330	00	RES 2667.00 OHM 1/10W .02%
102000331	00	RES 3333.00 OHM 1/10W .02%
102000332	00	RES 10.00K OHM 1/10W .02%
102000333	01	VRIS HV SURGE SUPPR
102000334	01	RES 30.00 OHM 3W 5%
102000335	01	RES 30.00 OHM 1W 5%
102000336	01	RES 1.00 OHM 25W 5%
102000337	01	RES 8.00 OHM 4W 1%
102000338	01	RES 30.00 OHM 10W 5%
102000339	01	RES 14.00 OHM 10W 1%
102000340	01	RES .10 OHM 5W 1%
102000341	01	RES 5.00K OHM 5W 1%
102000342	00	RES 510.00 OHM 2W 5%
102000343	00	RES 1.05K OHM 1/4W 1%
102000344	00	RES 1.21K OHM 1/4W 1%
102000345	00	RES 4.02K OHM 1/4W 1%
102000346	00	RES 2.05K OHM 1/4W 1%
102000347	00	RES 5.11K OHM 1/4W 1%
102000348	01	RES 1.00 OHM 30W 5%
102000349	01	RES 10.00 OHM 30W 5%
102000350	00	RES (DUPLICATE PART,SEE 102000260)
102000351	01	RES 14.00 OHM 10W 5%
102000352	01	RES 8.00 OHM 5W 1%
102000353	01	RES 33.00 OHM 10W 5%
102000354	00	RES DUPLICATE PART SEE 102000335
102000355	00	RES 330.00 OHM 1/8W 1%
102000356	00	RES 140.00 OHM 1/8W 1%
102000357	01	RES 10.00 OHM 5W 5%
102000358	00	POT 20.00K OHM 1/2W 20%
102000359	02	NET 4-105+-2% 1/10W
102000360	00	RES 20.00K OHM 5W 5%
102000361	00	RES 10.00K OHM 5W 5%
102000362	01	RES 11.100 OHM 4W 5%
102000363	00	P.O.T. 500.00 OHM 1/4W 10%
102000364	01	RES 12.00 OHM 4W 5% NON-IND
102000365	01	RES 15.00 OHM 3W 5%
102000366	00	VRIS 1KV2610A10QS
102000367	00	RES 180.00 OHM 1/2W 5%
102000368	01	RES 110.00 OHM 5W 5%
102000369	00	RES 2.37K OHM 1/4W 1%
102000370	00	THM 230.00 OHM .006W 5% KA22L2
102000371	00	RES 196.00 OHM 1/8W 1%
102000372	00	RES 464.00 OHM 1/8W 1%
102000373	00	RES 300.00 OHM 1W 5%
102000374	00	RES 51.10K OHM 1/4W 1%
102000375	00	POT 200.00 OHM 1W 10%
102000376	00	RES 150.00 OHM 1W 5%
102000377	00	RES 3.00 OHM 2.5W 5% ELZH
102000378	00	POT 100.00 OHM 3/4 10% CERMET
102000379	00	RES (OBSOLETE, SEE 102000344)
102000380	00	RES 931.00 OHM 1/4W 1%
102000381	00	RES 475.00 OHM 1/4W 1%
102000382	00	RES 442.00 OHM 1/4W 1%
102000383	00	RES 316.00 OHM 1/4W 1%
102000384	00	RES 150.00 OHM 1/4W 1%
102000385	00	RES 118.00 OHM 1/4W 1%
102000386	00	RES 100.00 OHM 1/2W 5%
102000387	01	RES 1.00 OHM 10W 5%
102000388	00	RES 1.00K OHM 1W 5%
102000389	00	RES 330.00 OHM 1/2W 5%
102000390	01	RES .10 OHM 2 1/2W 3%
102000391	01	RES 82.00 OHM 3W 1%
102000392	00	RES 680.00 OHM 1W 5% COMP
102000393	01	RES .20 OHM 1W 5%
102000394	00	POT 100.00 OHM 25T SQ 10% CERMET
102000395	00	RES 110.00 OHM 1/2W 5%
102000396	01	RES 5.00 OHM 225W OHMITE ADJ.
102000397	00	RES 33.00K OHM 1/2W 5%
102000398	00	RES 30.10 OHM 1/8W 1%
102000399	01	RES 510.00 OHM 2W 5% WR WND
102000400	00	RES 5.00 OHM 25W +5%
102000401	00	RES 2.00 OHM 25W +5%
102000402	00	POT 4.0000 OHM 3W 10%
102000403	00	RES 13.50K OHM 1/4W 1%
102000404	00	POT 5.00K OHM 100069-502
102000405	00	POT 20.00K OHM 100069-203
102000406	00	POT 500.00 OHM 100163-501
102000407	00	POT 1.00K OHM 100163-102
102000408	00	POT 5.00K OHM 100163-502
102000409	00	POT 10.00K OHM 100163-103
102000410	00	POT 20.00K OHM 100163-203
102000411	00	POT 50.00 OHM 100069-500
102000412	01	RES 4.00 OHM 10W 5%
102000413	01	RES .20 OHM 2W 5%
102000414	01	RES 2.2K OHM 1/2W 0% W/W
102000415	00	RES HAMMER DRIVER 800210-001

PART NO.	REV	DESCRIPTION
102000416	00	RES 34.00 OHM 1/4W +5%
102000417	00	RES 50.000 OHM 100W TR-AN500D
102000418	00	RES 15.00 OHM 25W TRAI150D
102000419	00	RES 1.10 OHM 1/2W +5%
102000420	00	RES 22.00 OHM 1/2W +5%
102000421	01	RES 10.00 OHM 10W +5% WW
102000422	01	RES RWR .30 OHM 7W +1%
102000423	00	RES 220.00 OHM 1W 570
102000424	00	RES 10.00 OHM 10W 10057-10
102000425	00	POT 1.00K OHM 1/2W 20%
102000426	00	POT 2.00K OHM 1/2W 20%
102000427	00	RES 2.00K OHM 1/2W 5%
102000428	01	RES 75.00 OHM 5W 5%
102000429	00	POT 500.00 OHN 1/2 W %
102000430	00	POT 2.00K OHM 1/2W %
102000431	00	POT 10.00K OHM 1/2W %
102000432	00	RES 18.20K OHM 1/10W 1%
102000433	00	RES 47.50K OHM 1/10W 1%
102000434	00	RES 121.00K OHM 1/10W 1%
102000435	00	RES 332.00 OHM 1/4W 1%
102000436	00	RES 8.25K OHM 1/10W+1-1%
102000437	00	RES 2.00K OHM 1/2W-5+5%
102000438	00	RES 150.00 OHM 1/2W-5+5%
102000439	00	RES 75.00 OHM 1/10W 1%
102000440	00	RES 750.00 OHM 1/10W+1-1%
102000441	00	JUMPER INSULATED .625
102000442	EE00	VARIAC 20AMP 0-280V 3100-5120 TSTEQ
102000443	EE00	POT 100.00 OHM 2W 5% TSTEQ
102000444	EE00	RES .40 OHM 20W 5% TSTEQ
102000445	EE00	POT 100.00 OHM 5W 10% TSTEQ
102000446	EE00	RES 97.24 OHM 25W 1% TSTEQ
102000447	EE00	REG 19.22 OHM 25W 1% TSTEQ
102000448	EE00	RES 24.00 OHM 25W 1% TSTEQ
102000449	EE00	RES 10.00 OHM 25W 1% TSTEQ
102000450	EE00	RES 12.00 OHM 25W 1% TSTEQ
102000451	00	SHUNT 100A +1-1% 6713 TSTEQ
102000452	EE00	POT 50.00 OHM 100W 10% TSTEQ
102000453	EE00	POT 500.00 OHM 2W 10% TSTEQ
102000454	00	RES 38.30 OHM 1/4W 1%
102000455	00	RES 51.10 OHM 1/4W 1%
102000456	00	RES 100.00 OHM 1/4W 1%
102000457	00	RES 118.00 OHM 1/4W 1%
102000458	00	RES 121.00 OHM 1/4W 1%
102000459	00	RES 261.00 OHM 1/4W 1%
102000460	00	RES 301.00 OHM 1/4W 1%
102000461	00	RES 316.00 OHM 1/4W 1%
102000462	00	RES 562.00 OHM 1/4W 1%
102000463	00	RES 619.00 OHM 1/4W 1%
102000464	00	RES 825.00 OHM 1/4W 1%
102000465	00	RES 931.00 OHM 1/4W 1%
102000466	00	RES 1.40K OHM 1/4W 1%
102000467	00	RES 2.21K OHM 1/4W 1%
102000468	00	RES 9.11K OHM 1/4W 1%
102000469	00	RES 13.30K OHM 1/4W 1%
102000470	00	RES 200.00K OHM 1/4W 1%
102000471	EE00	RES 15.00 OHM 2W 1% TSTEQ
102000472	EE00	RES 5.00 OHM 5N 5% TSTEQ
102000473	EE00	RES 2.00 OHM 5N 5% TSTEQ
102000474	EE00	RES 5.// 50W 5% TSTEQ
102000475	EE00	RES 5.00 OHM 2KN 5% TSTEQ
102000476	EE00	RES 1.00 OHM 2KN 5% TSTEQ
102000477	EE00	RES 10.00 OHM 25W 5% TSTEQ
102000478	EE00	RES 20.00 OHM 5/N 10% TSTEQ
102000479	00	RES 75.00 OHM 1/2W 5%
102000480	00	RES 22.00K OHM 1/2W 5%
102000481	00	POT 50.00K OHM 1/2W 10%
102000482	01	RES 4.00 OHM 3W 5%
102000483	01	RES 1.00K OHM 3W 5% WW
102000484	00	RES 2.20K OHM 1W 5% CARBON
102000485	00	RES 1.50K OHM 1W 5% CARBON
102000486	00	RES 5.10K OHM 1W 5% CARBON
102000487	01	RES 0.50 OHM 5W 5% WW
102000488	00	RES 47.00 OHM 1W 5%
102000489	00	RES 2.20K OHM 1/2W 5%
102000490	00	RES 1.30K OHM 1/2W 5%
102000491	00	RES 5.60K OHM 1/2W 5%
102000492	01	RES 5.00 OHM 55W 5% FLAT
102000493	01	RES 0.50 OHM 55W 5% FLAT
102000494	00	RES 300.00 OHM 1/2W 5% CARBON
102000495	01	RES 1200.00 OHM 1W 5% WW
102000496	00	RES 620.00 OHM 1/2W 5% CARBON
102000497	00	RES 750.00 OHM 2W 20% DIP NTW
102000498	EE00	RES 0.40 OHM 20W 5% TSTEQ
102000499	EE00	RES 51.00K OHM 1/2W 5%
102000500	EE00	RES 3.00 OHM 175N 5% TSTEQ
102000501	EE00	RES 1.00 OHM 175W 5% TSTEQ
102000502	EE00	RES 150.00 OHM 12W 5% TSTEQ
102000503	EE00	RES 25.00 OHM 50W 5% TSTEQ
102000504	EE00	RES 20.00 OHM 50W 5% TSTEQ
102000505	EE00	RES 3.00 OHM 25W 5% TSTEQ
102000506	00	RES 51.00K OHM 2W 5% CARBCOM
102000507	00	RES 732.00 OHM 1/4W 1%
102000508	00	RES 1.10K OHM 1/4W 1%
102000509	00	RES 1.27K OHM 1/4W 1%
102000510	00	RES 2.49K OHM 1/4W 1%
102000511	00	RES 3.16K OHM 1/4W 1%
102000512	00	RES 3.74K OHM 1/4W 1%
102000513	00	RES 9.09K OHM 1/4W 1%

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102000514 through 102000709

PART NO.	REV	DESCRIPTION
102000514	00	RES 9.31K OHM 1/4W 1%
102000515	00	RES 13.70K OHM 1/4W 1%
102000516	00	RES 15.80K OHM 1/4W 1%
102000517	00	RES 20.00K OHM 1/4W 1%
102000518	00	RES 22.10K OHM 1/4W 1%
102000519	00	RES 34.00K OHM 1/4W 1%
102000520	00	RES 38.30K OHM 1/4W 1%
102000521	00	RES 53.60K OHM 1/4W 1%
102000522	00	RES 78.70K OHM 1/4W 1%
102000523	00	RES 100.00K OHM 1/4W 1%
102000524	00	RES 121.00K OHM 1/4W 1%
102000525	00	RES 3.65K OHM 1/4W 1%
102000526	00	RES 61.90K OHM 1/8W 1%
102000527	00	RES 6.19K OHM 1/4W 1%
102000528	00	RES 40.20K OHM 1/4W 1%
102000529	00	POT 5.00K OHM 1W 10%
102000530	01	RES 300.00 OHM 3W 5% WW
102000531	01	RES 50.00 OHM 3W 5% WW
102000532	01	RES 0.30 OHM 5W 5% WW
102000533	01	RES 25.00 OHM 5W 5% WW
102000534	01	RES 200.00 OHM 10W 5% WW
102000535	01	RES 50.00 OHM 10W 5% WW
102000536	01	RES 15.00 OHM 10W 1% WW
102000537	01	OBSOLETE, REPLACED BY 102000554
102000538	00	RES 5.90K OHM 1/4W 1%
102000539	00	POT 1.00K OHM 1/2W 20% CERMET
102000540	EE00	POT 2.00K OHM 1/2W 20% CERMET
102000541	00	POT 10.00K OHM 1/2W 20% CERMET
102000542	00	RES 18.20K OHM 1/4W 1%
102000543	00	RES 200.00 OHM 1/4W 1%
102000544	00	RES 37.00K OHM 1/8W .5%
102000545	00	RES 27.10K OHM 1/8W .5%
102000546	00	RES 14.20K OHM 1/8W .5%
102000547	00	RES 10.00K OHM 1/8W .5%
102000548	00	RES 10.2K OHM 1/8W .5%
102000549	00	RES 2.10K OHM 1/8W .5%
102000550	EE00	RES 1.80K OHM 1/2W 5%
102000551	00	RES 243.00 OHM 1/2W 1%
102000552	00	RES 1.20K OHM 1/2W 5%
102000553	01	RES .025 OHM 5W 5%
102000554	01	RES .15 OHM 5W 5%
102000555	01	RES 15.00 OHM 10W 1%
102000556	01	RES .05 OHM 10W 5%
102000557	01	RES 50.00 OHM 55W TYPE HL
102000558	00	RES 2.55K OHM 1/4 W 1%
102000559	01	RES 8.00 OHM 14W 5%
102000560	01	RES .30 OHM 3W 5% WW
102000561	00	RES 634.00 1/4W 1%
102000562	01	RES 2.00 OHM 5W 1%
102000563	EE00	RES 127.00K OHM 1/4W 10%
102000564	00	RES 102.00K OHM 1/4W 1%
102000565	EE00	RES 97.60K OHM 1/4W 1%
102000566	00	RES 75.00K OHM 1/4W 1%
102000567	00	RES 42.20K OHM 1/4W 1%
102000568	00	RES 12.40K OHM 1/4W 1%
102000569	00	RES 11.00K OHM 1/4W 1%
102000570	00	RES 10.20K OHM 1/4W 1%
102000571	00	RES 8.87K OHM 1/4W 1%
102000572	00	RES 2.74K OHM 1/4W 1%
102000573	02	RES .05 OHM 10W 1%
102000574	00	RES 294.00 OHM 1/4W 1%
102000575	00	RES 294.00K OHM 1/4W 1%
102000576	00	RES 26.70K OHM 1/4W 1%
102000577	00	RES .10 OHM 15W 1%
102000578	00	RES 100.00 OHM 1W 5%
102000579	00	RES 430.00 OHM 1W 5%
102000580	01	RES 2.20 OHM 3W 5%
102000581	00	RES 115.00K OHM 1/4W 1%
102000582	00	POT 5.00K OHM 3/4W 10%
102000583	00	POT 200.00 OHM 3/4W 10%
102000584	00	RES 1.00 OHM 1/4W 5%
102000585	00	RES 4.70K OHM 1/2W 5%
102000586	00	RES 250.00 OHM 5W 5%
102000587	00	POT 2.00K OHM 3/4W 10%
102000588	01	RES 150.00 OHM 5W 5%
102000589	01	RES .82 OHM 1W 5%
102000590	01	RES 300.00 OHM 5W 5%
102000591	01	RES 100.00 OHM 10W 5%
102000592	01	RES 1.20K OHM 5W 5%
102000593	01	RES 2.00K OHM 3W 5%
102000594	01	RES 2.50K OHM 3W 5%
102000595	00	RES 110.00 OHM 1W 5% NETWORK
102000596	00	RES 820.00 OHM 1W 5% NETWORK
102000597	00	RES 4.64K OHM 1/4W 1%
102000598	EE00	POT 5.00K OHM 1W 10% TSTEQ
102000599	EE00	RES 4700.00 OHM 1W 10% TSTEQ
102000600	EE00	RES 1.00 OHM 2W 5% TSTEQ
102000601	00	RES 30.10K OHM 1/4W 1%
102000602	00	RES 200.00 OHM 1/2W 0.05% WW
102000603	EE00	RES 500.00 OHM 1W 5% WW
102000604	00	RES 7.50K OHM 1/4W 1%
102000605	00	RES 10.50K OHM 1/4W 1%
102000606	00	RES 11.80K OHM 1/4W 1%
102000607	00	RES 13.00K OHM 1/4W 1%
102000608	00	RES 14.70K OHM 1/4W 1%
102000609	00	RES 16.90K OHM 1/4W 1%
102000610	00	RES 17.40K OHM 1/4W 1%
102000611	00	RES 18.70K OHM 1/4W 1%
102000612	00	RES 21.00K OHM 1/4W 1%
102000613	00	RES 22.60K OHM 1/4W 1%
102000614	00	RES 23.20K OHM 1/4W 1%
102000615	00	RES 24.30K OHM 1/4W 1%
102000616	00	RES 28.00K OHM 1/4W 1%
102000617	00	RES 31.60K OHM 1/4W 1%
102000618	00	RES 35.70K OHM 1/4W 1%
102000619	00	RES 56.20K OHM 1/4W 1%
102000620	00	RES 80.60K OHM 1/4W 1%
102000621	00	RES 162.00K OHM 1/4W 1%
102000622	00	RES 169.00K OHM 1/4W 1%
102000623	00	RES 205.00K OHM 1/4W 1%
102000624	00	RES 243.00K OHM 1/4W 1%
102000625	00	RES 280.00K OHM 1/4W 1%
102000626	00	RES 18.00 OHM 1/2W 5%
102000627	00	POT 20.00K OHM 1/2W 20%
102000628	01	RES 1.80 OHM 3W 5% WW AXLD
102000629	01	RES 6.20 OHM 3W 5% WW AXLD
102000630	00	RES 39.00 OHM 1/2W 5% CARBON
102000631	00	THM 5.00K OHM UKA35J1
102000632	00	RES 510.00 OHM 1W 2% NETWK
102000633	00	RES 330.00 OHM 1W 2% NETWK
102000634	00	RES 10.00 OHM 1W 5%
102000635	00	RES 100.00 OHM 1W 5%
102000636	00	POT 5.00K OHM 1/4W 10%
102000637	00	RES 470.00 OHM .1W 5%
102000638	00	RES 28.00K OHM .125W 33% CDS
102000639	00	RES 113.00K OHM 1/4W 1%
102000640	00	RES 30.10K OHM 1/4W 1%
102000641	00	RES 232.00 OHM 1/4W 1%
102000642	EE00	RES JUMPER
102000643	00	RES 150.00K OHM 1/4W 1%
102000644	00	RES 154.00K OHM 1/4W 1%
102000645	00	RES 158.00K OHM 1/4W 1%
102000646	00	RES 165.00K OHM 1/4W 1%
102000647	00	RES 174.00K OHM 1/4W 1%
102000648	00	RES 178.00K OHM 1/4W 1%
102000649	00	RES 182.00K OHM 1/4W 1%
102000650	00	RES 187.00K OHM 1/4W 1%
102000651	00	RES 191.00K OHM 1/4W 1%
102000652	00	RES 196.00K OHM 1/4W 1%
102000653	00	RES 210.00K OHM 1/4W 1%
102000654	00	RES 215.00K OHM 1/4W 1%
102000655	00	RES 221.00K OHM 1/4W 1%
102000656	00	RES 226.00K OHM 1/4W 1%
102000657	00	RES 232.00K OHM 1/4W 1%
102000658	00	RES 237.00K OHM 1/4W 1%
102000659	00	RES 249.00K OHM 1/4W 1%
102000660	00	RES 255.00K OHM 1/4W 1%
102000661	00	RES 261.00K OHM 1/4W 1%
102000662	00	RES 267.00K OHM 1/4W 1%
102000663	00	RES 274.00K OHM 1/4W 1%
102000664	00	RES 287.00K OHM 1/4W 1%
102000665	00	RES 301.00K OHM 1/4W 1%
102000666	00	RES 309.00K OHM 1/4W 1%
102000667	00	RES 316.00K OHM 1/4W 1%
102000668	00	RES 324.00K OHM 1/4W 1%
102000669	00	RES 332.00K OHM 1/4W 1%
102000670	00	RES 340.00K OHM 1/4W 1%
102000671	00	RES 348.00K OHM 1/4W 1%
102000672	00	RES 357.00K OHM 1/4W 1%
102000673	00	RES 365.00K OHM 1/4W 1%
102000674	00	RES 374.00K OHM 1/4W 1%
102000675	00	RES 383.00K OHM 1/4W 1%
102000676	00	RES 392.00K OHM 1/4W 1%
102000677	00	RES 402.00K OHM 1/4W 1%
102000678	00	RES 412.00K OHM 1/4W 1%
102000679	00	RES 422.00K OHM 1/4W 1%
102000680	00	RES 432.00K OHM 1/4W 1%
102000681	00	RES 442.00K OHM 1/4W 1%
102000682	00	RES 453.00K OHM 1/4W 1%
102000683	00	RES 464.00K OHM 1/4W 1%
102000684	00	RES 475.00K OHM 1/4W 1%
102000685	00	RES 487.00K OHM 1/4W 1%
102000686	00	RES 499.00K OHM 1/4W 1%
102000687	00	RES 511.00K OHM 1/4W 1%
102000688	00	RES 523.00K OHM 1/4W 1%
102000689	00	RES 536.00K OHM 1/4W 1%
102000690	00	RES 549.00K OHM 1/4W 1%
102000691	00	RES 562.00K OHM 1/4W 1%
102000692	00	RES 576.00K OHM 1/4W 1%
102000693	00	RES 590.00K OHM 1/4W 1%
102000694	00	RES 604.00K OHM 1/4W 1%
102000695	00	RES 619.00K OHM 1/4W 1%
102000696	00	RES 634.00K OHM 1/4W 1%
102000697	00	RES 649.00K OHM 1/4W 1%
102000698	00	RES 665.00K OHM 1/4W 1%
102000699	00	RES 681.00K OHM 1/4W 1%
102000700	00	RES 698.00K OHM 1/4W 1%
102000701	00	RES 715.00K OHM 1/4W 1%
102000702	00	RES 732.00K OHM 1/4W 1%
102000703	00	RES 750.00K OHM 1/4W 1%
102000704	00	RES 768.00K OHM 1/4W 1%
102000705	00	RES 787.00K OHM 1/4W 1%
102000706	00	RES 806.00K OHM 1/4W 1%
102000707	00	RES 825.00K OHM 1/4W 1%
102000708	00	RES 845.00K OHM 1/4W 1%
102000709	00	RES 866.00K OHM 1/4W 1%

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102000710 through 102000904

PART NO.	REV	DESCRIPTION
102000710	00	RES 887.00K OHM 1/4W 1%
102000711	00	RES 909.00K OHM 1/4W 1%
102000712	00	RES 931.00K OHM 1/4W 1%
102000713	00	RES 953.00K OHM 1/4W 1%
102000714	00	RES 976.00K OHM 1/4W 1%
102000715	00	RES 2.00K OHM 1.1W 2%
102000716	00	RES 33.00 OHM 1.1W 2%
102000717	00	RES 470.00 OHM 1.1W 2%
102000718	00	RES 36.00 OHM 1W 5%
102000719	00	RES 180.00 OHM 1.1W 2% NTWRK
102000720	00	RES 220.00 OHM 1.1W 2% NTWRK
102000721	01	RES DUMMY
102000722	01	RES 180.00 OHM 5W 5%
102000723	EE00	RES 10.00K OHM 1/4W 1%
102000724	00	RES 220.00 OHM 2W 5% CARBON
102000725	00	RES 2.00K OHM 2W 5% CARBON
102000726	00	RES 402.00 OHM 1/4W 1%
102000727	00	POT 500.00 OHM 3/4W 10% CERMET
102000728	EE00	POT 1.00K OHM 3/4W 10% CERMET
102000729	01	RES 20.00 OHM 10W 5% AX LD
102000730	00	RES 100.00 OHM 1/8W .5%
102000731	EE00	RES 200.00 OHM 1/8W .5%
102000732	00	RES 301.00 OHM 1/8W .5%
102000733	00	RES 499.00 OHM 1/8W .5%
102000734	00	RES 604.00 OHM 1/8W .5%
102000735	00	RES 2.00K OHM 1/8W .5%
102000736	EE00	RES 2.37K OHM 1/8W .5%
102000737	00	RES 2.43K OHM 1/8W .5%
102000738	00	RES 3.40K OHM 1/8W .5%
102000739	EE00	RES 9.53K OHM 1/8W .5%
102000740	00	RES 9.76K OHM 1/8W .5%
102000741	00	RES 10.00K OHM 1/8W .5%
102000742	00	RES 2.49K OHM 1/8W .5%
102000743	00	RES 4.99K OHM 1/8W .5%
102000744	01	RES 7.00 OHM 70W 5%
102000745	00	POT 1.00K OHM 1/4W 10%
102000746	01	RES 2200.00 OHM 10W 5% WW
102000747	01	RES .50 OHM 3W 5% WW
102000748	01	RES 1.00 OHM 7W 5% WW
102000749	01	RES 1200.00 OHM 3W 5% WW
102000750	00	RES 10.00 OHM /W 5% CARBON
102000751	01	RES 36.00 OHM 14W 5% AX LD
102000752	00	RES 56.00 OHM 1W 5% CARBON
102000753	00	RES 130.00 OHM 1/4W 1%
102000754	01	RES 65.00 OHM 3W 1%
102000755	01	RES .75 OHM 5W 5% AX LD
102000756	00	RES 3.00 OHM 25W 5%
102000757	00	POT 50.00K OHM 3/4W 20% CERMET
102000758	00	RES 150.00 OHM 1W 2% NETWORK
102000759	01	RES 1.50 OHM 5W 5% AX LD
102000760	EE00	POT 10.005 OHM 1/4W 10% 12T CER
102000761	00	RES 162-00 OHM 1/2W 1%
102000762	00	RES 110.00 OHM 1/2W 1%
102000763	00	RES 750.00 OHM 2W 5% CARBON
102000764	00	RES 62.00 OHM 1W 5%
102000765	01	RES 10.00 OHM 3W 5% NON
102000766	00	RES 127.00 OHM 1/2W 1%
102000767	00	RES 174.00 OHM 1/2W 1%
102000768	00	POT 10.00K OHM 1/2W 10%
102000769	00	RES 1.00K OHM .6W 2% SP NETW
102000770	00	RES 10.00K OHM .6W 2% SP NETW
102000771	00	RES 500 OHM 1/2 W .05%
102000772	00	RES 4.7K 2% NTWK 10PIN BOURNS
102000773	00	RES 1.00 OHM 7W 5%
102000774	00	RES 1.5 OHM 5W 5%
102000775	00	POT 100.00 OHM .75W 10%
102000776	00	POT 20.00K OHM .75W 10%
102000777	00	POT 50.00K OHM .75W 10%
102000778	00	POT 100.00K OHM .75W 10%
102000779	01	RES 800.00 OHM 3W 5% WW
102000780	EE00	RES 12.170K OHM 1/4W 1% 6030
102000781	00	RES 11.30K OHM 1/4W 1% 6030
102000782	00	RES 9.53K OHM 1/4W 1%
102000783	00	RES 10.70K OHM 1/4W 1%
102000784	EE00	RES 11.50K OHM 1/4W 1% 6030
102000785	00	RES 9.76K OHM 1/4W 1%
102000786	00	RES 10.00K OHM 1W 2% 9R NTWK
102000787	00	RES 2.00K OHM .6W 2% SP NTWK
102000788	00	RES 4.70K OHM .6W 5% SP NTWK
102000789	00	RES 18.00K OHM 1W 2% 7R NTWK
102000790	EE00	RES 330/390.00 OHM 1.5W 2% 16P NTW
102000791	00	RES 1.00K OHM 1.25W 2% 10PIN
102000792	00	RES 51.00 OHM .4W 5% WW
102000793	00	RES 390.00 OHM 1W 2% NTWK 7R
102000794	00	RES 270.00 OHM 1W 2% NTWK 7R
102000795	EE00	RES 820.00 OHM 1W 5% CARBON
102000796	EE00	RES-CAP NTWK 68 OHM .01UF 8P SIP
102000797	00	RES 330.00 OHM .6W 2% NTWK 4R
102000798	00	RES 1.00K OHM .75W 2% NTWK 3R
102000799	00	RES 1.00 OHM 1W 1% WW
102000800	EE00	RES 1.50K OHM 1W 2% NTWK 7R
102000801	EE00	RES 330/390.00 OHM 1W % 8P NTWK
102000802	00	RES 1.00M OHM 1/4W 1%
102000803	00	RES 100.00 OHM 1/8W .1% 6060/61
102000804	00	RES 261.00 OHM 1/8W .1% 6060/61
102000805	00	RES 0.075 OHM 7W 1%
102000806	00	RES 1.00K OHM 1W 2% 7R NTWK

PART NO.	REV	DESCRIPTION
102000807	00	RES 820.00 OHM 1W 5% WW
102000808	00	POT 50K 801083-503
102000809	00	RES 15.00 OHM 10W 5% WW AXLD
102000810	00	RES .20 OHM 3W 5% WW
102000811	00	RES .82 OHM 7W 5% WW
102000812	00	POT 5.00K OHM 1/2W 10%
102000813	00	VAR . OHM 39V 10% MET OXD
102000814	00	RES 2.00 OHM 225W 5% PWR WW
102000815	00	POT 250-00K OHM 1W 20%
102000816	00	RES 69.80K OHM 1/4W 1% CERMET
102000817	00	RES 47.00 OHM W 2% NTWK 4R
102000818	00	RES 562.00 OHM 1/2W 1%
102000819	EE00	RES 210.00 OHM 1/2W 1%
102000820	00	RES 6.00 OHM 10W 1% WW
102000821	00	RES 20.00 OHM 5W 5% WW
102000822	00	RES .05 OHM 1W 1% WW
102000823	00	RES 9.10K OHM 5W 5% WW
102000824	00	RES 820.00 OHM 1/2W 5% CARBON
102000825	00	RES 2.70K OHM 1.25W 2% 10P
102000826	00	RES 330.00 OHM W 2% 9RES
102000827	00	RES 2.61K 1/4W 1%
102000828	00	RES .50 OHM 1W 5% NW
102000829	EE00	NOT USED SEE 103000438
102000830	00	RES 3.90 OHM 1W 5%
102000832	00	RES 470.00 OHM W 2% NTWK 9R
102000833	00	RES 22.00 OHM 1.1W 2% 4RES
102000834	00	RES 2.70 OHM 1/2W 1% WW
102000835	EE00	POT 2.5M OHM W 20%
102000836	00	RES 12.00K OHM W .01% MATCHED
102000837	00	POT 50.00K OHM W 20% 15T SS
102000838	00	RES SINGLE IN LINE NETWORK
102000839	00	RES SINGLE IN LINE NETWORK
102000840	00	RES SINGLE IN LINE NETWORK
102000841	00	RES SINGLE IN LINE NETWORK
102000842	00	RES SINGLE IN LINE NETWORK
102000843	00	RES SINGLE IN LINE NETWORK
102000844	00	RES SINGLE IN LINE NETWORK
102000845	00	RES 10.00 OHM 35W 5% WW
102000846	00	VAR METAL OXIDE 275VAC 20 JOULES
102000847	00	RES 8.20K OHM 2W 5%
102000848	00	RES 9.10K OHM 2W 5%
102000849	00	RES 6.80K OHM 2W 5%
102000850	00	RES 2.40K OHM 7W 5% WW
102000851	00	RES 4.00 OHM 7W 5%WW
102000852	00	RES 39.00 OHM 3W 5%
102000853	00	RES 1.00 OHM 3W 5% NON-IND
102000854	00	RES 200.00 OHM 1W 5% CARB
102000855	00	RES .025 OHM 1W 5% WW
102000856	00	RES 100.00K OHM .75W 2% WTWK 6P
102000857	00	RES 220/330.00 OHM SGL-IN-LINE NTWK
102000858	EE00	RES 100.00K OHM 2% 8P NTWK
102000859	00	VAR CURRENT SURGE SUPRESSOR 120HM
102000860	01	RES 8.00 OHM 7W 5% WW
102000861	00	RES 1.00 OHM 1/2W 5% CARBON
102000862	EE00	RES 178.00 OHM 1/4W 1% CEREMET
102000863	00	RES 470.00K OHM 1/2W 5%
102000864	00	RES .10 OHM 1W 1% WW
102000865	00	RES 2.40MEGOHM 1W 5%
102000866	00	RES 10.00K 7W 5%
102000867	00	RES 20.00 OHM 2W 5%
102000868	00	RES 8.06K OHM 1/4W 1% DGC-JR
102000869	00	RES 41.20K OHM 1/4W 1% DGC-JR
102000870	00	RES 33.20K OHM 1/4W 1% DGC JR
102000871	00	POT 200.00 OHM .5W 10% CERMET
102000872	00	RES 3.50K OHM 5W 5% WW
102000873	00	RES .20 OHM 5W 5% WW
102000874	00	RES 51.00 OHM 1.0W 2% 7R SIP
102000875	00	RES 330/390 DUAL TERM SIP 10P NTWK
102000876	00	RES 620-00 OHM W % 7RES
102000877	EE00	RES 270.00 OHM 1/8W 5% CARBON
102000878	00	RES 3.30 OHM 1/2W 5% CARBON
102000879	00	RES 680.00 OHM 1/2W 5% CARBON
102000880	00	POT 2.5M OHM 1/4W 20% VERT MT
102000881	00	RES 100.00 OHM W 2% NTWK
102000882	00	RES 6.80 OHM 50W 5% WW
102000883	00	RES 5.60K 10W 5% WW
102000884	00	27.00 OHM 1W 5% CARBON
102000885	EE00	RES 0.20 OHM 10W 3% PWR
102000886	EE00	RES 0.10 OHM 25W 1% PWR
102000887	00	RES .05 OHM 3W 1% WW
102000888	EE00	RES 100/150 DUAL TERM SIP 10P NTWK
102000889	EE00	RES 200.00 OHM W %
102000890	00	RES 220.00K OHM 1/2W 5%
102000891	00	RES 75.00 OHM 14W 5% AXLD WW
102000892	00	RES 500.00 OHM 7W 5% AXLD WW
102000893	00	RES 2.00 OHM 1/2W 5%
102000894	00	RES 560.00 OHM 1/2W 5% CARBON
102000895	EE00	RES 330/470 OHM LINE TERM 10P NTWK
102000896	00	RES .025 OHM 3W 5%
102000897	EE00	POT 20.00 OHM 3/4W 10% 15T
102000898	EE00	POT 50.00 OHM 3/4W 10% 15T
102000899	00	RES 470/560 OHM SIP 10PIN 16R NTWK
102000900	EE00	RES 2.70K OHM 1/2W 5% CARBON
102000901	EE00	RES 7.50K OHM 1W 5% CARBON
102000902	EE00	RES 1.80K OHM 1W 5% CARBON
102000903	00	RES 95.30 OHM 3W 1% WW
102000904	EE00	RES 0.40 OHM W 3% WW

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102000905 through 103000107

PART NO.	REV	DESCRIPTION
102000905	00	RES 20.0K OHM 1W 5% CARBON
102000906	00	RES 1.50K OHM SIP NTWK ISOL 3R
102000907	EE00	RES 27.00 OHM ISOLATED 3R NTWK
102000908	00	RES 46.40 OHM 1/4W 1% CERMET
102000909	00	POT 1.00K 20% SIDE ADJ
102000910	00	POT 10.00K OHM 20% SIDE ADJ
102000911	EE00	RES 110.00 OHM 1/4W 1%
102000912	EE00	RES 162.00 OHM 1/4W 1%
102000913	EE00	RES 499.00 OHM 1/4W 1%
102000914	EE00	RES 4120.00 OHM 1/4W 1%
102000915	EE00	RES 140.00 OHM 1/2W 1%
102000916	00	RES 470/560.00 OHM DUAL TERM 6P NTWK
102000917	EE00	RES 28.70K OHM 1/4W 1%
102000918	00	RES 330/390.00 OHM DUAL TERM 6P NTWK
102000919	EE00	RES 604.00 OHM 1/4W 1%
102000920	00	POT 2.00K OHM .5W 10%
102000921	00	RES 0.50 OHM 25W 3%
102000922	EE00	RES 33.00 OHM W 2% 3R NTWK
102000923	00	RES 2.10K OHM 1/4W 1%
102000924	00	RES .50 OHM 20W 5% WW RDLD
102000925	EE00	RES SLIDE CONTROL
102000926	00	THM INRUSH CURRENT LIMITER 5 OHM
102000927	EE00	RES 1.00K OHM 20W 5% WW RDLD
102000928	EE00	RES 10.00 OHM 20W 5% WW RDLD
102000929	EE00	THM 10 OHM INRUSH CURRENT LIMITER
102000930	EE00	RES 110.00 OHM W % 8P 4RES
102000931	EE00	RES 7.00 OHM 20W 5% WW PCMT
102000932	EE00	RES 250.00 OHM 3W 5% WW AXLD
102000933	00	RES 68.00K OHM 1W 5%
102000934	EE00	RES 82.00 OHM 2W 5%
102000935	EE00	VARISTOR 150VRMS 10 JOULES
102000936	EE00	RES 180.00 OHM 2% 8PIN
102000937	EE00	RES 181/390 OHM 10PIN NTWK
102000938	00	POT 5.00K OHM 1/2W SGL TURN
102000939	00	RES 1.20K OHM NETWORK TSTED
102000940	00	RES 1.80K OHM NETWORK TSTED
102000941	EE00	RES 1.50 OHM 20W 5%
102000942	EE00	RES 300.00 OHM 20W 5%
102000943	00	RES 12.00 OHM 20W 5%
102000944	00	RES .10 OHM 3W 1% WW
102000945	EE00	RES 2.50 OHM 20W 5% WW PCMT
102000946	EE00	VAR 275VRMS METAL OXIDE
102000947	EE00	RES .25 OHM 55W 5% WW
102000948	EE00	RES .40 OHM 3W 5% WW AXLD
102000949	EE00	RES .30 OHM 1W 5% WW AXLD
102000950	EE00	RES 25.00 OHM 10W 5% WW AXLD
102000951	EE00	RES 86.60K OHM 1/4W 1%
102000952	00	RES 16.00 OHM 7W 5% WW NI
102000953	EE00	RES 75.00K OHM 1W 5% CARBON
102000954	EE00	RES 10.00K OHM 1/2W 5% CARBON
102000955	EE00	RES 1.00K OHM 2% 4R NTWK
102000956	EE00	RES 150.00 OHM 2% 4R NTWK
102000957	EE00	RES 4.70 OHM 7RES
102000958	00	RES 600.00 OHM 10W % AXLD
102000959	00	RES 25.00 OHM 20W 5% RD LD
102000960	EE00	RES 200.00 OHM 3W 1% WW
102000961	EE00	RES 200.00 OHM 1/2W 1%
102000962	EE00	RES .125 OHM 30W % PWR WW
102000963	EE00	RES 49.90K OHM 1/4W 1%
102000964	00	RES 330.00K OHM 1W 5% CARBON
102000965	EE00	RES 390.00 OHM 4RES 8PIN NETWORK
102000966	EE00	RES 120.00 OHM 4RES 5PIN NETWORK
102000967	EE00	RES 82.00 OHM 1W 5% CARBON
102000968	EE00	RES 137.00K OHM 1/4W 1%
102000969	EE00	RES 25.50 OHM 1/4W 1%
102000970	EE00	RES 453.00 OHM 1/4W 1%
102000971	EE00	RES 887.00 OHM 1/4W 1%
102000972	EE00	RES 2670.00 OHM 1/4W 1%
102000973	EE00	RES 6.80K OHM W 2% 9RES
102000974	EE00	RES 120.00 OHM W 2% 4RES
102000975	EE00	RES 82.00 OHM NTWK
102000977	EE00	RES 402.00 OHM 1/8W .5%
102000978	EE00	RES 1.18K OHM 1/8W .5%
102000979	EE00	RES 1.54K OHM 1/8W .5%
102000980	EE00	RES 3.01K OHM 1/8W .5%
102000981	EE00	RES 6.04K OHM 1/8W .5%
102000982	EE00	RES 12.10K OHM 1/8W .5%
102000983	EE00	RES 80.60 OHM 1W .5% WW
102000984	EE00	RES 400.00 OHM 10W 5% WW
102000985	EE00	RES 10.00K OHM 7RES 8PIN NTWK
102000986	EE00	RES 1.50K OHM 4RES 8PIN NTWK
102000989	EE00	RES 120.00 OHM 7RES 8PIN NTWK
102000990	EE00	RES 6.80K OHM 7RES 8PIN NTWK
102000991	EE00	RES 2.00K OHM 1/8W .1%
102000992	EE00	RES 1.00K OHM 1/8W .1%
102000993	EE00	RES 47.00 OHM 2W 5%
102009999	00	RES NON-INSERTED 1/4W
102999800	00	RES PWR W/W G/F SPEC
103000001	01	CAP .0100MF +80-20% 50V CER
103000002	00	CAP 6.8000MF +10-10% 35V TANT
103000003	00	CAP .2200MF +10-10% 20V TANT
103000004	00	CAP 470.0000PF +5-5% 500V MICA
103000005	00	CAP 820.0000PF +5-5% 300V MICA
103000006	00	CAP 220.0000PF +5-5% 500V MICA
103000007	00	CAP 50.0000MF +5-5% 50V TANT
103000008	00	CAP 6000.0000MF
103000009	00	CAP 220.0000PF

PART NO.	REV	DESCRIPTION
103000010	00	CAP 100.0000PF
103000011	00	CAP .2200
103000012	00	CAP .1000MF +5-5% 250V FIL
103000013	00	CAP .5000
103000014	00	CAP 5.6000
103000015	00	CAP .0022MF -5+5% 500V
103000016	00	CAP 1.0000MF +10-10% 35V TANT
103000017	00	CAP 6.8000MF
103000018	00	CAP 6.8000MF +10-10% 6V TANT
103000019	00	CAP 25000.0000MF
103000020	00	CAP 48000.0000MF
103000021	00	CAP 25000.0000MF
103000022	00	CAP 13000.0000MF
103000023	00	CAP 530.0000MF
103000024	00	CAP 1000.0000MF
103000025	00	CAP 32000.0000MF
103000026	00	CAP 21000.0000MF +20-20% 40V ELEC
103000027	00	CAP 6000.0000MF +20-20% 10V ELEC
103000028	00	CAP 1000.0000MF
103000029	00	CAP 1100.0000MF
103000030	00	CAP 6.8000MF
103000031	00	CAP 100.0000PF +5-5% 500V MICA
103000032	00	CAP
103000033	00	CAP
103000034	00	CAP 122.0000PF
103000035	00	CAP 1200.0000PF +5-5% 100 V MICA
103000036	00	CAP 8.0000MF +20-20% 50V TANT
103000037	00	CAP 47.0000MF +20-20% 20V TANT
103000038	00	CAP
103000039	01	CAP .0500MF +80-20% 12V
103000040	00	CAP 33.0000PF +5-5% 500V MICA
103000041	00	CAP 560.0000PF +5-5% 300V MICA
103000042	00	CAP 300.0000PF
103000043	00	CAP 21000.0000MF +20-20% 25V ELEC
103000044	00	CAP 12.0000PF +5-5% 500V MICA
103000045	00	CAP 2.2000MF +20-20% 20V TANT
103000046	00	CAP 330.0000PF +5-5% 100V MICA
103000047	00	CAP .0068MF +10-10% 100V RCAP
103000048	00	CAP 24000.0000MF +20-20% 40V ELEC
103000049	00	CAP 38000.0000MF +20-20% 20V ELEC
103000050	00	CAP 63000.0000MF
103000051	00	CAP 20000.0000MF +20-20% 10V ELEC
103000052	00	CAP 47.0000MF +20-20% 6V TANT
103000053	00	CAP 68.0000PF +5-5% 500V MICA
103000054	00	CAP .0100MF +10-10% 50V RCAP
103000055	00	CAP 100.0000PF +5-5% 100V RCAP
103000056	00	CAP 82.0000PF +5-5% 500V MICA
103000057	00	CAP 6.8000MF +50-20% 6.3V T/T
103000058	00	CAP
103000059	00	CAP 110.0000MF 40V
103000060	00	CAP 31000.0000MF +20-20% 40V ELEC
103000061	00	CAP 20000.0000MF +20-20% 20V ELEC
103000062	00	CAP 6.8000MF +50-20% 35V T/T
103000063	00	CAP 161-193MF 110V 60HZ
103000064	00	CAP FILTER MURATA SFB455D
103000065	00	CAP 1.0000MF +10-10% 35V T/T
103000066	00	CAP 6300.0000 % 20V ELEC
103000067	00	CAP 33000.0000 % 50V ELEC
103000068	00	CAP 47.0000MF +50-20% 6.3V T/T
103000069	00	CAP 1.5000MF +20-20% 35V ELEC
103000070	00	CAP .0220MF +10-10% 100V RCAP
103000071	00	CAP 27.0000PF 5% 300V MICA
103000072	00	CAP 150.0000PF +5-5% 500V MICA
103000073	00	CAP .1000MF +5-5% 50V MYLAR
103000074	00	CAP 100.0000MF % 15V TANT
103000075	00	CAP 4.7000MF +50-20% 50V TAG
103000076	00	CAP 7000.0000MF % 20V ELEC
103000077	00	CAP .1000MF +10-10% 200V TANT
103000078	00	CAP 130-156MF 110V 60HZ
103000079	00	5600PF 10% 100V
103000080	01	CAP 47-56MF 200V 60HZ
103000081	00	CAP 1200.0000MF % 40V ELEC
103000082	00	CAP 1200.0000MF % 20V ELEC
103000083	00	CAP 20000.0000MF 10V ELEC
103000084	00	CAP 22.0000MF 10V TAG
103000085	00	CAP .2200MF 100V MYLAR
103000086	00	CAP .1000MF 50V
103000087	00	CAP .4700MF 50V
103000088	00	CAP 3600.0000MF 50V
103000089	00	CAP 800.0000MF 50V ELEC
103000090	00	CAP .2000FD +75-10% 10V
103000091	00	CAP 98000.0000MF +75-10% 20V
103000092	00	CAP 66000.0000MF +75-10% 20V
103000093	00	CAP NOT ASSIGNED
103000094	00	CAP .0010MF +10-10% 1000V
103000095	00	CAP .1000MF +10-10% 400V MYLAR
103000096	00	CAP 12000.0000MF +75-10% 20V SANG
103000097	00	CAP 12000.0000MF +75-10% 40V SANG
103000098	00	CAP 5.0000PF +5-5% 500V MICA
103000099	00	CAP 6.0000PF +5-5% 500V MICA
103000100	00	CAP 10.0000PF +5-5% 500V MICA
103000101	00	CAP 51.0000PF +5-5% 500V MICA
103000102	00	CAP 270.0000PF +5-5% 500V MICA
103000103	00	CAP .0150MF +10-10% 100V
103000104	00	CAP 77000.0000MF +75-10% 20V ELEC
103000105	00	CAP 71000MF/63000MF
103000106	00	CAP 13000.0000MF
103000107	00	CAP 13000.0000MF 40V

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103000108 through 103000302

PART NO.	REV	DESCRIPTION
103000108	00	CAP 22.0000MF 16V TAG
103000109	00	CAP (REPLACED BY 103000105
103000110	00	CAP 77000.0000MF +75-10% 20V ELEC
103000111	00	CAP .2300FD +75-10% 20V ELEC
103000112	00	CAP .6300FD +75-10% 6V ELEC
103000113	00	CAP 15.0000PF +5-5% 500V MICA
103000114	00	CAP 1.0000MF T20-20% 50V TANT
103000115	00	CAP 4.0000MF +50-20% 660V 60HZ
103000116	00	CAP .0500MF +50-20% 25V DISC
103000117	00	CAP .1000MF 250V 60HZ
103000118	00	CAP 4.000MF 660V
103000119	00	CAP AC LINE FILTER,RFI PWRLINE #20K6
103000120	00	CAP 160.0000PF +5-5% 500V MICA
103000121	00	CAP 12.5000MF +6-6% 370V
103000122	00	CAP .0470MF +10-10% 100V MYLAR
103000123	00	CAP .0033MF +10-10% 100V MYLAR
103000124	00	CAP 1.0000MF +10-10% 50V MYLAR
103000125	00	CAP 2.2000MF +50-20% 35V T/T
103000126	00	CAP .1500FD +75-10% 6V ELEC
103000127	00	CAP .0220 MF +10-10% 100V MYLAR
103000128	00	CAP .3300MF +10-10% 50V MYLAR
103000129	00	CAP 98000.0000MF +75-10% 20V ELEC
103000130	00	CAP 6.0000MF 660V OIL FILLED
103000131	00	CAP .01MF 400V
103000132	00	CAP 500MF 25V
103000133	00	CAP 10MF 660V
103000134	00	CAP 150,000 MF 6V
103000135	00	CAP 1600.0000PF +5-5% 500V MICA
103000136	00	CAP 1.0000MF 400V
103000138	00	CAP 24.0000PF 05% 300V MICA
103000139	00	CAP 1000 UF 25WV CRAMER WHB1000-25
103000140	00	CAP 15MFD 200-365VACGE45F165
103000141	00	CAP 5MFD 366-410VAC GE 45F273
103000142	00	CAP 1.0000PF +5-5% 500V MICA
103000143	00	CAP 2.0000PF +5-5% 500V MICA
103000144	00	CAP 3.0000PF +5-5% 500V MICA
103000145	00	CAP 4.0000PF +5-5% 500V MICA
103000146	00	CAP 7.0000PF +5-5% 500V MICA
103000147	00	CAP 8.0000PF +5-5% 500V MICA
103000148	00	CAP 18.0000PF +5-5% 500V MICA
103000149	00	CAP 20.0000PF +5-5% 500V MICA
103000150	00	CAP 22.0000PF +5-5% 500V MICA
103000151	00	CAP 24.0000PF +5-5% 500V MICA
103000152	00	CAP 30.000CPF +5-5% 500V MICA
103000153	00	CAP 36.000CPF +5-5% 500V MICA
103000154	00	CAP 39.000CPF +5-5% 500V MICA
103000155	00	CAP 43.000CPF +5-5% 500V MICA
103000156	00	CAP 47.000CPF +5-5% 500V MICA
103000157	00	CAP 62.000CPF +5-5% 500V MICA
103000158	00	CAP 75.000CPF +5-5% 500V MICA
103000159	00	CAP 91.000CPF +5-5% 500V MICA
103000160	00	CAP 110.000CPF +5-5% 500V MICA
103000161	00	CAP 120.000CPF +5-5% 500V MICA
103000162	00	CAP 130.000CPF +5-5% 500V MICA
103000163	00	CAP 180.000CPF +5-5% 500V MICA
103000164	00	CAP 200.000CPF +5-5% 500V MICA
103000165	00	CAP 240.000CPF +5-5% 500V MICA
103000166	00	CAP 300.000CPF +5-5% 500V MICA
103000167	00	CAP 360.000CPF +5-5% 500V MICA
103000168	00	CAP 390.000CPF +5-5% 500V MICA
103000169	00	CAP 430.000CPF +5-5% 500V MICA
103000170	00	CAP 510.000CPF +5-5% 500V MICA
103000171	00	CAP 620.000CPF +5-5% 500V MICA
103000172	00	CAP 680.000CPF +5-5% 500V MICA
103000173	00	CAP 750.000CPF +5-5% 500V MICA
103000174	00	CAP 910.000CPF +5-5% 500V MICA
103000175	00	CAP 1000.000CPF +5-5% 500V MICA
103000176	00	CAP 1100.000CPF +5-5% 500V MICA
103000177	00	CAP 1300.000CPF +5-5% 500V MICA
103000178	00	CAP 1500.000CPF +5-5% 500V MICA
103000179	00	CAP 1800.000CPF +5-5% 500V MICA
103000180	00	CAP 2000.000CPF +5-5% 500V MICA
103000181	00	CAP 2200.000CPF +5-5% 500V MICA
103000182	00	CAP 2400.000CPF +5-5% 500V MICA
103000183	00	CAP 2700.000CPF +5-5% 500V MICA
103000184	00	CAP 3000.000CPF +5-5% 500V MICA
103000185	00	CAP 3300.000CPF +5-5% 500V MICA
103000186	00	CAP 3600.000CPF +5-5% 500V MICA
103000187	00	CAP 3900.000CPF +5-5% 500V MICA
103000188	00	CAP 4300.000CPF +5-5% 500V MICA
103000189	00	CAP 4700.000CPF +5-5% 500V MICA
103000190	00	CAP 5100.000CPF +5-5% 500V MICA
103000191	00	CAP 5600.000CPF +5-5% 500V MICA
103000192	00	CAP 6200.000CPF +5-5% 500V MICA
103000193	00	CAP 6800.000CPF +5-5% 100V MICA
103000194	00	CAP 7500.000CPF +5-5% 100V MICA
103000195	00	CAP 8200.000CPF +5-5% 100V MICA
103000196	00	CAP .0010MF +10-10% 100V MYLAR
103000197	00	CAP .0012MF +10-10% 100V MYLAR
103000198	00	CAP .0015MF +10-10% 100V MYLAR
103000199	00	CAP .0018MF +10-10% 100V MYLAR
103000200	00	CAP .0022MF +10-10% 100V MYLAR
103000201	00	CAP .0027MF +10-10% 100V MYLAR
103000202	00	CAP .0039MF +10-10% 100V MYLAR
103000203	00	CAP .0047MF +10-10% 100V MYLAR
103000204	00	CAP .0050MF +10-10% 100V MYLAR
103000205	00	CAP .0056MF +10-10% 100V MYLAR
103000206	00	CAP .0068MF +10-10% 100V MYLAR
103000207	00	CAP .0082MF +10-10% 100V MYLAR
103000208	00	CAP .0100MF +10-10% 100V MYLAR
103000209	00	CAP .0120MF +10-10% 100V MYLAR
103000210	00	CAP .0150MF +10-10% 100V MYLAR
103000211	00	CAP .0180MF +10-10% 100V MYLAR
103000212	00	CAP .0270MF +10-10% 100V MYLAR
103000213	00	CAP .0330MF +10-10% 100V MYLAR
103000214	00	CAP .0390MF +10-10% 100V MYLAR
103000215	00	CAP .0500MF +10-10% 100V MYLAR
103000216	00	CAP .0560MF +10-10% 100V MYLAR
103000217	00	CAP .0820MF +10-10% 100V MYLAR
103000218	00	CAP .1000MF +10-10% 100V MYLAR
103000219	00	CAP .1200MF +10-10% 100V MYLAR
103000220	00	CAP .1500MF +10-10% 100V MYLAR
103000221	00	CAP .1800MF +10-10% 100V MYLAR
103000222	00	CAP .2700MF +10-10% 100V MYLAR
103000223	00	CAP .3300MF +10-10% 100V MYLAR
103000224	00	CAP .4700MF +10-10% 100V MYLAR
103000225	00	CAP .5000MF +10-10% 100V MYLAR
103000226	00	CAP .5600MF +10-10% 100V MYLAR
103000227	00	CAP .6800MF +10-10% 100V MYLAR
103000228	00	CAP .8200MF +10-10% 100V MYLAR
103000229	00	CAP 1.0000MF +10-10% 100V MYLAR
103000230	00	CAP 1.2500MF +10-10% 100V MYLAR
103000231	00	CAP 1.5000MF +10-10% 100V MYLAR
103000232	00	CAP 2.0000MF +10-10% 100V MYLAR
103000233	00	CAP 3.0000MF +10-10% 100V MYLAR
103000234	00	CAP 4.0000MF +10-10% 100V MYLAR
103000235	00	CAP .0680MF +10-10% 100V MYLAR
103000236	00	CAP .3900MF +10-10% 100V MYLAR
103000237	00	CAP 50.0000PF +5,5% 500V MICA
103000238	00	CAP 2500.0000PF +5-5% 500V MICA
103000239	00	CAP 500.0000PF +5-5% 500V MICA
103000240	01	CAP LINE FILTER EMI-F-0441
103000241	00	CAP 27.0000PF 05% 300V MICA
103000242	00	CAP .1000MF +20-20% 200V FILM
103000243	00	CAP LINE FILTER RFI EMI-F-0458
103000244	00	CAP .1 MF 16V 21104001
103000245	00	CAP MOTOR START 525064001
103000246	00	CAP 8R-108 UF 181384
103000247	00	CAP 4600.0000MF M60OL 00000200
103000248	00	CAP 10.0000MF M60OL 00000880
103000249	00	CAP 17.5000MF M60OL 00000202
103000250	00	CAP 3.0000MF M60OL 00000205
103000251	00	CAP 4.0000MF 00000204
103000252	00	CAP .1000MF -20% 50V CER
103000253	00	CAP 6.8000MF 010% 6V T/T
103000254	00	CAP 3.000 MFP 370V 386830525
103000255	00	CAP 9000.0000MF 40V AT382
103000256	00	CAP 160.0000MF 25V TC-WE167
103000257	00	CAP 50.0000MF 100V TC-HH506E
103000258	00	CAP 250.00MF 16V TC-WA257
103000259	00	CAP 6.0000MF 660V NOM (GE45F608)
103000260	00	CAP 1600.0000MF 10074-16
103000261	00	CAP 4.0000MF 6% 660V
103000262	00	CAP 100.0000PF +5-5% 50V CER
103000263	00	CAP .0470MF +20-20% 50V CER
103000264	00	CAP 1.0000MF -0+100% 50V CE/RDL
103000265	00	CAP 27.0000PF +5-5% 50V CER
103000266	00	CAP 180.0000PF +5-5% 50V CER
103000267	00	CAP 220.0000PF +5-5% 50V CER
103000268	00	CAP 360.0000PF +5-5% 50V CER
103000269	00	CAP 470.0000PF +5-5% 50V CER
103000270	00	CAP 820.0000PF +5-5% 50V CER
103000271	00	CAP 1200.0000PF +10-10% 50V CER
103000272	00	CAP 5600.0000PF +10-10% 50V CER
103000273	00	CAP 6800.0000PF +10-10% 50V CER
103000274	00	CAP .010MF +80-20% 50V CER
103000275	00	CAP .0100MF +10-10% 50V CER
103000276	00	CAP .015MF +10-10% 50V CER
103000277	00	CAP .022MF +10-10% 50V CER
103000278	01	CAP .82 UFD +100%-0% 50V CE/AX
103000279	00	SEE 103000280
103000280	00	CAP 2.2000MF -0+100% 50V CE/RDL
103000281	00	CAP .0470UF +80-20% 50V CER
103000282	00	CAP 150.0000PF +5-5% 50V CER
103000283	00	CAP 13800.0000MF 15VDCW 00000596
103000284	00	CAP USE 103-250 00000205
103000285	00	CAP 6200.0000MF 75VDCW 00000199
103000286	00	CAP .2200MF +20-20% 100V CER-R
103000287	00	CAP 100.0000MF +20-20% 25V ELEC
103000288	02	CAP LINE FILTER EMI PWR 10R6 10A
103000289	00	CAP .0050MF +20-20 500V CER
103000290	00	CAP 1.0000MF -0+100% 50V CE/AXL
103000291	EE00	CAP 24000.0000MF +20-20% 75V TSTEQ
103000292	EE00	CAP 38000.0000MF +10-10% 40V TSTEQ
103000293	00	CAP 3300.0000MF +80-20% 100V
103000294	00	CAP 20.0000MF -10+75% 100V
103000295	00	CAP 5600.0000PF +10-10% 50V CR
103000296	00	CAP 9000.0000MF +100-10% 50V ELECT
103000297	00	CAP 1500.0000PF +20-20% 50V CER
103000298	00	CAP 330.0000PF +5-5% 50V CER
103000299	00	CAP 160.0000PF +5-5% 50V CER
103000300	00	CAP 68.0000PF +5-5% 50V CER
103000301	00	CAP 33.0000PF +5-5% 50V CER
103000302	00	CAP 22.0000PF +5-5% 50V CER

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103000303 through 103000500

PART NO.	REV	DESCRIPTION
103000303	00	CAP 15.0000PF +5-5% 50V CER
103000304	00	CAP 10.0000PF +5-5% 50V CER
103000305	00	CAP 4.7000PF +5-5% 50V CER
103000306	00	CAP 3.9000PF +5-5% 50V CER
103000307	00	CAP 1.8000PF +5-5% 50V CER
103000308	00	CAP 470.0000 +1-1% 300V MICA
103000309	00	CAP EMI DC BUTTON FILTER 1021-000
103000310	00	CAP 0.0022MF +10-10% 50V CER
103000311	00	CAP .2200MF -0+100% 50V CR/RL
103000312	00	CAP 55.0000KMF -10+75% 50V
103000313	00	CAP 53.0000KMF -10+75% 25V
103000314	00	CAP 39.0000KMF -10+75% 35V
103000315	00	CAP 190.0000KMF -10+75% 15V
103000316	00	CAP 140.0000MF -10+75% 6V ELECT
103000317	00	CAP 50.0000MF -10+75% 25V ELECT
103000318	00	CAP .2200MF +10-10% 50V RL
103000319	00	CAP .4700MF +10-10% 50V RL
103000320	00	CAP POTTER AC LN FLTR 20A 250V
103000321	00	CAP .1000MF +10-10% 50V
103000322	00	CAP 75.0000PF +5-5% 50V AX LD
103000323	00	CAP .0010MF +5-5% 50V AX LD
103000324	00	CAP 1.0000MF +10-10% 400V
103000325	EE00	CAP .6800MF +10-10% 400V
103000326	00	CAP .1000MF +10-10% 4001/PLYCB
103000327	00	CAP .1000MF -20+80% 50V CERAX
103000328	00	CAP 2.0000MF +6-6% 660VNOM
103000329	00	CAP MOTOR START 75039701
103000330	00	CAP 1500.0000PF +10-10% 50V CR AX
103000331	00	CAP 22.0000MF +20-20% 10V TANT
103000332	00	CAP 10.0000MF +10-10% 50V TANT
103000333	00	CAP 20000.0000MF -10+75% 6V
103000334	EE00	CAP 3900.0000MF -10+75% 6V
103000335	00	CAP 9000.0000MF -10+75% 20V
103000336	00	CAP 3.3000MF +20-20% 50V CERRD
103000337	00	CAP 82.0000PF +5-5% 50V AXIAL
103000338	00	CAP 3.3000PF +.5-.5% 50V CERAX
103000339	00	CAP 39.0000PF +5-5% 50V CERAX
103000340	00	CAP 270.0000PF +5-5% 50V AXIAL
103000341	00	CAP 56.0000PF +5-5% 50V CERAX
103000342	00	OBSOLETE
103000343	00	OBSOLETE
103000344	01	CAP 1000.0000MF -10+100% 12V
103000345	00	CAP 78000.0000MF -10+75% 40V
103000346	00	CAP 430.0000PF +5-5% 50V AX LD
103000347	00	CAP 510.0000PF +5-5% 50V AX LD
103000348	00	CAP 1500.0000PF +10-10% 50V AX LD
103000349	00	CAP 525323-001
103000350	00	CAP 750.0000MF -10+75% 40V
103000351	00	CAP .0330MF &10-10% 50V
103000352	00	CAP .0100MF +10-10% 600V
103000353	00	CAP 27000.0000MF -10+75% 20V ELECT
103000354	00	CAP 560.0000MF -10+100% 20V
103000355	00	CAP 5600.0000MF -10+75% 25V
103000356	00	CAP 35000.0000MF +75-10% 40V
103000357	00	CAP 220.0000MF +100-10% 63V
103000358	00	CAP 470.0000MF +100-10, 16V
103000359	00	CAP 25000.0000MF +75-10% 75V
103000360	00	CAP 3000.0000MF +75-10% 75V
103000361	00	CAP 15.UF 330V 0452-12
103000362	00	CAP 21.0000 UF 330V 0452-23
103000363	EE00	CAP .0200MF +20-20% 1400V
103000364	EE00	CAP .2200MF +20-20% 500V
103000365	EE00	CAP 21000.0000MF +75-10% 20V
103000366	00	CAP 2.2000MF +10-10% 15V
103000367	EE00	CAP 150.0000MF -10+75% 50V TSTEQ
103000368	00	CAP 24000.0000MF +75-10% 40V
103000369	00	CAP .2700MF +5-5% 50V
103000370	00	CAP .0470MF +5-5% 50V
103000371	00	CAP 47.0000MF +10-10% 20V
103000372	00	CAP 240.0000MF -10+75% 20V
103000373	00	CAP .0680MF +10-10% 50V AX LD
103000374	00	CAP 220.0000MF +20-20% 6V
103000375	00	CAP 82.0000MF +20-20% 6V
103000376	EE00	CAP TRIMMER 14-150PF 175WVDC TSTEQ
103000377	00	CAP .0560MF +10-10% 50V
103000378	00	CAP 2.0000MF +10-10% 440V
103000379	00	CAP 10448
103000380	00	LINE FLTR, RFI 5A 230VAC
103000381	EE00	CAP 130-156MF % 165V
103000382	00	CAP 3300.0000PF +10-10% 50V AX LD
103000383	00	CAP 1.8000MF +20-20% 50V
103000384	00	CAP 47.0000PF +5-5% 50VCER/AX
103000385	02	LINE FILTER EMI PWR 6A (LUGS)
103000386	00	CAP 30-36.0000MF +20-0% 330V
103000387	00	CAP 145-175.0000MF +20-0% 165V
103000388	00	CAP AMC SUPPRESSION .1MF-100 OHM 400V
103000389	EE00	CAP 700.0000MF - 10&75% 50V
103000390	00	LINE FILTER EMI PWR 6A (FASTONS)
103000391	00	CAP 100.0000MF +10-10% 25V
103000392	00	CAP 100.0000MF +1--10% 30V
103000393	00	CAP 38000.0000MF -10+75% 20VDC ELC
103000394	00	CAP .1800MF +20-20% 50V
103000395	EE00	CAP 8.0000MF +20-20% 100V
103000396	00	CAP 680.0000MF-10+100% 6.3V
103000397	00	CAP 20000.0000MF -10+75% 10V ELEC
103000398	00	CAP 680.0000PF +5-5% 50V CERAX
103000399	00	CAP .0330MF +10-10% 50V CERAX
103000400	00	CAP .006AMF +10-10% 135V AX LD
103000401	00	CAP .0100MF +10-10% 135V AX LD
103000402	00	CAP .0220MF +10-10% 1351 AX LD
103000403	00	CAP .0470MF +10-10% 135V AX LD
103000404	00	CAP 5.0000MF +20-20% 135V AX LD
103000405	00	470.0000MF -10+100% 40V AXLD
103000406	00	CAP 250.0000MF -10+50% 100V ELECT
103000407	00	CAP 740.0000MF -10+50% 250V ELECT
103000408	00	CAP 9A000.0000MF +75-10% 20V AL EL
103000409	EE00	CAP AMC SUP NTWK .1VFD 22 OHM 400V
103000410	00	CAP .220MF 6.3V
103000411	00	CAP 47.0000MF +10-10% 35V
103000412	00	CAP .0470MF +80-20% 50V CERAM
103000413	00	CAP .1000MF +80-20% 50V CERAM
103000414	00	CAP .8200PF +5-5% 200V AX LD
103000415	00	CAP 4700.0000PF +5-5% 200V AX LD
103000416	00	CAP 2200.0000PF +5-5% 200V AX LD
103000417	00	CAP (REF 116-000310,311)
103000418	00	CAP 6.8000MF +10-10% 15V AX LD
103000419	00	CAP 60000.0000MF 501 95578105
103000420	00	CAP 330.00004F -10+100% 25V AL/EL
103000421	00	CAP LINE FILTER (CORCOM) 3R1
103000422	00	CAP 4700.0000PF +10-10% 50V AX LD
103000423	00	CAP 2700.0000FD +50-10% 250VDC AL
103000424	00	CAP 6800.0000PF +5-5% 200V AX LD
103000425	00	CAP 68.0 MF +10-10% 15V TANT
103000426	00	CAP 27000.0000MF +20-20% 7.5V AL EL
103000427	00	CAP .0390MF +10-10% 600V RD LDO
103000428	00	LINE FLTR 5A 120V 2.5A 240VAC 50/60HZ
103000429	00	CAP 2500-0000MF -10+75% 10V AE AL
103000430	00	CAP 2300-0000MF -10+75% 50V EL AL
103000431	00	CAP 16500.0000MF -10+75% 6.3V ELECT
103000432	00	CAP .0082MF +20-20% 275V
103000433	00	CAP 2.0000MF +20-20% 275V
103000434	00	CAP .0047MF +20-20% 275V
103000435	00	CAP 3100.0000MF +75-10% 16V AL EL
103000436	EE00	CAP 132000.0000MF +75-10, 10V AL EL
103000437	00	CAP .0033MF +20-20% 3000V CER
103000438	00	R-C SUPP NTWK 100 OHM .039MF 1/2W
103000440	EE00	CAP .01MF +3-3% 600V
103000441	00	CAP .5600MF +3-3% 200VDC
103000442	00	CAP .3300MF +5-5% 200VDC
103000443	00	CAP .0100MF +20-20% 1400VVDC CR
103000444	00	CAP 2200-0000PF +10-10% 100V
103000446	00	CAP .3300MF +20-20% 270V RMS
103000447	00	CAP 2900.0000MF +75-10% 40V AL EL
103000448	00	CAP 100-0000MF +75-10% 50V
103000449	01	CAP 3300.0000MF % 200V
103000450	00	CAP .0470MF +20-20% 100V
103000451	00	CAP 100.0000MF +20-20% 10V
103000452	00	CAP 120.0000MF +10-10% 15V
103000453	00	CAP 2200.0000MF +75-10% 16V AL EL
103000454	00	CAP .2200MF +80-20% 50V CERMC
103000455	00	CAP 900.0000MF +75-10% 25V AL EL
103000456	00	CAP 1700.0000MF +75-10% 12V AL EL
103000457	00	CAP 1400.0000MF +75-10% 25V AL EL
103000458	00	330 MFD 250VDC 75% -10%
103000459	00	CAP .0068MF +20-20% 270V
103000460	00	CAP 20000.0000MF +10-10% 6V ELECT
103000461	00	LINE FILTER R.F.I 12AMP
103000462	00	CAP 5000.0000PF +20-20% 3KV CER
103000463	00	CAP 1.2000MF +10-10% 15V
103000464	EE00	CAP 1200.0000MF +75-10% 25V AX LD
103000465	EE00	CAP 130.0000MF +75-10% 100V AX LD
103000466	FF00	CAP 250.0000MF +75-10% 250V ALEL
103000467	00	CAP 820.0000MF +10-10% 6V TANT
103000468	00	CAP 12.0000MF +10-10% 6V TANT
103000469	00	CAP .4700MF +80-20% 50V CR AX
103000470	01	CAP 1100.0000MF &75-10% 200V MAT PR
103000471	00	LINE FILTER SAMP IGC JR
103000473	00	CAP 250.0000MF +75-10% 50V AXLD
103000474	00	CAP 3600.0000MF +75-10% 40V AL EL
103000475	00	CAP 39.0000MF 250V ELEC
103000476	00	CAP 750.0000MF +75-10% 50V AXLD
103000477	00	CAP .3300MF +20-20% 270V
103000478	00	LINE FILTER 3PHASE 10AMP
103000479	00	LINE FLTR 30AMP SGL PHASE 30K6 TSTEQ
103000480	00	LINE FILTER 30AMP 3PHASE 30T49Y TSTEQ
103000481	00	CAP 390.0000MF 50V ELECT
103000482	00	CAP .0820MF +10-10% V CR AX
103000483	00	CAP 180.0000MF -10+50% 250V AL EL
103000484	00	CAP 8200.UFD +75-10% 6.3V PC MT
103000485	00	CAP 1200.0000MF +75-10% 25V AL EL
103000486	00	CAP 330.0000MF +75-10% 50V AL EL
103000487	00	CAP 130.0000MF -10+75% 100V AL EL
103000488	00	CAP 0.0050MF +3-3, 600V
103000490	00	CAP 10000.0000MF +75-10, 12V AL EL
103000491	00	CAP 3300.0000MF +75-10% 40V PC MT
103000492	EE00	CAP 150.0000MF 150V PC MOUNT ELECT
103000493	EE00	CAP 1800.0000MF ELECT 30V AX LD
103000494	EE00	CAP 470.0000MF ELECT 100V AX LD
103000495	EE00	CAP 6800.0000MF ELECT 30V AX LD
103000496	00	CAP R00183-001
103000497	00	CAP 1.0000MF +80-20, 100V RD LD
103000498	00	CAP 100.0000MF + 100-10% 50V AL EL
103000499	00	CAP 3.0000MF +10-10% 400V
103000500	EE00	CAP .0250MF +20-20% 1000V

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103000501 through 104000163

PART NO.	REV	DESCRIPTION
103000501	EE00	CAP 220.0000MF +10-10% 10V TANT
103000502	EE00	CAP 560.0000MF +75-10% 50V AL EL
103000503	EE00	CAP 1200.0000MF +50-10% 250V AL EL
103000504	00	LINE FILTER 2AMP STUD TERMINAL
103000505	EE00	CAP 200.0000MF +50-10% 250V PC MT
103000506	EE00	CAP .1500MF +5-5% 400V RD LD
103000507	EE00	CAP 12.0000MF 660VAC
103000508	EE00	CAP ALUMINUM ELECTROLYTIC
103000509	EE00	CAP 25.0000MF -10+75% 16V AX LD
103000510	EE00	CAP 2200.0000MF 40V ELECT
103000511	EE00	CAP 100.0000MF 400V ELECT
103000512	EE00	CAP 33.0000MF +100-10% 100V AL EL
103000513	00	CAP 680.0000MF +75-10% 50V PC M
103000514	00	CAP 940.0000MF +50-10% 200V
103000515	EE00	CAP 11.0000PF +5-5% 50V AX LD
103000516	EE00	DUPLICATE NO., USE 103-268
103000517	00	CAP MOTOR BRUSH FIELD SER 70801-03
103000518	00	CAP 500UF 250V FIELD SERVICE
103000519	00	CAP 10UF 250V FIELD SERVICE
103000520	00	CAP 1UF +10-10% 200V FIELD SERVICE
103000521	00	CAP 0.33UF 12V FIELD SERVICE
103000522	00	CAP 0.005UF 25V FIELD SERVICE
103000523	00	CAP 0.1UF 25V FIELD SERVICE
103000524	EE00	CAP 6600.0000MF +75-10% 16V AX LD
103000525	EE00	CAP 1100.0000MF +75-10% 30V AX LD
103000526	00	CAP 4700.0000PF +5-5% 50V CERAM
103000527	00	CAP .0470MF +20-20% 200V CR
103000528	EE00	CAP 1000.0000MF +75-10% 35V PC MT
103000529	EE00	CAP .3300MF +10-10% 50V CR
103000530	00	CAP 470.0000MF % 50V AL EL
103000531	EE00	CAP 560.0000PF +5-5% NPO CR
103000532	EE00	CAP 6.8000MF +10-10% 10V AX LD
103000533	EE00	CAP 6.8000MF +10-10% 20V AX LD
103009999	EE00	CAP NON INSERTIBLE
104000001	00	XFMR HALON NOVA
104000002	00	XFMR 3:1
104000003	00	XFMR 1:1
104000004	00	XFMR F-109U
104000005	05	XFMR F-60U
104000006	00	XFMR CHOKE CLOCK S/N
104000007	00	XFMR
104000008	00	XFMR
104000009	00	XFMR
104000010	03	XFMR PWR-S/N
104000011	00	XFMR
104000012	01	XFMR MEMORY
104000013	00	XFMR HALON S/N
104000014	00	XFMR F-106Z
104000015	00	XFMR N16
104000016	00	XFMR ISOLATION 230/115
104000017	03	XFMR PWR 1200/800
104000018	00	INDTR CHOKE 100 uH +5-5%
104000019	00	XFMR SOLENOID
104000020	01	XFMR SUPERCEDED BY 104000030
104000021	01	XFMR SUPERCEDED BY 104000031
104000022	04	XFMR PWR-1210
104000023	02	XFMR PWR-1220/820
104000026	00	XFMR F-108U 115V-24V 96VA
104000028	01	XFMR CENTER TAP BIFILAR COIL
104000029	00	XFMR SINGLE WOUND COIL
104000030	00	XFMR STEP DOWN/P5555
104000031	00	XFMR STEP DOWN 230/115 50/60HZ VA1000
104000032	00	INDTR 15 uH COIL
104000033	00	INDTR 1 uH COIL
104000034	EE00	XFMR COIL ASSY +- 15 MHD
104000035	EE00	XFMR COIL ASSY +5 MHD
104000036	00	COIL HOLD ELECTROMAGNET 4000 TURNS
104000037	00	XFMR TRIAD F107Z
104000038	01	XFMR MMC-4814
104000039	01	XFORMER 5-28/15-10
104000040	00	XFMR CONSTANT VOLTAGE 5-35/15-10
104000041	01	XFMR PWR LINEAR 170W
104000042	EE01	XFMR CONSTANT VOLTAGE
104000043	05	XFMR 36VOLT 16AMP & 36VOLT 13AMP
104000044	02	XFMR 50 HZ CUT 600 VA
104000045	02	XFMR CUT 5-60/15-15 60 HZ
104000046	02	XFMR CVT 5-60/15-15 50 HZ
104000047	02	XFMR COIL
104000048	00	XFMR 24:8
104000049	00	XFMR 110/220V 50HZ
104000050	00	XFMR PULSE,8H ELECTRONICS
104000051	01	XFMR 115V TO 230V,STEP UP,1000VA
104000052	00	XFMR MMC 5030 1:12
104000053	00	COIL CLOCK HEAD 35 TURNS
104000054	00	XFMR 25.2V CT @ .060A MICROTRAN 2512
104000055	00	INDTR .10 uH +10-10%
104000056	00	INDTR .12 uH +10-10%
104000057	00	INDTR .15 uH +10-10%
104000058	00	INDTR .18 uH +10-10%
104000059	00	INDTR .22 uH +10-10%
104000060	00	INDTR .27 uH +10-10%
104000061	00	INDTR .33 uH +10-10%
104000062	00	INDTR .39 uH +10-10%
104000063	00	INDTR .47 uH +10-10%
104000064	00	INDTR .56 uH +10-10%
104000065	00	INDTR .68 uH +10-10%
104000066	00	INDTR .82 uH +10-10%

PART NO.	REV	DESCRIPTION
104000067	00	INDTR 1.20 uH +10-10%
104000068	00	INDTR 1.50 uH +10-10%
104000069	00	INDTR 1.80 uH +10-10%
104000070	00	INDTR 2.20 uH +10-10%
104000071	00	INDTR 2.70 uH +10-10%
104000072	00	INDTR 3.30 uH +10-10%
104000073	00	INDTR 3.90 uH +10-10%
104000074	00	INDTR 4.70 uH +10-10%
104000075	00	INDTR 5.60 uH +10-10%
104000076	00	INDTR 6.80 uH +10-10%
104000077	00	INDTR 8.20 uH +10-10%
104000078	00	INDTR 10.00 uH +10-10%
104000079	00	INDTR 12.00 uH +10-10%
104000080	00	INDTR 18.00 uH +10-10%
104000081	00	INDTR 22.00 uH +10-10%
104000082	00	INDTR 27.00 uH +5-5%
104000083	00	INDTR 33.00 uH +5-5%
104000084	00	INDTR 39.00 uH +5-5%
104000085	00	INDTR 47.00 uH +5-5%
104000086	00	INDTR 56.00 uH +5-5%
104000087	00	INDTR 68.00 uH +5-5%
104000088	00	INDTR 82.00 uH +5-5%
104000089	00	INDTR 120.00 uH +5-5%
104000090	00	INDTR 150.00 uH +5-5%
104000091	00	INDTR 180.00 uH +5-5%
104000092	00	INDTR 220.00 uH +5-5%
104000093	00	INDTR 270.00 uH +5-5%
104000094	00	INDTR 330.00 uH +5-5%
104000095	00	INDTR 390.00 uH +5-5%
104000096	00	INDTR 470.00 uH +5-5%
104000097	00	INDTR 560.00 uH +5-5%
104000098	00	INDTR 680.00 uH +5-5%
104000099	00	INDTR 820.00 uH +5-5%
104000100	00	INDTR 1000.00 uH +5-5%
104000101	00	INDTR 1200.00 uH +10-10%
104000102	00	INDTR 1500.00 uH +10-10%
104000103	00	INDTR 1800.00 uH +10-10%
104000104	00	INDTR 2200.00 uH +10-10%
104000105	00	INDTR 2700.00 uH +10-10%
104000106	00	INDTR 3300.00 uH +10-10%
104000107	00	INDTR 3900.00 uH +10-10%
104000108	00	INDTR 4700.00 uH +10-10%
104000109	00	INDTR 5600.00 uH +10-10%
104000110	00	INDTR 6800.00 uH +10-10%
104000111	00	INDTR 8200.00 uH +10-10%
104000112	00	INDTR 10000.00 uH +10-10%
104000113	00	XFMR POWER MERRIMACK
104000114	00	XFMR ASSY 12-115V 20015601
104000115	00	XFMR ASSY 24-115V 20015501
104000116	00	XFMR 50/60HZ 115V 00000134
104000117	00	INDTR 330.00 uH -10%
104000118	03	XFMR LINEAR PWR CRT 6012 MMC5189
104000119	00	XFMR POWER FOR 4080B BT383
104000120	00	XFMR CONSTANT VOLTAGE ELB7-7 60HZ
104000121	00	XFMR 50HZ 7SLOT CON VLTG ELBD
104000122	00	DELAY LINE 0-50 NS DL 800
104000123	EE00	XFMR CON VLTG 16 SLOT 60HZ ELBD
104000124	EE00	XFMR CON VLTG 16 SLOT 50HZ ELBD
104000125	00	TRANSFORMER POWER DRIVE 50-55033-3
104000126	00	XFMR 4.5VA 50/60HZ PC2608
104000127	00	XFMR POWER SINGLE PHASE 560-306
104000128	00	XFMR IC REGULATOR 5V 00000632
104000129	00	XFMR TRANSFORMER ASSY 20127101
104000130	00	XFMR DELAY LINE 35NSEC
104000131	EE00	XFMR VARIAC W30463 TSTEQ
104000132	00	XFMR COIL ASSY 240753-001/801080-002
104000133	EE00	XFMR CONSTANT VOLTAGE 60HZ ECLIPSE
104000134	EE00	VARIAC 240W 50/60HZ 3150-5110 TSTEQ
104000135	00	DELAY LINE 2000HM 75NSGC 5%TOL 9ELBD
104000136	02	XFMR PWR 50/60HZ 5379
104000137	00	INDTR 56 uH#10% WEE-56,000
104000138	07	XFMR CONSTANT VOLTAGE MMC5537
104000139	01	XFMR PWR 5518
104000140	00	XFMR TRIAD PWR TY68S +250V/+100-100V
104000141	00	DELAY LINE 20-60NS VAR 0448-0060-50
104000142	04	XFMR 100-220V 50HZ FLEX DISK P/S
104000143	04	XFMR 115V 60HZ FLEX DISK P/S
104000144	EE00	XFMR 24V & 5V CD EQUIP
104000145	02	XFMR LINEA PWR UNIV COMM CHASSIS
104000146	EE00	CHOKE FILTER, ECLP
104000147	02	XFMR LINEAR 375W 50/60HZ 30V 5628
104000148	03	XFMR LINEAR 500W 50/60HZ 30V 5655
104000149	00	INDUCTOR 6.8uH +10-10% SWD-6.8
104000150	00	INDUCTOR 1.8uH +10-10% SWD-1.8
104000151	01	XFMR TOROIDAL N3/4
104000152	00	TRANSFORMER PWR SPLY 200264
104000153	00	DELAY LINE ANALOG TD 600
104000154	00	XFMR POWR XFMR ASSEMBLY 201103
104000155	01	XFMR CVT 208V PRI
104000156	01	XFMR LINEAR
104000157	04	XFMR CONSTANT VOLT 50HZ, CTG DISK
104000158	EE00	VARIAC GEN RADIO W5G2 TSTEQ
104000159	EE00	XFMR HI/LOW LN STO 10341
104000160	01	XFMR TOROIDAL N3/12
104000161	00	XFMR 92371-060
104000162	02	XFMR CV MMC5608
104000163	EE00	XFMR STEP DOWN 115/6.3V 10-5

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104000164 through 105000006

PART NO.	REV	DESCRIPTION
104000164	04	XFMR LINEAR 200W 50/60 MMC-5971
104000165	06	XFMR PWR, DSPL TERM
104000166	01	XFMR TOROIDAL MOM
104000167	01	INDTR TOROIDAL 88uH +10-10%
104000168	00	INDTR 300.00 uH 10% TOROID
104000169	EE00	XFMR VARIAC 120V 3060-5012 TSTEQ
104000170	EE00	XFMR VARIAC 240V 3100-5012 TSTEQ
104000171	EE00	XFMR 117V TRIAD F-207U TSTEQ
104000172	01	XFMR LINEAR 50/60HZ MMC5987
104000173	EE00	XFMR LINEAR 500W 50/60HZ 30V
104000174	EE00	XFMR LINEAR 800W 50/60HZ 30V
104000175	00	INDTR 35uH TOROIDAL
104000176	00	INDTR 45uH TOROID +10-10%
104000177	EE00	XFMR PT-22C TSTEQ
104000178	01	INDTR TOROID 750uH+10-10%
104000179	EE00	XFMR PT22D
104000180	03	XFMR LINEAR 50/60HZ MMC-5956-1
104000181	EE00	XFMR F-54X TSTEQ
104000182	01	DELAY LINE 30NS 10 TAP
104000183	00	XFMR TOROIDAL 6T, 50T
104000184	02	XFMR CURR TOROIDAL 500T : 1T
104000185	02	XFMR PRI 47 uH SEC 33 uH
104000186	02	CHOKE TOROID -5V +20-20% 20uH
104000187	02	CHOKE TOROID -5V +20-20% 8uH
104000188	02	XFMR 60HZ FERRO-RES MMC-5752-1
104000189	02	XFMR 50HZ FERRO-RES MMC-5807-1
104000190	01	XFMR LINEAR
104000191	01	XFMR CVT 208V 50HZ
104000192	EE00	XFMR LINEAR 900W 50/60HZ 30V
104000193	01	DELAY LINE TAPPED 75NSEC 200 OHM
104000194	01	XFMR 50HZ 30 LINEAR 208V SECONDARY
104000195	00	XFMR 220/240V 3730-159
104000196	00	XFMR 240V 3900-506
104000197	00	XFMR 220V 3900-502
104000198	03	XFMR TOROIDAL CHOKE +5V
104000199	EE00	XFMR CUP CORE CHOKE 80V
104000200	EE00	XFMR TOROIDAL CHOKE-5V
104000201	03	XFMR POT CORE PWR
104000202	EE00	XFMR PULSE
104000203	03	XFMR CORE, DRIVER
104000204	04	XFMR +15V CORE, PWR
104000205	03	XFMR +5V CORE, PWR
104000206	02	XFMR LINEAR 900W
104000207	01	XFMR CURRENT SENSING I.T.D.
104000208	01	INDTR 170uH
104000209	00	XFMR PC MTG I.T.D.
104000210	00	INDTR 88 uH TOROID
104000211	00	INDTR 129uH TOROIDAL
104000212	00	XFMR TOROID MNOVA A/D, D/A
104000213	01	INDTR 150 uH COMPATIBLE WITH TL 497
104000214	00	DELAY LINE DIGITAL 500 NS 5 TAPS
104000215	00	DELAY LINE DIGITAL 50NS 5 TAPS
104000216	02	XFMR TOROIDAL E500
104000217	01	INDTR TORIDAL 72UH F500
104000218	EE00	INDTR VARIABLE DELAY LINE V1570
104000219	02	XFMR LINEAR 50/60HZ 50M'BYTE
104000220	01	XFMR LINEAR 50/60HZ 50M'BYTE ZEBRA
104000221	00	XFMR FERRO RESN 50HZ 50M'BYTE ZEBRA
104000222	00	XFMR FERRO-RESN 60HZ 50M'BYTE ZEBRA
104000223	EE00	DELAY LINE 500NS 2TAPS
104000224	00	XFMR TOROIDAL 3.5:1 MNOVA
104000225	00	DELAY LINE 75NSEC TAPPED 50 OHM
104000226	00	XFMR CTL 120/240V PRI 24VCT SEC 75VA
104000227	01	REPLACED BY 104000233
104000228	00	XFMR FH DISC 16869
104000229	02	XFMR DRIVER
104000230	00	XFMR OVERCURRENT
104000231	03	XFMR MAIN PWR
104000232	00	INDTR 1.0 uH (TOROIDAL)
104000233	00	XFMR TOROIDAL 1:1 200 uH INDUCTANCE
104000234	00	XFMR E-CORE 5V 100AMPS
104000235	02	INDTR 5.50uH TOROIDAL
104000236	00	XFMR PWR POINT OF SALE SYSTEM
104000237	00	XFMR TOROIDAL 10:15019'
104000238	EE00	XFMR DRIVER
104000239	02	XFMR HI VOLTAGE FLYHACK
104000240	EE00	XFMR HORIZONTAL WIDTH COIL
104000241	02	XFMR MAGNETIC DEFLECTION YOKE
104000242	EE00	DELAY LINE 25NS 10TAP
104000243	00	INDTR 1.0uH TOROIDAL
104000244	03	XFMR AP-130 P/S
104000245	00	INDTR 10uH +10-10% 5AMP (ROD TYPE)
104000246	00	INDTR 1-3 uH +10-10% TOROID
104000247	01	XFMR FERRITE E CORE BASE DRIVE
104000248	01	XFMR,FERRITE CORE CURRENT
104000249	00	CHOKE +5V DGC SPEC# 009-131
104000250	01	INDTR LAMINATED STL 5UH DGC
104000251	01	XFMR POT CORE BASE DRIVE DGC
104000252	00	XFMR POT CORE 1011 DGC
104000253	EE00	CHOKE ASSY 26T PRIMARY
104000254	00	POT PHASING 50K LOGIC PCB 801083-503
104000255	00	XFMR POWER 2230 800942-003
104000256	00	XFMR POWER 2260 801199-001
104000257	00	XFMR POWER 2290 801139-001
104000258	00	XFMR TOROIDAL DGC BBU
104000259	EE00	XFMR LINEAR PWR
104000260	01	XFMR MINIATURE DGC P/S
104000261	01	XFMR LINEAR PWR 50/60HZ
104000262	EE00	INDTR COMMON MODE FILTER DGC P/S
104000263	01	XFMR MAIN INVERTER DGC P/S
104000264	00	XFMR 110-30VCT (1.2VA) 50/60HZ
104000265	00	INDTR 160UH
104000266	02	XFMR FLYBACK PWR
104000267	03	XFMR BASE DRIVE
104000268	00	INDTR 5UH
104000269	01	CHOKE MULTIPLE WINDING DGC-JR
104000270	01	CHOKE MULTIPLE WINDING DGC-JR
104000271	00	INDIR LINEARITY COIL
104000272	00	DELAY LINE 100 NSEC 100 OHM
104000273	00	DELAY LINE VARIABLE 30NSEC 100 OHM
104000274	00	INDTR TOROID DGC FILTER DGC P/S
104000275	02	XFMR FLYBACK SWITCH MODE
104000276	00	XFMR MMC 7061
104000277	01	XFMR SOC MAIN INVERTER
104000278	00	INDTR 25A PE51175
104000279	EE00	INDTR 1 uH 250MA
104000280	EE00	XFMR MMC 7060
104000281	EE00	INDTR COIL BASE-DRIVE
104000282	02	XFMR MDC MAIN INVERTER
104000283	00	XFMR HIGH FREQ INVERTER
104000284	00	XFMR 18VA 36V-CT 50/60HZ DGC-JR
104000285	02	INDIR FILTER VNR
104000286	00	REPLACED WITH 104-292
104000287	00	XFMR P8617 F-2137
104000288	01	INDUCTOR 20 uH
104000289	02	XFMR LINEAR PWR 50/60HZ
104000290	00	INDTR TOROIDIAL 12.6 UH
104000291	00	XFMR AC SIGNAL
104000292	02	XFMR TIMING 60HZ
104000293	01	XFMR MAIN INVERTER
104000294	00	INDTR 10uH
104000295	00	DELAY LINE 100 OHM 14PIN DIP SPECIAL
104000296	00	INDTR 1.5 uH DUAL WINDING
104000297	01	INDTR 2uH 15AMP
104000298	00	INTDR 400uH .5AMP
104000299	00	XFMR BBU E-CORE
104000300	00	XFMR BASE 6 TO 1 TO 1
104000301	01	XFMR FLYBACK 1.8 TO 1
104000302	00	DELAY LINE PULSE GENERATOR 41/41
104000303	EE00	XFMR PWR
104000304	00	INDTR 4.7uH +10-10% SEAL MINIATURE
104000305	00	INDTR 1.2uH +10-10% SEAL MINIATURE
104000306	00	INDTR 1000uH +10-10% SEAL MINIATURE
104000307	01	XFMR 1.0 uH PULSE PE61020
104000308	EE00	DELAY LINE 15NSEC
104000309	EE00	INDTR 250 uH IDC MAX=2.5AMPS
104000310	00	DELAY LINE PULSE GENERATOR 45/45
104000311	01	CHOKE 3PHASE COMMON MODE
104000312	EE00	XFMR PWR 400MA 40VRMS 50/60HZ
104000314	00	INDTR 65uH
104000315	00	CHOKE 12V OUTPUT
104000316	00	CHOKE 5V OUTPUT
104000317	00	XFMR PWR 20K HZ
104000318	00	XFMR OVERCURRENT SENSE
104000319	00	XFMR PWR 25W
104000320	00	INDTR MULTI-WINDING
104000321	00	XFMR BASEDRIVE
104000322	03	XFMR FLYBACK SWITCHMODE
104000323	00	INDTR 10uH 7AMP TOROID
104000324	01	INDUCTOR LINE FLTR INPUT
104000325	00	XFMR 60HZ STD 8300 N.AMER 251704-007
104000326	00	XFMR 50/60 HZ UNIV/INTNTL 251704-008
104000327	EE00	XFMR PWR SWITCHER
104000328	EE00	INDTR PWR SWITCHER TAP
104000329	00	INDUCTOR LINE FILTER
104000330	EE00	INDUCTOR 16uH
104000331	01	INDUCTOR LINE FILTER
104000332	EE00	XFMR LINEAR PWR
104000333	01	XFMR
104000334	01	INDTR TORROID 42uH
104000335	EE00	XFMR PCB MTG DST-4-12
104000336	EE00	XFMR LINEAR PWR HZ
104000337	00	XFMR PULSE
104000338	EE00	XFMR 24VCT 115V 60HZ
104000339	EE00	INDTR 2uH 20KHZ
104000340	EE00	INDTR 110UH 20KHZ
104000341	EE00	XFMR CVT
104000342	EE00	XFMR LINEAR
104000343	EE00	DELAY LINE 50NS 10TAP 50 OHM
104000344	EE00	CHOKE 1uH 10A
104000346	EE00	XFMR LINEAR PWR (12VA)
104000347	EE00	MAGNETIC DEFLECTION YOKE W/CONNECTOR
104800158	05	XFMR CONSTANT VOLTAGE MMC5537
104999800	00	TRANSFORMER FAMILY SPECIFICATION
105000001	00	CORE FERRITE CF102
105000002	00	CORE FERRITE S/N ONLY
105000003	01	CORE U FERRITE
105000004	00	CHOKE FERRITE LARGE
105000005	00	CHOKE FERRITE SMALL
105000006	00	CORE FERRITE

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105000008 through 110000167

PART NO.	REV	DESCRIPTION
105000008	02	CORE U FERRITE
105000009	00	CORE FERRITE CF101
105000010	00	CORE "I" FERRITE
105000011	00	CORE FERRITE TOROIDAL .018 EMM
105000012	00	CORE FERRITE SLUG 1X1X3 1/2"
105000013	00	CORE FERRITE 18 MIL DGC
105000014	00	CORE FERRITE HALF WITH 1/8 GAP
105000015	00	CORE 18/11 M7 MEM
105000016	00	CHOKE SPECIAL 10097-27
105000017	00	CORE FERRITE 18MULS MEM REPAIR
105000019	00	CORE MPP TOROID A050056-2
105000020	EE00	CORE FERRITE TOROID 768T188/3E2A
105000021	00	CHOKE VERTICAL 6-003-0321
105000022	EE00	COREE POWERED IRON TOROID A-206 068-2
105000023	EE00	CORE FERRITE MEM 14 MIL
105000024	00	CORE FERRITE-SMALL,UNGAPPED
105000025	00	CORE FERRITE TOROID A-254168-2
105000026	EE00	CORE FERRITE PWR FERROXCUBE EC-35
105000027	EE00	CORE FERRITE PWR FERROXCUBE EC-54
105000028	EE00	CORE FERRITE BOBBIN FERRXCUBE EC35PTB
105000029	EE00	CORE FERRITE BOBBIN FERRXCUBE EC54PTB
105000030	EE00	CORE TOROIDAL 1.3 ODX,785IDX,420HT
105000031	EE00	CORE FERRITE XFMR EC 72
105000032	EE00	CORE TOROID A083-081-2
105000033	00	CORE TOROID MOLYPERMALLOY
105000034	EE00	CORE PERMALLOY
105000035	00	CORE MOLYPERM TOROID 60M
105000036	EE00	CORE FERRITE TORID MAG 1.5" E500
105000037	EE00	CORE FERRITE 768T188-3C8
105000038	EE00	CORE MAGNETIC
105000039	EE00	CORE FERRITE 3E2A,846T250 TOROID
105000040	00	CORE FERRITE POT 3622
105000041	00	CORE TOROID
110000001	00	RELAY REED RBM 99401242-3
110000002	01	RELAY BRSR1-901
110000004	00	SWITCH MICRO 1321D8
110000005	00	SWITCH MICRO V3-23-D8
110000006	00	ACTUATOR KIT MICRO JV-91
110000009	00	SWITCH 83261A1561-238
110000010	00	ACTUATOR AH H 83503
110000011	00	CONTACT BLOCK 83500-90
110000013	00	LENS AH H 83500-90
110000014	00	SWITCH AH H 82603
110000015	00	SWITCH AH H 82613
110000016	02	SWITCH C&K 7101CSP
110000017	01	SWITCH C&K 7105CSP
110000018	02	SWITCH C&K 7205CSP
110000019	01	SWITCH C&K 7103A
110000020	00	SWITCH FECO 177608
110000021	00	SWITCH C&H 7691K74-F27
110000022	00	HARDWARE KIT 768G
110000023	01	SWITCH C&K 7201A
110000024	00	SWITCH CH 7561K74-F27
110000025	00	SWITCH CH 7561K54-F27
110000026	01	SWITCH CK 7105SYPZ
110000027	01	SWITCH CK 7211SYPZ
110000028	01	SWITCH CK 7301SYPZ
110000029	01	SWITCH CK 7109SYPZ
110000030	01	SWITCH CK 7101SYPZ
110000031	00	RELAY AC P&B KUP 12A95
110000032	00	RELAY REED P.B. JDT15DB1 FORM A
110000033	00	RELAY REED P.B. JDT62DB3 FORM C
110000034	01	SWITCH CK 7215SYPZ
110000035	01	SWITCH TOGGLE CK 7101CSPX-EQUIV
110000036	01	SWITCH CK7105CSPX SATIN OR EQUIV
110000037	01	SWITCH CK7205 CSPX SATIN OR EQUIV
110000038	00	SWITCH MICRO HONEYWELL 1SM1
110000039	00	RELAY POTTER BRUMFIELD 6VAC DPST PR
110000040	00	RELAY POTTER BRUMFIELD 6VAC PMT 17A
110000041	00	RELAY JRM 1000 PR 1AMP 10 WATT
110000042	00	RELAY 4897-990
110000043	01	RELUCTANCE PICK-UP 6815013
110000044	00	SWITCH THUMBWHEEL #189220 1 POLE DEC.
110000045	01	SWITCH 7103SY PWGEAV-2-X
110000046	00	RELAY RBM 91252-103
110000047	00	RELAY 50HZ 230V
110000048	00	SWITCH 435166-1
110000049	00	OBSOLETE REPLACED BY 110-63
110000050	00	SWITCH DIP 4 POS SWITCH AMP #435166-2
110000051	01	SWITCH CK 7304ZQEJ2
110000052	00	AMP DISTRIBUTOR 4325166-3
110000053	00	SWITCH DIP 5 POS AMP 435166-3
110000054	00	RELAY DRY REED W103MPCX-4
110000055	00	RELAY DRY REED W101MPCX-3
110000056	00	RELAY MERC WETTED 172-212EB3 MIDTEX
110000057	00	RELAY MERC WETTED W132MPCX-4
110000058	00	SWITCH 7203ZQEJ2 C&K
110000059	00	SWITCH DP3P ROCKER
110000060	EE00	SOLENOID LEDEX #124911-030
110000061	00	SWITCH SPST CUTLER HAMMER 7561K74
110000062	00	RELAY W107DIP-1
110000063	00	SWITCH 8-POS AMP 435166-5
110000064	00	SWITCH 3PDT 15A/CONTACT
110000065	03	SWITCH MINI TOGGLE MOMENTARY
110000066	03	SWITCH MINI TOGGLE MAINTAINING
110000067	05	SWITCH SELECTOR
110000068	06	SWITCH SELECTOR (POWER)
110000069	01	SWITCH TOGGLE,MOMENTARY
110000070	01	SWITCH TOGGLE,MAINTAIN
110000071	00	SWITCH MICRO #311SM701-T
110000072	00	SW PRESS 10" FAIRCHILD #PSF100A-10C
110000073	00	SW PRESS 20" FAIRCHILD #PSF100A-20C
110000074	00	SWITCH MOM ACT 101 SN11
110000075	00	SWITCH OAK 390 DP TWO POS
110000076	00	SWITCH LOW TORQUE 1-NO,CHERRY#E51-51T
110000077	00	SWITCH .251 STM RLR, MICRO#311SM4-T
110000078	00	SWITCH FLEX LEAF W/RLR,MICRO#111SM2-T
110000079	00	SWITCH OPT 2-CHAN, HEI#0S562A-060LW
110000080	00	RELAY TP DR 1435-IC-12D GUARDIAN
110000081	00	SWITCH ON/OFF 525492001
110000082	00	SWITCH SELECT 525493001
110000083	00	SWITCH TOP OF FORM 525494001
110000084	00	SWITCH OVERRIDE 525495001
110000085	00	SWITCH LIMIT (REED) 525721001
110000086	00	SWITCH & INDICATOR FORWARD100104-001
110000087	00	SWITCH & INDICATOR LOAD 100104-002
110000088	00	SWITCH & INDICATOR ON LINE100104-003
110000089	00	SWITCH & INDICATOR REVERSE100104-004
110000090	00	SWITCH REWIND 100130-001
110000091	00	SWITCH RESET 100130-002
110000092	00	SWITCH MICRO 15MI-T/J55 100012
110000093	00	SWITCH PAPER OUT 525272001
110000094	00	SWITCH & INDICATOR POWER 100179-001
110000095	00	SWITCH LOAD RUN 10541
110000096	00	SWITCH TOGGLE 197081
110000097	00	RELAY 181810
110000098	00	RELAY 25A 120V AC 00000901
110000099	00	SWITCH PB SPDT POWER 00000319
110000100	00	SWITCH PB SPDT RESET 00000320
110000101	00	SWITCH PB SPST STOP 00000321
110000102	00	RELAY TIME DELAY 90380-001
110000103	00	RELAY GENERAL PURPOSE 90381-001
110000104	00	SWITCH MICRO 90734-001
110000105	00	RELAY POWER DIST 90382-001
110000106	00	SWITCH MICRO 800129-001
110000107	00	SWITCH MERCURY 800222-001
110000108	00	SWITCH 800303-001
110000109	00	SWITCH MOMENTRY STDP 800305-002
110000110	00	SWITCH 800306-001
110000111	00	SWITCH RIBBON REVERSE 206840-001
110000112	00	SWITCH PAPER OUT UPPER 212634-001
110000113	00	SWITCH PAPER OUT LOWER 214959-001
110000114	00	SWITCH MOM PUSH CHEAT INTLK E69-30A
110000115	00	RELAY DRL POLE, 10 SEC DELAY
110000116	00	SWITCH TOGGLE 3 POSITION TDT02DD93
110000117	00	SWITCH REWIND 150006701
110000118	00	SWITCH C&K 52 PODL HNDL U33-J2 CRT DSP
110000119	00	SWITCH ALT ACTION 416004901
110000120	00	SWITCH MOM ACTION 416004902
110000121	00	RELAY 384105013
110000122	00	SWITCH PUSH 805015006
110000123	01	SWITCH MINI TOGGLE, MOMENTARY ELBD
110000124	00	SWITCH PAPER OUT LWR 2440 218811-001
110000125	00	SWITCH PAPER OUT #1 2440 218086-001
110000126	00	SWITCH PAPER OUT #1 2240 800944-001
110000127	00	SWITCH ROCKER 2440 800931-001
110000128	00	SWITCH USE 110-332 235595-001
110000129	00	SWITCH USE 110-297 233585-001
110000150	00	SWITCH TOGGLE 800502-004
110000151	00	SWITCH TOGGLE 800502-003
110000152	01	SWITCH MINI TOGGLE MAINTAIN 4SURFDISK
110000153	00	SWITCH SNAP-ACTION 100252-001
110000154	00	SWITCH SUMP PUMP F59A-2
110000155	00	SWITCH PUSH TYPE 416004903
110000156	00	SWITCH REWIND 150006701
110000157	00	SWITCH ARROW-HART DPST #82607
110000158	00	SWITCH HOUSING 120-856
110000159	00	SWITCH SNAP ACTION SPDT 120-563
110000140	00	SWITCH AUTO SHUT 120-851
110000141	00	SWITCH DOOR INTERLOCK 120-865
110000142	00	SWITCH PUSHBUTTON 120-965
110000143	00	RELAY DPST, R40-E2-W2-V200
110000144	00	RELAY SOCKET W/RTNR R40-S410 R40-P33
110000145	00	SWITCH HOPPER ACTUATOR 20111301
110000146	00	SWITCH HOPPER EMPTY ASSY 20137601
110000147	00	SWITCH OPTICAL SW ASSY 20127601
110000148	00	SWITCH TACTILE(STOP-START)00000946
110000149	00	SWITCH 2 POLE (POWER) 00000947
110000150	00	SWITCH REED 01045-001
110000151	00	SWITCH ROT 9 POS 2 POL 01017-003
110000152	00	SWITCH SLIDE SPOT 01017-004
110000153	00	SWITCH SLIDE 2 POL 2POS 01017-005
110000154	00	SWITCH 3P PROTECTOR 60HZ 250V A/HPAX
110000155	00	SWITCH THMBWHL 8012G STOP PINS BLK
110000156	00	RELAY 12 VOLT 801010-001
110000157	00	RELAY REED 50VA CONTACTS 6VDC COIL
110000158	00	SWITCH WRITE ENABLE ASSY 200378
110000159	00	SWITCH MAC-100-1 MUG HD CTG DISK
110000160	00	RELAY BREAK 100215
110000161	00	SWITCH BSIC V3L-1420D8 CTG DISK
110000162	00	SWITCH POWER 120-976
110000163	00	SWITCH CARTRIDGE INTERLOCK15250
110000164	00	RELAY 6PDT 6-3V W67CSX-11 TSTEQ
110000165	00	SWITCH SPDT PUSH ON-OFF MSP1050 TSTEQ
110000166	EE00	SWITCH 15120 TSTEQ
110000167	EE00	SWITCH 1405 TSTEQ

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110000168 through 110000363

PART NO.	REV	DESCRIPTION
110000168	EE00	SWITCH JBT MS25068-23 TSTEQ
110000169	EE00	SWITCH C&H 7561K74-F27 TSTEQ
110000170	EE00	SWITCH ROTARY 2501 TSTEQ
110000171	EE00	SWITCH 5 POS 6P JV9007 TSTEQ
110000172	EE00	SWITCH ROTARY 1403 TSTEQ
110000173	EE00	SWITCH ROTARY CTS T205 12 POS TSTEQ
110000174	EE00	SWITCH ROTARY CTS T2053 POS TSTEQ
110000175	EE00	RELAY 15A CONT 6W 250HM W88KX-1 TSTEQ
110000176	00	SWITCH PACK DETECT AA01AA
110000177	EE00	SWITCH ROTARY JV9001 1P 2-17 POSTSTEQ
110000178	00	SWITCH C+K 5A UL APR DPDT U213ZQJX
110000179	00	SWITCH MINI TOGGLE MNTN DPDT
110000180	00	SWITCH CLEAR/DETECT 15300
110000181	00	SWITCH WRITE PRCTECT 70682
110000182	00	SWITCH LOAD/RUN 10709
110000183	00	RELAY REED 8VA FORM C W172DIP-4
110000184	EE00	SWITCH 3P PROT 230/50
110000185	EE00	SWITCH 6 POS ROTARY CTS T-226 TSTEQ
110000186	00	SWITCH DPDT 3 PCSITION
110000187	00	SWITCH INDICATING PLATE MAN/AUTO
110000188	00	SWITCH LOCKING RING FOR 3POS SW
110000189	00	SWITCH DUAL IN-LINE 435385-4 AMP
110000190	01	SWITCH DBL POLE SGL THROW CARLING
110000191	03	RELAY SOLID STATE 240V 10 AMP
110000192	00	SWITCH OPTICAL OS-561A-060W
110000193	00	SWITCH SUBMINIATURE 92335003
110000194	00	SWITCH SUBMINIATURE 92335011
110000195	00	SWITCH SUBMINIATURE 94141014
110000196	00	SWITCH MINIATURE 93984000
110000197	EE00	SWITCH ROTARY 4 POLE 6POS TSTEQ
110000198	01	SWTICH MINI-TG,, DPDT, 2 POS
110000199	00	RELAY 2PDT 24VDC KUP11D15
110000200	00	RELAY 2PDT 24VDC PR11DY0
110000201	00	SWITCH SNAP ACTION E22-75HX CHERRY
110000202	EE00	SWITCH DPDT 20A 80975 TSTEQ
110000203	EE00	SWITCH INTLK CHEAT DBL POLE E79-30A
110000204	EE00	SWITCH MINI TOGGLE DPDT 7201
110000205	EE00	SWITCH MICRO 5A 250VAC L4 311SX3-T
110000206	00	SWITCH PRESSURE PSF100A-3
110000207	00	RELUCTANCE PICK UP 1R250-1000ST
110000208	EE00	RELAY PACK DPST W117DIP-9 TSTEQ
110000209	00	SWITCH SUBMINIATURE 75724402
110000210	00	RELAY 15A 3PDT 24VDC FPR-33-UNDC-AE
110000211	EE00	SWITCH DPDT 6 TERM MS35059-21 TSTEQ
110000212	EE00	SWITCH 5POS DP ROTARY MRA-2-5 TSTEQ
110000213	EE00	SWITCH MAG OPER SOL STATE 553S16
110000214	01	SWITCH SELECTOR
110000215	01	SWITCH SELECTOR N3
110000216	00	SWITCH MAG OPER CYL HALL 103SR5
110000217	00	RELAY POWER 100280
110000218	00	RELAY MOTOR STARTING 115V 100258
110000219	00	SWITCH VACUUM SWITCH 100287
110000220	00	RELAY MOTOR STARTING 230V 100374
110000221	00	SWITCH + IND RESET/UNIT 100104-011
110000222	00	SWITCH THUMBWHEEL 200544
110000223	00	SWITCH MICRO 100071
110000224	00	SWITCH TOGGLE SWITCH 100015
110000225	00	RELAY K1 RELAY 100279
110000226	00	SWITCH DPDT 15/125 10/250 TGD0511-THB
110000227	00	SWITCH MAG SENSOR #3050
110000228	00	SWITCH PUSH-PULL E68-30A GOLD
110000229	00	SWITCH MIN BASIC STYLE 35 1.40 LG
110000230	00	RELAY 12V 4PDT 5A
110000231	01	RELAY 30 SEC TIME DLY CAP 230VAC
110000232	00	RELAY DPST DUAL INLINE 191TE2A1-12G
110000233	00	RELAY SPST 6VDC NORM OPEN MRB 1A06
110000234	00	RELAY SPST 6VDC NORM CLOSED MRB 1B06
110000235	00	RELAY SGL POLE LTCHG 193REIA-2501A
110000236	00	SWITCH MICRO 156/1
110000237	01	RELAY 30SEC TIME-DLY CAP 120VAC
110000238	01	SWITCH SLIDE DPDT 8S-91-1/GF-126
110000239	01	SWITCH SLIDE DP3T 8S-93/G-128-S
110000240	00	SWITCH IND 91529-001
110000241	00	SWITCH 120-857
110000242	EE00	RELAY TEL 6V 1 FORM C MH80915
110000243	02	SWITCH MINI TOGGLE MNTN ON-NONE-ON
110000244	EE00	SEITH MINI TOGGLE MNTN ON-OFF-ON7103
110000245	00	SWITCH DIP SLIDE 7 POS 500-107
110000246	EE00	SWITCH MOM PUSH-BUTTON 10M79
110000247	EE00	RELAY REED 8P DUAL IN-LINE TSTEQ
110000248	00	RELAY DPDT 12V COIL A410-365630-00
110000249	01	RELAY 3PDT 10AMP 12VDC COIL
110000250	00	SWITCH 10POS ROT THMBWHL 213251
110000251	00	FILE PROTECT ASSY 120-859
110000252	EE00	SWITCH FOOT CONTROLFLEX #111 TSTEQ
110000253	EE00	SWITCH ENDPLATE THMBWHL MBW "M" TSTEQ
110000254	EE00	SWITCH THMBWHL MB731 TYPE M TSTEQ
110000255	01	SWITCH MINI-TOGGLE DPDT MOMENTARY
110000256	00	RELAY START 0694-01
110000257	00	SWITCH TOGGLE PC MNT 3POS 7211L3D9AH
110000258	00	SWITCH TOGGLE PC MNT SPDT 7108L3D9AH
110000259	00	RELAY DIP 1 FORM A 5V COIL W171DIP-1
110000260	00	REPLACED BY 110C00338
110000261	00	SWITCH E63-61HB
110000262	00	SWITCH SLOTTED ACTUATOR E21-66H
110000263	00	SWITCH MICRO SPNO 15A 250V V3-23-D84
110000264	00	SWITCH THERMOSTAT 78TD6D-7-1 TI
110000265	00	RELAY MAG LATCHING DPDT 12VDC
110000266	00	SWITCH TOGGLE SPDT UL11-M-D9-A-G
110000267	01	SWITCH LIGHTED 16A 250/DP 2600W11E
110000268	00	SWITCH SEL (PWR) N3
110000269	00	SWITCH SPDT RT ANGL HORZ PC MNT C&K
110000270	EE00	SWITCH RT ANGL MNTG 4PDT TOGGLE 7401A
110000271	EE00	SWITCH PUSH-BTN LIGHTED 125VAC TSTEQ
110000272	00	SWITCH MSS-104DG-RA SPDT PCB SLIDE
110000273	00	SWITCH PCB PUSH-BUTTON 39-201 SPDT
110000274	01	SWITCH SEL CTS 8POS
110000275	02	SWITCH CTL 4Y-3094
110000276	02	SWITCH MAG SENSOR VR250-1000PP
110000277	00	(USE 110-109) 800305-002
110000278	EE00	SWITCH SEL 2 POS T-BIRD
110000279	00	SWITCH PUSH BUTTON 20 POS 1KS212
110000280	00	SW C&K 7101-S-D9-C-B-E-BLK OXD BUSH
110000281	00	SW C&K 7103-S-D9-C-B-E-BLK OXD BUSH
110000282	00	SW C&K 7105-S-D9-C-B-E-BLK OXD BUSH
110000283	00	SW C&K 7201-S-D9-C-B-E-BLK OXD BUSH
110000284	00	SW C&K 7215-S-D9-C-B-E-BLK OXD BUSH
110000285	00	SWITCH ROTARY 12 POS 01-080-00-17-3
110000286	00	SWITCH ROTARY 10 POS
110000287	00	SWITCH OPT, POST READ 20140201
110000288	00	SWITCH OPT, PICK MARK SEN 20127602
110000289	00	SWITCH 1P START-STOP 00000946
110000290	00	RELAY DP CUF-42-70010 TIME DELAY
110000291	02	SWITCH ROT 4 POS CTS 227-34275-1
110000292	00	SWITCH PRESSURE PSF100A-6179I
110000293	EE00	SWITCH DIP SLIDE SER 206 TSTEQ
110000294	00	SWITCH USE 110-78 MS-249
110000295	00	SWITCH POWER (ILLUM) MS-279
110000296	00	SWITCH PUSHBUTTON C2006 MS-256
110000297	00	SWITCH LIMIT ASSY LEFT 233585-005
110000298	00	SWITCH LIMIT ASSY RT 233585-006
110000299	00	RELAY W171DIP-12
110000300	EE00	SWITCH IND WALDOM PUSH ON/OFF TSTEQ
110000301	EE00	RELAY MTR START 91252-7667
110000302	02	SWITCH DUAL OPTICAL AEW01-CR
110000303	00	RELAY 2PDT 24VDC KUP11D55
110000304	01	RELAY 4PDT 5A 12VDC
110000305	00	SWITCH CENTRLB PA2011 MS212
110000306	00	RELAY 10A CONT KUP11D556V
110000307	01	SWITCH 2 POS 60 DEG DETENT SP
110000308	01	SWITCH 6 POS 30 DEG DETENT SP
110000309	EE00	SWITCH 3 POS 8 POLE TSTEQ
110000310	EE00	SWITCH TOG SPDT RA MNT 7101L3A
110000311	EE00	RELAY MTR START 110V 4CR1-650
110000312	EE00	RELAY MTR START 220V 4CR1-623
110000313	EE00	SEE 113000147
110000314	00	SWITCH ROT 10POS 02-050-05-17-3071151
110000315	00	SWITCH ROCKER CARLING TA101-TWB
110000316	00	SWITCH 2 POSITION 76A02
110000317	01	RELAY SOLID STATE TL110
110000318	01	RELAY 110VAC KUP11A55
110000319	01	RESAY 240CAC KUP11A55
110000320	00	SWITCH ON-OFF 3730-18
110000321	00	SWITCH HI-LOW 3730-152
110000322	00	SWITCH FORMS RESET TOGGLE 800502-011
110000323	00	SWITCH 6/8 LPI TOGGLE 800502-010
110000324	EE00	RELAY 4PDT 3A 12 VDC COIL
110000325	00	RELAY 2-POLE 25A 110VAC A.M.
110000326	00	RELAY 2-POLE 25A 220VAC A.M.
110000327	EE00	RELAY MERC WET CONTACT,SPDT,5V
110000328	00	SWITCH PLENUM 2260 800129-007
110000329	00	SWITCH THUMBWHEEL 6040
110000330	00	SWITCH MOMENTARY PUSHBUTTON 6040
110000331	00	SWITCH SOL STATE 15AMPS 94376500
110000332	00	NUSE 110-339)
110000333	EE00	SWITCH PUSHBUTTON MNOVA
110000334	EE00	SWITCH 6-BIT DIP 6 TOGGLE SPST MNOVA
110000335	00	SWITCH SOLID STATE 30AMPS 94371302
110000336	EE00	RELAY FORM 1A 24 COIL HG WETTED
110000337	EE00	RELAY FORM 1C 24V COIL HG WETTED
110000338	01	SWITCH 10 POSN BIN CODED DECIMAL LCD
110000339	00	SWITCH PAPER OUT ASSY 237403-001
110000340	01	SWITCH 3 POSITION ROCKER DPDT
110000341	00	RELAY 15A 2PDT 24VDC 50M*BYTE
110000342	00	SWITCH PRESSURE 1" H20 50M*BYTE
110000343	00	RELAY CNTOR 3P 20A MIN @600V 24VAC CL
110000344	00	RELAY 4PDT 24V 94294106
110000345	00	SWITCH ONE LIGHT PUSHBUTTON ALT ACT
110000346	00	SWITCH ONE LIGHT PUSHBUTTON MOMENTARY
110000347	00	RELAY PWR SUPPLY 100030
110000348	01	SWITCH THERMOSTAT MANUAL RESET
110000349	EE00	SWITCH TOGGLE 3 POS DPDT
110000350	00	RELAY W/5V COIL FORM A HG-WETTED CONT
110000351	00	SWITCH ROTARY 10POSITION B.C.D.
110000352	02	SWITCH ROTARY 8POS SGL POLE 1/2"DIA
110000353	00	SWITCH 10AMP SPDT SNAP ACTION
110000354	01	SWITCH ROTARY S.P. 2 POSITION
110000355	00	RELAY 10AMP 120/240VAC 3PDT 12VDC CL
110000356	01	SWITCH REED CURRENT SENSING
110000357	01	SWITCH KEY LOW PROFILE 61-04001-002
110000358	00	SWITCH LP CNTRL PNL BASE 801403-001
110000359	00	SWITCH 3POLE SINGLE THROW 15A
110000361	00	RELAY SOLID STATE 25AMP (RMS) 6020SER
110000363	00	SWITCH TOGGLE ON-CENTER OFF MOM

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110000364 through 111000120

PART NO.	REV	DESCRIPTION
110000364	00	RELAY 12V COIL 15A 120/240VAC SPST-NO
110000365	00	SWITCH 8POSITION DIP
110000368	02	SWITCH ANTI-STATIC, LGC & PWR
110000369	00	THERMOSTAT NON HERMETIC AUTO RESET
110000370	00	RELAY PWR 30A DPST-NO 12VAC COIL
110000371	02	SWITCH PULL ON PUSH OFF W/100 OHM POT
110000372	00	SWITCH PWR 2POLE 15AMP @125VAC ON-OFF
110000373	00	SWITCH RIGHT ANGLE DIP APDS
110000375	00	RELAY 2PDT 20A PC MOUNT 12V COIL
110000376	00	RELAY SOCKET MIDTEX 670-0014
110000377	01	RELAY 2POLE 5V COIL
110000378	00	RELAY PC MOUNT DPST 20A 12V COIL
110000379	EE00	SWITCH TOGGLE DPDT (ON-ON-ON)
110000380	EE00	SWITCH ROTARY 2POLE 5POS PC CONTACTS
110000381	EE00	SWITCH TOGGLE SPDT (MOMENTAY)
110000382	EE00	SWITCH THUMBWHEEL BACK MOUNT 5POS
110000383	EE00	SWITCH TOGGLE SPDT (ON-NONE-ON)
110000384	EE00	RELAY DRY REED FORM 1A1B 12V COIL
110000385	EE00	SWITCH LOW PROFILE SEALED 4P SGL THRW
110000386	00	SWITCH MINI ROCKER DPDT 2P FAST TERM
110000387	00	SWITCH THERMAL CUTOFF NON-RESET 100 C
110000389	00	RELAY INDUCTION SPDT BSC FR-102 TSTEQ
110000390	00	RELAY INDUCTION 230V VERSION TSTEQ
110000391	00	RELAY AC FULL VOLT 25A 2POLE TSTEQ
110000392	00	RELAY AC FULL VOLT 30A 2POLE TSTEQ
110000393	00	RELAY AC FULL VOLT 30A 3POLE TSTEQ
110000394	00	RELAY DIP REED W107 DIP-5 TSTEQ
110000396	EE00	SWITCH MINI ROCKER SPDT
110000397	00	RELAY REED FORM C DIP
110000398	00	SWITCH DUAL VHF 59307A TSTEQ
110000399	00	RELAY 4PDT PC MT 12VDC COIL 3A CONT
110000400	00	SWITCH AIR FLOW
110000401	00	RELAY 24V COIL 2FORM C/10A CONTACTS
110000402	00	SWITCH 3PDT SLIDE 4A@125V 1.5A@250VAC
110000403	00	SWITCH BAND SPEED 800744-001
110000404	00	SWITCH SINGLE CYCLE 800931-004
110000405	00	SWITCH BAND GATE INTERLK 800129-006
110000406	00	SWITCH TACH/PF ADJ 800129-002
110000407	00	SWITCH PAPER OUT 2550 800129-008
110000408	00	SWITCH PLENUM INTERLOCK 235296-001
110000409	00	SWITCH RIBBON POS SENSOR 800129-004
110000411	00	SWITCH SPST 12AMP 250VAC 16AMP @125V
110000412	00	RELAY 8300 800795-001
110000413	00	SWITCH ON/OFF AC 8300 800931-005
110000414	EE00	SWITCH, THERMOSTATIC 1-POLE
110000415	EE00	SWITCH THERMOSTATIC 2-POLE
110000416	00	SWITCH REED 15AMP TURNS
110000419	00	SWITCH DIP 5 POS
110000423	EE00	SWITCH ROTORY 10POS
110000424	EE00	SWITCH TOGGEL
110000425	EE00	SWITCH TOGGEL
110000426	EE00	SWITCH TOGGLE
110000427	EE00	SWITCH TOGGLE
110000428	EE00	SWITCH TOGGLE
110000429	EE00	SWITCH TOGGLE
110000430	00	SWITCH MOM SPDT 42502-10
110000431	00	SWITCH DPDT TOGGLE 10811
110000432	00	SWITCH PUSH BUTTON 10895-01
110000433	00	SWITCH SPDT ROCKER 42501-10
110000434	00	SWITCH SPDT TOGGLE 10809
110000435	00	SWITCH ROTARY 12POS 42510-01
110000436	00	SWITCH ON/OFF 42644-03
110000437	00	SWITCH CVR OPEN 10961
110000438	00	SWITCH PRINT INTENSITY 24464
110000439	00	SWITCH RIBBON OUT SENSOR 13018-02
110000440	00	SWITCH PAPER OUT24436-05
110000441	00	RELAY 800795-301
110000443	EE00	SWITCH SUBMINIATURE GOLD CONTACTS
110000444	00	RELAY DPDT
110000445	EE00	RELAY REED 3FORM C 5V W/EM/FS SHIELD
110000446	00	RELAY DPST DIP 12V COIL ELECT SHIELD
110000447	EE00	SWITCH INTRA 40COND FLAT RBN CABLE
110000450	EE00	SWITCH 4PDT TOGGLE
111000000	00	DEVICE CONN CARD READER
111000001	00	CONN 9 CONTACT PLUG DEC 9P WITH PINS
111000002	01	CONN 9 CONT SKT DEC 9S SZ 20 WITH PNS
111000003	00	CONN 25P ITT DBC25FO (DBC25P)
111000004	00	CONN 25 CONT SKT DBC 25S SZ 20 W/PNS
111000005	00	CONN 50 CONT PLUG DDC 50P SZ 20 W/PNS
111000006	00	CONN 50 CONT SKT DDC 50S SZ 20 W/PNS
111000007	00	CONN 19 CONT PLUG 20E19P WITH PINS
111000008	00	CONN 19 CONT SKT 20E19S WITH PINS
111000009	00	CONN 52 CONT PLUG 20B52P WITH PINS
111000010	00	CONN 52 CONT SKT 20B5ES WITH PINS
111000011	00	CONN 100 CONT PLUG 20D100P WITH PINS
111000012	00	CONN 100 CONT SKT 20D100S WITH PINS
111000013	00	CONN 20-18 CONTACT PIN 030-1954
111000014	00	CONN 20-18 CONTACT SOCKET 030-1
111000015	00	CONN 20 CONTACT PIN 030-1952-00
111000016	00	CONN 20 CONTACT SOCKET 030-1953
111000017	00	CONN 22 CONTACT PIN 031-9540-00
111000018	00	CONN 22 CONTACT SOCKET 030-9542
111000019	00	CONN JUNCTION SHELL DF 24657
111000020	00	CONN JUNCTION SHELL DB24659
111000021	00	CONN JUNCTION SHELL DD24661
111000022	00	CONN SCREW LOCK ASSY FEMALE
111000023	00	CONN SCREW LOCK MALE D20419-16

PART NO.	REV	DESCRIPTION
111000024	00	CONN SCREW LOCK MALE 20419-21
111000025	00	CONN SCREW LOCK MALE 20420-15
111000026	00	CONN A/C OUTLET PS
111000027	00	CONN CABLE 20 DUAL POS AMP 86148-1
111000028	00	CONN PC HW-5000-111
111000029	00	CONN CONTACT COMP LD 4-330808-9
111000030	00	CONN DIP SOCKET 16 PIN 041-001 112N
111000031	00	REPLACED BY 111000209
111000032	00	CONN FASTON RECEPTACLE SERIES 250
111000033	00	TERM RCPT 250 22-18 AWG
111000034	00	TERM RCPT 250 16-14 AWG
111000035	00	TERM R TNG #10STUD 16-14 AMP 2-31903-2
111000036	00	TERM R TNG #10 STUD 22-16
111000037	00	TERM R TNG #6STUD 22-16 AMP 2-32403-1
111000038	00	TERM RCPT 187 22-18 AWG
111000039	00	TAB POLARIZING WINCHESTER 109-8340-1
111000040	00	CONN CABLE 22 DUAL POS AMP 86148-2
111000041	00	CONN RCPT 50 DUAL POSN AMP 86018-2
111000042	00	TERM TAB 250 .097STUD 90 AMP 41204
111000043	00	CONN 36 CONT FOR DISK
111000044	00	TERM TAB 250 .130STUD 90 AMP 42117-2
111000045	00	TERM TAB 250 .130STUD OFS AMP 42506-2
111000046	00	CONN T&B 18RA-6F
111000047	00	CONN WIRE SPLICE T&B 2RBR
111000048	00	TERM RCPT 187 20-16 FLG AMP42486-2
111000049	00	CONN TERM AMP
111000050	00	CONN HI-CLAMP PPC-11
111000051	00	CONN FASTENER CB4-2 1/8 DIA BUTTON
111000052	00	CONN 6 PIN AM
111000053	00	CONN DISK FROM 111-000-043 LG
111000054	00	CONN DISK FROM 111-000-043 SM
111000055	00	CONN T&B RBB-25
111000056	00	CONN SPLICE 18-12AWG T&B RCC-26
111000057	00	TERM TAB 250 130STUD 1PR AMP 41480
111000058	00	CONN CRP 24-20 AWG
111000059	00	CONN AMP 1-480435-0
111000060	00	CONN CONTACT MALE D-110238-2
111000061	00	CONN SOCKET FEMALE D110238-3
111000062	00	CONN SOLDER SLEEVE D142-51
111000063	00	REPLACED BY 111000753
111000064	00	OBSOLETE, REPLACED BY 111-753
111000065	00	CONN HAYCO T-101-S TIN PLATE TAB
111000066	00	CONN MAG TAPE 1800-22 MOLEX
111000067	00	CONN MAG TAPE MOLEX PINS 1799-T
111000068	00	CONN AMPHENOL 17-10500 MALE 50
111000069	00	CONN STYLE A 5353867
111000070	00	CONN STYLE B 5353868
111000071	00	CONN TERMINAL CONTACT 66341-2
111000072	00	CONN 6 CIRCUIT FASTON P/18 480003-5
111000073	01	CONN CONTACT PC 125CF 50
111000074	00	REPLACED BY 111000711
111000075	00	TERM POST 025SQ .210 AMP 86144-8
111000076	EE00	CONN TERMINAL BUSH GREEN DC-87-3-2
111000077	00	CONN TERMINAL BUSH ORG DC-87-3-2
111000078	00	CONN TERMINAL TAB BRASS T-202-55
111000079	00	CONN 26 POSITION 583679-1
111000080	00	CONN MOLEX 4 POS W/EARS
111000081	00	REPLACED WITH 111000267
111000082	00	CONN MOLEX 4 POS
111000083	00	REPLACED WITH 111000269
111000084	00	CONN AMPHENOL MIN RAC 17 17-300-01
111000085	00	CONN AMPHENOL RT ANGLE PIN 17-1208-02
111000086	00	CONN AMPHENOL RT ANGLE PIN 17-1209-02
111000087	00	CONN COMPONENT LEAD SOCKET 380635-1
111000088	00	CONN EPO GROUND TAB 5271288
111000089	00	CONN TAPE LU9 BA14-BM
111000090	00	CONN TAPE LU9 BA16-BM
111000091	00	CONN PWR RECEPT, MS3102 A24-25
111000092	01	CONN PLUG & CORD CLAMP 20A 2501
111000093	00	CONN BLOCK SKT 75 CONT AMP 201311-1
111000094	00	CONN BLOCK 29 POSN AMP 202477-4
111000095	00	CONN CONT SKT 18-16AWG AMP 66100-1
111000096	00	CONN CONT SKT 10-8AWG AMP 66257-2
111000097	00	CONN SKT RG/U CA AMP 329013
111000098	01	PIN LOCATING KEY 583532-1
111000099	00	CONN MINI BRASS RIVIT .116X3/16
111000100	00	CONN 24 PIN (PART # 111000040)
111000101	00	CONN 28 PIN DUAL POSN AMP 86148-5
111000102	00	CONN PLUG RECP P&S TURNLOCK
111000103	00	CONN ASSY DIGITRONICS PTR 2540
111000104	00	CONN CRIMP LUG T&B RC1157
111000105	00	CONN RETANGULAR MRAC 42SJ
111000106	00	CONN PIN CONTACT
111000107	00	CONN MOLEX STD NYLON P/N 126-P-1
111000108	00	CONN MOLEX STD NYLON P/N 1261-R
111000109	00	CONN MRAC 42PJ
111000110	00	CONN PIN CONTACT 8114
111000111	00	CONN TERM R TNG MS-#10 #12-#10 AWG
111000112	00	CONN PCB 28 DUAL POSITION
111000113	00	CONN CABLE 20 POSN AMP 86402-1
111000114	00	CONN 12 POSITION AMP 86402-4
111000115	00	CONN CONTACT TWIN LEAF AMP 583616
111000116	00	CONN KEY AMP
111000117	01	CONN PC EDGE 50 DUAL POS AMP1-583717-9
111000118	00	CONN CINCH 252-15-30-160
111000119	01	CONN PC EDGE 10 DUAL POS AMP 583717-1
111000120	00	CONN FERRULE COAX 328664

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111000121 through 111000417

PART NO.	REV	DESCRIPTION
111000121	00	CONN RETENTION SPRING COAX 243332-1
111000122	00	CONN ALIGN BSHG RED AMP 329051
111000123	00	CONN SPR RTNG AMP 583691-3
111000124	00	CONN RECEPTACLE
111000125	00	CONN PIN FEMALE MOLEX 02091133
111000126	00	CONN PLUG MALE MOLEX
111000127	00	REPLACED WITH 111000268
111000128	00	CONN RIVET FLAT HD AK41H
111000129	01	CONN RECEPTACLE MOLEX
111000130	00	CONN PLUG MOLEX 1261P-1
111000131	00	CONN PIN MOLEX 02092132
111000132	00	CONN RF PNL RECEPTOR 83-798-1050
111000133	00	CONN JACKSCREW FEMALE 200875
111000134	00	CONN 9 PIN W/MOUNTING TABS
111000135	00	REPLACED WITH 111000270
111000136	01	CONN PLUG 2 PIN
111000137	01	CONN RECEPTACLE 2 PIN
111000138	00	CONN 22 PIN 583533-9
111000139	00	TERM SLTD TNG FLG #6 16-14A
111000140	00	TERM R TNG #6STUD 16-14 AMP 2-32442-1
111000141	00	TERM R TNG #8 STUD 22-16
111000142	00	CONN MALE A/C PLUG 15AMP 125V
111000143	00	CONN DAISY CHAIN .025 SQ POST 5"SP
111000144	00	TERM R TNG #2STUD 22-16 AMP 2-320440-1
111000145	00	CONN FEMALE/D110238-35
111000146	00	CONN MALE/D110238-34
111000147	00	CONN 13 POS SINGLE ROW MOD IV
111000148	00	REPLACED WITH 111000692
111000149	00	CONN HOUSING,TWIN LEAF,100CTRS
111000150	00	CONN 10 POS DUAL CONTACT
111000151	00	CONN 18 POS DUAL CONTACT
111000152	00	CONN AMP 57-30360
111000153	00	CONN FLAG FASTON TERM
111000154	00	CONN OUTPUT ELCO 00-8016-038-000-707
111000155	00	CONN BERG #75307-002
111000156	00	CONN JACK SCREW AMP #202490-2
111000157	00	CONN FLANGED INLET AH 5278 NEMA 5-15P
111000158	00	CONN WIRE MOLD ASSY 10P AMCO PM60-10
111000159	00	CONN RUBBER BOOTH AH 7511
111000160	00	CONN 30PIN W/FRAME,VIKING#3VH30/1JN3
111000161	EE00	CONN WIRE MOLD ASSY 6 POS
111000162	00	CONN PIN CONTACT 14 AWG AMP 61118-5
111000163	00	CONN PIN CONTACT 26 AWG AMP 60910-5
111000164	00	CONN SOCKET AC ARROW HART #5278
111000165	00	CONN SOCKET AMP 61117-5
111000166	00	CONN CONT SKT 30-22 AWG AMP 60909-
111000167	00	CONN 6 SKT MATE-N-LOK AMP 1-480273-0
111000168	00	CONN 12 SKT MATE-N-LOK AMP 1-480275-0
111000169	00	CONN 12 PIN MATE-N-LOK AMP 1-480275-0
111000170	01	CONN PLUG MOLEX 12CKT 1360P
111000171	01	CONN RCPT MOLEX 12CKT 1360R-1
111000172	00	CONN VIKING 3VH30/1JN3
111000173	00	CONN AMP 57-30360
111000174	00	CONN MOLEX 5 PIN WAFERCON
111000175	00	CONN MOLEX 5 PIN
111000176	00	CONN BASELESS CRTG LAMP AMP 61528-1
111000177	00	TERM TAB 250 .130STD 2PR AMP 41481
111000178	00	CONN USM POP RIVET .125 DIA
111000179	01	CONN PC EDGE 25 DUAL POS AMP1-583717-1
111000180	00	CONN WIRE MOLD ASSY
111000182	00	CONN WIRE MOLD ASSY MODIFIED
111000183	00	CONN TEST PROBE FEM #53061
111000184	00	CONN TEST PROBE MALE #20357
111000185	00	CONN 50 DUAL POS
111000186	00	CONN AMP FSTON 187 SERIES TAB 61947-1
111000187	00	CONN AMP FSTON 187 SERIES TAB 61951-1
111000188	00	CONN AMP FSTON"187" RECP AMP 61697-1
111000189	00	CONN HOUSING MALE 9 PIN
111000190	00	CONN HOUSING FEMALE 9 PIN
111000191	00	OBS REPLACED BY 111000993
111000192	00	CONN BARRIER STRIP 6 TERMINAL
111000193	00	CONN SPADE LUG #10-12
111000194	00	CONN WAFER 9 PIN MOLEX 0918-5094
111000195	00	CONN AMP FSTON 110 TAB 42971-1
111000196	00	CONN AMP FSTON 187 TAB 61761-1
111000197	00	CONN 40 PIN W/STRAIN RELIFF #3417-3000
111000198	01	CONN 40 PIN PCB HEADER #3432-1002
111000199	00	CONN POLARIZING KEY
111000200	00	CONN VIKING 3VH35/1CND-12
111000201	00	TERM R TNG #4STUD 22-16 AMP 51878
111000202	00	TERM R TNG #10 STUD 6AWG R40018FT1
111000203	00	TERM RCPT 250 14-10AWG AMP 41450
111000204	00	CONN HSG 250 TERM RCPT AMP 1-480416-0
111000205	00	TERM RCPT 187 22-18AWG MAP 60972-2
111000206	00	TERM RCPT 110 22-18AWG AMP 61048-2
111000207	00	TERM TAB 187 130STUD ANLR AMP 61761-2
111000208	00	TERM TAB 110 136STUD STR AMP 60858-1
111000209	00	TERM POST 025SQ .165 AMP 87022-9
111000210	00	SPLICE COAX TO AWG AMP#330592
111000211	00	RIVET OBSOLETE SEE 123000568
111000212	00	CONN PNL RCPT TYPE UHF AMPHENOL 83-1R
111000213	00	TERM RCPT 28-22 AWG BERG 47712
111000214	00	CONN HSG 4 PIN BERG 65039-033
111000215	03	OBSOLETED REPLACED BY 111-780
111000216	00	TERM R TNG #8 STUD 16-14 AMP
111000217	00	CONN DUPLICATE SEE 111000129
111000218	01	CONN PLUG MOLEX # 1261-P

PART NO.	REV	DESCRIPTION
111000219	00	CONN 9 PIN MOLEX #1840-9-2
111000220	00	CONN 12 PIN MOLEX #1840-12-2
111000221	00	CONN QUICK DISC TAB ETC#3531
111000222	00	CONN QUICK DISC TAB ETC#3523
111000223	00	CONN 25 PIN DUAL POSN #PJDM-25S
111000224	00	CONN POLARIZING KEY #109-8597
111000225	00	TERM R TNG #10STUD GAWG BUR YAEUSC-L1
111000226	00	TERM RCPT 250 12-10 AWG
111000227	00	CONN 29 PIN WINCHESTER#SRE29PD4J
111000228	00	CONN MR 4PIN HDR(TIN) AMP#9-350255-1
111000229	00	CONN MR 4SKT HSG AMP#1-350240-9
111000230	00	CONN MR 6PIN HDR(TIN) AMP#9-350258-1
111000231	00	CONN MR 6SKT HSG
111000232	00	CONN MR 9PIN HDR(GOLD) AMP#9-350261-2
111000233	00	CONN MR 9SKT HSG AMP#1-350242-9
111000234	00	CONN MR 12PIN HDR(TIN) AMP#9-350264-1
111000235	00	CONN MR 12 SKT HSG
111000236	01	CONN MR SKT CON 26-18 TIN AMP350665-1
111000237	01	CONN MR SKT CON 26-18 GLD AMP350665-2
111000238	00	CONN HOUSING AMP 1-480305-0
111000239	00	CONN PIN AMP 61118-1
111000240	00	REPLACED WITH 111000269
111000241	00	CON PIN FEMALE 20-14 MOLEX#20-09-1101
111000242	00	CONN 60 PIN AMP 582459-1
111000243	00	REPLACED WITH 111000268
111000244	00	REPLACED WITH 111000270
111000245	00	CONN PLUG FOR .093 TERM MOLEX TYPE1619
111000246	00	CONN RCPT FOR .093 TERM
111000247	00	CONTACT,CONN, AMP#66135-2
111000248	00	SHIELD,CONN, AMP#200532-1
111000249	00	JACKSCREW AMP#582360-3
111000250	00	CONNECTOR,DUAL,36PIN600-061-18SL
111000251	00	CONNECTOR 582388-9 AMP
111000252	00	CONTRACT,CONN,66088-3 AMP
111000253	00	CONTRACT,CONN,66150-3 AMP
111000254	00	CONNECTOR WINCHESTER #MRAC50PJTDH8
111000255	00	CONN W/FRAME,CINCH#251-25-30-160
111000256	00	CONNECTOR 57-30240
111000257	00	CONN CARD CAGE-TERMINAL
111000258	00	CONN CARD CAGE 15 PIN
111000259	00	CONN MR 15PIN HDR(TIN) AMP#9-350267-1
111000260	00	CONN MR 15SKT HSG AMP#1-35024409
111000261	00	CONN PIN .025SQ,WW,,660LG #75401-015
111000262	00	CONN CANNON 19S SK-19-21C-1/2
111000263	00	CONN PC QUICK-CONNECT .187 TAB FEMALE
111000264	00	TERM R TNG #6STUD 18-22 AMP 2-34144-1
111000265	00	TERM R TNG #6STUD 10-12 AMP 2-34168-1
111000266	00	CONN RIVET
111000267	01	TERM FEMALE .093 DIA 14-20G
111000268	00	TERM MALE .093DIA 18-22GA MOLEX1380
111000269	01	TERM MALE .093 DIA 14-20G
111000270	00	TERM FEMALE.093DIA18-22GA MOLEX1381
111000271	00	CONN USM POP RIVET #AD44H
111000272	00	TERM POST .025SQ UMINSUL, AMP#87022-4
111000273	00	TERM AMP 250 FASTON ADT 61765-2
111000274	00	CONN KEY,POLARIZING FOR AMPMODU TYPE
111000275	00	CONN CONTRACT,LOCK CLIP=,025POST
111000276	00	CONN HOUSING,LOCK CLIP,2 ROW 6 POS
111000277	00	CONN HOUSING,LOCK CLIP,2 ROW 20 POS
111000278	00	CONN PLDG 20A 250V HUBBELL 2421
111000279	00	CONN AMP PINS (BRIGHTTIN DIP)
111000280	00	CONN RCPT 2-PIN MOLEX #03-09-1021
111000281	00	CONN SCREW LOCK PNL RECEPTICLE
111000282	00	CONN SCREW LOCK CA PLUG
111000283	00	CONN MATE-N-LOCK 8PIN HDR,#350212-1
111000284	00	CONN MATE-N-LOCK 8PIN,AMP #1-480283-0
111000285	00	CONN 20-14 TIN PIN AMP
111000286	00	CONN POST INSUL POD AMP #1-480306-1
111000287	00	CONN FLAG INSUL SPT AMP #60290-2
111000288	00	CONN WINCHESTER HW50D2-111-28
111000289	00	TERM MALE-MOLEX 1854-02-06-2132
111000290	00	TERM RECEP,2 CKT MOLEX 1625-2R1
111000291	00	CONN ADPTR 1/4" PUSHON TAB-112
111000292	EE00	CONN HOUSING,LOCK CLIP 12 POS
111000293	00	CONN 11 POS 22 PIN,EDGE CARD
111000294	00	CONN 4PIN MR HDR(GOLD) AMP-9-350255-2
111000295	00	CONN 15PIN MR HDR(GOLD) AMP-9-350267-2
111000296	00	REPLACED BY 111000713
111000297	00	CONN M-N-L 8 PIN HDR GLD AMP#350212-2
111000298	00	CONN HSG 50 DUAL POS,AMP #1-583717-7
111000299	00	CONN 50 POS, 4 SURF DISK 3426-0000 3M
111000300	00	CONN 25 POS, 4 SURF DISK 3415-0000 3M
111000301	00	CONN 34 POS, 4 SURF DISK 3M P/N 3402
111000302	00	CONN 34 POS, 4 SURF DISK 3M 3424
111000303	00	TERM .250 INLINE FEM N2/4-2/10
111000304	00	TERM INSUL=CONNECT 18-20 GA WIRE
111000305	00	CONN AMP FASTON 45 250SER SGL42822-2
111000306	00	CONN AMP FASTON 45 250SER DRL 41477
111000409	EE00	CONN PLUG, MALE PS25GR TSTEQ
111000410	EE00	CONN PLUG, MALE PS100GR TSTEQ
111000411	EE00	CONN PLUG, FEMALE RP25GY TSTEQ
111000412	EE00	CONN PLUG, FEMALE DF21RC TSTEQ
111000413	EE00	CONN PLUG, FEMALE DF21WTC TSTEQ
111000414	EE00	CONN PLUG, FEMALE DF21BC TSTEQ
111000415	EE00	CONN PLUG, FEMALE RP100GB TSTEQ
111000416	00	CONN PLUG, FEMALE RP25GBL TSTEQ
111000417	EE00	CONN PLUG, FEMALE RP25GWT TSTEQ

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111000418 through 111000408

PART NO.	REV	DESCRIPTION
111000418	EE00	CONN PLUG, FEMALE RP25GGN TSTEQ
111000419	EE00	CONN PLUG, FEMALE RP25GR TSTEQ
111000420	EE00	CONN PLUG, FEMALE RP100GR TSTEQ
111000421	EE00	CONN PLUG, MALE PS25GBL TSTEQ
111000422	00	TERM R TNG 1/4STD 22-16 AMP 31251
111000423	EE00	CONN PLUG M TWIST LOCK 20A 125V 60HZ
111000424	EE00	CONN RCPT F 4X 220V 50HZ TSTEQ
111000425	EE00	CONN RCPT F 4X 110V 60HZ TSTEQ
111000426	00	CONN 2P POS AMP 9-350359-2
111000427	EE00	CONN 50POS WINCHESTER HW25C2-111
111000428	00	CONN N/R 12PIN HDR 3/32 GOLD 93502662
111000429	01	CONN CKT CD HDR 34 CONT STR 3431-2003
111000430	00	REPLACED BY 111000770
111000431	00	CONN COMP LEAD SKT 1-380737-0
111000432	01	CONN DIABLO M44 I/O CONN
111000433	EE00	CONN 3VH22/1JN3 TSTEQ
111000434	EE00	CONN IC TST SKT TSTEQ
111000435	00	TERM INSUL 4099-1 05-19 TEFLON
111000436	00	CONN PLUG 15A 250V PVC 5666
111000437	00	CONN SOCKET CONTRACT WIN MRAC 50SJTDH
111000438	01	CONN PIN GOLD FEMALE 1189-0Z-5106 MLX
111000439	00	CONN GOLD PIN-MALE (PC TATL)MOLEX
111000440	00	TERM SPADE LUG .196 (#10ADW) 626
111000441	00	TERM SPADE LUG .257 (1/4") 571
111000442	00	CONN RECEPT ELECT 250V 15A DPLX 5662
111000443	00	CONN RECEP MOLEX 9 PIN 0309-1093
111000444	00	CONN RECPT, 9 PIN MOLEX 03-09-1094
111000445	01	CONN RCPT AC AMP1-480700-0 CDA3435302
111000446	00	CONN PINS AC AMP 350550-1 CD 83435510
111000447	EE00	CONN 14 PIN DIABLO 10524-11 TSTEQ
111000448	EE00	CONN PIN-MALE DIABLO 10525-10 TSTEQ
111000449	02	CONN ELCO 20 DUAL POS CARD EDGE CONN
111000450	00	CONN PLUG STR BL 50A 125/250V 9451
111000451	00	TERM SOCKET #66108-3
111000452	EE00	CONN 100X200 GRID SPACING 50 DUAL
111000453	00	CONN DUAL 12 PIN 280-033-03
111000454	01	CONN 6 PIN MADE FROM DGC 111000113
111000455	00	CONN 12 PIN BURNDY MD12MXP-17TC
111000456	00	CONN BURNDY HOOD M2H 50PC 1P2
111000457	00	CONN MALE PIN GOLD MLX 1380T02096124
111000458	00	CONN FMALE GOLD PIN MLX 1381T02095124
111000459	EE00	CONN PLUG 230V 50HZ FEMALE TSTEQ
111000460	EE00	CONN DUAL 28 POS AMP 1-86792-3
111000461	00	CONN PIN CRIMP ELCO 60-801703-13
111000462	EE00	CONN DUAL 15 POS AMP 86792-5
111000463	EE00	CONN CONTACT AMP 86935-2
111000464	EE00	CONN SPRING, RET AMP 5836-91-2
111000465	EE00	CONN DUAL 25 POS AMP 2-86743-3
111000466	EE00	CONN RCPT W/O PINS 38POS
111000467	00	CONN CONTACT WINCHESTER 100710265
111000468	00	CONN WINCHESTER PGB510
111000469	00	TERM STRP FDTHRU SCR 9POS 13009
111000470	00	TERM STRP FDTHRU SCR 2PIS 13002
111000471	00	TERM STRP DIR SLDR FDTHRU 3POS 13503
111000472	00	TERM STRIP DIR SLDR FDTHRU 2POS 13502
111000473	00	TERM STRP DIR SLDR FDTHRU 9POS 13509
111000474	00	TERM STRIP 14POS DIR SLDR FDTHRU13514
111000475	00	CONN PC DBL ROW 28CONT HW2802-111
111000476	EE00	CONN ARMORED CLAMP RCPT 15A 250V 5037
111000477	00	TERM PRE-INSUL 34855
111000478	00	CONN SOCKET, RELAY 27E046
111000479	00	TERM RCPT 250V 9A 03091064
111000480	00	TERM RCPT 250V 9A 03091049
111000481	EE00	RCPT AC 15A 5251 TSTEQ
111000482	00	TERM GND CLIP BLADE 8182-84-01
111000483	EE00	CONN AMP FASTON 250 SER RCPT W/TABV
111000484	00	CONN PCB PIN HEADER 20CKTS 1/16-GOLD
111000485	EE00	CONN 5 PIN PLUG 67-06-C14-5P TSTEQ
111000486	EE00	CONN RCPT 5 PIN PNL67-02-F14-5P TSTEQ
111000487	EE00	CONN EDGE .125" CENT31H22/.1CND5 TSTEQ
111000488	EE00	CONN EDGE .100" CENT3VH22/1JND5 TSTEQ
111000489	00	CONN SGL MOD AMP 87175-2
111000490	00	CONN CONTACT FEMALE AMP 66100-3
111000491	EE00	CONN COAX CONTACT FEMALE AMP 51565-1
111000492	00	CONN CONTACT FEMALE AMP 66104-3
111000493	00	CONN CONTACT MALE AMP 66106-3
111000494	EE00	CONN FERRULE AMP 1-332056-0
111000495	00	CONN RCPT 50 POS AMP 201358-1
111000496	EE00	CONN JACKSCREW FEMALE AMP 200867-2
111000497	00	CONN RCPT AMP 201311-1
111000498	00	CONN JACKSCREW FEMALE TIP #201910-2
111000499	00	CONN JACKSCREW MALE TIP AMP #202871-2
111000500	00	CONN SHIELD 50 POS AMP 202670-1
111000501	00	CONN SHIELD 75 POS AMP #202713-1
111000502	00	CONN CD & DGE 20 CONT 3461-0001
111000503	00	CONN IRNSN 20 CONT 3422-0000
111000504	EE00	DUPLICATE SEE 111000523
111000505	00	TERM STRIP 7POS 800 KT121 & KT126
111000506	EE00	TERM STRIP 7POS KULKA 602-7
111000507	00	CONN 35 DAUL POSITION WINCHEST PGB35D
111000508	00	CONN PIN 20 TO 24 AWG WIN 100711205
111000509	00	CONN PANAPLEX DSPL SRE 3501
111000510	EE00	CONN PANAPLEX DSPL SRB 1741
111000307	00	CONN CONT TWINLEAF AMP 583853-5
111000308	00	CONN 22PIN W/FRAME,VIKING#3VH22/1JN3
111000309	00	CONN FASTON 14-20AWG NON-INSUL42452-2
111000310	00	CONN 18 CONT SINGLE ROW 00000032
111000311	00	CONN 18 CONT DUAL POS 00000033

PART NO.	REV	DESCRIPTION
111000312	00	CONN 18 CONT DUAL POS HSG 00000029
111000313	00	CONN OUTPUT J2 00000028
111000314	00	CONN CONT MALE PIN 22-26AWG
111000315	00	CONN CONT FEM SKT PIN 22-26AWG
111000316	00	CONN 250 FASTON 10-20 AWG TERM
111000317	00	CONN 75 POS M SER 100 MBYTE
111000318	00	CONN W/FRM CINCH 251-22-30-160
111000319	00	CONN PLUG 30A 250V HUBBELL 45215
111000320	00	CONN 50 POS M SERIES 100 MBYTE
111000321	00	CONN CONTACT 15 AMP 1332
111000322	00	CONN PWR POLE MDL 15AMP 600V 1315
111000323	00	CONN MOLEX RCPTCLE W/O EARS
111000324	00	CONN WAFERCON 3 PINS MOLEX 09-18-5031
111000325	00	CONN TWIST LOCK 30A 125/250V 2713
111000326	00	CONN TWST-LCK 30A 125/250V 2715
111000327	00	CONN ASSY DIGITRONICS BC7611-2 22PINS
111000328	00	CONN DEAD FRONT CAP 15A 250V N2 5666C
111000329	00	CONN 29 PIN SOCKET SRE-29S-JT
111000330	00	TERM PRE-INSUL #6 WIRE AMP 52042-3
111000331	00	CONN 9 CONT PLUG DEC9PW/O PINS
111000332	00	CONN 9 CONT SKT DEC9S W/O PINS
111000333	00	CONN 25 CONT PLUG DRC25P W/O PINS
111000334	00	CONN 25 CONT SKT
111000335	00	CONN 50 CONT PLUG DDC50P W/O PINS
111000336	00	CONN 50 CONT SKT DDC50S W/O PINS
111000337	00	CONN 19 CONT PLUG 2DE19P W/O PINS
111000338	00	CONN 19 CONT SKT 2DE19S W/O PINS
111000339	00	CONN 52 CONT PLUG 2DB52P W/O PINS
111000340	00	CONN 52 CONT SKT 2DB52S W/O PINS
111000341	00	CONN 100 CONT PLUG 2DD100P W/O PINS
111000342	00	CONN 100 CONT SKT 2DD100S W/O PINS
111000343	00	CONN CONT TW LF 20-24AWG AMP 583853-2
111000344	00	CONN TWIST LOCK HUBBELL 2313
111000345	00	CONN TWIST LOCK CAP HUBBELL 2311
111000346	00	CONN TWIST LOCK INLET HUBBELL 2315
111000347	00	CONN 1 POLE MTG PLATE ITE FP9508 ELBDO
111000348	00	CONN 2 POLE MTG PLATEITE FP9555 ELBD O
111000349	00	CONN 3 POLE MTG PLATE ITE FP9556 ELBDO
111000350	00	CONN SEAL-TITE CVR HUBBELL 6031 ELBD
111000351	00	CONN SEAL-TITE CVR HUBBELL 6032 ELBD
111000352	00	CONN SEAL-TITE CVR HUBBELL 6035
111000353	00	CONN SEAL-TITE CVR HUBBELL 6021 ELBD
111000354	00	CONN CAP TWIST LOCK 30A 125/250V 2711
111000355	00	CONN RCPT DUPLEX 20A 125V 5392 ELBD
111000356	00	CONN RCPT SGL 20A 125V 5361 ELBD
111000357	00	CONN PLZ SKT 203964-2
111000358	00	CONN PLZ PIN 200833-4
111000359	00	CONN JACKSCREW FIXED FEM 200875-1
111000360	00	CONN PLZ SKT 201047-4
111000361	00	CONN PLZ PIN 201046-4
111000362	00	CONN JACKSCREW FIXED MALE 200874-2
111000363	00	CONN SKT PIN PCB 85861-4 AMP ELBD
111000364	00	CONN INLET 3 WIRE 30A 250V 2625
111000365	00	CONN 3 WIRE 30A 250V 2623
111000366	00	CONN PLUG 3 WIRE 30A 250V 2621
111000367	00	CONN FASTON 45DEG MALE 42822-2
111000368	00	CONN 50P EDGE 3415-0001
111000369	00	CONN 34 PIN W/W POST 3424
111000370	00	CONN R/W HD 5P FEMALE 15427
111000371	00	CONN 22/44PIN CD EDGE .125" CTRS
111000372	00	TERM PRE-INSUL #8AWG R3031BFT1
111000373	00	TERM BARRIER STRIP 2 PIN 99999-026
111000374	00	TERM BARRIER STRIP 6 PIN 99999-027
111000375	00	CONNECTOR 22 PIN CUSTOM 01021-006
111000376	00	CONN PLUG 52-66-C CAB ASSY
111000377	00	CONN 14P DIP SKT FINISH TIN 583527-1
111000378	00	TERM BLOCK END SECTION 230V
111000379	00	TERM BLOCK SECTION HD PHNLC 212
111000380	00	CONN 50/100 PIN CARD EDGE CPH70000
111000381	00	CONN BUS BAR 6 1/2" 98438 1100SERIES
111000382	00	CONN HSG LOCK CLIP 2ROW 8POS
111000383	00	CONN RECEPT BRN PHEN DPLX 15A 125V
111000384	00	PLUG 50A 3P 3WIRE 3761
111000385	00	PLUG 50A 3P 4 WIRE 3765
111000386	00	CONN FLANGED INLET 50A 3P4WIRE 3775
111000387	00	CONN BODY 50A 3P 4 WIRE 3764
111000388	00	CONN INLET 50A 3P 3WIRE 3776
111000389	00	CONN BODY 50A 3P 3WIRE 3760
111000390	00	CONN PWR POLE MDL 15AMP 600V 1327
111000391	00	TERM RCPT 28-32AWG BERG 47711
111000392	EE00	TERM JUMPER PINS 8136-650
111000393	00	CONN PLUG CORR-RESIST 30A 125V 26CM11
111000394	00	CONN BODY CORR-RESIST 30A 125V 26CM13
111000395	00	CONN SEAL TITE CVR 60CM31
111000396	00	CONN SEAL TITE CVR W/RING 60CM33
111000397	00	CONN PWR INLET 30A 125V60CM61
111000398	00	TERM 4 SIRIP THRU CHAS 4-140Y TSTEQ
111000399	EE00	CONN PLUG, FEMALE DF21YC TSTEQ
111000400	EE00	CONN PLUG, FRMALE PF21GNC TSTEQ
111000401	EE00	TERMINAL 269RR TSTEQ
111000402	EE00	TERMINAL 269BB TSTEQ
111000403	EE00	TERMINAL 1519 TSTEQ
111000404	EE00	TERMINAL 257 TSTEQ
111000405	EE00	CONN PLUG, F 15A 50HZ 377-R1 TSTEQ
111000406	EE00	CONN PLUG, MALE PS100GB TSTEQ
111000407	EE00	CONN PLUG, MALE PS25GWT TSTEQ
111000408	EE00	CONN PLUG, MALE PS25GGN TSTEQ

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111000511 through 111000707

PART NO.	REV	DESCRIPTION
111000511	EE00	CONN PANAPLEX DSPL SRB 1941
111000512	EE00	CONN TWIN LEAF PC EDGE 10POS 583718-1
111000513	00	CONN MR3 SKT HSG AMP 1-350355-9
111000514	00	CONN MR2 SKT HSG AMP 1-350354-9
111000515	EE00	CONN SOC HSG 6P AMP 1-480690-0
111000516	00	CONN PIN MTG HSG 6P AMP 1-480693-0
111000517	00	CONN MR3PIN HDR AMP 9-350362-1
111000518	00	CONN SKT HSG 6P AMP 1-480270-0
111000519	00	CONN PCB PIN HDR 6P AMP 1-380999-0
111000520	00	CONN SKT HSG 12P AMP 1-480287-0
111000521	00	CONN PCB PIN HDR 12P AMP 350213-1
111000522	00	OBS DUPLICATE SEE 111000718
111000523	00	CONN 30P .200X.100 GRID 2HWP30111948
111000524	00	CONN RCPT 4 CONT 56-0482000
111000525	00	CONN RMVBL CONT PIN 156-1/18P
111000526	00	CONN 15P .250X.125 GRID 3VH15/1CND
111000527	00	CONN PLUG 4 CONT 56-04P1000
111000528	00	CONN RMVBL CONT SKT 156-1018S
111000529	00	CONN MR 2P HDR AMP 9-350359-1
111000530	EE00	TERM WING #6 STUD 33464
111000531	00	CONN LCKG KEY, CRIMP-TWIN LEAF 530213
111000532	EE00	DUPLICATE SEE 111000529
111000533	EE00	CONN MGB50D 100P TSTEQ
111000534	EE00	CONN 50P 57-60500 TSTEQ
111000535	EE00	NOT USED
111000536	01	CONN VERT MOUNT PCB AMP 552116
111000537	EE00	CONN PIN 100-710205 15 TSTEQ
111000538	00	CONN POLAR KEY-3M CD EDGE 3439
111000539	00	CONN 25DUAL EDGE BRD 1-583891-1
111000540	00	CONN PC EDGE BRD 22DUAL W/O EARS
111000541	EE00	CONN PC EDGE BRD 15DUAL W/O EARS
111000542	00	CONN PC EDGE BRD 25DUAL W/O EARS
111000543	00	CONN EDGE BRD 6DUAL W/O EARS
111000544	EE00	CONN 3P 4W 120/250 20A TWIST-LK CAP
111000545	00	CONTACT MALE PLUG 75724586
111000546	00	CONN PLUG 75724543
111000547	01	OBS REPLACED BY 111000630
111000548	00	CONN V-BLADE GRD OUTLET 15A 250V 5581
111000549	00	CONN PLUG 4 CKT W/O MTG EARS MOLEX
111000550	00	CONN SKT BODY 34P
111000551	00	CONN MR 20P HSG AMP #1-350245-9
111000552	00	CONN WIRE, SET SCR TYPE 10-305
111000553	EE00	CONN PNL MOUNT RCPT 206036-2 UL APP
111000554	EE00	CONN PNL MOUNT RCPT, SKT CON 206425-1
111000555	EE00	CONN PLUG, SHELL, SKT CONT 206037-2
111000556	EE00	CONN PLUG, SHELL 206426-1 UL APPROVED
111000557	EE00	CONN FEMALE TYPE AC PINS 66257-1
111000558	EE00	CONN MALE TYPE AC PINS 66259-1
111000559	00	CONN PIN GOLD FEMALE 1381T-02-5123MLX
111000560	00	CONN PLUG 6 CKT 093 DIA TERM W/O EARS
111000561	00	TERM .093 PC TAIL MALE MLX 02-09-2133
111000562	00	CONN PCB MOLEX 09-50-3021
111000563	00	CONN PCB MOLEX 09-50-3031
111000564	00	CONN PCB MOLEX 09-50-3041
111000565	00	CONN PCB MOLEX 09-50-3061
111000566	00	CONN PCB MOLEX 09-50-3081
111000567	00	CONN CONT,RMVLB SKT .062 02-06-1101
111000568	00	CONN CONT,RMVLB PIN .062 02-06-2101
111000569	00	CONN SW-MIN 2191-3 MOLEX
111000570	00	CONN MR 20P HDR AMP 9-350270-1
111000571	00	CONN 2P HSG AMP 1-480318-0 MATE-N-LOK
111000572	00	CONN 2P HDR AMP 350209-1 MATE-N-LOK
111000573	02	CONN WAFER MOLEX 09-65-1021
111000574	00	CONN WAFER MOLEX 09-65-1031
111000575	00	CONN WAFER MOLEX 09-65-1041
111000576	00	CONN WAFER MOLEX 09-65-1061
111000577	00	CONN WAFER MOLEX 09-65-1081
111000578	00	TERM 2478 18-24AWG MOLEX 08-50-0105
111000579	00	CONN RCPT 4POS .62 MOLEX 03-06-1042
111000580	00	CONN SKT HSG 6 CKT MR AMP #1-480613-9
111000581	00	CONN HSG 6 CKT PIN AMP #1-480612-9
111000582	00	CONN PC EDGE 30 DUAL POS NO EARS
111000583	00	TERM SPR SPADE 16-22GA AMP #6
111000584	00	TERM #6 SPR SPADE 14-16GA AMP 52420-2
111000585	00	TERM #6 SPR SPADE 10-12GA AMP
111000586	00	TERM RCPT 187 22-18AWG S09774-T1
111000587	00	TERM RCPT 16-14 AWG
111000588	00	TERM RCPT 250 22-18 AWG
111000589	00	TERM RCPT 110 SER 22-18 AWG
111000590	00	TERM RCPT 110SER 14-16AWG S09779-T1
111000591	00	TERM RCPT 250 FASTON 10-12 AWG
111000592	00	TERM RCPT 250 16-14 AWG
111000593	EE00	CONN RCPT PNL 4 CONT 59-0482000
111000594	EE00	CONN PLUG PNL 4 CONT 59-04P2000
111000595	00	CONN KIT 90917-001
111000596	00	CONN HDR 50P 3M 3433-1002
111000597	00	CONN SOC 50P 3M
111000598	EE00	CONN 7P PNL MOUNT 91-T-3478-9
111000599	00	CONN TWIN LEAF CONT AMP #583875-2
111000600	EE00	CONN PIN HSG 4 POS AMP #1-480676-9
111000601	EE00	CONN PIN SKT 4 POS AMP #1-480677-9
111000602	00	CONN PIN AMP #350036-1
111000603	00	CONN HALL LOCK HDW KIT 552562-1
111000604	00	CONN 36P CHAMP PC MOUNT 552235-1
111000605	00	CONN 39 CONT AMP #360048-2
111000606	EE00	CONN 36P CHAMP PLUG AMP #552144-1
111000607	00	CONN RCPT FLNGD 5WIRE 20A 2515
111000608	EE00	CONN PLUG BANANA BLU 10A1010001 TSTEQ
111000609	EE00	CONN PLUG BANANA YEL 1081007001 TSTEQ
111000610	EE00	CONN PLUG BANANA GRN 1081004001 TSTEQ
111000611	EE00	CONN PLUG BANANA BLK 1081003001 TSTEQ
111000612	EE00	CONN PLUG BANANA RED 1081002001 TSTEQ
111000613	EE00	CONN PLUG BANANA WHT 1081001001 TSTEQ
111000614	EE00	CONN STRN RLF CVR 36P 3-552414-1
111000615	00	CONN FEMALE PIN 26-30AWG MOLEX 1433T
111000616	01	TERM BD, PCB MTG 2599A-19
111000617	00	TERM STRIP 17 POS 3597A-17
111000618	00	TERM STRIP 25POS 3597A-25
111000619	00	CONN TEST JACK #2202-1-03
111000620	00	TERM JUMPER 17 SECTION 600RJS-17
111000621	00	CONN 50 POS VERT MOUNT 552118-1
111000622	01	CONN 50 POS EDGE MOUNT 552130-1
111000623	00	HSG HDW KIT BAIL LOCK AMP #552566-1
111000624	00	CONN 100 POS SPECIAL HNP50C
111000625	00	CONN SKT, DIP, LOW PROFILE 316-AG40D
111000626	00	CONN CONT SKT #16 AMP 66428-1
111000627	01	TERM PIN 26-18 AWG CRIMP MR 350663-6
111000628	00	TERM BLOCK 8 POS KULKA 600A8
111000629	00	CONN MOD IV CRIMP SNAP-IN AMP85967-2
111000630	00	CONN HEADER 40 CNTCT ST PC TAIL 3M,
111000631	00	TERM WING 1/4" 14-16AWG B-71
111000632	EE00	TERM INSUL 16-22AWG AMP #2-32561-1
111000633	00	CONN MR 6P HDR GOLD AMP #9-350258-2
111000634	00	CONN MR 12P HDR GOLD AMP #9-350264-2
111000635	00	CONN MR 20P HDR GOLD AMP #9-350270-2
111000636	EE00	CONN BNC UG88/U TSTEQ
111000637	EE00	CONN BNC UG-414/U TSTEQ
111000638	EE00	CONN BNC UG-1094 A/U TSTEQ
111000639	EE00	CONN PIN FEMALE SKT 201580-1 TSTEQ
111000640	EE00	CONN 104P RCPT 201532-2 TSTEQ
111000641	EE00	CONN SHIELD AMP #202110-1 TSTEQ
111000642	EE00	CONN PIN MALE AMP #201578-1 TSTEQ
111000643	EE00	CONN 104P JACK AMP #201692-4 TSTEQ
111000644	EE00	CONN CLAMP MS97-3057-1016 TSTEQ
111000645	EE00	CONN SHELL MS3106B-24 TSTEQ
111000646	EE00	CONN 7P PLUG MS9724-2P TSTEQ
111000647	00	TERM STRIA 20 POS 20-141 TSTEQ
111000648	EE00	TERM STRIP 6 POS 6-141 TSTEQ
111000649	EE00	CONN PIN 583649-2 AMP
111000650	00	CONN RT ANGL 6P PCB MOUNT 09-75-1061
111000651	00	CONN 5P PCB MOUNT W/LCKG RAMP09651051
111000652	00	CONN GND CONTACT 16453
111000653	00	CONN RT ANGL 12P PCB MNT MLX 09751121
111000654	00	CONN 12P CRIMP TYPE W/LCKG RAMP MOLEX
111000655	00	RELAY SKT 1360-91
111000656	00	CONN RNG TERM 1/4" 10-12AWG R5110-T1
111000657	EE00	CONN MTG EARS MINTR MOLEX 1625-2
111000658	01	CONN DIP SKT 16POS FLT CA 3416-0000
111000660	00	CONN DSPL 35P CHERRY W30-060
111000661	00	CONN DSPL 38P CHERRY W30-120
111000662	00	CONN HSG 5P MOLEX 09-50-305
111000663	00	CONN POLARIZING KEY W/FL CAP MOLEX
111000664	EE00	CONN 15P MR AMP #1-480621-9
111000665	EE00	CONN PLUG 15P MR AMP #1-480620-9
111000666	00	CONN PC MTG PHONO-JACK MLX 15-24-0501
111000667	00	CONN WAFER, 6P MOLEX 09-18-5069
111000668	00	CONN PLUG 2P MOLEX 09-50-7021
111000669	00	CONN PC MOUNTED 2P MOLEX 09-88-2021
111000670	00	CONN 3P AMP #87270-3
111000671	01	CONN CONTACT AMP 87270 SER 87269-1
111000672	00	CONN 2P AMP #87270-2
111000673	00	CONN DUAL 12P RT ANGLE 88DJ12M00
111000674	02	CONN 12POS UNIV M-N-L AMP #350433-1
111000675	EE00	TERM BLOCK 5 POS FASTON 800-5-KT21
111000676	00	CONN SKT 24P DUAL IN-LINE IC 324-AG2D
111000677	01	CONN TEST JACK MIN PC 8041-15G6
111000678	00	CONN 22 DUAL POS 583458-2
111000679	00	TERM INSUL RING #22-26AWG R26243
111000680	00	TERM INSUL SPRING SPADE #18-22AWG
111000681	03	CONN 50P FEMALE 552409-1
111000682	02	CONN 50P MALE 1-552020-1
111000683	EE00	TERM STRIP 20 TERM 20-141 TSTEQ
111000684	00	CONN UNIV MATE-N-LOK 350429-1
111000685	00	CONN UNIV MATE-N-LOK 350431-1
111000686	EE00	SEE 111000705
111000687	EE00	TERM BLOCK BARRIER 2POS 2-141
111000688	EE00	CONN MOLEX MINI 03-06-1022 .062DIA
111000689	00	TERM RCPT 187 14-22 AWG
111000690	00	CONN SKT CONT .084 DIA UNIV 350551-1
111000691	01	CONN PLUG 12 POS UNI M-N-L 1-480708-0
111000692	00	CONN KEYING PLUG MOD IV 87077-1
111000693	00	CONN 6P MOD IV 86427-9
111000694	00	CONN 10P EDGE .156 CTRS 583299-1
111000695	00	CONN CONTACT CRIMP FORK 583259-3
111000696	00	TERM BLOCK BARRIER 353-11-09-001
111000697	00	CONN JUMPER 2 POS 422-13-11-026
111000698	EE00	CONN SLDR SLEEVE COAX TERM D-133-17
111000699	00	CONN INLINE PCB 16P AMP 1-87235-5
111000700	00	TERM PIN FEMALE #18-22 02-05-3204 MLX
111000701	01	CONN UNI M-N-L 12 POS CAP HSG
111000702	01	CONN PIN, GNDG BHASS PRF TIN 350654-1
111000703	01	CONN PIN BHASS PRF TIN 350538-1
111000704	01	CONN SKT BHASS PRF TIN 350537-1
111000705	00	CONN 10POS . 125 CTR AMP #87235-9
111000706	00	CONN UNI M-N-L 6 POS PLUG 1-480704-0
111000707	00	CONN FASTON 110 SER RCPT 61677-1

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111000708 through 111000901

PART NO.	REV	DESCRIPTION
111000708	EE00	CONN 3M 50P SLDR TAIL STR 3433-2003
111000709	02	CONN W/LN FLTR & VOLT SEL 6J4
111000710	00	CONN CONTACT, MALE 100-1024P
111000711	00	CONN 250 FASTON 18-22AWG AMP60413-1
111000712	00	CONN PIN AMP 61118-1
111000713	00	CONN 20-14GOLD PIN TPDR AMP#61117-5
111000714	00	TERM RING 1/4 STUD 10-12 2-35110-1
111000715	00	TERM RCPT COUPLE MALE 22-18AWG
111000716	00	TERM RCPT COUPLE FEM 22-18AWG
111000717	EE00	CONN EDGE PCB DUAL 25
111000718	00	CONN EDGE PCB DUAL 30
111000719	EE00	TERM PUSH-IN TO-3 1238
111000720	EE00	CONN WIRE SPLICE NONINSUL H18738
111000721	00	TERM TAB 250 8 STUD #H118
111000722	00	TERM TAB .250 8 STUD #H108
111000723	00	CONN POLARIZING KEY BETWEEN CONTACT
111000724	EE00	CONN SOLDER SLEEVE SPLICE D-133-59
111000725	EE00	CONN SOLDER SLEEVE SPLICE D-133-37
111000726	EE00	CONN CONT STRIPS 50 DUAL POS 31178276
111000727	00	OBSOLETE, REPLACED BY 111000867
111000728	EE00	CONN 10 CONT 3M STRAIGHT PIN 34912003
111000729	EE00	TERM STRIP SPEED NUT KULKA 1599SN
111000730	00	CONN PIN 2-87022-3
111000731	00	CONN CONT PIN 90DEG 030-2087-000
111000732	00	CONN CONT PIN 90DEG 030-2086-000
111000733	00	CONN CONT PIN 90DEG 030-2088-000
111000734	00	CONN 16P FEMALE 3327-0000 SCOTCHFLEX
111000735	00	SEE 111000368
111000736	01	TERM STRIP 8 POS FEED-THRU IN 3597A-8
111000737	00	CONN KEY, POLAR, PC EDGE AMP 583462-1
111000738	00	REPLACED WITH 111000692
111000739	00	CONN 86402-7
111000740	00	CONN PWR 25-6-200
111000741	00	CONN PLUG, PHONE SUB-MIN 25-6-200
111000742	00	CONN PLUG, PHONE MIN 25-308-B
111000743	00	CONN 1-86402-2
111000744	00	TERM RING PRE-INSUL 16-14AWG R1906ST1
111000745	00	TERM RING PRE-INSUL 22-18AWG R1894ST1
111000746	EE00	TERM STRIP 12 POS 12-541 TSTEQ
111000747	EE00	CONN OUTLET HUBBEL DPLX 5230 TSTEQ
111000748	EE00	TERM BUSHBUTTON 274-315 TSTEQ
111000749	00	CONN NYL MIN 1625-6/03-06-2061 MOLEX
111000750	00	CONN NYL MIN 1625-6/03-06-1061 MOLEX
111000751	00	CONN NYL 12POS 1340/03-09-1125 MOLEX
111000752	00	TERM 30A PWR POLE #1331
111000753	00	TERM BUSHING 3/16 TERM DC-251-1
111000754	00	TERM BLOCK 10POS KULKA #600-10-UH
111000755	EE00	CONN RCPT, FLAG #FFT-1 .250-18-14AWG
111000756	00	CONN PCB 50P DBL ROW 90DEG
111000757	00	TERM ARKLES PGGYBK 3500H21A
111000758	00	TERM ARKLES .250 FLG FEM 3000H484A
111000759	00	CONN PCB 50P
111000760	01	CONN PCB 60P
111000761	00	TERM PGGYBK .250 300H121A
111000762	00	CONN MALE P-412-CCT TSTEQ
111000763	00	CONN FEMALE S-412-CCT TSTEQ
111000764	00	TERM STRIP ETC 38002-3820-3822-3823
111000765	EE00	TERM STRIP ETC 18002-3820-3831
111000766	00	CONN 10 POS AMP 86402-8 MICRO NOVA
111000767	EE00	TERM WIRE - RING TONGUE 90DEG 35508
111000768	EE00	TERM WIRE - RING TONGUE 35183 AMP
111000769	EE00	CONN CD EDGE 20 POS FL CA
111000770	00	TERM 10-12AWG GLAG ARK-LES 3000H60A
111000771	EE00	CONN TERM PLUG 9 POS .093DIA 19092092
111000772	EE00	CONN TERM RCPT 9 POS .093DIA 19091091
111000773	EE00	CONN SKT 3M 40 CONT 3417-0000
111000774	00	CONN CONT MATE-N-LOK AMP #61117-1
111000775	EE00	CONN PLUG UNIV M-N-L 9POS 350720-1
111000776	EE00	CONN CAP UNIV M-N-L 9POS 350782-1
111000777	EE00	CONN PLUG 20A 3 PHAS WYE 277/480 2521
111000778	EE00	CONN RCPT 20A 3 PHAS WYE 277/480 2525
111000779	00	CONN SKT 90DEG VERT MNT 14-810-90
111000780	00	CONN 100 CTRS 50 DUAL POS 000201-4895
111000781	00	CONN 86PPCB HW-43-C-0-111
111000782	01	TERM BRASS 3/16" HEYCO T-101-S
111000783	EE00	CONN COMP ADPTR 16P 616-DGS TSTEQ
111000784	00	CONN PLUG NYL 3POS MIN MOLEY 03062032
111000785	00	CONN RCPT NYL 3POS MIN MOLEY 03061032
111000786	EE00	CONN CD EDGE 20POS FL CA
111000787	00	TERM TAB .250 .171 STUD AMP 42214-2
111000788	00	CONN HOOD STRN RLF 1-350523-9 AMP
111000789	00	CONN HOOD CA STRN RLF 1-350373-9 AMP
111000790	00	CONN STRN RLF GROMMET 1-350380-1 AMP
111000791	00	CONN STRN RLF GROMMET 1-350377-0 AMP
111000792	EE00	CONN CAP PLUG 8P 1/2 X 3/4 PROT CLOS
111000793	00	TERM STRIP 3 POSITION 14303
111000794	EE00	CONN PC EDGE AMP #86792-3
111000795	EE00	CONN CONTACT EDGE AMP #86797-2
111000796	00	CONN 60P PGH300
111000797	00	CONN CONT REMOVABLE CRIMP 100-711268
111000798	00	CONN SKT 4P M-N-L AMP #1-480424-0
111000799	00	CONN HEADER 4PM-N-L AMP #350211-1
111000800	00	CONN RCPT FLNGD 20A HUBBELL TYPE 2535
111000801	EE00	CONN CONT, CRIMP 26-30AWG AMP 86015-1
111000802	EE00	CONN CA 3P AMP 86402-9
111000803	00	CONN SOCKET 20P DIP C8320-02 SE-0
111000804	00	CONN PLUG 20P DIP SHRTG
111000805	00	CONN CD EDGE 30 POS/60 CONT GOLD DOT
111000806	00	CONN PLUG, SHRTG 28P DIP
111000807	EE00	CONND 37P CINCH DCM-37P TSTEQ
111000808	EE00	CONN SHELL D CINCH DC-19678-3 TSTEQ
111000809	EE00	CONN DIP HEAD AUGAT 616-DGS TSTEQ
111000810	EE00	CONN RT ANGL POLAR .04580 P 3POS
111000811	00	CONN 12P .045DIA,TIN PLTD BRASS
111000812	00	CONN 3PHA Y 120/220AV 20A #2513
111000813	00	CONN 3PHA Y 347/600V 20A #2533
111000814	00	CONN PLUG 3PHA Y 120/208V 20A #2511
111000815	00	CONN PLUG MOLEX 03-06-2042
111000816	00	CONN HEADER 1X36 RT ANGLE 65275-001
111000817	00	CONN HEADER 4P RT ANGLE
111000818	00	CONN HEADER 4P RT ANGLE
111000819	00	CONN HEADER 5P RT ANGLE
111000820	00	CONN HEADER 6P RT ANGLE
111000821	EE00	TERM SLDR TAIL MALE 1778 PC
111000822	01	TERM SLDR TAIL FEMALE 1779 PC
111000823	00	CONN PLUG, STRIP LINE SGL ROW 13POS
111000824	00	CONN PLUG STRP LN 13POS, POS 10 RMOVE
111000825	00	TERM FASTON 3/16 S09309F-T1
111000826	EE00	CONN CD EDGE 100P 006064-100-061-003
111000827	EE00	CONN CD EDGE 100P WS11GR50DRIAH
111000828	EE00	CONN KEY POLAR 091-004-000
111000829	EE00	CONN KEY POLAR 6064-3317
111000830	00	TERM FASTON .110X.020 16-14AWG
111000831	01	REPLACED BY 111000531
111000832	EE00	CONN 40P RT ANGLE 3M 3432-3005
111000833	00	CONN CD EDGE 10 POS 20 CONT .125 CTRS
111000834	00	CONN KEY, POLAR, BETWEEN POSITION
111000835	00	CONN HDR SGL POS 90 DEG
111000836	00	CONN CONTACT MATE FROM 111-275
111000837	00	CONN PCB PIN HDR 9-CKT UNIV M-N-L
111000838	00	CONN PCB PIN HDR 15-CKT UNIV M-N-L
111000839	EE00	TERM IC 7R PRECUT STRIP 1938-4G1-7
111000840	EE00	TERM IC 8P PRECUT STRIP 1938-4G1-8
111000841	EE00	CONN SKT WIRE WRAP PIN
111000842	01	CONN RT ANGLE HDR W/LATCH STYLE B
111000843	00	TERM STRIP 3 POS 600-3-UH
111000844	EE00	CONN HSG 15 CKTS UNIV M-N-L
111000845	EE00	CONN HSG 9 CKTS UNIV M-N-L
111000846	EE00	CONN STRAIN RELIEF GROMMET .218ID
111000847	00	CONN STRAIN RELIEF GROMMET .250ID
111000848	EE00	CONN PC EDGE, DASHER KEYBD
111000849	01	TERM RING TNG #22-18AWG #10 STUD SIZE
111000850	00	TERM 6 POS TERM BLOCK W/UNASS HDW
111000851	EE00	TERM STRIP 18 POSITION THERMOPLASTIC
111000852	EE00	TERM STRIP 5 POSITION THERMOPLASTIC
111000853	EE00	CONN STRAIN RELIEF MATE-N-LOK
111000854	EE00	TERM MARKING STRIP 18 POSITION
111000855	EE00	TERM MARKING STRIP 5 POSITION
111000856	EE00	CONN CD EDGE 50POS MASS TERM
111000857	EE00	CONN HEADER PC THANS 50 POS
111000858	00	CONN FOIL GROUND PAD 1-023-5035
111000859	00	CONN 3M POLARIZING KEY #3439-0000
111000860	EE00	CONN CONTACT
111000861	EE00	TERM STRP 6POS FEEDTHRU MKD THERMOPLA
111000862	00	TERM CRP REM SKT CONT 26,28&30 AWG
111000863	00	TERM JUMPER STP 17POS SPADE 3/8 C/L
111000864	02	TERM STRIP 6 POSITION E500
111000865	00	CONN PIN AMP #117794-2 .125 SPACE
111000866	00	CONN KEY AMP #117646-1
111000867	00	CONN HSG AMP #1-117797-0 .125X.250
111000868	00	TERM LOW PF DIP SKT 18 CONT TIN PLD
111000869	EE00	CONN RECEPTACLES # 85861-2 MOD 2
111000870	EE00	CONN,PCB TRANSITION 60 POS
111000871	EE00	CONN AMP 10 DUAL POS
111000872	EE00	CONN RT ANGLE PCB MNTG 20CONT SLDR TL
111000873	EE00	CONN 60P CARD EDGE TO FLAT CA W/EARS
111000874	00	CONN 15 DYAL EDGE .100 CTR W/O EARS
111000875	00	CONN 20 PIN DIP SOCKET P/N C932010
111000876	00	CONN RECEPTACLES TYPE "C" E250
111000877	00	TERM FEED THRU POST E250
111000878	00	CONN WAFER
111000879	00	CONN FASTON .250 INSUL FLAG 14-16AWG
111000880	00	CONN FASTON .250 INSUL FLAG 18-22AWG
111000881	00	CONN AC RCPT EAC-302
111000882	00	CONN 26 PIN
111000883	00	CONN 34 PIN
111000884	00	CONN 20 PIN
111000885	EE00	CONN EDGE 16 PIN
111000886	00	CONN 36 PIN
111000887	00	CONN 20P DIP W/5 SHORTED PAIRS
111000888	00	CONN 14P DIP SHRTG PLUG W/7 JMPRS
111000889	03	TERM HLOCK, MODULAR
111000890	00	CONN 25/50 EDGE BD, WN, NO EARS
111000891	00	CONN SOLDERLESS MOLTITE CONT SKT E250
111000892	00	CONN EDGE 20 PIN
111000893	00	CONN SOCKET 16 PIN
111000894	00	TERM JUMPER STP 2POSN SPADE TYPE 3/8L
111000895	01	CONN WIRE WRAP 6CONTACTS E500
111000896	00	CONN RCPT 125V 15A 3 WIRE STR BLADE
111000897	EE00	TERM WIRE WRAP PIN FOR SUPER KLUGE BD
111000898	EE00	CONN SCREW LOCK ASSY MALE E500
111000899	EE00	CONN SCREW LOCK ASSY FEMALE E500
111000900	EE00	CONN STRAIN RELIEF SHELL E500
111000901	00	CONN RCPT .093DIA PINS 3CONT NYL HSG

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111000902 through 111001097

PART NO.	REV	DESCRIPTION
111000902	00	CONN PLUG .093DIA PINS 3CONT NYL HSG
111000903	00	CONN PLUG .093DIA PINS 2CONT NYL HSG
111000904	00	CONN RING LUG FOR #2AWG CA TO 5/16BLT
111000905	00	OBSOLETE REPLACED BY 123001392
111000906	00	CONN, CONTACT RECPT, .025 SQ.
111000907	00	CONN,INSULATOR,26POS,125X.250 CTRS
111000908	00	TERM QUICK DISCONNET .187 18-22 AWG
111000909	00	TERM SPADE LUG #8 STUD #18AWG WIRE
111000910	00	TERM SPADELUG #8 STUD #12AWG WIRE
111000911	00	TERM SPADE LUG #10 14AWG
111000912	EE00	TERM SPADE LUG #8 14AWG
111000913	00	TERM SPADE LUG #10 STUD 18-22AWG
111000914	00	TERM QUICK DISCONNECT .187 TAB 12AWG
111000915	00	CONN 40 PIN & CVR W/O STRAIN RELIEF
111000916	00	CONN INSULINK BUTT SPLICE NYLON INSUL
111000917	00	TERM QUICK CONN FULLY INSUL #22-18AWG
111000918	EE00	CONN SOCKET I/C W/STANDOFF 1JPIN E100
111000919	00	TERM BUS STRIP CLIP ON SOLDERLESS
111000920	EE00	CONN FEMALE BVODY 60A 600VAC 5 WIRE
111000921	00	CONN MALE PLUG 60A 600VAC 5WIRE E500
111000922	00	CONN MALE HEADER RT ANGLE -025SQ
111000923	00	CONN POST MALE .025SQ RT ANGLE 5POS
111000924	00	CONN RIBBON CABLE TO PCB 40 COND
111000925	00	CONN SOCKET 40P DIP C9340-02
111000926	01	OBS REPLACED BY 111000508
111000927	00	CONN TERM RING TONGUE M5 12-10AWG
111000928	00	CONN CONTACTS (CHAIN)
111000929	00	CONN HEADER 2CIRCUITS SELECT GOLD
111000930	00	CONN HEADER 3CIRCUITS SELECT GOLD
111000931	00	CONN HEADER 4 CIRCUITS SELECT GOLD
111000932	00	CONN HSG 2 PIN
111000933	00	CONN HSG 3 PIN
111000934	00	CONN HSG 4 PIN
111000935	00	TERM BUTT SPLICE
111000936	EE00	CONN RECEPTACLE 7 CIRCUIT 3.96 CTRS
111000937	EE00	CONN RECEPTACLE 10CIRCUIT 3.96MM CTRS
111000938	00	CONN NEMA L21-30P FLANGED MTG
111000939	00	CONN NEMA L-21-30R
111000940	00	CONN NEMA L6-15R
111000941	00	CONN NEMA 5-15P FLANGED MTG
111000942	00	CONN NEMA L-6-15P FLANGE MTG
111000943	00	CONN NEMA L-21-30P
111000944	00	CONN RECPT HOUSING 12 POS
111000945	00	CONN MOUNTING HARDWARE "D"
111000946	00	CONN MOUNTING HARDWARE "D"
111000947	EE00	CONN HDR 10POS 1.14MM SQ 3.96MM CTRS
111000948	02	CONN CARD EDGE 25POS DUAL 3.2X6.4MM
111000949	EE00	CONN HEADER 7POS 1.14MM SQ 3.96MM CTR
111000950	00	CONN CONTACT MALE 2.38MM DIA P.C.TAIL
111000951	00	CONN SOCKET 2.38MM ID P.C. TAIL
111000952	00	CONN PC MOUNT RT ANGLE 8PIN
111000953	01	CONN PLUG HSG 36POS 4.19MM CTRS
111000954	01	CONN RECPT HSG 36POS 4.19MM CTRS
111000955	EE00	CONN RECPT HSG 4CONTACT 4.19MM CTRS
111000956	EE00	CONN PLUG HSG 4CONTACT 4.19MM CTRS
111000957	00	CONN HSG CARD EDGE 2X15 3.96MM CTRS
111000958	00	CONN CONTACT CARD EDGE 3.96MM CTRS
111000959	00	CONN 16POS 2X8 .1X.1 CTRS .25SQ RECPT
111000960	01	CONN HSG 26 CIRCUIT RECT
111000961	01	CONN HSG 26 CIRCUIT RECT
111000962	00	CONN CONTACT .062 DIA 16AWG F
111000963	00	CONN CONTACT .062DIA M
111000964	01	CONN HSG .125X.250CTRS 100POS
111000965	01	TERM SPEC BLOCK ASSY 4 POSITION
111000966	02	CONN CARD EDGE .125X.250 CTRS 100POS
111000967	00	CONN HSG 12 POS .1 CTRS
111000968	00	CONN HSG 2X7 .125X.250 CTRS
111000969	00	CONN HSG 2X10 .125X.250 CTRS
111000970	EE00	CONN CONTACT .25SQ' 20AWG W/STOP
111000971	00	TERM RING TONGUE 1/4 8AWG E500
111000972	EE00	CONN DP SCKT 18P MACHINED CONTACTS
111000973	00	CONN DIP SOCKET 28 PIN EDGE GRIP
111000974	00	CONN DIP SOCKET 24 PIN EDGE GRIP
111000975	EE00	CONN DIP SOCKET 22 P EDGE GRIP
111000976	00	CONN DIP SOCKET 18 PIN EDGE GRIP
111000977	00	CONN DIP SOCKET 16 PIN EDGEGRIP
111000978	00	CONN DIP SOCKET 14PIN EDGE GRIP
111000979	00	CONN M 2X10 2.54CTRS AU
111000980	00	CONN RECPT 5POS 2.54CTRS W/LOCK
111000981	EE00	CONN HEADER (MADE FROM 111-824)
111000982	00	CONN STRAIN RELIEF GROMMET
111000983	00	CONN STRAIN RELIEF
111000984	02	CONN POST RTANGLE 3.2 CTRS 14XL
111000985	02	CONN POST RTANGE 3.2CTRS 14XU
111000986	00	CONT 025 F W/INS SUPPORT MOD IV 22AWG
111000987	00	CONT POL KEY .1CTRS HSG
111000988	01	OBS REPLACED BY 111001336
111000989	00	CONN 12CIR M .086 DIA .250 CTRS
111000990	00	CONTACT.062 DIA F 20 AWG
111000991	01	CONN CARD EDGE 100 CIR .125X.250 CTRS
111000992	00	REPLACED BY 123001411
111000993	00	TERM QIK DISC .250FLAG REC 60851-1
111000994	00	CONN HSG CARD EDGE 2X25.1X.2 CTRS
111000995	00	CONN DEAD FRONT PLUGS 15A 125V 5266-C
111000996	EE00	TERM BLOCK 5POS 3/8 CTRS
111000997	00	CONN PRESSEIT SOCKET .025SQ 25POS
111000998	00	CONN PRESSFIT SOCKET .025SQ 18POS

PART NO.	REV	DESCRIPTION
111000999	00	TERM SPRING SPADE #8 22-16 AWG
111001000	00	TERM SPRING SPADE #8 16-14AWG CS/20
111001001	00	CONN IC SOCKET 16 POS RT ANGLE MTG
111001002	00	CONN HSG 6CIR NO EARS .062 D CONTACT
111001003	00	CONN PIN .062 DIA AU PLATE 20AWG
111001004	00	CONN FAST ON MALE PC MOUNT DGC P/S
111001005	01	TERM RING TNG #8 STUD 14-16AWG
111001006	00	TERM RING TNG # 1/4" 2-35345-1
111001007	01	CONN EDGEBD 30POS 60 CONT PC MOUNT
111001008	00	CONN SOCKET PLUG DGC JR
111001009	00	CONN HEADER RT ANGLE DGC JR
111001010	EE00	CONN MR 36P HSG AMP 1-350356-9
111001011	EE00	CONN MR 36P HDR GOLD AMP 9-350276-2
111001012	00	CONN CARD EDGE 50PIN INS DISPLACEMENT
111001013	00	CONN HSG 9POS .100 AMP 1-87499-5
111001014	00	CONN 9POS .100 RT ANGLE AMP 87528-4
111001015	00	CONN RIGHT ANGLE 9POS 22-12-2091
111001016	00	CONN 6CIRCUIT INS DISPLACEMENT 22AWG
111001017	00	CONN HSG 12POS .156CTRS PCB EDGE
111001018	EE00	CONN HSG 6 CKT .250 GRID
111001019	00	CONN CARDEDGE 50 CONT .1X.2 CTRSWOEAWS
111001020	00	CONN CARDEDGE .1X.2 SELECT LOADED
111001021	00	CONN HSG 2X35 .1X.2 CTRS
111001022	00	CONN PC MTG .250 CTRS 9 POS F
111001023	EE00	CONN PC MTG .250 CTRS 12POS F
111001024	EE00	CONN SKT 10 COND FLAT CABLE
111001025	EE00	TERM SPADE TNG#10 14-16AWG INSULATED
111001026	EE00	CONN PCB 10 COND FLAT CABLE
111001027	EE00	CONN HDR RT ANGLE 10 COND FLAT CABLE
111001028	00	TERM RG TNG 3/8 STUD 16-22
111001029	00	CONN CARDEDGE .1X.2 50POS W/O EARS
111001030	EE00	TERM SPADE #8 16-14AWG 34166 BA14EF8
111001031	EE00	CONN DIPSOCKET 16PIN MACHINED SOCKET
111001032	00	CONN POST .1CTRS 3 POS RT ANGLE
111001033	00	CONN TELJACK 6POS-4WIRE-
111001034	00	CONN TELJACK 8POS POLARIZED
111001035	00	CONN RIB CABLE PLUG HDR 50 PIN
111001036	00	CONN HSG .250CTRS 4CIR 1-480703-D
111001037	00	KEY POLARIZING 3M-3439-1
111001038	00	TERM MALE TAB 18-22AWG .110X.020 E250
111001039	00	CONN JUMPER PLUG
111001040	01	CONN HSG .250CTRS 3CIRCUIT
111001041	00	CONTACT .086DIA MALE 24-18 AWG
111001042	EE00	CONN HSG .250CTRS 4 CIRCUIT
111001043	00	CONN .1CTRS RTANGLE PC MTG GOLDPLATED
111001044	00	CONN SUB D 25 CIRCUIT RT ANGLE PC MTG
111001046	EE00	TERM SPADE TONGUE 10-12AWG #8 STUD
111001047	00	CONN PIN HSG (CAP) 2 CIRCUITS
111001048	EE00	CONN CONTACT,MALE AMP 350967-2
111001049	EE00	CONN 16DUAL AMP 1-583715-4
111001050	00	CONN PC EDGE W/EARS & CRIMP CONTACTS
111001051	00	CONN HSG & PINS AMP 88398-3
111001052	00	CONN HSG & PINS AMP 86673-5
111001053	EE00	CONN HSG & PINS AMP 86792-3
111001054	00	CONN HSG & PINS AMP 88270-3
111001055	00	CONN 100CIRCUIT .025SQ FEMALE PDL BD
111001056	00	SHUNT PROGRAMMABLE
111001057	00	CONN CARD EDGE 60PIN INS DISPLACEMENT
111001058	EE00	CONN EDGEBD RT ANGLE 50/100 .100/.200
111001059	00	CONN .1X.1CTRS RT ANGLE MTG WW TAILS
111001060	EE00	CONN CARD EDGE I/O BD RETAINER
111001061	EE00	TERM TRANSFORMER BOBBIN DGC-JR
111001062	00	TERM RING TONGUE M4 10-12AWG STUD #8
111001063	00	CONN HSG .198CTRS 4CIR
111001064	00	CONN HSG .198CTRS 15CIR
111001066	00	CONN PIN HEADER 12CIR LONG TAIL
111001067	00	CONN PWR 12PIN RIGHT ANGLE
111001068	EE00	TERM FLANGED FORK (SPADE) TONGUE
111001069	EE00	CONN HOOD 25 C/R SUB D "DATAPHONE"
111001070	EE00	CONN CARD GUIDE AMP 583671-1
111001071	00	CONN 26 CONTACT HEADER 3M 3429-1302
111001072	EE00	TERM FASTON REC 14-16GA .110TAB X.032
111001073	00	TERM FOUR BARRIER STP JMPR
111001074	00	TERM TWO BARRIER STP JMPR
111001075	00	CONN HSG 2CIRCUIT .250CTRS LOCKING
111001076	00	CONN CONTACT SOCKET 18AWG AMP350570-1
111001077	EE00	TERM .110X.032 18-22AWG INSULATED
111001078	EE00	CONN PNL MTG COAX-PWR
111001079	EE00	CONN PC MTG .101 DIA PHONE JACK
111001080	EE00	CONN HSG 50CIRCUIT,1CTRS AMP1-583861-7
111001081	EE00	SOCKET PCB .025SQ P AUGAT 8134-HC-8P3
111001082	00	RECEPTACLE .062 TAB AMP 60900-1
111001083	00	CONN PIN HSG 6POS AMP 1-480271-0
111001084	00	CONN HSG 3CIR .250CTRS AMP1-480701-0
111001085	03	CONN SOCKET CRT 7CIRCUIT ASSY
111001086	EE00	CONN 2CIR .250CTRS PC MTG SOCKETS
111001087	00	BINDING POSTS GRN 257-104 TSTEQ
111001088	00	BINDING POSTS BLK 257-103 TSTEQ
111001089	00	BINDING POSTS RED 257-102
111001090	00	BINDING POSTS WHITE 257-101 TSTEQ
111001091	00	CONN BANANA JACK WHITE 256-101 TSTEQ
111001092	00	CONN BANANA JACK RED 256-102 TSTEQ
111001093	00	CONN BANANA JACK BLK 256-103 TSTEQ
111001094	00	CONN BANANA JACK GRN 256-104 TSTEQ
111001095	00	CONN PLUG BANANA RED 476-102 TSTEQ
111001096	00	CONN PLUG BANANA WHT 476-101 TSTEQ
111001097	00	CONN PLUG BANANA BLK 476-103 TSTQ

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111001098 through 111001316

PART NO.	REV	DESCRIPTION
111001098	00	CONN PLUG BANANA GREEN 476-104 TSTEQ
111001099	00	CONN PLUG BANANA BLUE 476-105 TSTEQ
111001100	00	BUSHING,TELESCOPING CA18220-10 TSTEQ
111001101	00	BUSHING,TELESCOPING CA18220-12 TSTEQ
111001102	00	BUSHING TELESCOPING CA18220-16 TSTEQ
111001103	00	TERM BARRIER BLOCK 12TERM 140SER TSTQ
111001104	00	TERM BARRIER BLOCK 4TERM 142SER TSTEQ
111001105	00	TERM BARRIER BLOCK 6TERM 142SER TSTEQ
111001106	00	TERM BARRIER BLOCK 8TERM 142SER TSTEQ
111001107	00	TERM BARRIER BLOCK 12TERM 142SER TSTQ
111001108	00	TERM BARRIER BLOCK 4TERM 150SER TSTEQ
111001109	00	TERM BARRIER BLOCK 6TERM 150SER TSTEQ
111001110	00	TERM BARRIER BLOCK 8TERM 150SER TSTEQ
111001111	00	TERM BARRIER BLOCK 4TERM 140SER TSTEQ
111001112	00	TERM BARRIER BLOCK 6TERM 140SER TSTEQ
111001113	00	CONN DIP SOCKET 8P 508AG10F TSTEQ
111001114	00	CONN DIP SOCKET 14P 514AG10F TSTEQ
111001115	00	CONN DIP SOCKET 16P 516AG10F TSTEQ
111001116	00	CONN PGB-30C WINNCHESTER TSTEQ
111001117	00	CONN PGB-25C WINNCHESTER TSTEQ
111001118	00	RECP 30A 1PHASE 125V 2815 TSTEQ
111001119	00	CONN MIRROR IMAGE 40P RCCO-2540P TSTQ
111001120	00	CONN DIP SOCKET-8P C850800 TSTEQ
111001121	00	CONN RF AMPH 31-222 TSTEQ
111001122	00	BUSHING,TELESCOPING CA18220-18 TSTEQ
111001123	00	BUSHING,TELESCOPING CA18220-6 TSTEQ
111001124	00	BUSHING,TELESCOPING CA18220-4 TSTEQ
111001125	00	BUSHING,TELESCOPING CA18220-3 TSTEQ
111001126	00	TERM BLOCK MRKR STP MS-4-140 TSTEQ
111001127	00	TERM BLOCK MRKR STP MS-6-140 TSTEQ
111001128	00	TERM BLOCK MRKR STP MS-8-140 TSTEQ
111001129	00	TERM BLOCK MRKR STP MS-12-140 TSTEQ
111001130	00	TERM BLOCK MRKR STP MS-4-142 TSTEQ
111001131	00	TERM BLOCK MRKR STP MS-6-142 TSTEQ
111001132	00	TERM BLOCK MRKR STP MS-8-142 TSTEQ
111001133	00	TERM BLOCK MRKR STP MS-12-142 TSTEQ
111001134	00	TERM BLOCK MRKR STP MS-4-150 TSTEQ
111001135	00	TERM BARRIER MRKR STP MS-6-150 TSTEQ
111001136	00	TERM BLOCK MRKR STP MS-8-150 TSTEQ
111001137	00	TERM BARRIER BLOCK 8TERM 140SER TSTEQ
111001138	00	CONN SOLDERLESS TERM PL10-5535 TSTEQ
111001139	EE00	CONN CONTACT 90 AMP 583285-4
111001140	EE00	CONN POLARIZING PLUG 90 AMP 583661-1
111001141	EE00	CONN PC EDGE 90 12PIN AMP 582376-9
111001142	00	CONN HSG .198CTRS 4CIR
111001143	00	CONN HSG .198CTRS 15CIR
111001144	00	CONN CARDEDGE .156CTRS 6POS 6CIR
111001145	00	TERM RING TONGUE M4 #8 10-12AWG
111001146	00	CONN MALE SPCL PIN AMP 204219-1 TSTEQ
111001147	00	CONN RECEPTACLE SPR-25W-2 TSTEQ
111001148	00	CONN DIP CLIP 14PIN 61-105 TSTEQ
111001149	00	CONN DIP CLIP 16PIN 61-106 TSTEQ
111001150	00	CONN BINDING POSTS BLU 257-105 TSTEQ
111001151	00	CONN CA PLUG 20P MALE 1FT TSTEQ
111001152	00	CONN CA PLUG 20PIN MALE 2FT TSTEQ
111001153	00	CONN PROBE SPA-25H-1 TSTEQ
111001154	00	CONN HEADER RT ANGLE 40P 3M 3432-1302
111001156	00	CONN MATE-N-LOCK 9POS AMP 1-480706-0
111001157	00	CONN 50PIN .100IN 3VH25/1JN05 TSTEQ
111001158	00	COMPONENT CARRIER 16PIN TSTEQ
111001159	00	TERM PCB SNAP-IN .10MAX INSUL 18-22GA
111001160	EE00	CONN COAX BNC PNL/PC MTG RTANGLE
111001161	EE00	CONN COAX PLUG BNC 1RG59B
111001162	00	CONN CONTACT 0.64 (0.25) SQ FEMALE
111001163	00	CONN PIN HEADER 3CIR LG TAIL
111001164	00	CONN PINS BERG 75691-018 TSTEQ
111001165	00	HSG 16PIN BERG 65039-021 TSTEQ
111001166	01	CONN PANAPLEX 51POS
111001167	00	CONN CAPTIVATING WEDGE FOR PANAPLEX
111001168	00	FF SPRING PINS 833-137 TSTEQ
111001169	00	FF INT PNL PINS 833-025 TSTEQ
111001170	00	RECEPTACLE WIRE WRAP 833148 TSTEQ
111001171	EE00	CONN 100CIR .025SQ F PADDLE BD .1CTRS
111001172	00	CONN 12CIR PC MTG .250 CTRS W/PINS
111001173	00	CONN CONTACT CRIMP SKT .093D 14-20AWG
111001174	EE00	CONN CARDEDGE .125X.250 100CIR
111001175	00	TERM CONTACT PC PIN GOLD OVER NICKEL
111001176	00	TERM CONTACT PC SKT GOLD OVER NICKEL
111001177	EE00	CONN HSG 3POS .100 CENTER AMP 87175-8
111001178	00	TERM JUMPER BLK
111001179	EE00	CONN ACC RETAINING SCREW ASSY
111001180	EE00	CONN PIN HSG 2POS AMP 350777-1
111001181	EE00	CONN PIN HSG 3POS AMP 350766-1
111001182	EE00	CONN CONTACT PIN 24-18 AMP 350561-1
111001184	00	TERM FASTON FULLY INSUL .110X.016
111001185	00	CONN RIBBON CA SOCKET 50CIR W/STHAIN
111001186	EE00	CONN POST .025SQ .640LG
111001187	00	CONN STRAIN RELEIF
111001188	00	CONN CONTACT PDDL BD PC MTG .025SQ"F"
111001189	EE00	CONN EDGEBD RT W/O EAR 50-100
111001190	00	CONN CARD EDGE W/O MTG EAR 50P TSTEQ
111001191	00	CONN CARD EDGE W/MTG EAR TSTEQ
111001192	00	TERM FASTON .110 X .020 PC MTG
111001193	00	CONN CONTACT CRIMP MOLEX 08-50-0187
111001194	00	CONN HSG MOLEX 26-03-4061
111001195	EE00	CONN ADAPTER .4X.1TO.3X.1CTRS 22PIN
111001196	EE00	POLARIZING KEY .156 CTRS

PART NO.	REV	DESCRIPTION
111001197	00	CONN HSG 7POS FOR LCK .025SQ F CONT
111001198	00	CONN HSG 9POS LOCKING CONT025SQF
111001199	00	RECP CONTACT MAXI PV .025SQ 75694-010
111001200	EE00	CONN HSG DBL ROW MAXI LATCH 40POS
111001201	00	CONN HSG SGL ROW MAXI LATCH 6POS
111001202	00	CONN HSG DBL ROW MAXI LATCH 52POS
111001203	EE00	TERM WALL "D" TST PIN 82000017 TSTEQ
111001204	00	POLARIZING KEY MINI-MAXILATCH HSG
111001205	00	CONN 50CIR U RIBBON CABLE MTG F
111001206	00	CONN 15PIN WINCHESTER PGB 15BS
111001207	00	CONN SOCKET 25P PCB GOLD PLATED
111001208	EE00	SOCKET ZERO INSERTION 16PIN TEXTOOL
111001209	EE00	SOCKET ZERO INSERTION 20PIN TEXTOOL
111001210	EE00	SOCKET ZERO INSERTION 40PIN TEXTOOL
111001211	EE00	RECP WIRE WRAP 20PIN TEXTOOL
111001212	EE00	RECP WIRE WRAP 40PIN TEXTOOL
111001213	EE00	RECP WIRE WRAP 16PIN TEXTOOL
111001214	00	CONN PC MTS .250 CTRS FOR .093 PC BRD
111001215	00	TERM PUSH-IN .062DIA HOLE TIN PLATE
111001216	00	RECP MOD 4 CRIMP SNAP IN CONTACT HIPR
111001217	00	CONN PINS 2550 800203-024
111001218	00	CONN HEADER 20P BERG 65610-120
111001219	00	CONN HEADER 26PIN BERG 65610-126
111001220	00	CONN HEADER 34P BERG 65610-134
111001221	EE00	CONN AC PLUG 15A-250V L6-15P
111001222	EE00	HSG TRANSDUCER
111001223	EE00	CONN PIN HEADER PCB MTG 6CKTS
111001224	EE00	CONN PLUG HSG 15 CIRCUIT
111001225	EE00	CONN PIN HEADER PCB MTG 15CIRCUIT
111001226	EE00	CONN D SOCKET 25POS
111001227	00	CONN CARD EDGE .100 CNTS DUAL 17
111001228	EE00	CONN D PIN 25 POS
111001229	00	CONN HSG SGL ROW 18POS BERG 65302-019
111001230	EE00	DUPLICATE PART SEE 111-798
111001232	EE00	CONN 34CIR RIB CA PC HDR W/LOCK STR
111001233	EE00	CONN 20 CIR RIB CA PC HDR WO LCK STR
111001234	EE00	CONN 9C1R .125CTRS PC RA TIN PLTD
111001235	EE00	CONN 20CIR RIB CA SOCKET W/ST RN RELF
111001237	EE00	RECP CONTRACT HI PRESSURE 18-20AWG
111001238	00	RECP CONTACT HI PRESSURE 22-26AWG
111001239	00	CONTACT PIN .025SQ 22-26AWG
111001240	00	CONN HDR 60P RIBBON
111001241	00	CONN SCK 60P RIBBON
111001242	EE00	CONN RIB CA HDR W/LOCK60CIR
111001243	EE00	CONN STR HDR 50CIR W/LOCKS
111001244	00	CONN INP/OUP 45POS DUAL WINCH PGB-45D
111001245	EE00	CONN KEY CARD EDGE RIB CA 109-101037
111001246	EE00	CONN KEY CARD EDGE RIB CA 609-0005
111001248	00	TERM SLOTTED SOLDER
111001249	00	TAB MALE .250 ANGLED #8 STUD
111001250	EE00	CONN 9POS .145CENTERS
111001251	EE00	RECEPTACLE 9POS CONN .145CENTERS
111001253	EE00	CONN "D" 25POS STRAIGHT POST
111001255	00	TERM SPADE FLANGED #8 1-2-10AWG INS
111001256	EE00	TPRM RING TNGE 5/16 10-12 AWG
111001257	EE00	TERM RING TNGE 5/16 6AWG 430INS
111001258	EE00	CONTACT .062 M 24-30AWG .090INS
111001259	EE00	CONN FLT CA HEADER RT ANGLE W/W TAILS
111001260	EE00	CONN HSG 15CIR .25CTRS CAP
111001261	EE00	TERM RING TNGE #6 STUD 8 AWG
111001262	EE00	TERM RING TOUNGE 1/4 14-16AWG
111001263	EE00	TERM RT #10 14-16AWG
111001264	EE00	TERM RING TONGUE LUG 10AWG #8STUD
111001265	EE00	CONN HSG HI CURRENT EDGE
111001266	EE00	CONN CONTACT HI CURRENT EDGE
111001267	EE00	SOCKET PIN FOR WIRE WRAP BDS
111001268	00	SOCKETS BURNDY SC14M-1TK6
111001269	EE00	VERTICAL HEADER 50 POS
111001270	EE00	CONN CONTACT CRIMP FORK
111001272	EE00	TERM FSTN FULLY INSU 14-16AWG
111001273	00	CONN PIN HOUSING 6POS
111001274	EE00	CONN HEADER 14POS RIGHT ANGLE
111001277	00	CONN 25/50PIN EDGE RT ANGLE PINS
111001286	00	CONN 14POS .100CENTERS
111001287	EE00	CONTACT BELLOWS-WINCHESTER HW SERIES
111001288	EE00	CONTACT CANTILEVER-SYLVANIA 6AD07
111001289	EE00	CONN 25POS "D" STRIGHT PCB MOUNT
111001290	EE00	CONN BANANA M W/8-32X1/2 STUD
111001292	EE00	CONNECTOR HOLDER 8 POSITION .1X.2
111001293	EE00	CONN SUB D PC MTG RTANGLE 25 CIR
111001294	EE00	CONN SOCKET PRESSFIT 025 TIN
111001295	EE00	CONN 8PIN DIP SOCKET SOLDER TAIL
111001296	EE00	TERM RING TONGUE #8-10
111001297	EE00	CONTACT LOCKING CLIP
111001299	EE00	CONN DIP SOCKET WW TAIL 14 CIR
111001303	EE00	TERM HOT TIP DIP
111001305	00	PLUGMOLD 5' W/6" CENTERS TSTEQ
111001306	00	WIREMOLD ENTRANCE END FITTING TSTEQ
111001307	00	CONN HSG MATE-N-LOCK 4PIN
111001309	EE00	TERM .250X.032 TAB .200 MTG HOLE
111001310	00	CONN SKT CRT 7CIRCUIT WAVE SOLDERABLE
111001311	00	CONN D 15POS PIN PCB MTG
111001312	00	CONN HSG 15 CIR SUB D FEMALE
111001313	EE00	CONN PDLCBD .125X.250 100 CIR
111001314	00	CONN PLUG BNC CRIMP TYPE
111001315	00	CONN RECEPT BNC W/PCB MT POST R/ANGLE
111001316	00	CONN CO-AX TEE ADPTR BNC CRIMP TYPE

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111001317 through 113000165

PART NO.	REV	DESCRIPTION
111001317	EE00	CONN HEADER STRAIGHT 26PIN
111001318	EE00	CONN SOCKET 26PIN
111001327	EE00	CONN PCB .250CTRS 9 POS PIN
111001329	00	CONN FASTON TAB .187MALE PC MT .200CT
111001330	00	CONN ACSSY BACKSHELL 15CIR D 90-45
111001331	00	CONN PIN 26-30 MATE-N-LOCK
111001332	00	CONN STRAIN RELIEF AMP 1-350589-0
111001333	EE00	CONN HSG IBM "A" STYLE I/O
111001334	EE00	CONN HSG IBM "B" STYLE I/O
111001335	EE00	CONTACT MODULE 24POS AMP 207221-1
111001336	00	CONN SOCKET PRESSFIT .025SQ 20POS
111001337	EE00	CONN HSG SGL ROW 14PIN .125CTRS
111001338	EE00	CONN HSG 9CIR .250CTRS PNL MTG
111001339	EE00	CONTACT R ANGLE POST 25DUAL POSITION
111001340	EE00	CONN HDR 20CIR RT ANGL PCB RIBCABLE
111001341	EE00	CONN CARD EDGE 60CIRCUIT
111001342	EE00	RECPT MOD V 22-26AWG WIRE
111001343	EE00	CONN CARD EDGE 100CIR .125X.250
111001344	EE00	CONN NEMA 14-30P
111001345	EE00	CONN 2CIR CAP PNCMTG .250CTRS
111001351	00	CONN HEADER 20PIN UNSHROUDED
111001352	EE00	HEADER RIGHT ANGLE .125 CENTER
111001353	EE00	HEADER PROG 10POS .100X.300
111001355	EE00	CONN HDR 3PIN RT ANGLE
111001356	00	CONN HSG CAP 15PIN
111001357	EE00	TERM WING TONGUE 5/16 #2AWG 90°INSUL
111001370	EE00	CONN HSG SCK 15DUAL W/SHORT EAR CRIMP
111009999	00	PLUG 20P DIP NON-INSERTED
111111111	00	MAINTENANCE DATE RECORD
113000001	00	CB 10A 65V MAX AIRPAX APG1-1
113000002	00	FUSE 10A 250V 3AB
113000003	00	FB 2-POLE,3AG MTG,LITTLFLFUSE #357002
113000004	00	FUSE 1/2A 250V 8AG
113000005	00	FUSE 3/4A 250V 8AG
113000006	00	FUSE (REPLACED BY 113000004)
113000007	00	FUSE 3/4A FAST ACTING
113000008	00	FUSE CLIP,EARLESS, BUSS #5680-05
113000009	00	FUSE 2A 250V 8AG
113000010	00	FUSE 3A 250V 3AG SLO-BLO
113000011	00	FUSE 2A 250V 3AG SLO-BLO
113000012	00	FUSE 1/2A 250V 3AG SLO-BLO
113000013	00	FUSE 3/8A 250V 3AG SLO-BLO
113000014	00	FUSE 1A 250V 8AG FAST ACTING
113000015	00	FUSE 4A 250V 3AG
113000016	00	CB 15A 50V 1-POLE TI#51MC2-29-15
113000017	00	FUSE 15A 32V LITTELFUSE 1AG#301015
113000018	00	FUSEHOLDER PNL MTD,R-A TERM,LF#342004
113000019	00	FUSE 15A 250V 3AB
113000020	00	FUSE 30A 600V
113000021	00	FUSE BLOCK 3-POLE 250V BUSS #2809
113000022	00	FUSE 5A 32V LITTELFUSE 1AG#301005
113000023	00	FUSE 10A 32V LITTELFUSE 1AG#301010
113000024	00	FUSE (REPLACED BY 113000023)
113000025	00	FUSEHOLDER PNL MTD,STR TERM,LF#342012
113000026	00	FUSE 30A 125V 3AB
113000027	00	FUSEHOLDER PNL MTD,H-V KNOB, LF#340276
113000028	00	PICOFUSE AX, LEAD 3/4A 125V
113000029	00	FUSE 2 1/2A 32V BUSS AGW GLASS TUBE
113000030	00	FUSE 1/4A 250V 8AG FAST ACTING
113000031	00	FUSE (REPLACED BY 113000045)
113000032	00	FUSE 15A 32V BUSS MDL FUSETRON
113000033	00	FUSE 5A 250V 3AB
113000034	00	FUSE 1A 125V 1AG
113000035	00	FUSE 3A 32V 1AG
113000036	00	FUSE 6A 32V BUSS AGA GLASS TUBE
113000037	00	FUSE 8A 250V 3AB
113000038	00	FUSEHOLDER PNL MTD,STR TERM,LF#342038
113000039	00	PICOFUSE (REPLACED BY 113000028)
113000040	00	FUSE 15A 32V BUSS AGC FAST ACTING
113000041	00	FUSE 2A 250V 3AG
113000042	00	OBSOLETE, REPLACED BY 113000191
113000043	00	FUSE 313005
113000044	00	FUSE 3A 32V LITTELFUSE 1AG#301003
113000045	00	FUSE 4A 32V BUSS AGW FAST ACTING
113000046	01	CB 20A 65V 2P AIRPAX #UPG11-2746-1
113000047	00	FUSE 5A 250V 3AG
113000048	00	FUSE HOLDER IN LINE FOR 3AG
113000049	01	FUSE HOLDER,MODIFIED,INLINE FOR 3AG
113000050	00	FUSE 1/4A 250V 3AG SLO-BLO
113000051	00	FUSE 1/8A 250V 3AG SLO-BLO
113000052	00	FUSE 4A 32V LITTLEFUSE 311004
113000053	00	FUSE 5A 32V LITTLEFUSE 311005
113000054	00	FUSE 10A 32V LITTLEFUSE 311010
113000055	00	CB 8A 50160HZ 250V AIRPAX 00000188
113000056	00	FUSE 1A 250V SLO BLO 3AG
113000057	00	FUSE 1A 250V 3AG
113000058	00	FUSE 1/8A 3AG 800316-001
113000059	00	FUSE USE 113-37 800316-080
113000060	00	FUSE 15A USE 113-19 800316-150
113000061	00	FUSE 1/2A 250V 3AG
113000062	00	FUSE 3A 125V 203115401
113000063	00	FUSE 2A 250V 203115305
113000064	00	CB 3POLE 20A 209-3-1-62F-3-8-20
113000065	02	CB 2POLE 20A 20A AIRPAX 209-2-3737
113000066	02	CB 1P 20A AIRPAX 209-1-3736-1
113000067	00	CB 4POLE 20A 209-4-1-62F-3-8-20 ELBD
113000068	00	PICOFUSE AX, LEAD 5A 125V
113000069	00	CB 10A 4POLE CAB 230V
113000070	00	CB 10A 3POLE 230V CAB
113000071	00	CB 10A 2POLE CAB 230V
113000072	00	FUSE 1A 125V 3AG 00000633
113000073	00	FUSEHOLDER 00000594
113000074	00	CKT BREAKER 3A 250V 00000593
113000075	00	CB 6P 10A,10A,10A,10A,15A,15A
113000076	00	CB 4P 10A,10A,15A,15A 209-4-3417-1
113000077	01	CB 2P 15A AIRPAX 209-2-3738-1
113000078	00	CB 4P 20A,20A,20A,10A 209-4-3415-1
113000079	00	CB 3P 20A,20A,10A 209-3-3414-1
113000080	00	CM BOUT 2 POLE 1113/34 OR 006-10196
113000081	EE00	CB 3A 50VDC 431-203-101 TSTEQ
113000082	EE00	CB 15A 250V 60H7 512-215-101 TSTEQ
113000083	EE00	CB 10A 109-210-101 TSTEQ
113000084	EE00	CB 25A 109-225-101 TSTEQ
113000085	EE00	CB 30A 109-230-101 TSTEQ
113000086	EE00	CB 35A 109-235-101 TSTEQ
113000087	00	CB OBSOLETE SEE 116-240 11499
113000088	00	FUHLR PNL LITTLEFUSF #342028
113000089	00	FUSE LINE 1A 250V 3AG 313001
113000090	00	FUHLR FUSE CLIP 391
113000091	00	FUSE 8A 250V SLO-BLO
113000092	00	PICOFUSE AX,LEAD 2A 125V
113000093	00	PICOFUSE AX, LEAD 4A 125V
113000094	01	CB 3P 20A 15A 15A 209-3-3684-1
113000095	01	CB 4P 15A, 20A, 20A 209-4-3683-1
113000096	01	CB 4P 20A, .20A, 15A, 15A 209-4-3685-1
113000097	01	CB 6P 15A, .15A, 15A, 15A, 20A, 20A
113000098	01	CB 5P 20A,20A,20A, 15A,15A209-5-3686-1
113000099	01	C.B. SWITCH 3P 2.5A 250V
113000100	01	C.B. SWITCH 3P 5.0A 250V
113000101	00	FUSE 3A,250V 3AB
113000102	00	FUSE 5A 250V 3AG
113000103	00	CB 3P AC 15A UPGH-666-1-6-600-153
113000104	00	CB 2P DC 10A UPGH-66-1-5-1-103
113000105	EE00	CB 3A 511-203-101 TSTEQ
113000106	EE00	CB 10A 511-210-101 TSTEQ
113000107	01	CIR BKR 1.5 AMP 250V 50-60HZ AIRPAX
113000108	01	CIR BKR 3.0 AMP 250V 50-60HZ AIRPAX
113000109	EE00	CABINET BUD TYPE C-1892 TSTEQ
113000110	00	PICOFUSE AX, LEAD 15A 32V
113000111	00	FUSE 20A 1AG 32V 301-020
113000112	EE00	CB 10A 112-210-101 TSTEQ
113000113	00	CB 125/250V 60HZ 10A 2P A/RPAX
113000114	00	FUSE 7.5 AMP 100026-026
113000115	00	FUSE 8 AMP 100028-022
113000116	00	FUSE 2A 32V 1AG
113000117	00	FUSE 6A 32V LITTLEFUSE 3AG #311006
113000118	00	CB AIRPAX UPG-U-3971-1
113000119	EE00	CB AIRPAX UPG-11-3972-1
113000120	00	FUSE 1.5A 32V LITTLEFUSE/BUSS
113000121	00	FUSE 2A 250V 3AB SLO-BLO
113000122	00	FUSE 6A 250V 3AG
113000123	00	CB 91977-007
113000124	00	FUSE 10A 220V 93142-010
113000125	EE00	CB THERMAL 1A 374-201-101
113000126	00	FUSE 3A 250V 3AB SLO-BLO
113000127	00	CB 2P 2A 277V UPGH-11-1-6-2-202-C
113000128	00	CB 2P 3A UPGH-11-1-6-2-302
113000129	00	FUSE 3/4A 250V 3AG 0143630
113000130	00	FUSE 1AG 32V 7.5A
113000131	00	FUSE 7A 250V 3AG
113000132	00	FUSE 20A TRON FAST BLOW GBB20
113000133	00	FUSE 10604-01
113000134	01	FUHLR PNL MIN 3AG QUICK CONN 342-038A
113000135	00	FUHLR PNL MIN 3AG QUICK CONN 342-028A
113000136	00	FUSE 1.5A SLO/BLO 00000874
113000137	00	FUSE 1A SLO/BLO 00000147
113000138	00	FUSE 5A 250V SLO-BLO
113000139	00	FUSE 7A 250V SLO-BLO
113000140	00	FUSE 10A 250V SLO-BLO
113000141	01	FUSE CLIP 1/4 DIA 631 MODIFIED ZIERCK
113000142	EE00	FUSE CLIP FOR 3AG 121002 LITTLEFUSE
113000143	00	FUSE 1A 250V 3AB 90437-001
113000144	00	FUSE 4A 250V 3AB 90437-004
113000145	00	FUSE 35A BUSS FAST-ACTG AGC 32V
113000146	00	FUSE 6.25A 250V 3AG SLO-BLO
113000147	00	CKT BKR ELECTROMAG UPGH-1-1-6-2-103
113000148	00	FUSE 220V .6A
113000149	00	CKT BREAKER 81504.5
113000150	00	CKT BKR 5 POLE 20,20,3,2,4A
113000151	01	CIRCUIT BRKR 3POLE 480VAC 15A
113000152	00	CKT BREAKER 230/50 6A 00000185
113000153	01	CB 3P 480VAC 8A 50/60HZ 83MC4-128-8
113000154	00	FUSE 15A 7AG FAST-BLOW
113000155	00	FUSE 15A 250V 7AG SLO-BLO
113000156	EE00	PICOFUSE AX, LEAD .125A 125V
113000157	01	FUSE CLIP PCB MTG 250 DIA
113000158	00	CIR BKR "E" FRAME 1PIN 15A
113000159	00	CIB BKR 5 POLE 15AMP 250V
113000160	00	CIR BKR 4 POLE 15AMP 250V
113000161	00	PICOFUSE RADIAL LEAD .5A 125V
113000162	00	CIR BKR 2 POLE 15AMP 240V "E" FRAME
113000163	00	CIR BKR 6 POLE 15AMP 240V "E" FRAME
113000164	00	CIR BKR 2POLE RKR MDL 15A 240V 50/60
113000165	00	FUSE 40AMP 32V STANDARD

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113000166 through 115000087

PART NO.	REV	DESCRIPTION
113000166	00	FUHLR SPARE
113000167	01	CIR BRK 10AMP DBLPOLE 250V 50/60HZ
113000168	00	CIR BKR THERMAL 5AMP KDI TYPE
113000169	00	CIR BKR THERMAL 8AMP KD-1 TYPE
113000170	00	CIR BKR THERMAL 3AMP KD-1 TYPE
113000171	01	CIR BKR 3P 40A 250V 24VAC DUAL ON 1P
113000172	EE00	CB 1P AC 15A
113000173	00	CB 1P AC 20A
113000174	00	CB 2P AC 15A
113000175	00	FUSE 7A SLO BLO
113000176	00	FUSE 1.5A FAST BLO
113000177	00	FUSE 4A 250V SLO BLO
113000178	02	FUHLR IN LINE HEAVY DUTY TYPE
113000179	00	FUSE 4A 250V 3AB
113000180	00	FUSE 1A 250V 3AB
113000181	01	CIR BKR SEW TRIP 2P 15A 250V 50/60HZ
113000182	01	CIR BKR SEW TRIP 2P 20A 250V 50/60HZ
113000183	01	CIR BKR SEW TRIP 1P 15A 250V 50/60HZ
113000184	01	CIR BKR SER TRIP 3P 20A 250V 50/60HZ
113000185	01	CIR BKR SEW TRIP 2P 30A 250V 50/60HZ
113000186	00	CIR BKR 3AMPS 250V
113000187	EE00	CIR BKR SEW TRIP 2P 40A 250V 50/60HZ
113000188	EE00	FUSE PICOFUSE RADIAL LEAD 10A 125V
113000189	00	FUSE CLIP PC MNT W/FUSE STOP
113000190	00	FUHLR PANEL
113000191	00	PICOFUSE AX LD 1.5A 125V
113000192	00	CIR BKR THERMAL 45-700-P-3A TSTEQ
113000193	00	CIR BKR THERMAL 45-700-P-15A TSTEQ
113000194	00	CIR BKR MAG-HYD 30A 1P TSTEQ
113000195	00	CIR BKR MAG-HYD 30A 3P TSTEQ
113000196	00	FUSE SLOBLO 5AMP 250V PIGTAIL
113000197	00	FUSE 15A SLO BLO 800917-150
113000198	00	FUSE 200A
113000199	00	FUSE 20A 250V 3AB 314020
113000200	00	FUSE 12A 250V 3AB 314012
113000201	00	FUSE 3AG 6A B300 800316-060
113000202	00	FUSE 3AG 12A B300 800316-120
113000203	00	FUSE 3AG 2A SLO BLO B300 800917-020
113000204	00	FUSE 3AG 20A SLO BLO B300 800917-200
113000205	00	FUSE 2A PICOFUSE B300 801702-001
113000206	00	CIR BKR UNIV (ININTL B300) 801732-003
113000207	00	CIR BKR UNIV & STD B300 801732-004
113000208	EE00	FUSE SEMICONDUCTOR
113000209	EE00	FUSE SEMICONDUCTOR
113000210	EE00	CIR BKR SINGLE POLE 10A 250V
113000211	00	FUSE 808-960301-002A
114000001	00	HUDSON 28V BULBS 2187D
114000002	00	HUDSON BULB 2176
114000003	00	INDICATOR CARTRIDGE CML 640321-
114000004	00	INDICATOR CARTRIDGE CML
114000005	00	INDICATOR CARTRIDGE CML 64 0272
114000006	00	INDICATOR CARTRIDGE 6V CML 240272 GR W
114000007	00	INDICATOR CARTRIDGE 115V CML 240321 RE
114000008	00	LAMP TUNGSOL #561
114000009	00	BULB-PLT LAMP CML 84-0421
114000010	00	LAMP PILOT 115V NEON (SEE 114000009)
114000011	00	LAMP INCANDESCENT AMBER 14V
114000012	00	LAMP INCANDESCENT RED 14V
114000013	00	INDICATOR RDOUT DIG SP-331 1.5D16.33"
114000014	00	INDICATOR RDOUT DIG SP-332 2DIG.33 IN
114000015	00	INDICATOR RDOUT DIG SP-333 3DIG.33 IN
114000016	00	INDICATOR RDOUT DIG SP-353 3DIG.55 IN
114000017	00	INDICATOR RDOUT DIG SP-354 2.5D.55IN
114000018	00	LAMP GE 379 37253790
114000019	00	INDICATOR FILE PROTECT 100105-002
114000020	00	LAMP NO.382 14V 10545
114000021	00	USE 114-33
114000022	00	LAMP GE 1638 TLNBE0009
114000023	00	LAMP 302005102
114000024	00	LAMP 302104001
114000025	00	LAMP INDICATOR 800163-002
114000026	00	LAMP INDICATOR 800785-002
114000027	00	LAMP LED VISIBLE 801082-001
114000028	00	LAMP UV 4000W 10862
114000029	00	BULB GE 683 5V .06A 525372001
114000030	00	LAMP INCANDESCENT 060-419
114000031	00	LAMP INCANDESCENT 060-434
114000032	00	LAMP ASSY INCAND 5V 00000312
114000033	00	LAMP INCAN 6V .20A T1-3/4 00000318
114000034	00	LAMP NO.387 28V 800163-003
114000035	00	BULB LAMP 6-3V RED CML-240271 TSTEQ
114000036	00	BULB LAMP 6-3V GRN CML-240272 TSTEQ
114000037	EE00	INDICATOR LIGHT 32R TSTEQ
114000038	00	LAMP ASSY OUTLINE CTG DISK 200-7236
114000039	00	BULB GE337 060-436
114000040	00	BULB HI-INTENSITY 6V 15W FM 150521
114000041	EE00	
114000042	00	LAMP G.E. 16651F
114000043	00	LAMP BASE 4345-006-UP
114000044	00	LAMP INDICATOR 24516803
114000045	00	LAMP INDICATOR 24V 94039102
114000046	EE00	LAMP PILOT IDI 105001 TSTEQ
114000047	00	LAMP PHOTOCELL 100176
114000048	EE00	BULB LAMP 222 OR 222X GE
114000049	00	BULB #120 PS 3W 120V 25MA
114000050	00	LAMP 12V 100W OSRAM
114000051	00	LAMP,EPX FOR MICROFICHE 3770-506

PART NO.	REV	DESCRIPTION
114000052	00	LAMP ESA 3363-5
114000053	00	LAMP PROJECTOR 500W CZA/CZB
114000054	00	LAMP INCANDESCENT 800163-006
114000055	EE00	BULB HIGH INTENSITY LAMP # 2500T3/CL
114000056	00	BULB MINIATURE LAMP E250/500
114000057	EE00	BULB LAMP ULTRAVIOLET #SL-36-G
114000058	00	LAMP INCANDESCENT 75WATT GE
114000059	00	INDICATOR CNTRL PNL LED 801082-002
114000060	EE00	LAMP NEON CARTRIDGE
114000061	EE00	LAMP DUAL RING NIKON REPLACEMENT
115000001	00	FAN AXIAL-PAMOTOR 8500
115000002	00	REPLACED BY 115000120
115000003	EE00	MOTOR DISC DRIVE
115000004	00	BLOWER AMCO B-350-25 BS-350 2REQD BHA
115000005	00	FAN ROTRON SARGENT 115V 50/60
115000006	03	MOTOR DRIVE
115000007	01	MOTOR HEAD LOAD
115000008	00	FAN, SKIPPER
115000009	00	MOTOR DRIVE 50 HZ
115000010	01	MOTOR DRIVE 60 HZ DISC 6000
115000011	05	MOTOR CAPSTAN OUTLINE DWG
115000012	05	MOTOR REEL OUTLINE DWG
115000013	00	MOTOR UNMODIFIED 3M103 GRANGER
115000014	05	MOTOR SHADED POLE TRIEM 1012
115000015	00	BLOWER ADPT BRKT
115000016	00	MOTOR FILTER (350 CFM)
115000017	00	MOTOR SCREEN OUTLET (350 CFM)
115000018	00	MOTOR AIR DUCT (350 CFM)
115000019	00	MOTOR ALUM GRILL
115000020	00	BLOWER (350 CFM)
115000021	00	FAN SKIPPER ROTON #SK2A-1
115000022	00	FAN ADAPTER,AIR DUCT
115000023	00	FAN 105 CFM HOWARD #3-90-8010-115V
115000024	02	BLOWER LAMB #115721-0
115000025	03	MOTOR 1/3 HP GE#5KCP19PG285T
115000026	00	BLOWER AUXILLARY
115000027	00	BLOWER AUXILLARY 230V
115000028	02	MOTOR HYSTERESIS SYNCH SPEC
115000029	00	REPLACED BY 115000121
115000030	00	(USE 115-132)
115000031	03	BLOWER SPEC CABINET 115V 50/60HZ
115000032	00	MOTOR MAIN 525836001
115000033	00	MOTOR DRIVE 63002402-1
115000034	00	MOTOR 1.6A 60HZ 182241
115000035	00	MOTOR WIND JAMMER BLOWER 00000541
115000036	00	FAN COOLING 117V 60HZ 20237301
115000037	00	MOTOR ASSY BLOWER 00001093
115000038	00	MOTOR ASSY SP-R 00001101
115000039	00	MOTOR BRUSH DRIVE 91528-001
115000040	00	MOTOR DRUM 800899-001
115000041	00	MOTOR USE 115-110 800264-001
115000042	00	FAN 800131-001
115000043	00	MOTOR 115V 50/60 HZ 150086001
115000044	00	MOTOR 230V 50/60 HZ 150086002
115000045	00	MOTOR DRIVE 900RPM 115V CT381-2
115000046	04	BLOWER SPEC CABINET 230V 50HZ
115000047	00	MOTOR ASSY CC7073-6
115000048	00	MOTOR SPINDLE ASSY DIABLO 15536-02
115000049	00	MOTOR 50/60HZ 115V 327000001
115000050	00	MOTOR HD POS SYS 4 SURF DISK
115000051	00	MOTOR SYNCH SPECIAL 4 SURF DISK
115000052	00	MOTOR RIBBON 801148-001
115000053	00	MOTOR DRUM MOTOR 800954-001
115000054	00	MOTOR USE 115-115 235145-001
115000055	00	MOTOR BLOWER(USE 115-145) 801117-001
115000056	00	MOTOR 181870
115000057	EE00	MOTOR DRIVE 60HZ
115000058	EE00	MOTOR DRIVE 50HZ
115000059	00	MOTOR 60HZ BRPE-11 TTY 151795
115000060	00	MOTOR DRUM 93030-001
115000061	00	MOTOR FAN ASSY 32810000
115000062	00	MOTOR DRIVE MOTOR ASSY 30136703
115000063	00	MOTOR PICK MOTOR ASSY 30136805
115000064	00	(USE 115-61) 32810000
115000065	00	BLOWER AIR COND 115V 60HZ
115000066	00	BLOWER HEAT EXCHANGER 115V 50/60HZ
115000067	01	MOTOR NOVADISC DRIVE 6004-1,-2
115000068	01	MOTOR NOVADISC DRIVE 6004
115000069	02	BLOWER HEAT EXCHANGER 230V 50/60HZ
115000070	02	BLOWER AIR COND 230V 50/60HZ
115000071	00	MOTOR BLOWER CDS 114 91185-001
115000072	00	MOTOR SPINDLE ASSY 97721-003
115000073	00	MOTOR BRUSH MOTOR 16023
115000074	00	MOTOR SPINDLE ASSY 16117-12
115000075	00	(USE 002-3715) 16099
115000076	00	MOTOR USE 115-126 72801106
115000077	00	(USE 103-329) 75039701
115000078	00	MOTOR USE 115-124 72801103
115000079	00	REPLACED BY 115000121
115000080	01	BLOWER 3 PHASE 208V HI-PERF
115000081	00	FAN PEWEE BOXER PWS2107FL
115000082	EE00	MOTOR HYSTERESIS SYNC 4 SURF CTG DISKO
115000083	EE00	MOTOR DR INDUCTION PC26A18CRO
115000084	00	MOTOR DRIVE 60HZ 120V 75291911
115000085	00	MOTOR DRIVE 50HZ 220V 75291912
115000086	00	MOTOR USE 118-662 75747802
115000087	04	BLOWER RADIAL 60HZ CTG DISK 4 SURF

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115000088 through 116000085

PART NO.	REV	DESCRIPTION
115000088	02	BLOWER RADIAL 50HZ 4 SURF CTG DISK
115000089	05	MOTOR TIMING 24VAC 3W CRAMER
115000090	02	MOTOR 3 PHASE AC INDUCTION ZEBRA
115000091	00	MOTOR FILE REEL ASSY 201087
115000092	00	MOTOR FIXED REEL ASSY 201088
115000093	00	MOTOR CAPSTAN/TACH ASSY 201089
115000094	00	MOTOR VAC BLOWER ASSY 115 201104
115000095	00	MOTOR VAC BLOWER ASSY 230 200912
115000096	00	MOTOR VACUUM MOTOR 115V 100259
115000097	00	MOTOR VACUUM MOTOR 230V 100375
115000098	00	MOTOR FAN 100380
115000099	01	MOTOR AC IND GEARMOTOR W/CLUTCH S2M
115000100	EE00	MOTOR PPR FEED M061DF03
115000101	EE00	MOTOR CARR DRIVE M062ED04
115000102	00	FAN 525321001
115000103	00	MOTOR FORM FEED 525319001
115000104	01	MOTOR RIBBON D3C-DD 100RPM
115000105	00	MOTOR DRIVE 50HZ 100V 75291914
115000106	00	MOTOR DRIVE 50HZ 240V 75727510
115000107	EE00	MOTOR SHADED POLE 1575
115000108	00	MOTOR STEPPING 15 DEG M061-DF-305
115000109	00	MOTOR STEPPING 5 DEG M062-ED-304
115000110	00	MOTOR AC 800264-001
115000111	EE00	BLOWER CAB, SIDE DISCHARGE
115000112	00	BLOWER, AIR IN/OUT K2THE500
115000113	00	BLOWER, CONDENSER 230V K2CC476
115000114	00	BLOWER, EVAPORATOR 230V K2CE476
115000115	00	MOTOR TACH GEAR 801040-001
115000116	04	MOTOR SGL PHASE IND
115000117	00	(USE 115-37) 00001093
115000118	00	MOTOR DRIVE 115V 60HZ 30136701
115000119	00	MOTOR PICK 115V 50/60 HZ 10150802
115000120	02	BLOWER TUBE-AXIAL 4 11/16" MED-PERFRM
115000121	02	BLOWER TUBE-AXIAL 4 11/16" HI-PERFORM
115000122	00	MOTOR REEL ASSY 200182
115000123	00	MOTOR CAPSTAN 200079
115000124	00	MOTOR DR 92MB 60HZ 77430700/77440100
115000125	00	MOTOR DR 100V 50MHZ 75291926
115000126	00	MOTOR DRIVE 50HZ 77440101
115000127	00	BLOWER MOTOR 50HZ 00001092
115000128	00	MOTOR DRIVE 115V 50HZ 10147401
115000129	02	BLOWER BELT DRIVEN PAGING DISC
115000130	03	MOTOR SGL PHASE INDUCTION, PAGING DSK
115000131	02	BLOWER 4 11/16" HI-PERF 230V TUBE-AXL
115000132	00	FAN GUARD 6-182-039
115000133	03	BLOWER CROWNED PULLEY K-27881-CP
115000134	00	MOTOR STEPPER MM-83
115000135	EE00	BLOWER 30" CAB E500
115000136	00	DUPLICATE SEE 115000135
115000137	00	MOTORASSY BLOWER 2850RPM 00001091
115000138	00	MOTOR ASSY 115/230 50/60 00001098
115000139	00	FAN MOTOR 3730-713
115000140	00	MOTOR PAPER FEED 801325-002
115000141	EE00	MOTOR STEPPING, CARR DRIVE 5 DEGREE
115000142	04	BLOWER 19" CAB, PLATE MNT 200,20,40V
115000143	02	BLOWER 19" CAB,PLATE MNT, 115V 50/60
115000144	01	BLOWER 30" CAB 200V 220V 240V 50/60HZ
115000145	00	MOTOR BLOWER 2230/2260 801346-001
115000146	02	BLOWER 19" CAB PL MTD MULTITAP F250/3
115000147	02	MOTOR STEPPING 7.5DEG PUR ASSY
115000148	00	FAN
115000149	00	FAN SKELETAL DUAL V 22 C.F.M. 50/60HZ
115000150	EE00	FAN SKELETAL 70 CFM 120V 50/60HZ
115000151	00	FAN TUBE-AXIAL 70 CFM
115000152	04	BLOWER 60 HZ 50 MB ZEBRA
115000153	00	BLOWER MTR ASSY 75025200
115000154	00	FAN 70 CFM TUBE AXIAL 115V 50/60HZ
115000155	00	MOTOR STEPPING 2.5 DEGREE
115000156	01	BLOWER HIGH PERFORMANCE 50HZ ZEBRA
115000157	00	MOTOR INDUCTION A.C. SINGLE PHASE
115000158	EE00	MOTOR IND SGL PHASE EXTENDED SHAFT
115000159	01	MOTOR IND EXTENDED SHAFT MULTI-VOLT
115000160	EE00	MOTOR IND MULTI-VOLT EXPAND CAPACITY
115000161	03	MOTOR,DC STEPPING 4PH PERM MAG 1.8
115000162	00	FAN TUBE-AXIAL 3 1/8"SQ AIR MVG DVC
115000163	00	BLOWER MED PRFM 5" 115V AIR MVG TBAX
115000164	00	MOTOR ARCS 2290 801150-001
115000165	01	BLOWER ASSY 50HZ ZEBRA
115000166	02	BLOWER 19"CAB PLATE MTG 6POLE DUAL V
115000167	01	BLOWER CAB 30" 170-264V 50/60HZ
115000168	00	BLOWER TUBE-AXIAL BALL BRG 4 11/16"
115000169	00	FAN TUBE AXIAL 3 1/8"SQ 115V
115000170	00	MOTOR PAPER PULLER 2290 247587-001
115000171	00	MOTOR W/CAP ASSY 100/115V 50747-0
115000172	00	MOTOR W/CAP ASSY 230V 50748-0
115000173	00	MOTOR 50HZ 117V TAPE DRIVE BLOWER
115000174	EE00	MOTOR CAPSTAN
115000175	EE00	MOTOR REEL
115000176	00	MOTOR RIBBON DRIVE 2550 239343-001
115000177	00	MOTOR BAND DRIVE 2550 801071-001
115000178	00	MOTOR RIBBON DESKEW 245295-001
115000179	00	MOTOR PAPER PULLER 2550 801355-001
115000180	EE00	MOTOR SGL PHASE INDUCTOR
115000181	EE00	BLOWER ASSY 50/60 HZ
115000182	01	FAN AIR MOVE 119.1(4.69)SQ 115V 50CFM
115000183	00	FAN B300 246039-001
115000184	00	MOTOR BAND MTR ASSY B300 246164-002
115000185	00	MOTOR PAPER FEED 246200-004
115000186	00	MOTOR CARRIAGE ASSY D16XX 40715-02
115000187	00	MOTOR PAPER FEED D16XX 24283
115000188	00	FAN 115V D16XX 14011-02
115000189	01	FAN TUBE AXIAL 230V 50CFM
115000190	00	MOTOR RIBBON ADVANCE 24427
115000191	00	FAN 804-020247-GRP-A
115000192	01	MOTOR REEL
115000193	00	MOTOR LF ASSY 136-031585-A
115000194	00	MOTOR SPACING ASSY 136-031583-A
115000195	EE00	MOTOR STEPPING 7.5
115000196	EE00	MOTOR, REEL, 75 IPS TP DR
116000001 *	02	CKT MOD 8789 ADC 12 QM/BIN/SN
116000002 *	01	CKT MOD 8788 DAC 12QZ-BIN
116000003 *	01	CKT MOD BPM 15/150-D5 PS-2402
116000004 *	03	CKT MOD 8790 SHA1A
116000005	00	CKT MOD PS 2405
116000006 *	00	CKT MOD 10Z-3
116000007 *	02	CKT MOD ADC 10 QU
116000008	00	CKT MOD POWER DRIVER 63002242
116000009	00	CKT MOD USE 116-253 63002302-1
116000010	00	CKT MOD USE 116-253 63002302-2
116000011	00	CKT MOD CARD #2 MOD A 63002303-1
116000012	00	CARD #2 USE 116-11 63002303-2
116000013	00	CKT MOD BOARD J-1 11981
116000014	00	CKT MOD BOARD J-2 11111
116000015	00	CKT MOD BOARD J-3 11026
116000016	00	CKT MOD BOARD J-8 11085
116000017	00	CKT MOD BOARD J-9 11071
116000018	00	CKT MOD BOARD J-10 11082
116000019	00	CKT MOD USE 116-293 181A23
116000020	00	CKT MOD CLOCK CARD 400765-03
116000021	00	CKT MOD CNTRL CARD 400619-07
116000022	00	CKT MOD ERROR CARD 400610-07
116000023	00	CKT MOD SYNCH CARD 40035301
116000024	00	CKT MOD XTEND CARD 30099501
116000025	00	CKT MOD BOARD AF-10 90202-001
116000026	00	CKT MOD BOARD AF-11 90206-001
116000027	00	CKT MOD BOARD AF-13 91069-001
116000028	00	CKT MOD BOARD AL-10 90210-001
116000029	00	CKT MOD BOARD AL-11 90246-001
116000030	00	CKT MOD BOARD AL-12 90258-001
116000031	00	CKT MOD BOARD AL-13 90222-001
116000032	00	CKT MOD BOARD AL-14 90226-001
116000033	00	CKT MOD BOARD AL-15 90218-001
116000034	00	CKT MOD BOARD AL-16 90230-001
116000035	00	CKT MOD BOARD AL-19 91089-001
116000036	00	CKT MOD BOARD AN-11 90254-001
116000037	00	CKT MOD BOARD AN-14 91073-001
116000038	00	CKT MOD BOARD AP-14 90559-001
116000039	00	CKT MOD USE 116-44 90680-001
116000040	00	CKT MOD BOARD AP-21 91093-001
116000041	00	CKT MOD USE 116-256 91101-001
116000042	00	CKT MOD BOARD AP-25 91109-001
116000043	00	CKT MOD BOARD AP-28 91826-001
116000044	00	CKT MOD BOARD DP-52 13150-001
116000045	00	CKT MOD BOARD AP-39 94081-001
116000046	00	CKT MOD BOARD AP-47 97740-001
116000047	00	CKT MOD BOARD AR-12 90383-001
116000048	00	CKT MOD BOARD AR-16 91126-001
116000049	00	CKT MOD BOARD AR-17 91122-001
116000050	00	CKT MOD BOARD AR-18 91057-001
116000051	00	CKT MOD BOARD AR-19 91061-001
116000052	00	CKT MOD USE 116-254 91065-001
116000053	00	CKT MOD BOARD AT-10 90266-001
116000054	00	CKT MOD BOARD AX-10 90262-001
116000055	00	CKT MOD BOARD AZ-10 EXT 90557-001
116000056	00	CKT MOD BOARD AP-10 90306-001
116000057	00	CKT MOD REGULATOR ASSY 200495
116000058	00	CKT MOD DATA ELECT MRZI 200521-012
116000059	00	CKT MOD CARD AZ-18 212470-001
116000060	00	CKT MOD CARD AS-13 212475-001
116000061	00	CKT MOD CARD AZ-84 216525-001
116000062	00	(USE 116-72) 233715-001
116000063	00	CKT MOD CARD AP-10 212480-001
116000064	00	CKT MOD CARD AJ-14 216005-001
116000065	00	CKT MOD CARD AZ-78 216200-001
116000066	00	CKT MOD CARD AK-10 213060-001
116000067	00	CKT MOD CARD AG-32 217195-001
116000068	00	CKT MOD CARD AG-18 212525-001
116000069	00	CKT MOD CARD AG-17 212520-001
116000070	00	CKT MOD CARD AV-10 212495-001
116000071	00	CKT MOD CARD AH-10 212465-001
116000072	00	CKT MOD CARD AM-21 233715-001
116000073	00	CKT MOD AZ-15 216525-001/212490-001
116000074	00	CKT MOD CARD AZ-19 212500-001
116000075	00	CKT MOD CARD AT-13 212510-001
116000076	00	CKT MOD CARD AG-45 233920-001
116000077	00	CKT MOD CARD AG-20 212535-001
116000078	00	CKT MOD CARD AG-29 215035-001
116000079	00	CKT MOD CARD AL-32 230420-001
116000080	00	CKT MOD EXTENDER BD 800580-001
116000081	00	CKT MOD CARD AZ-49 215285-001
116000082	00	CKT MOD CARD AZ-51 215290-001
116000083	00	CKT MOD CARD AZ-79 216205-001
116000084	00	(USE 116-46) 97740-001
116000085	00	CKT MOD TRANS ELECT NRZI 200488-012

* Denotes drawings that follow the 116 listings.

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116000086 through 116000279

PART NO.	REV	DESCRIPTION	
116000086	00	CKT MOD 4080 CSST	200004101
116000087	00	CKT MOD PHOTO HEAD ASSY	DCR0079-1
116000088	00	CKT MOD CIRCUIT BOARD	DQ63-1
116000089	00	CKT MOD PRINTED CKT BOARD	DQ62-1
116000090	00	CKT MOD TV MONITOR	00237-00
116000091	00	CKT MOD KEYBOARD	01047-001
116000092	00	CKT MOD POWER SUPPLY 60HZ	00599-G03
116000093	00	CKT MOD MEMORY 7 BIT	00717-G04
116000094	00	CKT MOD SERIAL INTERFACE	00880-G01
116000095	00	CKT MOD TIMING/CONT 60HZ	00846-G01
116000096	00	CKT MOD MEMORY CONTROL	00557-G01
116000097	00	CKT MOD VIDEO GENERATOR	00563-G01
116000098	00	CKT MOD FF12	110100001
116000099	00	CKT MOD BD & INVERT 12	110110201
116000100	00	CKT MOD COUNTER	110117901
116000101	00	CKT MOD READER CONTROL	110124901
116000102	00	CKT MOD CURRENT DRIVER	111037301
116000103	00	CKT MOD COUNT DECODER	111037401
116000104	00	CKT MOD CARD AC-16 2440	218015-001
116000105	00	CKT MOD CARD AC-17 2440	218020-001
116000106	00	CKT MOD CARD AG-33 2440	217980-001
116000107	00	CKT MOD CARD AG-34 2440	218045-001
116000108	00	CKT MOD CARD AG-37 2440	217105-001
116000109	00	CKT MOD CARD AG-44 2440	233125-001
116000110	00	CKT MOD CARD AH-22 2440	217970-001
116000111	00	CKT MOD CARD AH-25 2440	231750-002
116000112	00	CKT MOD CARD AL-23 2440	218630-001
116000113	00	CKT MOD CARD AL-25 2440	218490-001
116000114	00	CKT MOD CARD AM-16 2440	217975-001
116000115	00	CKT MOD CARD AP-15 2440	217985-001
116000116	00	CKT MOD CARD AP-17 2440	219805-001
116000117	00	(USE 116-302)	242710-001
116000118	00	CKT MOD CARD AS-26 2440	218010-001
116000119	00	CKT MOD CARD AS-40 2440	231445-001
116000120	00	CKT MOD CARD AT-24 2440	218030-001
116000121	00	CKT MOD CARD AV-17 2440	218005-001
116000122	00	CKT MOD CARD AV-18 2440	233020-001
116000123	00	CKT MOD CARD AZ-111 2440	217995-001
116000124	00	CKT MOD CARD AZ 113 2440	217990-001
116000125	00	CKT MOD CARD AZ-115 2440	218025-001
116000126	00	CKT MOD CARD AZ-116 2440	218035-001
116000127	00	(USE 116-303)	242710-002
116000128	00	CKT MOD CARD AZ-126 2440	218485-001
116000129	00	CKT MOD CARD AV-21 2440	236145-001
116000130	00	CKT MOD USE 116-313	240817-001
116000131	00	CKT MOD SERVO BOARD	235645-001
116000132	00	CKT MOD HAMMER DR BD	238005
116000133	00	CKT MOD USE 116-314	235030-001
116000134	00	CKT MOD USE 116-298	235612-001
116000135	00	CKT MOD USE 116-315	241442-001
116000136	00	CKT MOD EXTENDER BOARD	00259-G01
116000137	00	CKT MOD CARD AZ-167	215565-001
116000138	00	CKT MOD CARD AR-25	214550-001
116000139	00	CKT MOD CARD AR-16	214555-001
116000140	00	CKT MOD CARD AT-18	214560-001
116000141	00	CKT MOD CARD AG-22	214565-001
116000142	00	CKT MOD CARD AG-23	214575-001
116000143	00	CKT MOD CARD AZ-94	216690-001
116000144	00	CKT MOD CARD AC-15	217395-001
116000145	00	CKT MOD CARD AR-15	214570-001
116000146	00	CKT MOD CARD AZ-55	215500-001
116000147	00	CKT MOD TRANSPORT ELECT	3125829-01
116000148	00	CKT MOD DATA ELECTRONICS	3125610-01
116000149	00	CKT MOD SERVO AMPLIFIER	3129400-01
116000150	00	CKT MOD TTY CARD	184168
116000151	00	CKT MOD PWR SUPPLY ASSY	30124001
116000152	00	CKT MOD PC ASSY EXTENDER	30126101
116000153	00	CKT MOD 115V PWR SUPPLY	40107001
116000154	00	CKT MOD 12V PWR SUPPLY	00000750
116000155	00	CKT MOD RD/LIT STATION	20154401
116000156	00	CKT MOD PCB ASSY	401143-02
116000157	00	CKT MOD POWER SUPPLY RDR	183087
116000158	00	USE 116-294	
116000159	00	USE 118-201	
116000160	00	USE 118-201	
116000161	00	CKT MOD MAIN CHASSIS BD	6-002-0530
116000162	00	CKT MOD BOARD VP-11	92639-001
116000163	00	CKT MOD ADDRESS #1 AL-1	11404-20
116000164	00	CKT MOD ADDRESS #2 AL-2	11407-20
116000165	00	CKT MOD SERVO BOARD SO	11633-20
116000166	00	CKT MOD SENSOR CKT SR	11411-01
116000167	00	CKT MOD OSCILLATOR OR	11873-01
116000168	00	CKT MOD SPINDLE DR SD	11613-00
116000169	00	CKT MOD HEAT SINK HS	16939
116000170	00	CKT MOD READ/WRITE RW	11486-20
116000171	00	CKT MOD SEQUENCE SL	11471-XX
116000172	00	CKT MOD CIRCUIT BD RDR-1	11431-XX
116000173	00	CKT MOD CIRCUIT PD RDR-2	11647-00
116000174	00	CKT MOD SECTOR CNTR SC	11459
116000175	00	CKT MOD SEPARATOR D/CS	11637-01
116000176	00	CKT MOD EXTENDER BOARD	11427
116000177 *	01	CKT MOD DIFF A=1 OR 2	
116000178 *	01	CKT MOD PROG DIFF AMP	
116000179	EE00	CKT MOD CONDUCTOR NETWORK	(D/P)
116000180	EE00	CKT MOD CONDUCTOR NETWORK	(DUAL D/P)
116000181	00	CKT MOD BOARD AX-14 D	93062-001
116000182	00	CKT MOD USE 116-255	93146

PART NO.	REV	DESCRIPTION	
116000183	00	OBSOLETE SEE 121000034	
116000184	00	REPLACED BY 121000035	
116000185	00	CKT MOD COND NET 16 PIN DIP	
116000186	00	CKT MOD CARD DZPN	72829612
116000187	00	CKT MOD CARD 2JYV	54258900
116000188	00	CKT MOD CARD 2FZV	54229301
116000189	00	CKT MOD CARD 1FWV	54228100
116000190	00	CKT MOD CARD 2FVV	54227701
116000191	00	CKT MOD CARD 4FUV	54227306
116000192	00	CKT MOD CARD CFRV	54226107
116000193	00	CKT MOD CARD DFPV	54225305
116000194	00	CKT MOD CARD 2FNV	54224901
116000195	00	CKT MOD CARD AFMV	54224503
116000196	00	CKT MOD CARD 1FLV	54224100
116000197	00	CKT MOD CARD AFJV	54223302
116000198	00	CKT MOD CARD 3EJV	54213301
116000199	00	CKT MOD CARD BWZV	54199304
116000200	00	CKT MOD CARD AWMV	54194501
116000201	00	CKT MOD CARD 1WMV	54194500
116000202	00	CKT MOD CARD 0WDV	54191300
116000203	00	CKT MOD CARD 0WCV	54190900
116000204	00	CKT MOD CARD 1WBV	54190501
116000205	00	CKT MOD CARD 0WAV	54190100
116000206	00	CKT MOD CARD 4UCV	54170901
116000207	00	CKT MOD CARD 1TCV	54160901
116000208	00	CKT MOD CARD CSAV	54150104
116000209	00	CKT MOD CARD 1RCV	54140901
116000210	00	CKT MOD CARD AQZV	54139301
116000211	00	CKT MOD CARD 3PBV	54120501
116000212	00	CKT MOD CARD 1CVV	54117701
116000213	00	CKT MOD CARD CCUV	54117306
116000214	00	CKT MOD CARD 3CTV	54116906
116000215	00	CKT MOD CARD 0CSV	54116501
116000216	00	CKT MOD CARD ECGV	54112507
116000217	00	CKT MOD CARD 1ATV	54096900
116000218	00	CKT MOD CARD 1ALV	54094100
116000219	00	CKT MOD CARD AAHV	54092901
116000220	00	CKT MOD CARD AAFV	54092102
116000221	00	CKT MOD MATCHED SET CARDS	73482300
116000222	00	CKT MOD OBSOLETE 4XCN	73484800
116000223	00	CKT MOD CARD 3ZCN	75183600
116000224	00	CKT MOD OBSOLETE 1AJV	54093300
116000225	00	(USE 116-319)	75179800
116000226	00	CKT MOD REGULATOR -5V	75184100
116000227	00	CKT MOD SERVO PREAMP	73485301
116000228	00	CKT MOD OBSOLETE ABPV	54105301
116000229	00	CKT MOD OBSOLETE ABZN	54109301
116000230	00	CKT MOD OBSOLETE 2WGV	54192502
116000231	00	CKT MOD OBSOLETE 1WHV	54192901
116000232	00	CKT MOD EXTENDER 1/2 SIZE	54099700
116000233	00	CKT MOD EXTENDER FULL	54109700
116000234	00	CKT MOD ALIGNMENT CARD	87007900
116000235	00	CKT MOD CARD DFSV	54226505
116000236	00	CKT MOD USE 116-313	240817-004
116000237	00	CKT MOD USE 116-300	237745-001
116000238	01	REPLACED BY 005007668	
116000239	00	CKT MOD FLEX DISC PCB	75865206
116000240	00	CKR MOD CB PANEL	11499
116000241	00	CKT MOD LOW PASS FLTR F119	
116000242	00	CKT MOD DATA ELECTRONICS	201142-016
116000243	00	CKT MOD TRANS ELECTRONICS	201004-004
116000244	00	CKT MOD POWER SUPPLY ASSY	201049
116000245	00	CKT MOD PWR SUPP REG ASSY	200993-001
116000246	00	CKT MOD WRITE DATA ASSY	201276
116000247	00	CKT MOD SERVO ELECT ASSY	200974-001
116000248	00	CKT MOD USE 002-5292	200882-003
116000249	00	CKT MOD USE 002-5293	201096-003
116000250	00	CKT MOD P/S	233154-001
116000251	00	CKT MOD CD, MTR CTL	63011130
116000252	00	CKT MOD USE 116-253	63002302-2F
116000253	00	CKT MOD CARD #1 REV #40	63002302-1F
116000254	00	CKT MOD BD DR-53	13144-001
116000255	00	CKT MOD BOARD DP-56	14856-001
116000256	00	CKT MOD BOARD DP-57	14891-001
116000257 *	01	CKT MOD A/D CONV 12 BIT, HI-SPEED	
116000258	EE00	CKT MOD D/A CONV 10 BIT CURRENT	
116000259 *	01	CKT MOD D/A CONV,12BIT,CURR,HYBRID	
116000260	01	CKT MOD PREC VLTG REF, MONOL AD2700L	
116000261	01	CKT MOD AD7520LN DAC, CMOS, 10 BIT	
116000262	00	CKT MOD USE 116-316	237605-001
116000263	00	CKT MOD USE 116-304	237590-001
116000264	00	CKT MOD REGULATOR PCB	237580-001
116000265	00	USE 116000291	
116000266	00	USE 116000292	
116000267	00	CKT MOD AFNV	5422490501
116000268	00	CKT MOD PC ASSY MARK SENS	40139806
116000269	00	CKT MOD P/S 115V MARK SEN	30127201
116000270	00	CKT MOD PT LGC PCB	40114301
116000271	00	CKT MOD XPORT ELEC PCB	201378
116000272	00	CKT MOD DATA ELEC PCB	200566-004
116000273	00	(USE 116-45)	94081-001
116000274	00	CKT MOD USE 116-254	13144-001
116000275	00	CKT MOD USE 116-256	14891-001
116000276	00	CKT MOD INPUT BUFFER BD	1-30
116000277	00	CKT MOD STEPPER DR BOARD	1-37
116000278	00	CKT MOD OSC/SEQUENCE BD	6520-108
116000279	00	CKT MOD PEN LIFT BOARD	1-33

* Denotes drawings that follow the 116 listings.

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116000280 through 116000422

PART NO.	REV	DESCRIPTION
116000280	00	CKT MOD HI SPEED STPPPER 1-319
116000281	00	CKT MOD SR PCB REV M 11411-01
116000282	00	CKT MOD USE 116-296 237675-001
116000283	00	CKT MOD OM PICK PCB 400881XX
116000284	00	CKT MOD OM ERROR PCB 400899XX
116000285	00	CKT MOD OM CONTROL PCB 400889XX
116000286	00	CKT MOD OM DATA PCB 40087201
116000287	00	CKT MOD DATA ELECT PE 200692-003
116000288	00	CKT MOD TRANS ELECT PE 200632-003
116000289	03	CM DC TO DC CONV 200Z604S
116000290	01	CKT MOD D-C TO D-C CONV 200Z6255
116000291	01	CKT MOD SYNC CARD 400353-05
116000292	01	CKT MOD SYNC CARD 400353-03
116000293	00	CKT MOD MAGNET DR PCB 181821
116000294	00	CKT MOD XFMR ASSY 6-0030320
116000295	00	CKT MOD (USE 116-312) 237748-011
116000296	00	CKT MOD HAMMER BANK SUP 237865-001
116000297	00	CKT MOD (USE 116-312) 237748-012
116000298	00	CKT MOD CONTROL PNL PLB 241520-001
116000299	00	CKT MOD P/S PCB (6052) 84V25019A2
116000300	00	CKT MOD VFU PCB 5172W 238044-001
116000301	01	CKT MOD 12 BIT D/A CONV
116000302	00	CKT MOD CARD AP-33 242710-001
116000303	00	CKT MOD CARD AP-34 242710-002
116000304	00	CKT MOD SERVO PCB 237880-001
116000305	00	CKT MOD HMR DRVR BP 2230 236790-001
116000306	00	CKT MOD HMRDRV BP-UPR2260 237595-001
116000307	00	CKT MOD HMRDRV BP-LWR2260 237600-001
116000308	00	CKT MOD PPR FD EMTTR 2260 237640-001
116000309	00	CKT MOD PPR FD SENSR 2260 237635-001
116000310	01	CM AD363 HYBRID DATA ACQ FR END
116000311	01	CM AD363-2 12 BIT HYBRID A/D CONV
116000312	00	CKT MOD DAVFU 2230/2260 243269-012
116000313	00	CKT MOD LOGIC PCB 2230 244708-001
116000314	00	CKT MOD REGULATR PCB 2230 238030-001
116000315	00	CKT MOD T/O HARNESS PCB 240845-001
116000316	00	(USE 116-326) 237628-001
116000317	00	CM 250V 30MA DC TO DC CONV POS
116000318	01	CM +100-100V 25MA DC TO DC CONV POS
116000319	00	CKT MOD +5V REGULATOR 75179802
116000320	00	CKT MOD BRAKE LOGIC ASSY 200518
116000321	00	CKT MOD 5365 CNTRLLR PCB 27010
116000322	00	CKT MOD ANALOG PCB 5365 21950-1
116000323	00	CKT MOD DIGITAL LOGIC PCB 21955-1
116000324	00	CKT MOD ERROR CARD M400 400610-08
116000325	00	CKT MOD CLOCK CARD M400 400765-04
116000326	00	CKT MOD LOGIC PCB 2260 244706-001
116000327	00	CKT MOD IO CHAR CIO 241442-001
116000328	00	CKT MOD HMRDRVR BP 2230AB 235090-001
116000329	00	CKT MOD SERVO PCB 2290 241975-002
116000330	00	CKT MOD AC DISTR 2230 236847-001
116000331	00	CKT MOD FLSS (USE 118-693) 237407-001
116000332	00	CKT MOD REGULATOR PCB /90 238125-001
116000333	00	CKT MOD ACT RIBBON CNTRL 237650-001
116000334	00	CKT MOD ARC RIBBON SENSOR 237655-002
116000335	00	CKT MOD ARC CAM SENSOR 237950-001
116000336	00	CKT MOD TP CNTRL VFU PCB 243371-017
116000337	00	CKT MOD PRGRMBL VFU PCB 243371-112
116000338	00	CKT MOD MICROPROCESSOR/90 246735-003
116000339	00	CKT MOD LOGIC PCB 2230 247425-001
116000340	00	CKT MOD LOGIC PCB 2260 247464-001
116000341	00	CKT MOD IO PCB 64 CHAR 247355-001
116000342	00	CKT MOD IO PCB 96 WO VFU 244540-001
116000343	00	CKT MOD IO PCB 96 W/VFU 247420-001
116000344	00	CKT MOD PRINT PROCESSOR 246735-003
116000345	00	CKT MOD PRGRMBL VFU 251407-057
116000346	00	CKT MOD PPRTP PROGRMBL VFU 251407-017
116000347	00	CKT MOD 850 R/W PCB 25067-3
116000349	00	CKT MOD DAVFU CNTRL IV 245185-001
116000350	00	CKT MOD VOLTAGE REG AV-ZZ 240520-001
116000351	00	CKT MOD PPR FEED AMPAP-33 236310-001
116000352	00	CKT MOD CHAR COUNTR AC-25 236405-001
116000353	00	CKT MOD COLUMN CNTR AC-29 236595-001
116000354	00	CKT MOD DATA COMPAR AC-36 245180-001
116000355	00	CKT MOD AUX LOGIC 111AGR9 242935-001
116000356	00	CKT MOD MASTER CLR AG-101 244315-001
116000357	00	CKT MOD AUX CONTROL AG105 245170-001
116000358	00	CKT MOD IF RCVR/DRV AL-62 238160-001
116000359	00	CKT MOD OCP RCV/DRV AL-86 247210-00
116000360	00	CKT MOD CNTRL LOGIC AP-25 236620-00
116000361	00	CKT MOD AC MTR CNTRL AP29 236960-00
116000362	00	CKT MOD HMR CONTROL AP-35 245160-00
116000363	00	CKT MOD LINE BUFFER AR-45 236340-00
116000364	00	CKT MOD BAND IDNTFR AR-57 244290-00
116000365	00	CKT MOD MODE REGIS AR-59 244300-00
116000366	00	CKT MOD DATA REGIS AR-61 244340-001
116000367	00	CKT MOD HMR TRIGGER AS-62 243240-004
116000368	00	CKT MOD IO CONTROL AT-60 236570-002
116000369	00	CKT MOD HMR TIME IV AT-56 245165-004
116000370	00	CKT MOD HMR DRIVER AM-28 236115-001
116000371	00	CKT MOD BAND GATE ELECTRN 239470-003
116000372	00	CKT MOD BAND MTR SWCH III 239410-001
116000373	00	CKT MOD PULLER MTR SWCH 247120-001
116000374	00	CKT MOD SELF TEST 2550 236985-002
116000375	00	CKT MOD DAVFU CNTRL V 247265-001
116000376	00	CKT MOD FORMAT MEMORY 244210-001
116000377	00	CKT MOD HMR TRIGGER II 245175-003

PART NO.	REV	DESCRIPTION
116000378	00	CKT MOD CHARAC MEM (053) 238580-045
116000379	00	CM VFV LOGIC AG-103 243245-001
116000380	00	CM TAPE CHANNEL CTL AG-66 236390-001
116000381	00	CM VFV CTL AP 27 236615-001
116000382	00	CM STACKER INTFC 4 AL 83 245340-001
116000383	00	CKT MOD CH MEM AM-31 CBNK 238580-001
116000384	00	CKT MOD CH MEM AM-31FRFLNG252167-001
116000385	00	CM HARN I/O WINCHESTER 257305-001
116000386	00	CM CCA RECTIFIER UNIV 251985-001
116000387	00	CKT MOD TIMING&STATUS B300251155-001
116000388	00	CKT MOD HAMMER DRVR B300 251165-001
116000389	00	CM CCA PWR BD 251990-001
116000390	00	CKT MOD STD RECTIFIERB300 251725-001
116000391	00	CKT MOD MICROPROCESSORB300251770-001
116000392	00	CKT MOD MTHR BD W/RELAYB30251995-001
116000393	00	CKT MOD INTRLK XISTION 256440-001
116000394	00	CM CCA INTFC VFU OPT 256455-002
116000395	00	CKT MOD PRINTWHEEL AMP 40530-08
116000396	00	CKT MOD CARRIAGE AMP 40525-08
116000397	00	CKT MOD SERVO PCB 40520-04
116000398	00	CKT MOD XDUCER PCB 40515-03
116000399	00	CKT MOD LOGIC II PCB 40510-48
116000400	00	CKT MOD HRP 02 PCB 23702
116000401	00	CKT MOD 8080 INTFC 40644-05
116000402	00	CKT MOD MOTHERBOARD 40614-04
116000403	00	CKT MOD XTNDR PCB 1610/20 40539-03
116000404	00	CM CCA INTERFACE 257345-002
116000405	00	CM CCA TIMING & STATUS 257325-001
116000406	00	CMCCA POWER BOARD 257320-001
116000407	00	CM CCA PROCESSOR 257315-001
116000408	00	CM CONTROL PANEL RO 136-440935
116000409	00	CM CURRENT LOOP I/O 136-430575-A
116000410	00	CM R/S MPU G9DWH 136-430989-A
116000411	00	CM MOTHER BOARD G9CUL 136-430872-A
116000412	00	CM SERVO G9CUN 136-430874-A
116000413	00	CM DRIVER G9CUM 136-430873-A
116000414	00	CM REGULATOR G9BMT 136-430570-A
116000415	00	CM POWER SUPPLY 804-020198-GRP-B
116000416	00	CM POWER SUPPLY 230V 8040 20198-003-B
116000417	00	CM PRINT PROCESSOR PCB 251625-003
116000418	00	CM TIMING AND STATUS 257520-001
116000419	EE00	CKT MOD B300 SER INTFC 256585-001
116000420	EE00	CM DPC STANDARD 2260REGULATOR PCB
116000421	EE00	CM DPC STANDARD 2230 REGULATOR PCB
116000422	EE00	CM DPC STANDARD 2290 REGULATOR PCB

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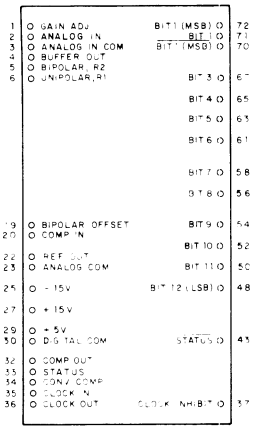
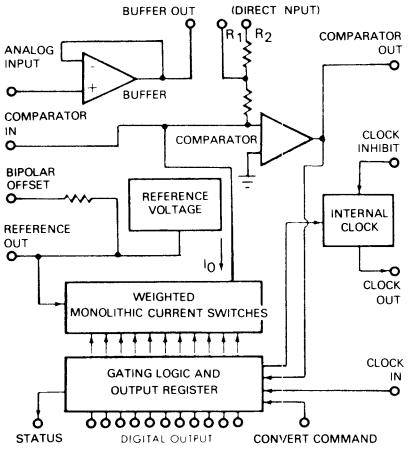
116000001

A/D Converter

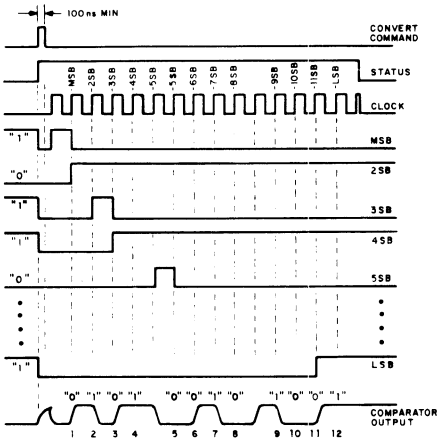
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAM



PIN DESIGNATIONS

Pin No.		Pin No.	
1	Gain Adj.	72	Bit 1 (MSB)
2	Analog In	71	Bit 2
3	Analog In Com	70	Bit 1 (MSB)
4	Buffer Out	69	No pin
5	Bipolar, R2	68	No pin
6	Unipolar, R1	67	Bit 3
7	No pin	66	No pin
8	No pin	65	Bit 4
9	No pin	64	No pin
10	No pin	63	Bit 5
11	No pin	62	No pin
12	No pin	61	Bit 6
13	No pin	60	No pin
14	No pin	59	No pin
15	No pin	58	Bit 7
16	No pin	57	No pin
17	No pin	56	Bit 8
18	No pin	55	No pin
19	Bipolar Offset	54	Bit 9
20	Comp In	53	No pin
21	No pin	52	Bit 10
22	Ref Out	51	No pin
23	Analog Com	50	Bit 11
24	No pin	49	No pin
25	-15V	48	Bit 12 (LSB)
26	No pin	47	No pin
27	+15V	46	No pin
28	No pin	45	No pin
29	+5V	44	No pin
30	Digital Com	43	STATUS
31	No pin	42	No pin
32	Comp Out	41	No pin
33	Status	40	No pin
34	Conv Comm	39	No pin
35	Clock In	38	No pin
36	Clock Out	37	Clock Inhibit

The 116000001 circuit module is a 12-bit binary analog-to-digital converter.

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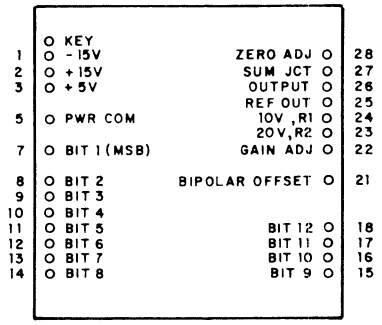
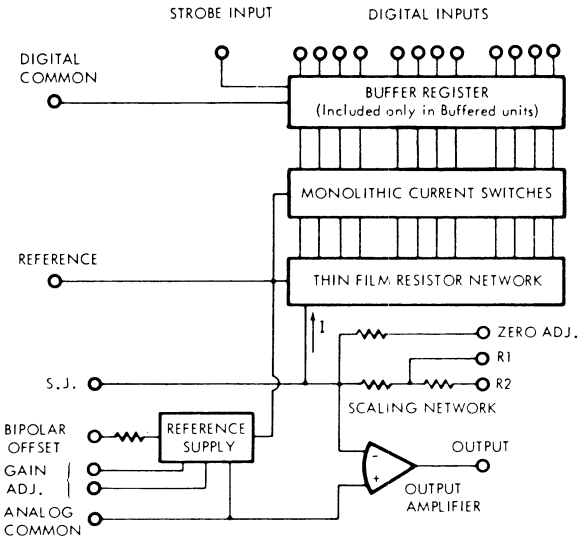
116000002

D/A Converter

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESIGNATIONS

Pin No.	
K	Key
1	-15V
2	+15V
3	+5V
4	No pin
5	Pwr Com
6	No pin
7	Bit 1 (MSB)
8	Bit 2
9	Bit 3
10	Bit 4
11	Bit 5
12	Bit 6
13	Bit 7
14	Bit 8
15	Bit 9
16	Bit 10
17	Bit 11
18	Bit 12
19	No pin
20	No pin
21	Bipolar Offset
22	Gain Adj
23	20V
24	10V
25	Ref
26	Output
27	Sum JCT
28	Zero Adj

The 116000002 circuit module is a 12-bit binary digital-to-analog converter with an externally programmable output amplifier.

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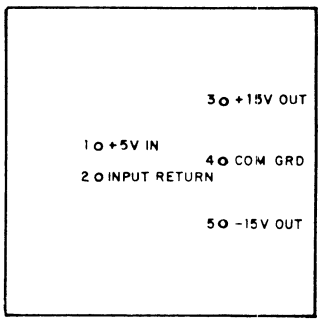
116000003

Power Supply DC/DC

PIN CONFIGURATION

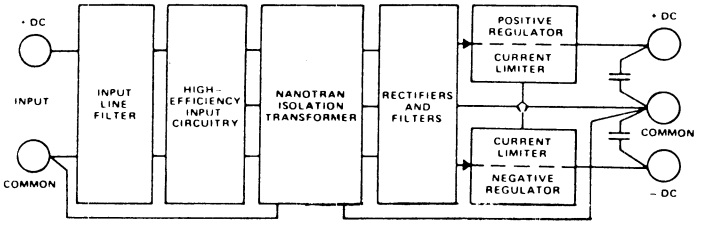


Bottom View

PIN DESIGNATIONS

Pin No.	
1	+5VDC Input
2	Input Return
3	+15VDC Output
4	Common Grd
5	-15VDC Output

BLOCK DIAGRAM



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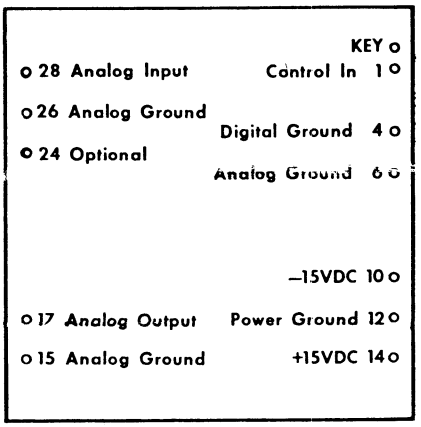
116000004

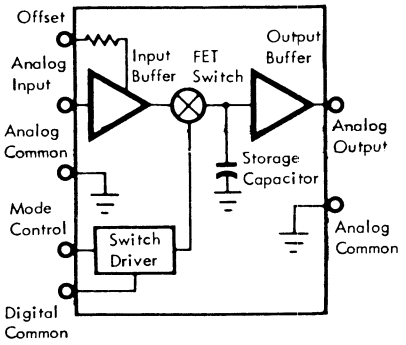
Sample and Hold

PIN CONFIGURATION



Bottom View

BLOCK DIAGRAM



PIN DESIGNATIONS

Pin No.	
K	Key
1	Control In
2	No pin
3	No pin
4	Digital Ground
5	No pin
6	Analog Ground
7	No pin
8	No pin
9	No pin
10	-15VDC
11	No pin
12	Power Ground
13	No pin
14	+15VDC
15	Analog Ground
16	No pin
17	Analog Output
18	No pin
19	No pin
20	No pin
21	No pin
22	No pin
23	No pin
24	Offset (Grd)
25	No pin
26	Analog Ground
27	No pin
28	Analog Input

The 116000004 circuit module is a fast sample-and-hold device with low droop rate and overall accuracy compatible with 12-bit A/D conversion systems operating to 1/2LSB accuracy. This module accepts ±10 volt data, a TTL/DTL and C/MOS compatible control signal, and requires ±15Vdc power.

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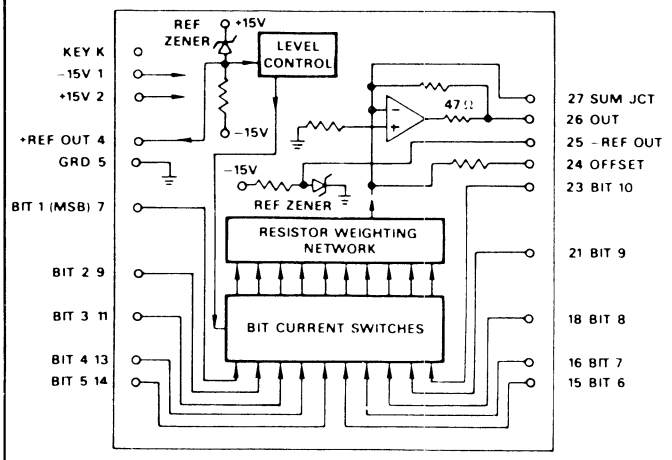
116000006

D/A Converter

PIN CONFIGURATION AND BLOCK DIAGRAM



PIN DESIGNATIONS

Pin No.	
1	-15V
2	+15V
3	No pin
4	+Ref Out
5	Grd
6	No pin
7	Bit 1 (MSB)
8	No pin
9	Bit 2
10	No pin
11	Bit 3
12	No pin
13	Bit 4
14	Bit 5
15	Bit 6
16	Bit 7
17	No pin
18	Bit 8
19	No pin
20	No pin
21	Bit 9
22	No pin
23	Bit 10
24	Offset
25	-Ref Out
26	Out
27	Sum JCT
28	No pin

The 116000006 circuit module is a 10-bit binary, unipolar digital-to-analog converter with a built-in I. C. output amplifier.

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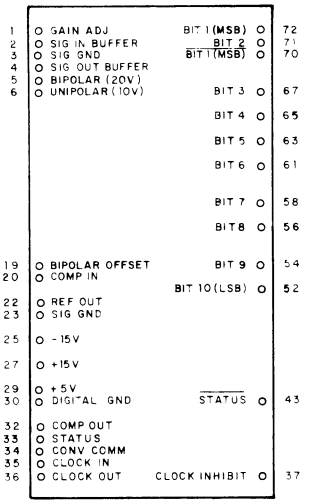
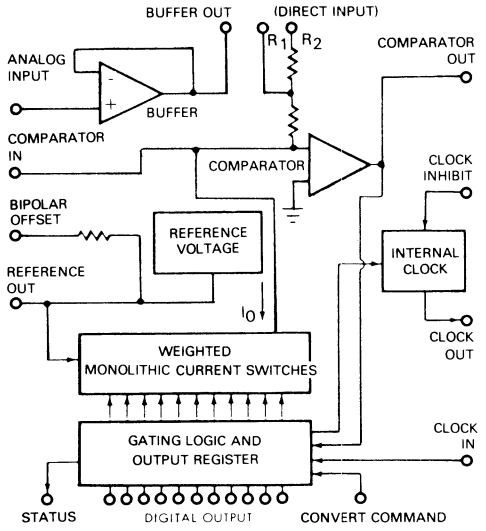
116000007

A/D Converter

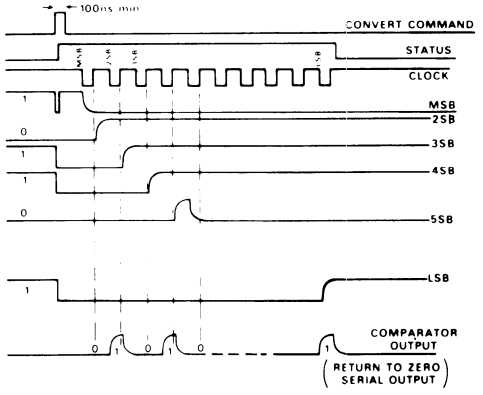
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAM



PIN DESIGNATIONS

Pin No.		Pin No.	
1	Gain Adj.	72	Bit 1 (MSB)
2	Sig. In Buffer	71	Bit 2
3	Sig. Grd	70	$\overline{\text{Bit 1 (MSB)}}$
4	Sig. Out Buffer	69	No pin
5	Bipolar (20V)	68	No pin
6	Unipolar (10V)	67	Bit 3
7	No pin	66	No pin
8	No pin	65	Bit 4
9	No pin	64	No pin
10	No pin	63	Bit 5
11	No pin	62	No pin
12	No pin	61	Bit 6
13	No pin	60	No pin
14	No pin	59	No pin
15	No pin	58	Bit 7
16	No pin	57	No pin
17	No pin	56	Bit 8
18	No pin	55	No pin
19	Bipolar Offset	54	Bit 9
20	Comp. In	53	No pin
21	No pin	52	Bit 10 (LSB)
22	Ref. Out	51	No pin
23	Sig. Grd	50	No pin connection
24	No pin	49	No pin
25	-15V	48	No pin connection
26	No pin	47	No pin
27	+15V	46	No pin
28	No pin	45	No pin
29	+5V	44	No pin
30	Digital Grd	43	$\overline{\text{STATUS}}$
31	No pin	42	No pin
32	Comp. Out	41	No pin
33	Status	40	No pin
34	Conv. Comm.	39	No pin
35	Clock In	38	No pin
36	Clock Out	37	Clock Inhibit

The 116000007 circuit module is a 10-bit binary analog-to-digital converter capable of $\pm$1/2LSB.

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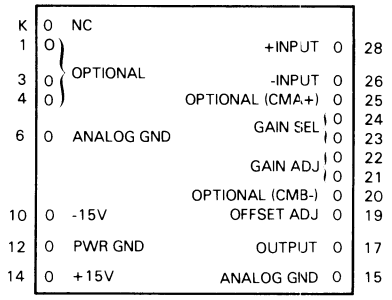
116000177

Instrumentation Amplifier

PIN CONFIGURATION



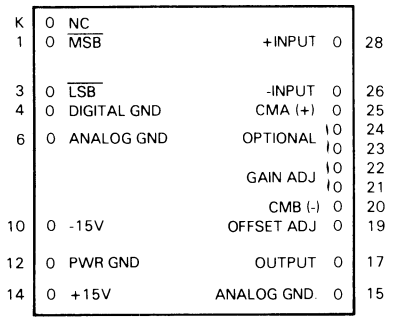
GAIN=1 FOR PINS 23 AND 24 CONNECTED.

GAIN=2 FOR PINS 23 AND 24 OPEN.

116000178

Programmable Differential Amplifier

PIN CONFIGURATION



GAIN SELECTION

$\overline{MSB}$	$\overline{LSB}$	GAIN
1	1	1
1	0	2
0	1	4
0	0	8

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116000257

A/D Converter

PIN CONFIGURATION

1	O GAIN	MSB BIT1	O	72
2	O ANALOG IN	BIT2	O	71
3	O ANALOG OUT	$\overline{\text{MSB}}$ BIT1	O	70
4	O BUFFER OUT			
5	O 20V IN			
6	O 10V IN	BIT3	O	67
		BIT4	O	65
		BIT5	O	63
		BIT6	O	61
		BIT7	O	58
		BIT8	O	56
		BIT9	O	54
19	O BIPOLAR OFFSET			
20	O COMP IN	BIT10	O	52
22	O REF OUT	BIT11	O	50
23	O ANALOG GND			
		LSB BIT12	O	48
25	O -15V			
27	O +15V			
29	O +5V			
30	O DIGITAL	$\overline{\text{STATUS}}$	O	43
			O	42
32	O COMP OUT		O	41
33	O STATUS			
34	O CONV COMM	SPARE PINS*	O	39
35	O CLK IN			
36	O CLK OUT		O	37

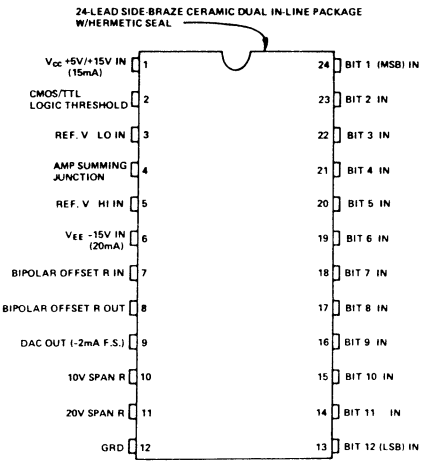
*PIN 37 MAY BE USED FOR CLK INH ON SOME MODULES.
PINS 41 AND 42 MAY BE USED FOR CLOCK ON SOME MODULES.

The 116000257 is a high-speed, 12-bit A/D converter with an optional buffer.

116000259

D/A Converter

PIN CONFIGURATION



The 116000259 is a 12-bit D/A Converter.

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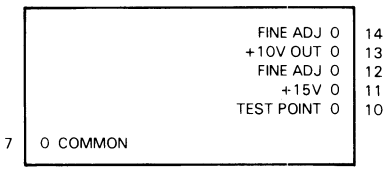
116000260

+10V Precision Reference

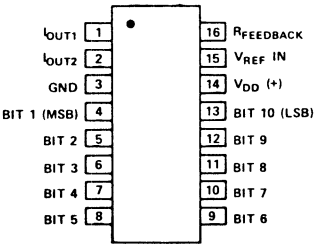
PIN CONFIGURATION



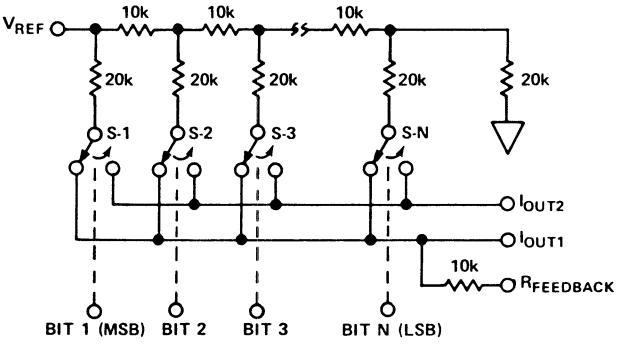
116000261

D/A Converter

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

N=10

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

The 116000261 is a 10-bit multiplying D/A converter.

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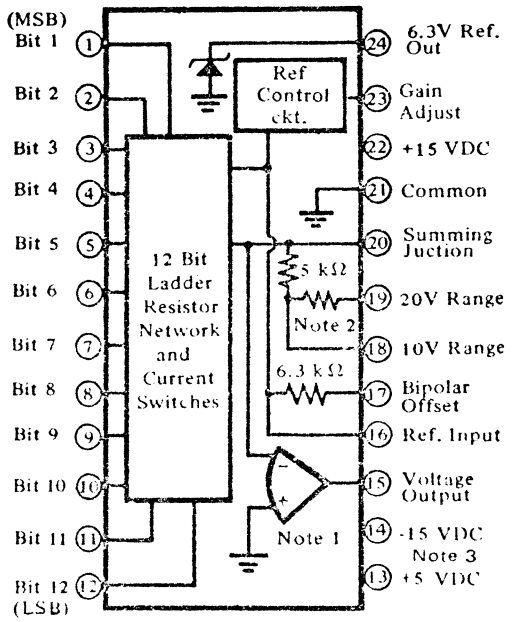
116000301

D/A Converter

CONNECTION DIAGRAM
(VOLTAGE MODELS)



Note 1: Amplifier not included in current output models.
Note 2: 3 kΩ for CCD models
5 kΩ for CBI models
Note 3: +5V supply input may be connected to +15V supply if +5V supply is not available. This will increase internal power dissipation by 200 mW.

DIGITAL INPUT CODES

	LOGIC INPUTS	CSB	COB	CTC*
CBI Models	MSB LSB 0000 ... 000 0111 ... 111 1000 ... 000 1111 ... 111	Compl. Straight Binary + Full Scale +½ Full Scale Mid Scale -1 LSB Zero	Compl. Offset Binary +Full Scale Zero -1 LSB -Full Scale	Compl. Two's complement -1 LSB -Full Scale +Full Scale Zero
CCD Models	MSD LSD 0110 . . . 0110 1111 . . . 1111	CCD (Complementary Coded Decimal) 3 Digits +Full Scale Zero		*Invert the MSB of the COB code with an external inverter to obtain CTC code.

The 116000301 is a 12-bit D/A converter which features internal reference and optional output amplifier. It accepts complementary digital input codes either binary (CBI) format or decimal (CCD) format.

116000310

Hybrid Data Acquisition Front End

PIN DESIGNATIONS

Pin No.	
1	SINGLE ENDED/DIFFERENTIAL MODE CONTROL
2	DIGITAL GND
3	+5 VOLTS
4	CHANNEL 7
5	CHANNEL 6
6	CHANNEL 5
7	CHANNEL 4
8	CHANNEL 3
9	CHANNEL 2
10	CHANNEL 1
11	CHANNEL 0
12	HOLD CAP
13	SAMPLE/HOLD MODE CONTROL
14	OFFSET ADJ
15	OFFSET ADJ
16	ANALOG OUTPUT
17	ANALOG GND
18	CHANNEL 15
19	CHANNEL 14
20	-15 VOLTS
21	+15 VOLTS
22	CHANNEL 13
23	CHANNEL 12
24	CHANNEL 11
25	CHANNEL 10
26	CHANNEL 9
27	CHANNEL 8
28	A3 (MSB)
29	A0 (LSB)
30	A1
31	A2
32	ADDRESS LATCH

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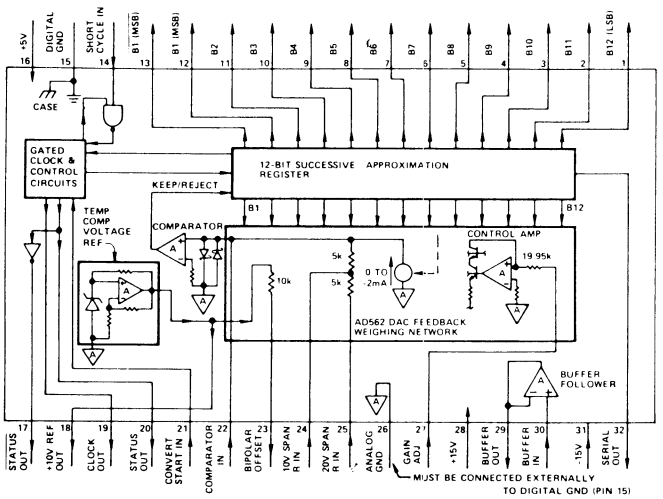
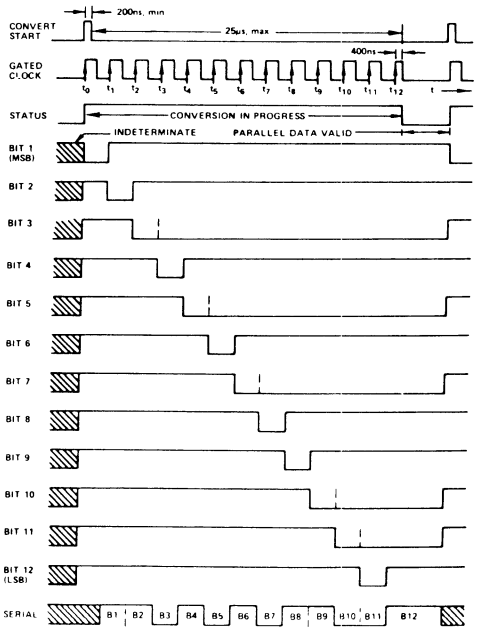
116000316

A/D Converter

FUNCTIONAL DIAGRAM



TIMING DIAGRAM

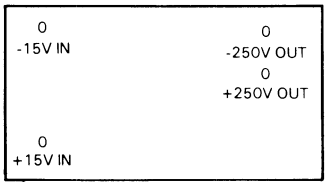


The 116000316 is a 12-bit successive approximation A/D converter. It features an internal clock, reference comparator, and buffer amplifier.

116000317

250V DC/DC Converter

PIN CONFIGURATION



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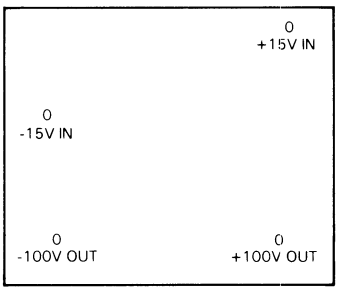
116000318

100V DC/DC Converter

PIN CONFIGURATION



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121000000 through 121999800

121000000	00	CRYSTAL OSCILLATOR MODS, FAMILY SPEC
121000001	00	CRYSTAL 14.08 KHZ
121000002	00	CRYSTAL 16.00 KHZ
121000003	00	CRYSTAL 10 MHZ
121000004	00	CRYSTAL 20 MHZ
121000005	00	CRYSTAL 19.200 KHZ
121000006	00	CRYSTAL 8.8 KHZ
121000007	00	CRYSTAL 230.4 KHZ
121000008	00	CRYSTAL 153.6 KHZ
121000009	00	CRYSTAL 65.536 KHZ
121000010	00	CRYSTAL 307.2 KHZ
121000011	00	CRYSTAL 38.4 KHZ
121000012	00	CRYSTAL 76.8 KHZ
121000013	00	CRYSTAL 192.0 KHZ
121000014	00	CRYSTAL 13.33 MHZ
121000015	00	CRYSTAL 40 KHZ
121000016	00	CRYSTAL 204.8 KHZ
121000017	00	CRYSTAL 25.6 KHZ
121000018	00	CRYSTAL 10.752 KHZ
121000019	00	CRYSTAL 1228.800 KHZ VR6 E-5
121000020	00	CRYSTAL 11.5 MHZ
121000021	00	CRYSTAL 100 KHZ
121000023	00	CRYSTAL 614.4 KHZ
121000024	00	CRYSTAL XTA2 1.54 MHZ
121000025	00	CRYSTAL 11.004 MHZ
121000026	00	CRYSTAL 50 MHZ
121000027	00	CRYSTAL 15.36 MHZ
121000028	00	CRYSTAL 160.000 KHZ
121000029	00	CRYSTAL 8.33 MHZ
121000030	00	CRYSTAL 6.912 MHZ
121000031	00	CRYSTAL CER RESNR 460KHZ +.2-.2%
121000032	00	CRYSTAL 3.685 MHZ 01030-006
121000033	00	CRYSTAL 9.38MHZ +.01-.01 SERIES RES
121000034	00	CHRYSTAL 20MHZ OSC K1114A
121000035	00	CRYSTAL OSC 13.33MHZ
121000036	EE00	CRYSTAL 1.25MHZ 175OHMS .1%
121000037	00	CTYSTAL OSC 15.360 MHZ 51114A
121000038	00	CRYSTAL 12.672MHZ DIP OSCILLATOR
121000039	00	CRYSTAL 10MHZ OSC
121000040	00	CRYSTAL 9.8304 MHZ +.01-.01 SER RES
121000041	00	CRYSTAL 2.4576MHZ
121000042	00	CRYSTAL 22.932MHZ "AT" CUT FUND MODE
121000043	EE00	CRYSTAL K1114A 9.984MHZ OSC
121000044	00	CRYSTAL OSC K1114A-8.333MHZ
121000045	EE00	CRYSTAL 1.8432MHZ VR6E-5 PKG PRL MODE
121000046	00	CRYSTAL 13.82400MHZ VM6-5
121000047	00	CRYSTAL 17.2 KHZ
121000048	00	CRYSTAL OSC MOD 5.76MHZ
121000049	00	CRYSTAL OSCILLATOR 40MHZ
121000050	00	CRYSTAL 6MHZ .015%
121000051	00	CRYSTAL 23.5872 MHZ
121000052	00	CRYSTAL OSILLATOR MODULE 12.00MHZ
121000054	00	CRYSTAL CLOCK OSCILLATOR 16.666MHZ
121000055	00	CRYSTAL CERAMIC RESONATOR FA 240KHZ
121000056	00	CRYSTAL 10.1376MHZ
121000057	00	CRYSTAL 18.414MHZ
121000058	00	CRYSTAL OSCILLATOR MODULE 18.18MHZ
121000059	EE00	CRYSTAL 18.750 MHZ
121000060	00	CRYSTAL 14.322MHZ
121000061	00	CRYSTAL 16.000MHZ
121000062	EE00	CRYSTAL 23.1084MHZ
121000063	EE00	CRYSTAL 5.0688MHZ
121000064	00	CRYSTAL 12MHZ
121000065	EE00	CRYSTAL 8.188MHZ
121000066	00	CRYSTAL OSCILLATOR MODULE 4.194MHZ
121000067	00	CRYSTAL OSCILLATOR MODULE 50.00MHZ
121000068	00	CRYSTAL OSCILLATOR MODULE 45.455MHZ
121000069	00	CRYSTAL OSCILLATOR MODULE 41.667MHZ
121000070	EE00	CRYSTAL OSCILLATOR MODULE 4.5MHZ
121000071	EE00	CRYSTAL OSCILLATOR MODULAR 800KHZ
121000072	EE00	CRYSTAL OSCILLATOR MODULE 32.0MHZ
121000074	00	CRYSTAL QUARTY 23.373 MHZ
121000075	00	CRYSTAL OSCILLATOR MODULE 24.00MHZ
121000076	EE00	CRYSTAL 16.00MHZ OSCILLATOR MODULE
121000078	00	CRYSTAL 14.3220MHZ OSCILLATOR MODULE
121999800	00	CRYSTAL OSC MODS, FAMILY SPEC

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ARITHMETIC ELEMENTS

CHARACTER GENERATORS

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