MIRAGE UART PROGRAMMING

Some CP/M applications require that you have direct access to the asynch ports for the CRT or the AUX line. In most cases, the Extended BIOS Entry Points documented in Chapter 1 of the MIRAGE Reference Manual should be adequate for accessing these ports. This Application Note is intended for the assembler programmer who needs to go beyond the capabilities provided by the Extended BIOS Entry Points, and must directly access the UARTs which control these EIA RS-232C lines.

Note: This Application Note is intended to be used in conjunction with the Data Sheet for the Motorola MC6850 integrated circuit. We strongly recommend that you obtain a copy of this publication before proceeding to program the UARTs on your own.

Baud Rates

The baud rates for both the CRT and AUX ports are controlled entirely via hardware from the DIP-switches on the edge of the MIRAGE 102 Processor board. Baud rates may not be selected via software.

UART Registers

The UARTs used on the MIRAGE board are the 6850 type manufactured by Motorola. Each UART has four registers accessible by the programmer. Two of these registers are read-only; the other two are write-only. The read-only registers are Status and Received Data; the write-only registers are Control and Transmit Data. The following table gives the I/O locations (in hex) of these registers:

FUNCTION	I/O LOCATION
CRT Received Data	IN 34
CRT Transmit Data	OUT 24
CRT Status	IN 30
CRT Control	OUT 20
AUX Received Data	IN 3C
AUX Transmit Data	OUT 2C
AUX Status	IN 38
AUX Control	OUT 28

Status Register

The meaning of the bits in the Status Register is as follows:

Bit 0 (least significant bit): Receive Data Register Full. A one in this bit indicates that a character has been received and is available for reading in the Received Data Register. This bit will be cleared after reading the data, until the next character is ready.

Bit 1: Transmit Data Register Empty. A one in this bit indicates that the previous character (if any) has been transmitted and that a character may be placed in the Transmit Data Register for transmission. A zero indicates that the previous character has not yet been transmitted.

Bit 2: Data Carrier Detect. This bit is not used by MIRAGE and will always appear as a zero.

Bit 3: Clear To Send. A zero in this bit indicates that the Clear To Send input is true, and that characters may be transmitted. A one indicates that CTS is false, and that transmission is inhibited. This input signal comes from pin 5 of the RS-232C connector, and may be used by a printer or other device to stop transmission from MIRAGE until the printer is ready to accept more characters. Note that the UART itself will not transmit characters when the CTS signal is false. Also note that if disconnected, CTS will appear true to the MIRAGE Processor.

Bit 4: Framing Error. A one in this bit indicates that a received character was improperly framed by start and stop bits. A zero indicates that no framing error occured. This bit will always reflect the status of the character currently in the Received Data Register, and will be cleared by reading that register.

Bit 5: Receiver Overrun. A one in this bit indicates that one or more characters were lost due to another character being received before the previous character was read from the Received Data Register. A zero indicates that no characters were lost. When this bit is set, the latest character received is available in the Received Data Register. This bit will be cleared by reading the Received Data Register.

Bit 6: Parity Error. A one in this bit indicates that a parity error was detected on the character currently in the Received Data Register. A zero indicates that no parity error occured. Reading the Received Data Register clears this bit.

Bit 7: Interrupt Status. A one in this bit indicates that an interrupt is being requested by the UART. As we do not support user interrupt routines, we recommend that UART interrupts not be enabled (see the section on the Control Register).

Control Register

The meaning of the bits in the Control Register is as follows:

Bits 0 and 1 (least significant bits): Counter Divide Select Bits. The values of these two bits determine how the external clock is divided by the UART. In order for the baud rates to be accurate, always write a one in bit 0 and a zero in bit 1.

Bits 2, 3 and 4: Character Format. Determine the values for these bits from the following table:

Bit 4	Bit 3	Bit 2	Data Bits	Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	1	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Bits 5 and 6: Transmitter Control. These two bits combine to control three functions: (1) interrupts from the UART Transmitter, (2) the output of the Request-to-Send (RTS) signal, and (3) the transmission of a Break. Note that although the UART documentation refers to the RTS signal, on the the MIRAGE board this signal actually appears on pin 20 of the RS-232C connector. This is the Data Terminal Ready (DTR) signal. Refer to the following table for the values of bits 5 and 6:

Bit 6	Bit 5	(DTR)	Transmitter Interrupts	Transmitter Output Held at BREAK State
0	0	True	Disabled	No
0	1	True	Enabled	No
1	0	False	Disabled	No
1	1	True	Disabled	Yes

As we do not support user interrupt routines, we recommend that UART interrupts not be enabled (see the section on the Status Register).

Bit 7: Receive Interrupt Enable. A one in this bit will enable interrupts from the UART receiver. An interrupt will occur when the Receive Data Register becomes full, or an Overrun condition occurs. The MIRAGE CP/M BIOS runs with receiver interrupts enabled. However, if you want to process the received data yourself, we recommend that you disable these interrupts.

Sample Routines

The following routines are examples of assembler code to initialize the AUX port's UART, and to read and write characters via that port.

```
AUXIN     EQU  3CH        ; AUX PORT RECEIVED DATA
AUXOUT    EQU  2CH        ; AUX PORT TRANSMIT DATA
AUXSTAT   EQU  38H        ; AUX PORT STATUS REGISTER
AUXCTRL   EQU  28H        ; AUX PORT CONTROL REGISTER

PARAMS    EQU  09H        ; /16 CLOCK; 7 DATA BITS; 1 STOP BIT;
                          ; EVEN PARITY; ALL INTERRUPTS DISABLED

XMTRDY    EQU  02H        ; MASK: "TRANSMIT DATA REGISTER EMPTY"
RCVRDY    EQU  01H        ; MASK: "RECEIVE DATA REGISTER FULL"
ERFLAGS   EQU  70H        ; MASK: FRAMING, OVERRUN & PARITY ERRORS


INIT:     MVI  A,PARAMS   ; INITIALIZE THE UART
          OUT  AUXCTRL
          RET


GCHAR:    IN   AUXSTAT    ; READ UART STATUS
          ANI  RCVRDY     ; TEST FOR CHARACTER RECEIVED
          JZ   GCHAR      ; LOOP UNTIL ONE COMES IN
          IN   AUXSTAT    ; GOT ONE: READ STATUS AGAIN
          ANI  ERFLAGS    ; ARE THERE ANY ERRORS?
          JNZ  ERROR      ;   YES (ERROR HANDLER NOT SHOWN)
          IN   AUXIN      ; NO, READ THE DATA BYTE
          RET             ; RETURN WITH DATA IN 'A' REGISTER


PCHAR:    PUSH PSW        ; SAVE CHAR PASSED IN 'A' REGISTER
PCHAR1:   IN   AUXSTAT    ; READ UART STATUS
          ANI  XMTRDY     ; IS THE TRANSMITTER READY?
          JZ   PCHAR1     ;   NO, LOOP UNTIL IT IS
          POP  PSW        ; READY, RETRIEVE CHAR IN 'A' REG.
          OUT  AUXOUT     ; SEND THE CHARCTER
          RET
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