

REVISION HISTORY		
ECO	DATE	DESCRIPTION
0258	3-13-84	SHEET 15
0283	3-30-84	SHEET 4
0337	7-3-84	SEE ECO
0418	12-7-84	SHEETS 4 & 5
0511	10-85	SHEETS

DC-296C

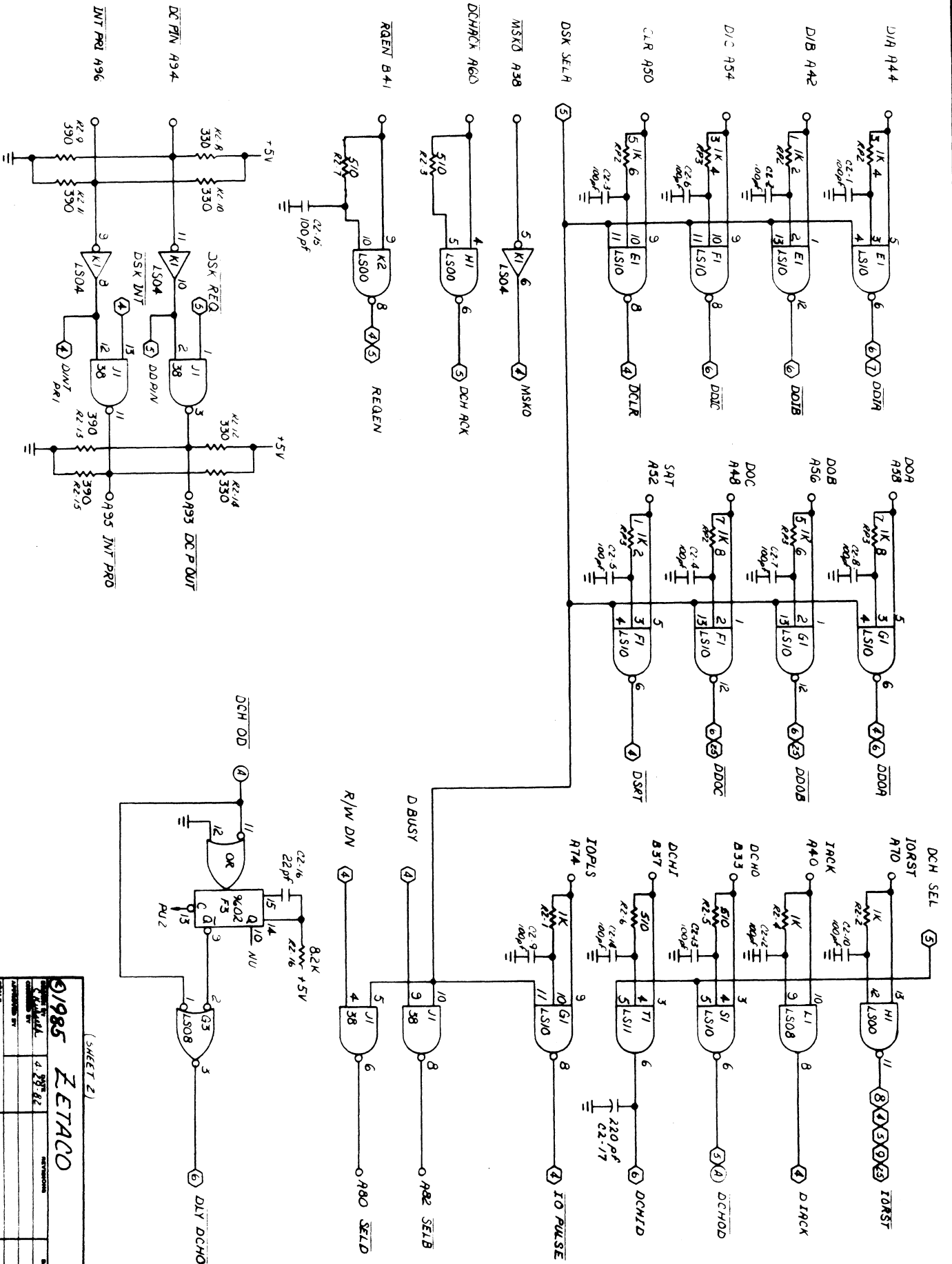
NOTE:
 1. NUMBERS FOUND WITHIN THE
 HEXAGON SYMBOLS INDICATES SHEETS
 WHERE CONTINUED LOGIC WILL BE FOUND
 EXAMPLE (2) = SHEET 2

(SHEET 1 OF 25)

01985	ZETACO
DATE	6-27-84
DESIGNED BY	
CHECKED BY	
DATE	
PROJECT NO.	700-296C
DATE	

700294-000B

700284-000B



(SHEET 2)

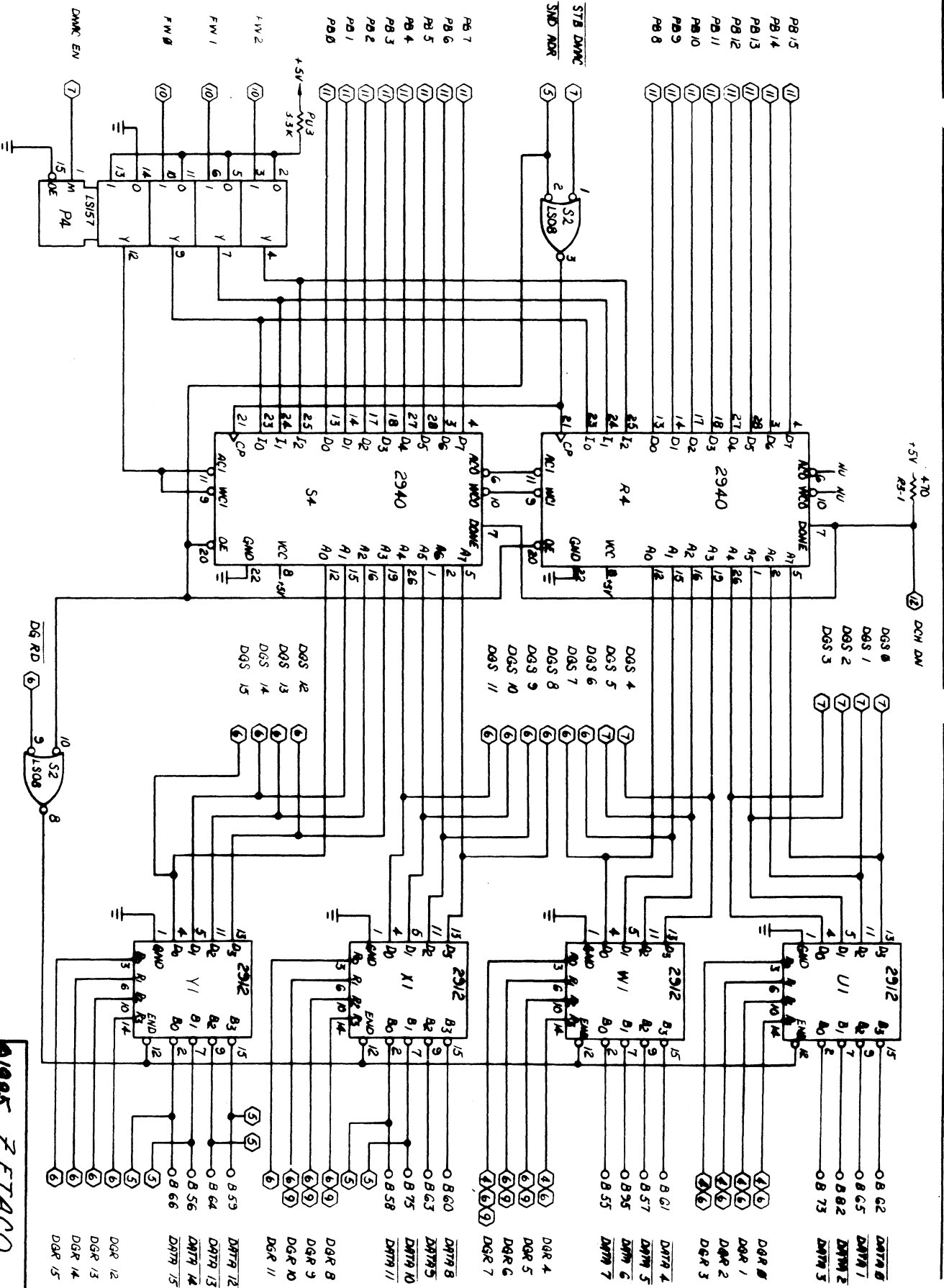
01985 ZETACO

DATE	4-29-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
REVISIONS	
NO.	
DATE	

DIGITAL INTERFACE

700-284-00

700284-0008

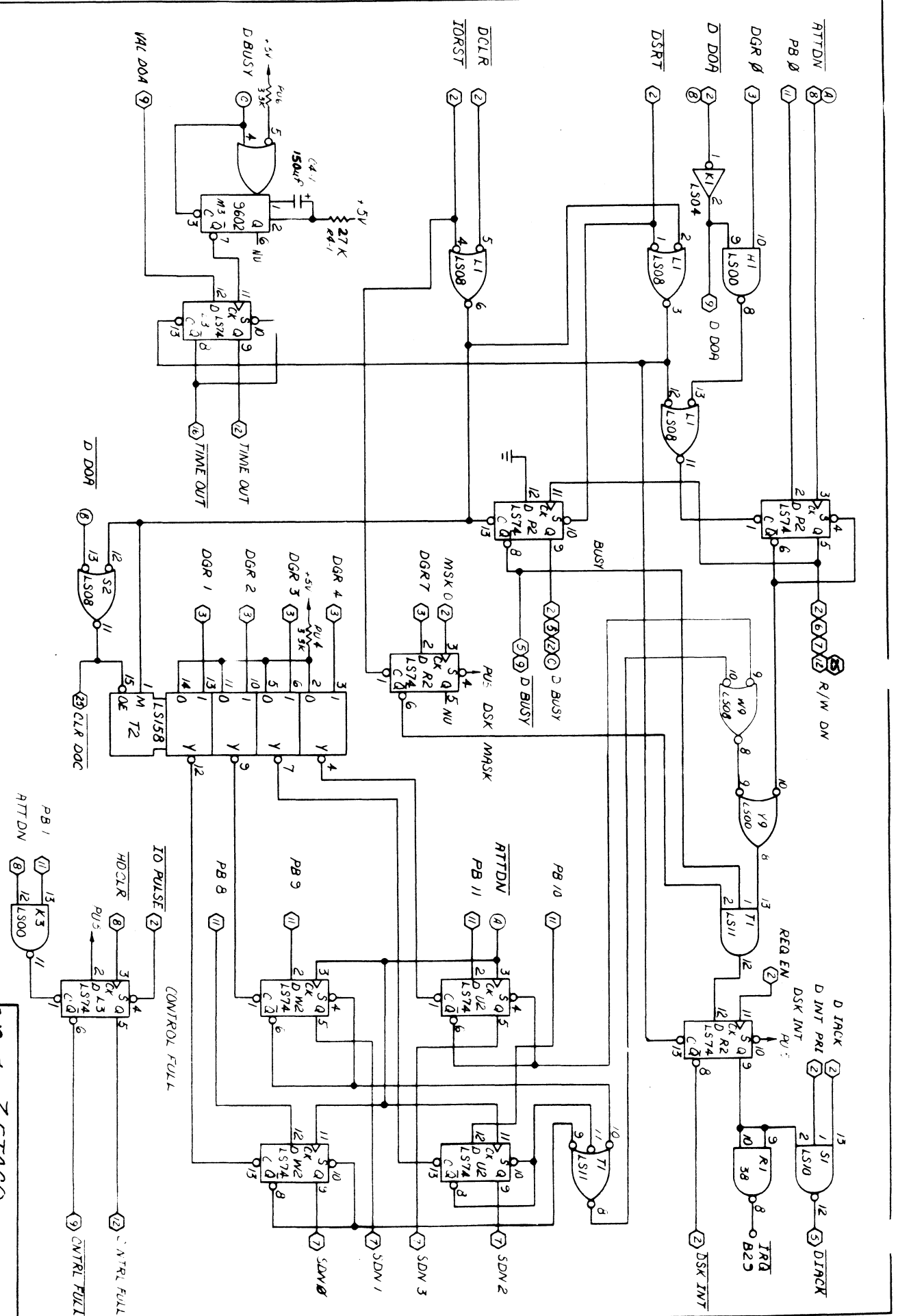


(SHEET 3)

01985 ZETACO

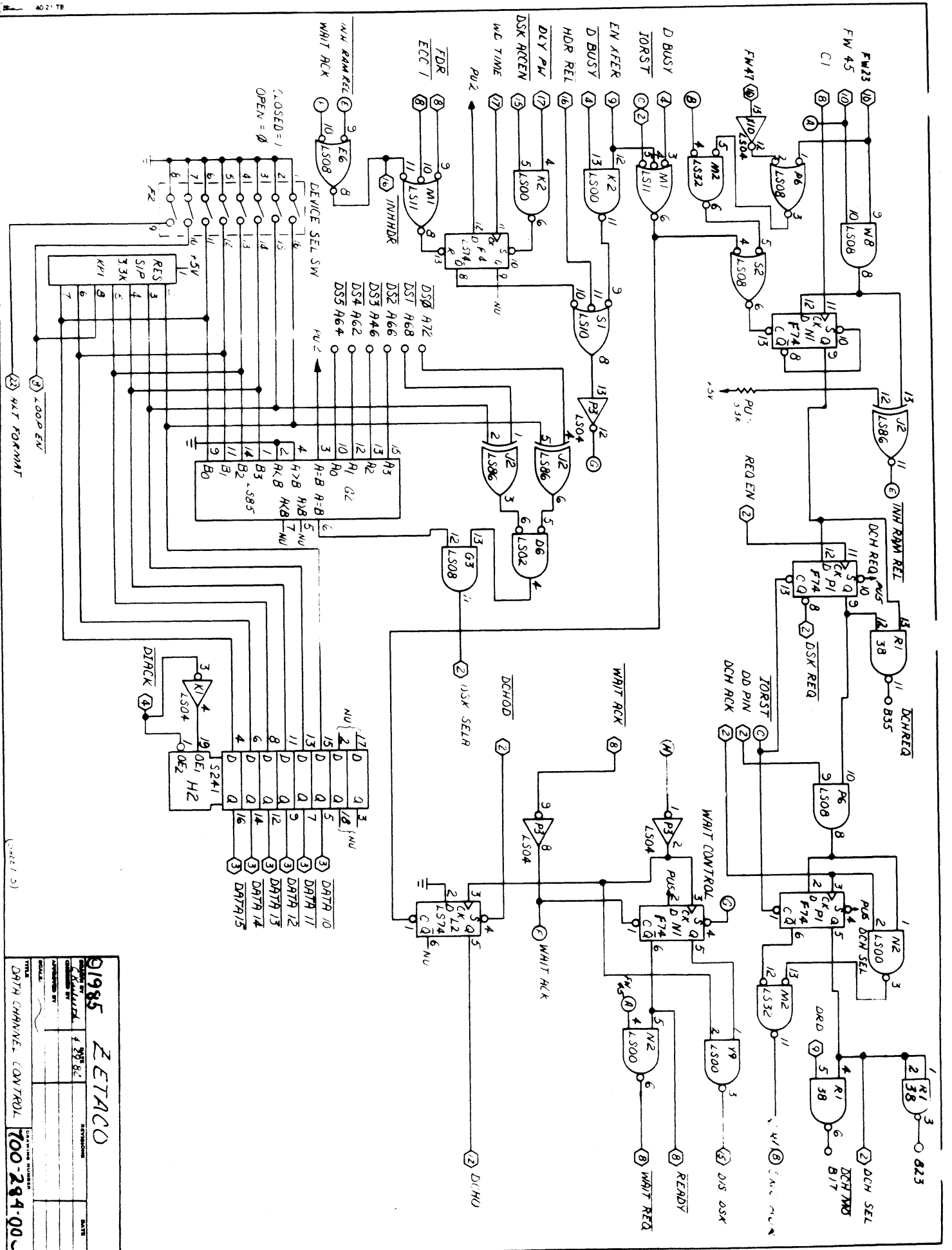
DATE	4-18-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
DATE	
DCN	DR/REC 1 ADDR GEN
700-284-00C	

700284-000 B



Sheet #1

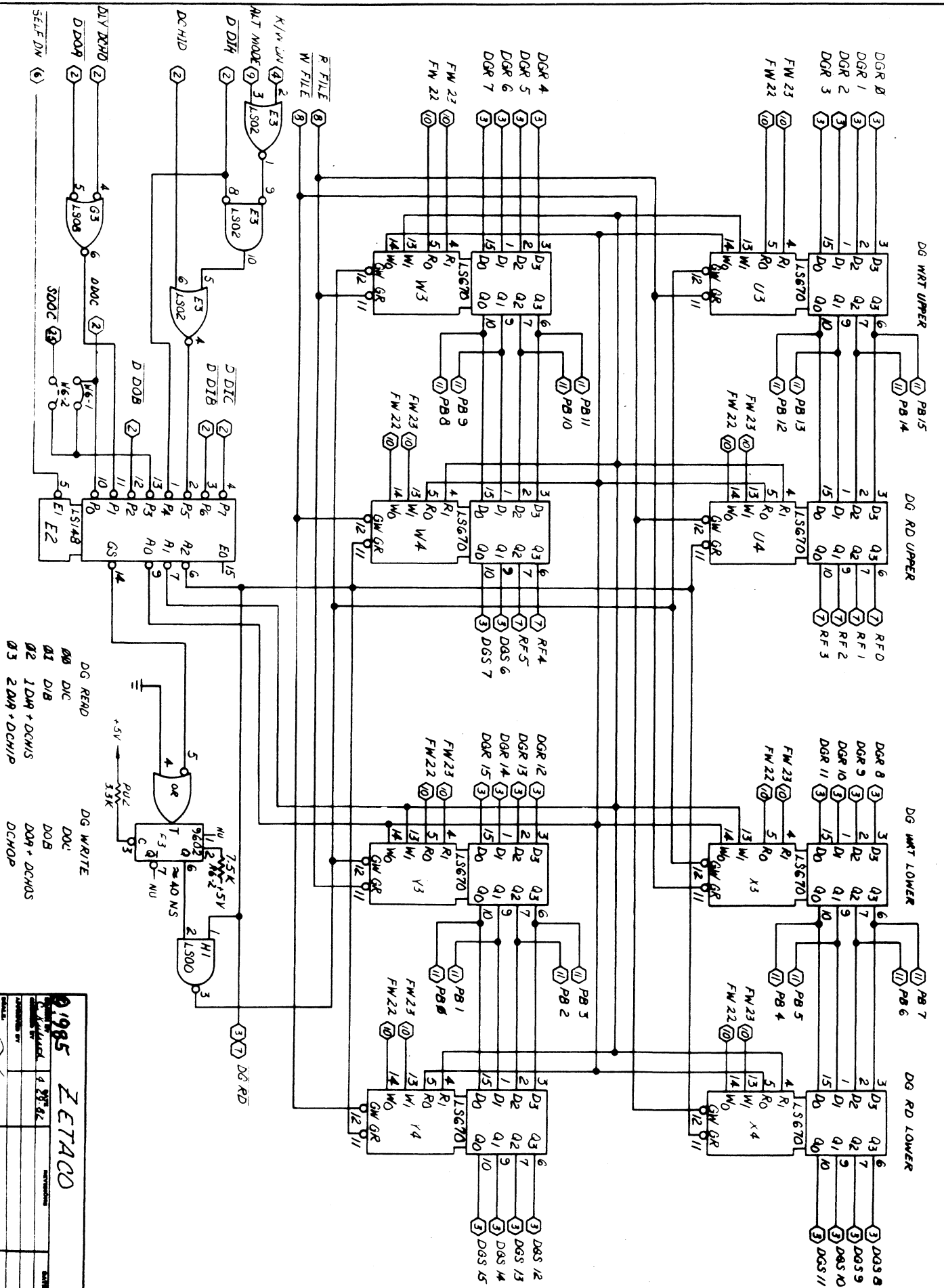
<p>91985</p> <p>ZETACO</p>	
<p>REVISED BY: <i>[Signature]</i></p> <p>DATE: <i>[Blank]</i></p>	<p>REVISED BY: <i>[Blank]</i></p> <p>DATE: <i>[Blank]</i></p>
<p>DESIGNED BY: <i>[Blank]</i></p> <p>CHECKED BY: <i>[Blank]</i></p>	<p>DESIGNED BY: <i>[Blank]</i></p> <p>CHECKED BY: <i>[Blank]</i></p>
<p>TITLE: <i>[Blank]</i></p>	<p>DATE: <i>[Blank]</i></p>
<p>DB PURCHASED BY: <i>[Blank]</i></p>	<p>DATE: <i>[Blank]</i></p>
<p>700-284-000</p>	<p>700-284-000</p>



Q1985 ZETACCO

DATE: _____
 DRAWING NUMBER: 700-284-00
 TITLE: DATA CHANNEL CONTROL

700284-000 B



- DG READ
- DG WRITE
- D00 D0C
- D01 D0B
- D02 1 D09 + DCHIS
- D03 2 D09 + DCHIP
- D04 D0B
- D05 2 D09 + DCHIP
- D06 D0B
- D07 D09 + DCHIS
- D08 D0B
- D09 D09 + DCHIP
- D10 D0B
- D11 D09 + DCHIP
- D12 D0B
- D13 D09 + DCHIP
- D14 D0B
- D15 D09 + DCHIP

91985 ZETACCO

DATE: 4 28 82

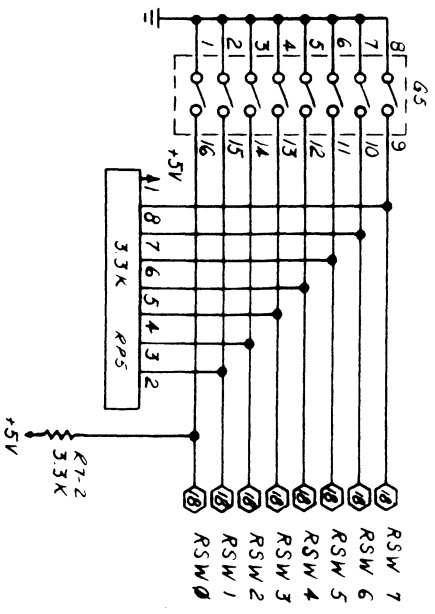
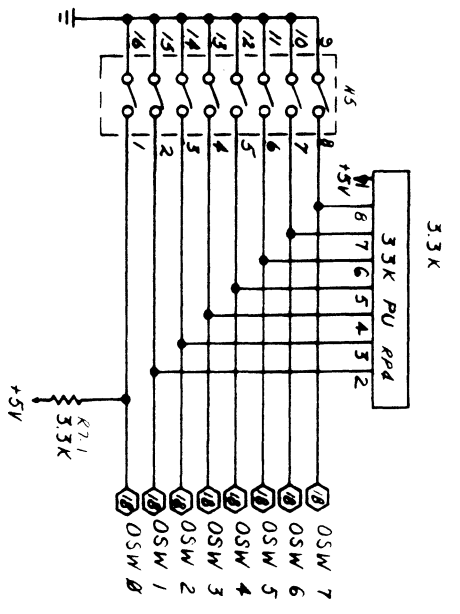
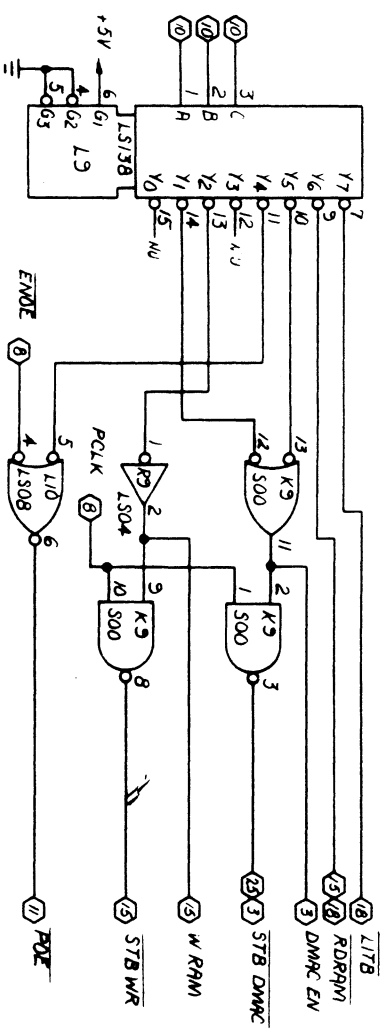
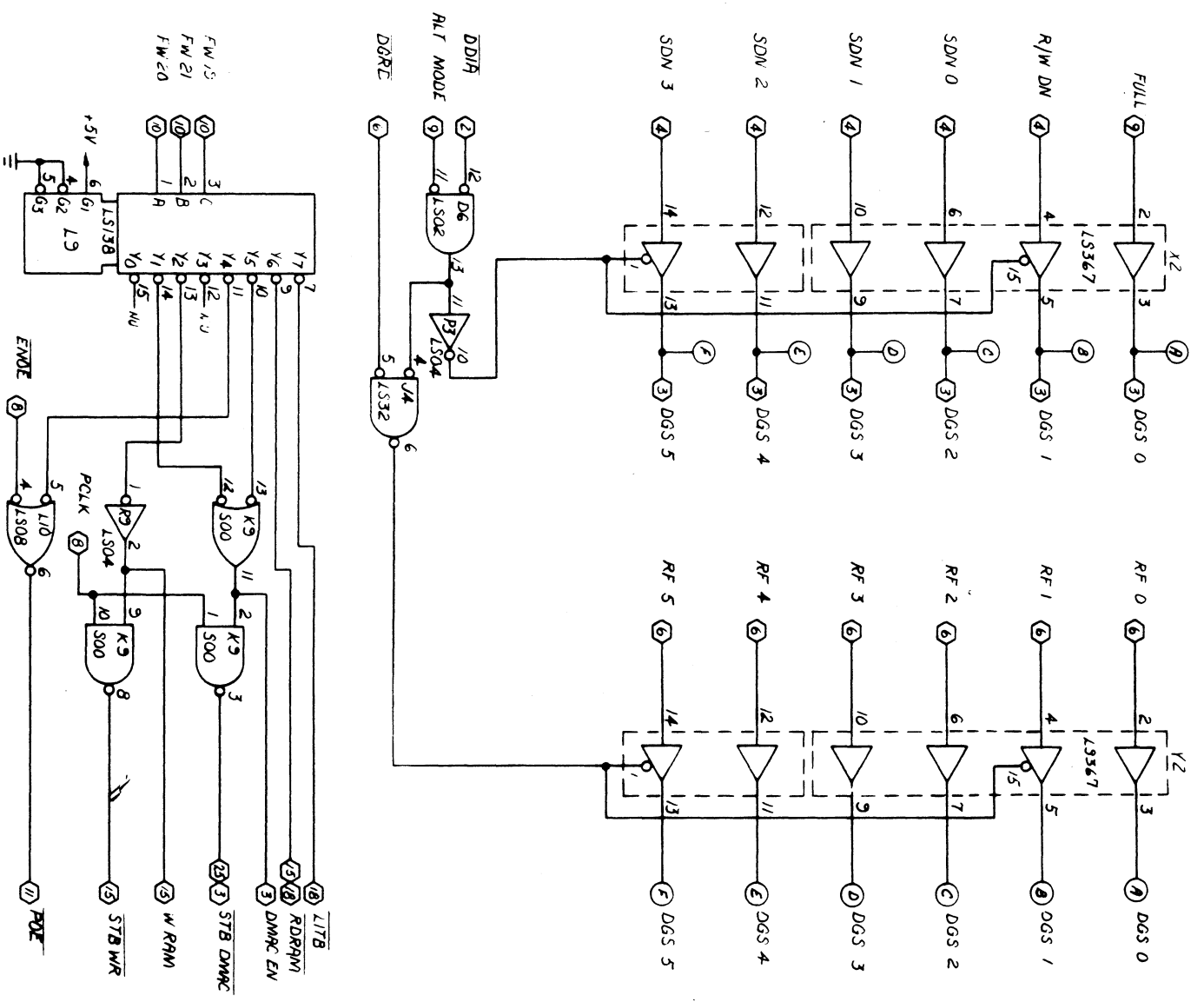
DESIGNED BY: []

CHECKED BY: []

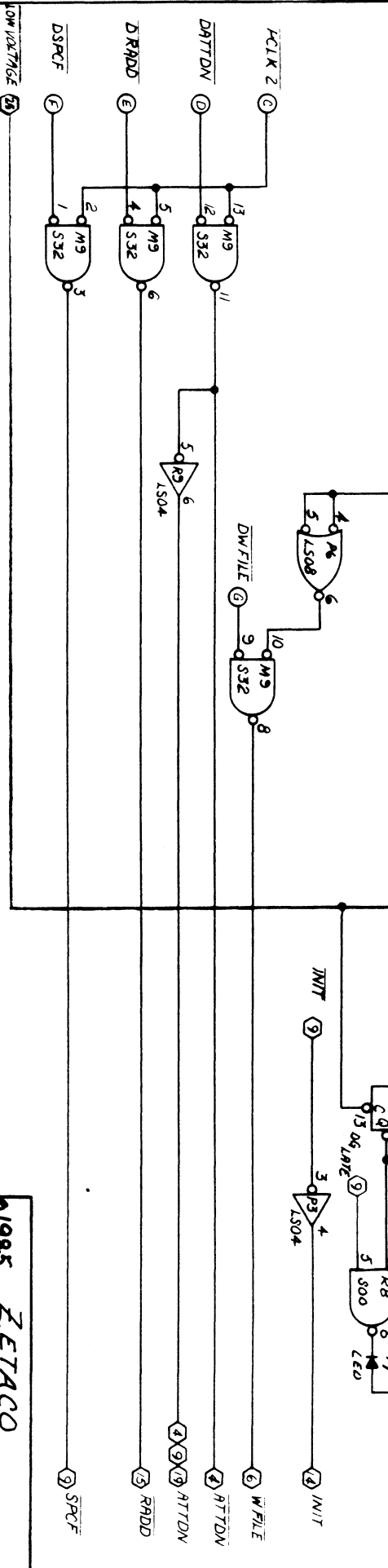
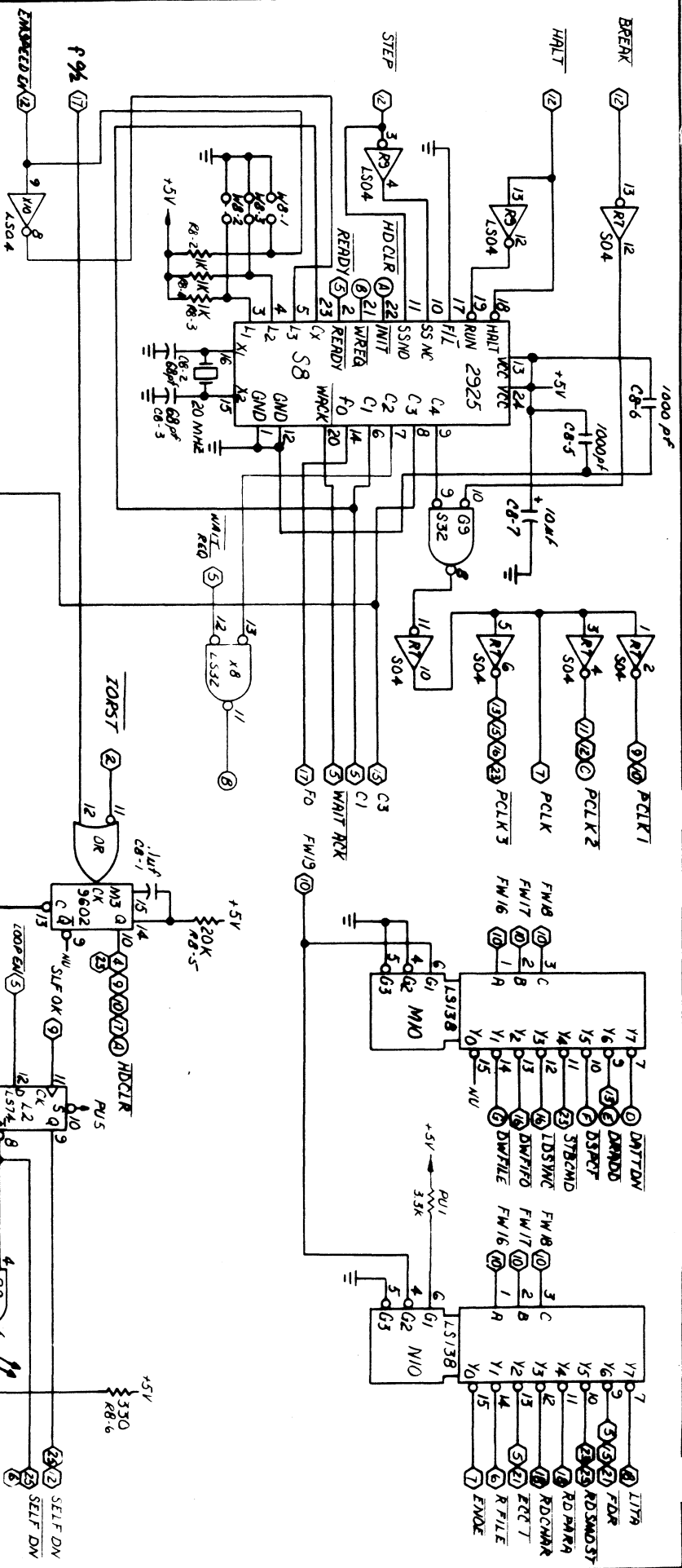
APPROVED BY: []

TITLE: REGISTER FILE

700-284-000 L



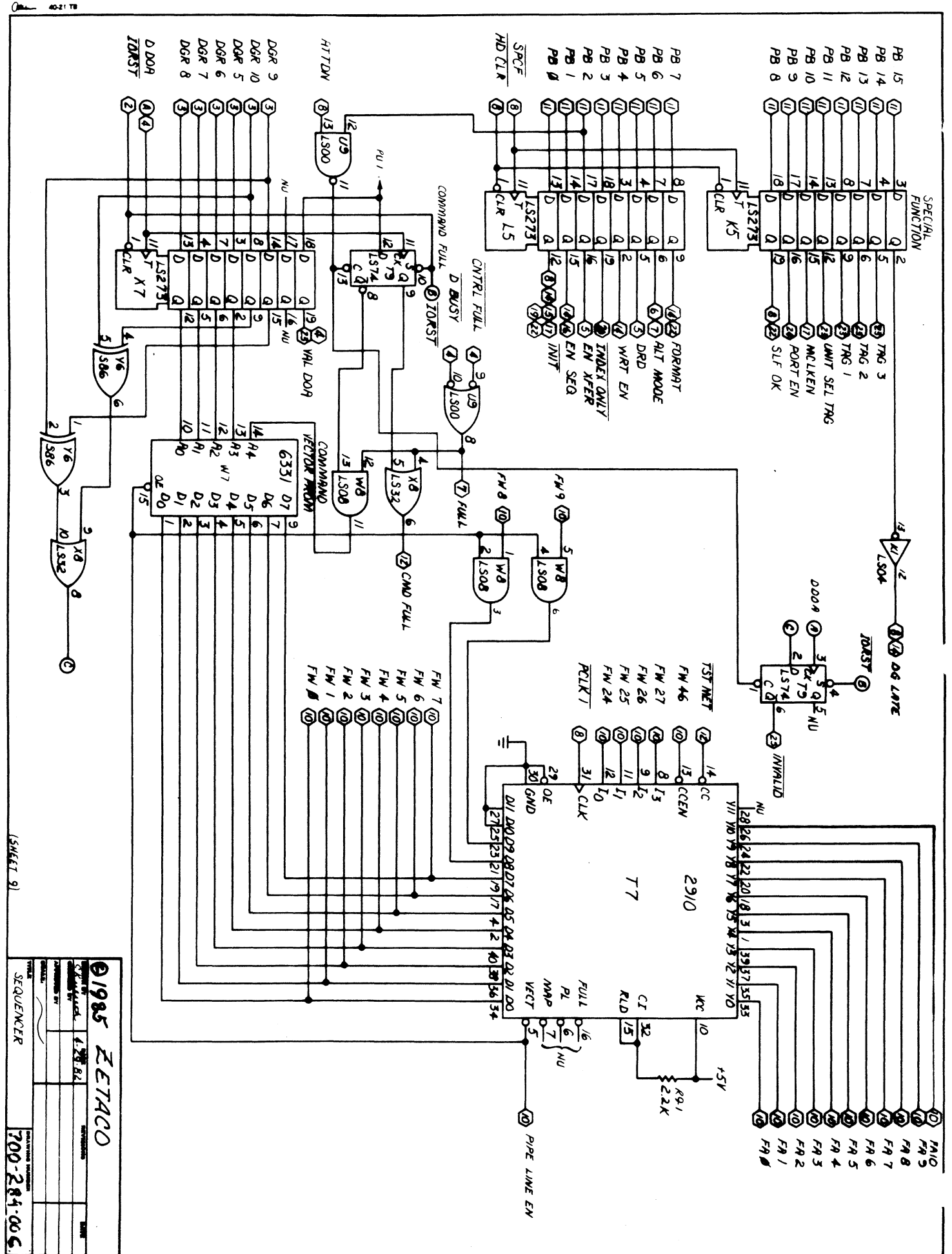
91985 ZETACO
 DRAWING NUMBER: **700-284-00 C**
 DATE: **4 29 82**
 DRAWN BY: **AW/ML**
 CHECKED BY: **AW/ML**
 TITLE: **DVA DRIVER**



700284-000 B

(SHEET 8)

91985 ZETACO	
DATE	
REVISION	
DESIGNED BY	
CHECKED BY	
APPROVED BY	
DATE	
MICRO CONTROL	
700-281-00 C	



700284-000 B

(SHEET 9)

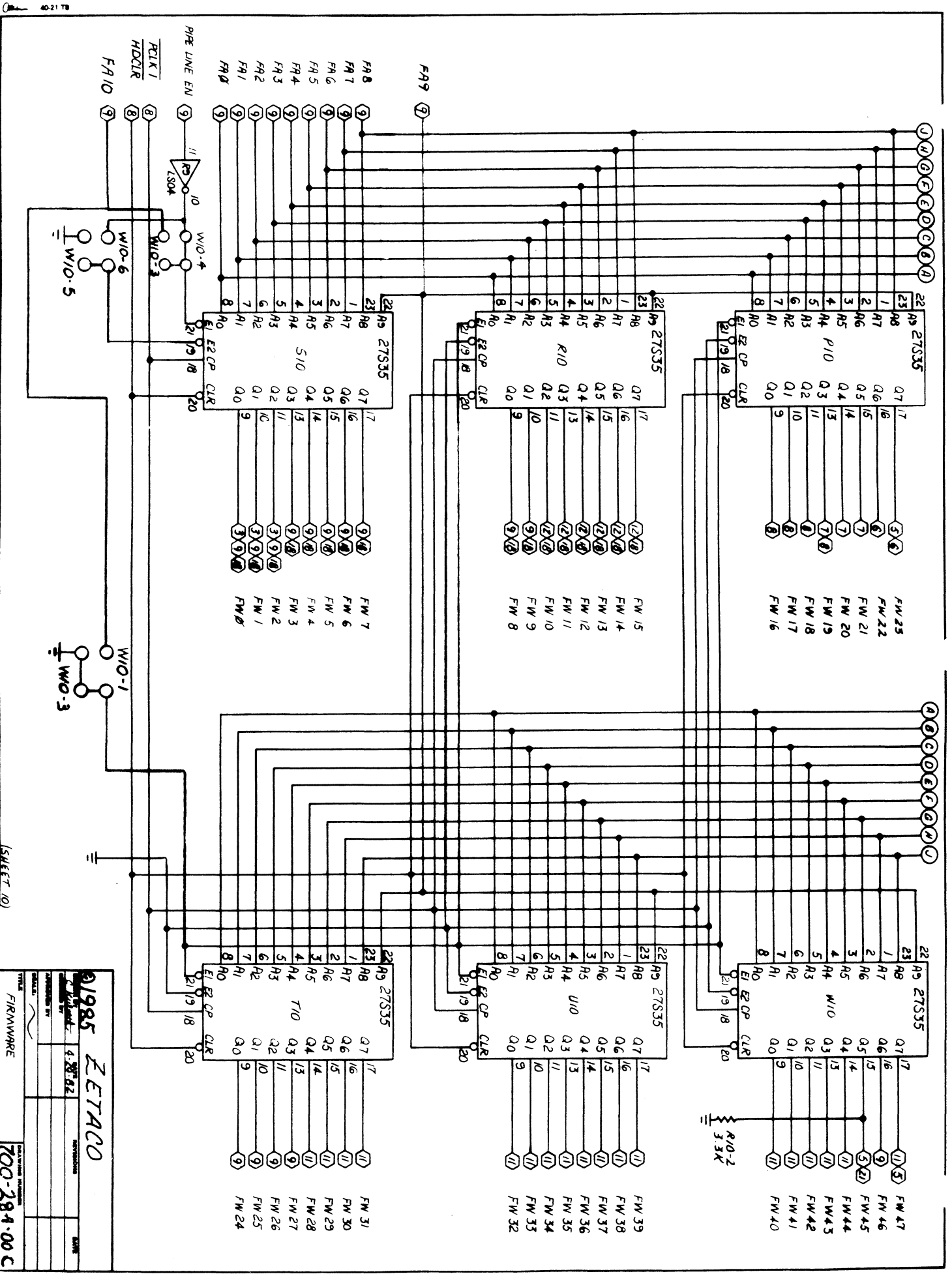
1985 ZETACO

SEQUENCER

700-284-000 C

DATE	4-28-84
DESIGNED BY	
CHECKED BY	
APPROVED BY	
DATE	

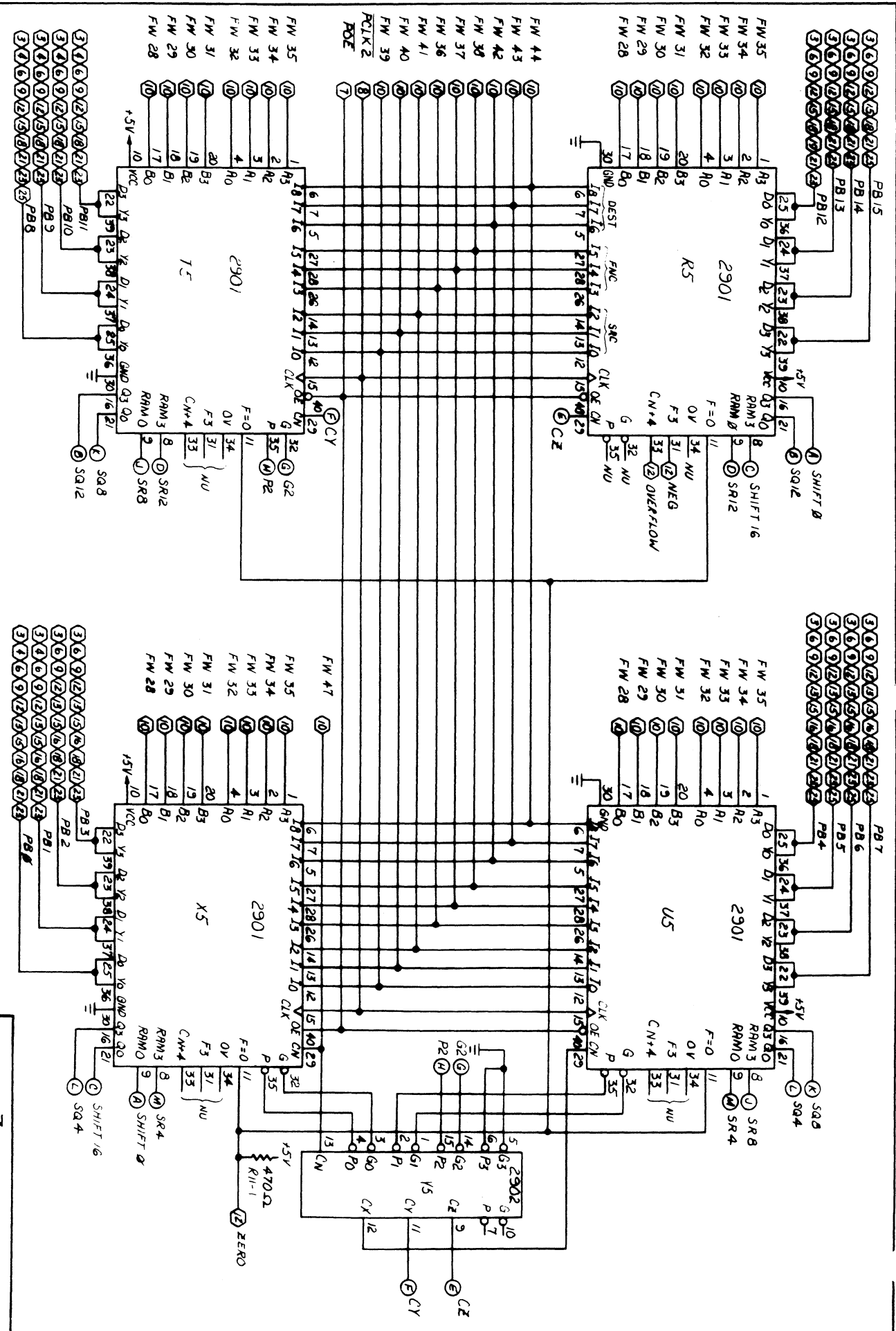
700284-000B



SHEET 10

91985 ZETACO		DATE
DESIGNED BY	4-28-82	REVISIONS
CHECKED BY		DATE
SYMBOL	FIRMWARE	
700-294-00 C		

700284-000B



(SHEET 11)

91985 ZETACO

DESIGNED BY: *C. R. Smith* DATE: *4-27-82*

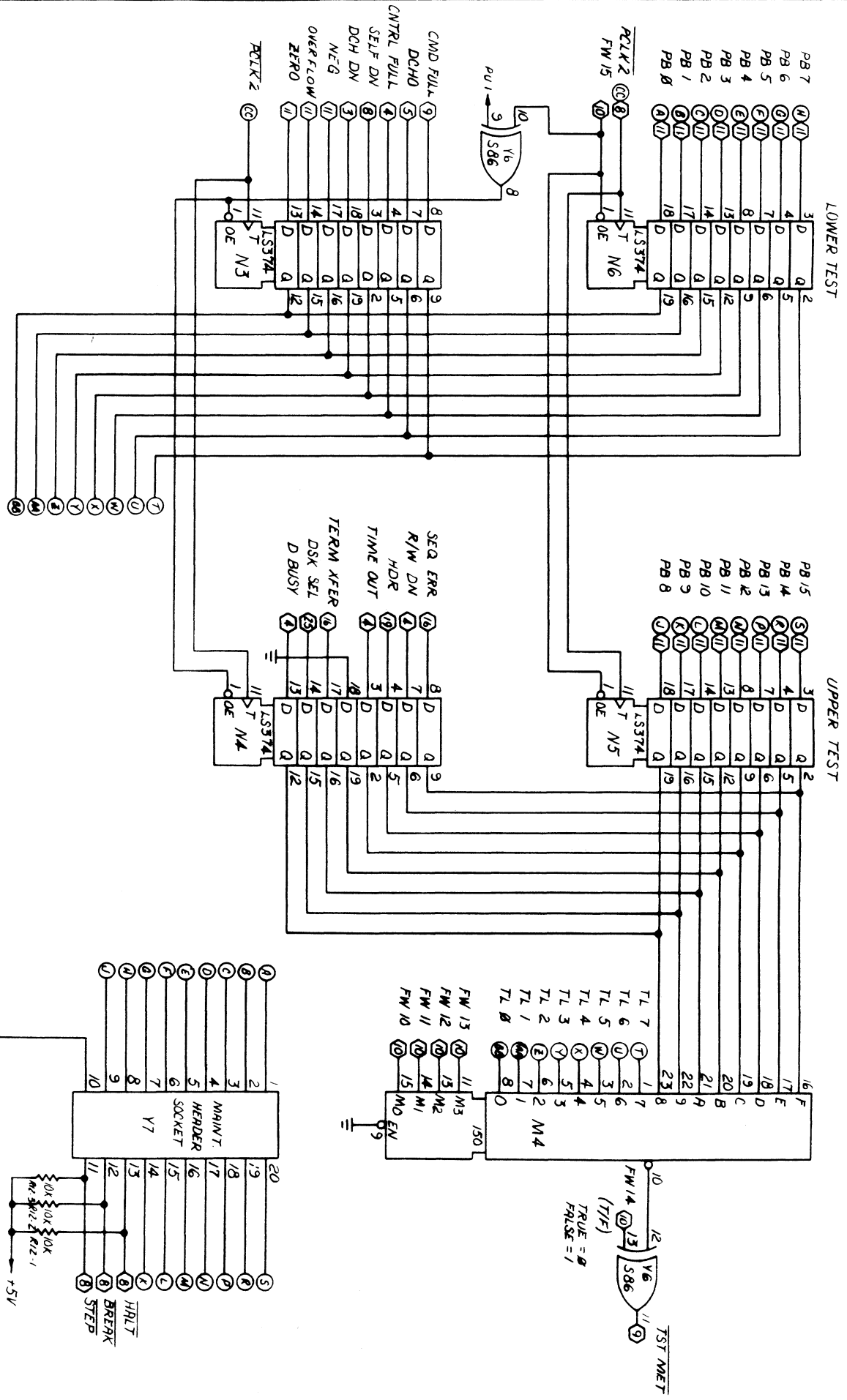
APPROVED BY: _____

DATE: _____

PROCESSOR: _____

DRAWING NUMBER: **700-284-00 C**

700284-000B

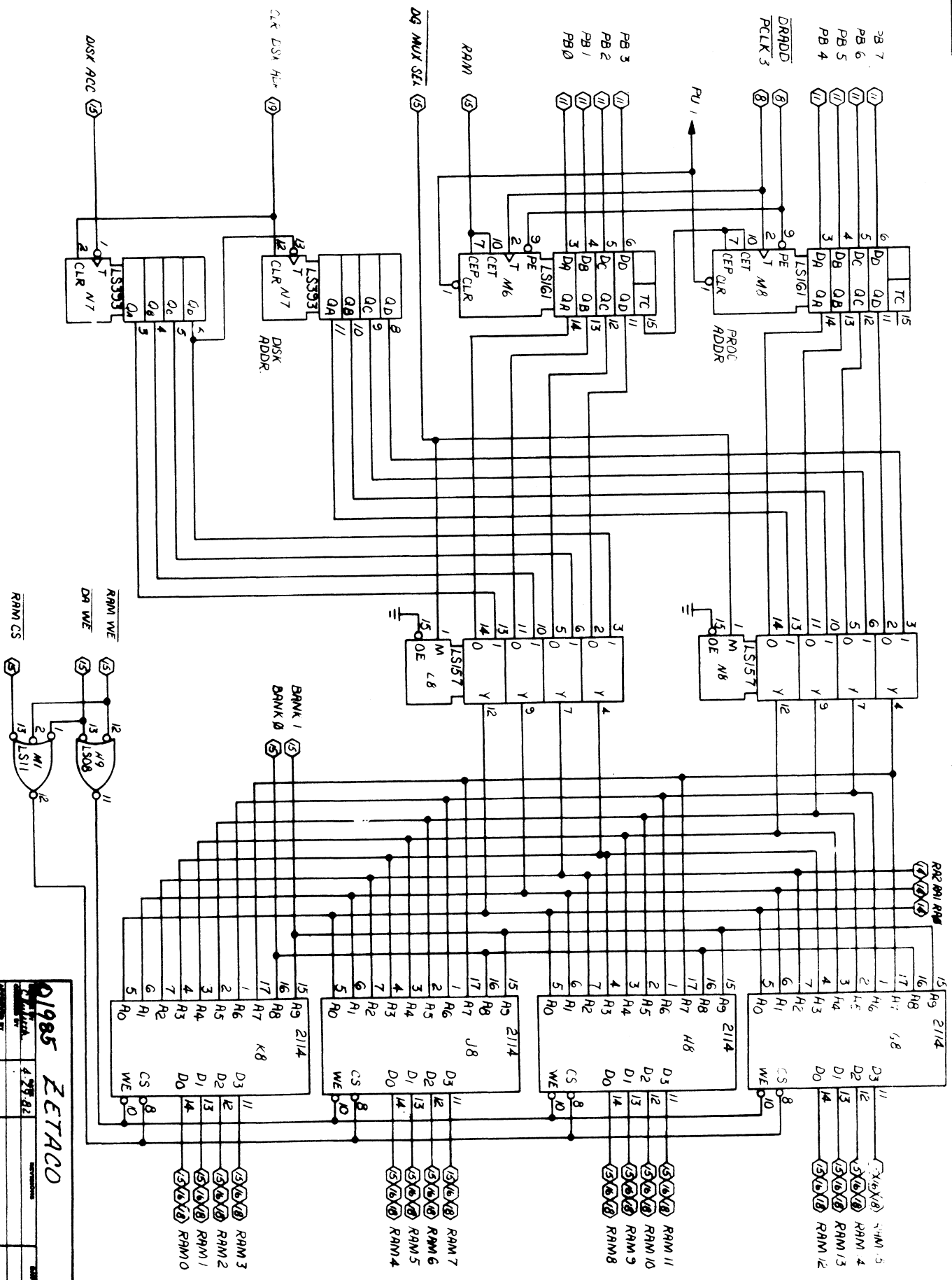


(SHEET 12)

01985 ZETACD		REV. 1	DATE
DESIGNED BY	4 28 82	APPROVED BY	
DRAWN BY		CHECKED BY	
TEST CONDITION		ESTIMATED QUANTITY	
		700-284-00 C	

EM-SPEED EV

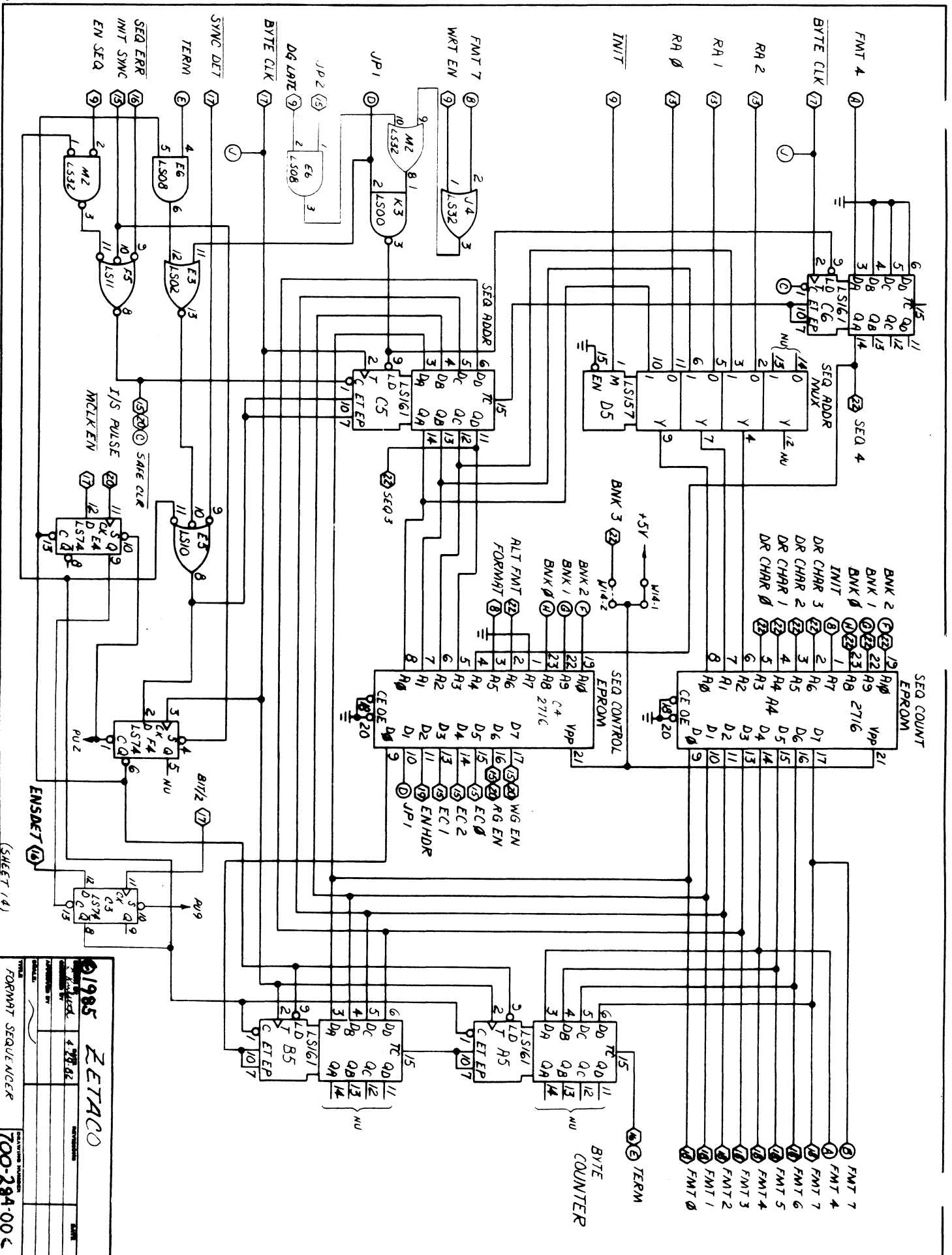
700284-000B



(SHEET 3)

01985 ZETACO	
DATE	4-23-82
DESIGNED BY	
CHECKED BY	
TYPE	MEMORY
700-284-00C	

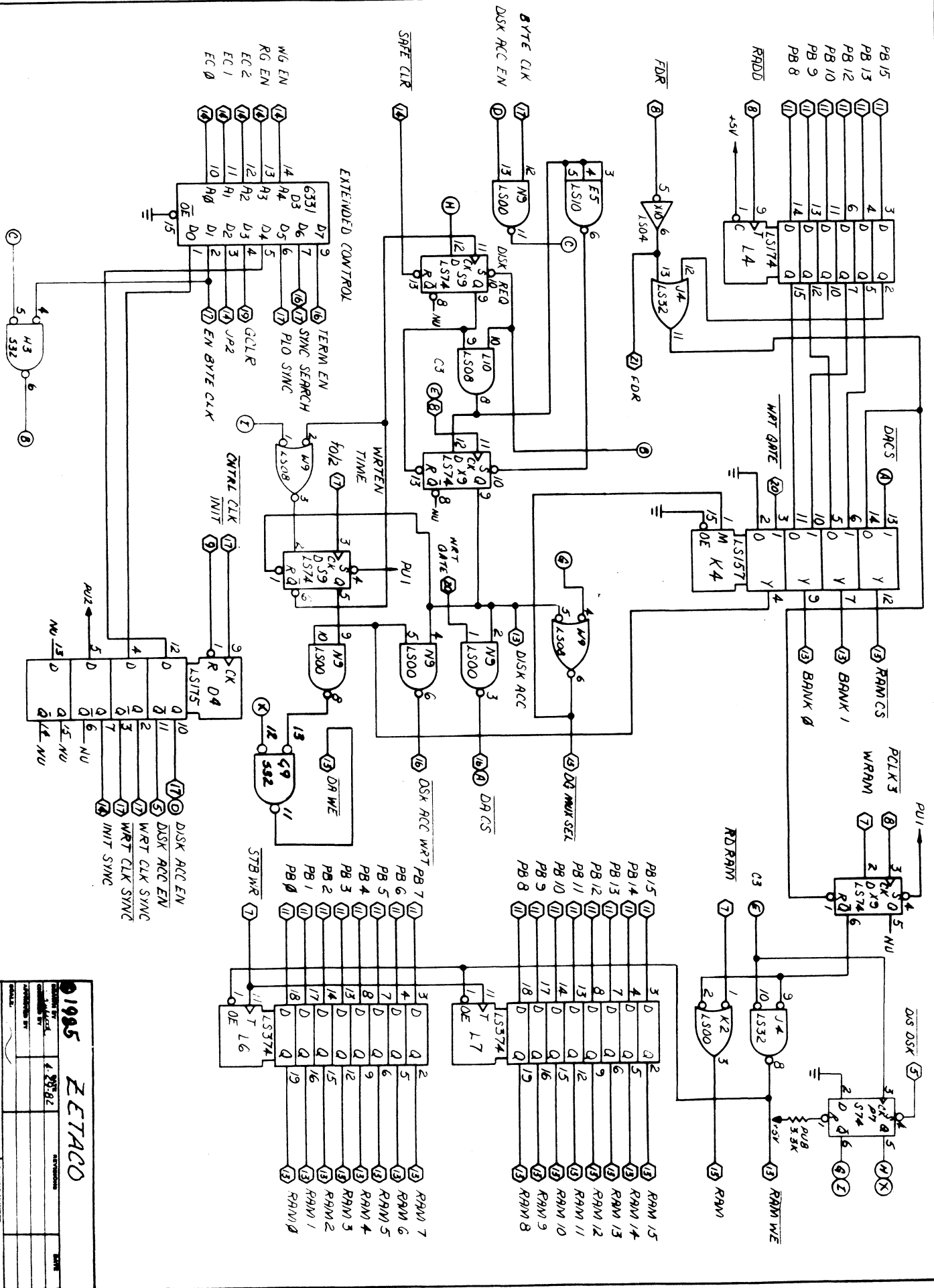
700284-000 B



(SHEET 14)

<p>1985 ZETACCO</p>	
<p>FORMAT SEQUENCER</p>	<p>700-284-00 C</p>
<p>DATE</p>	<p>REVISION</p>
<p>DESIGNED BY</p>	<p>CHECKED BY</p>
<p>DATE</p>	<p>DATE</p>

700284-000B

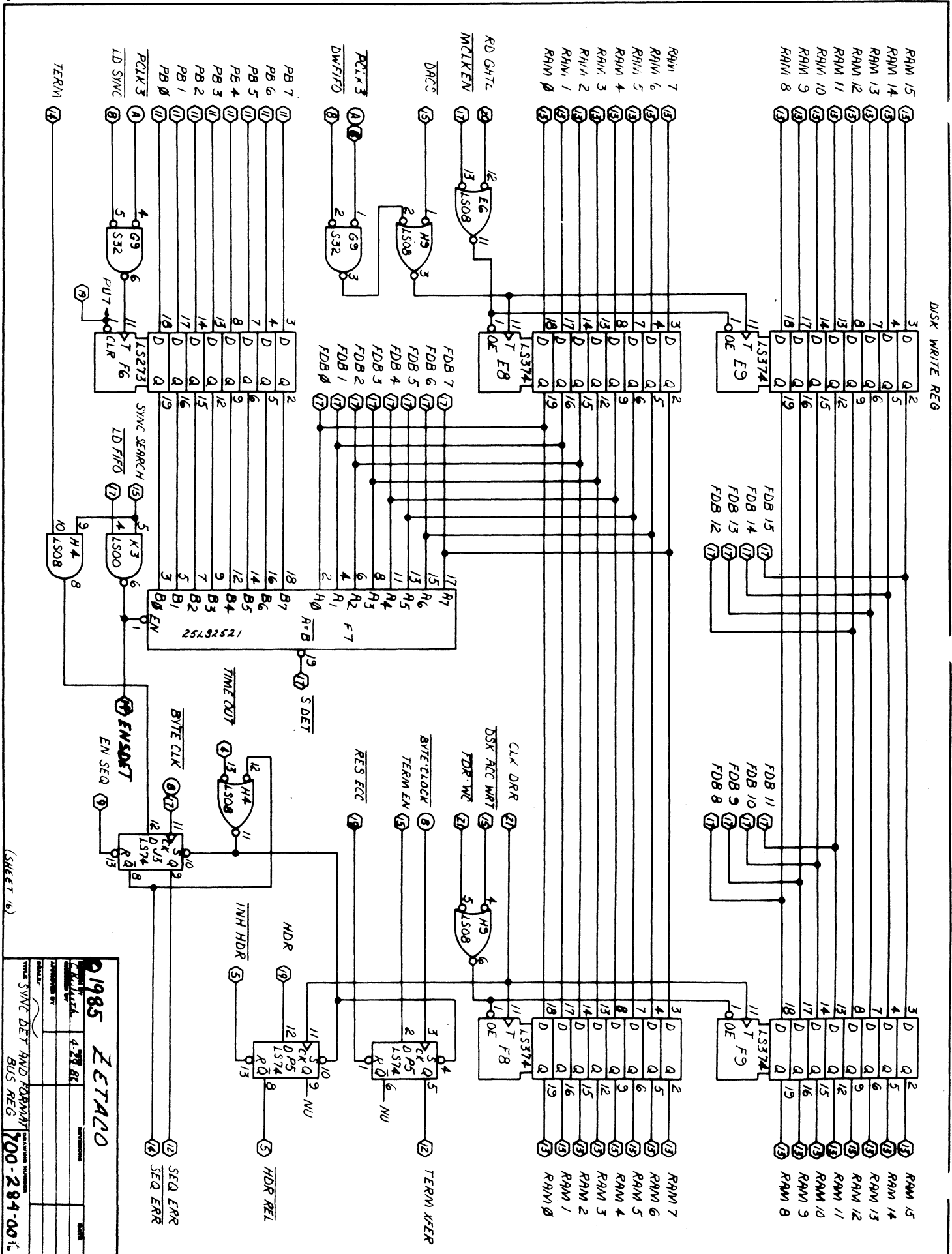


(SHEET 1/5)

1985 ZETACO

DATE	4/28/82	REVISION	
DESIGNED BY		APPROVED BY	
CHECKED BY			
TITLE	RAM CONTROL	DRAWING NUMBER	700-284-00

700284-000 B



01985 ZETACOR

DATE: 4-28-82

DESIGNED BY: []

CHKD BY: []

DATE: []

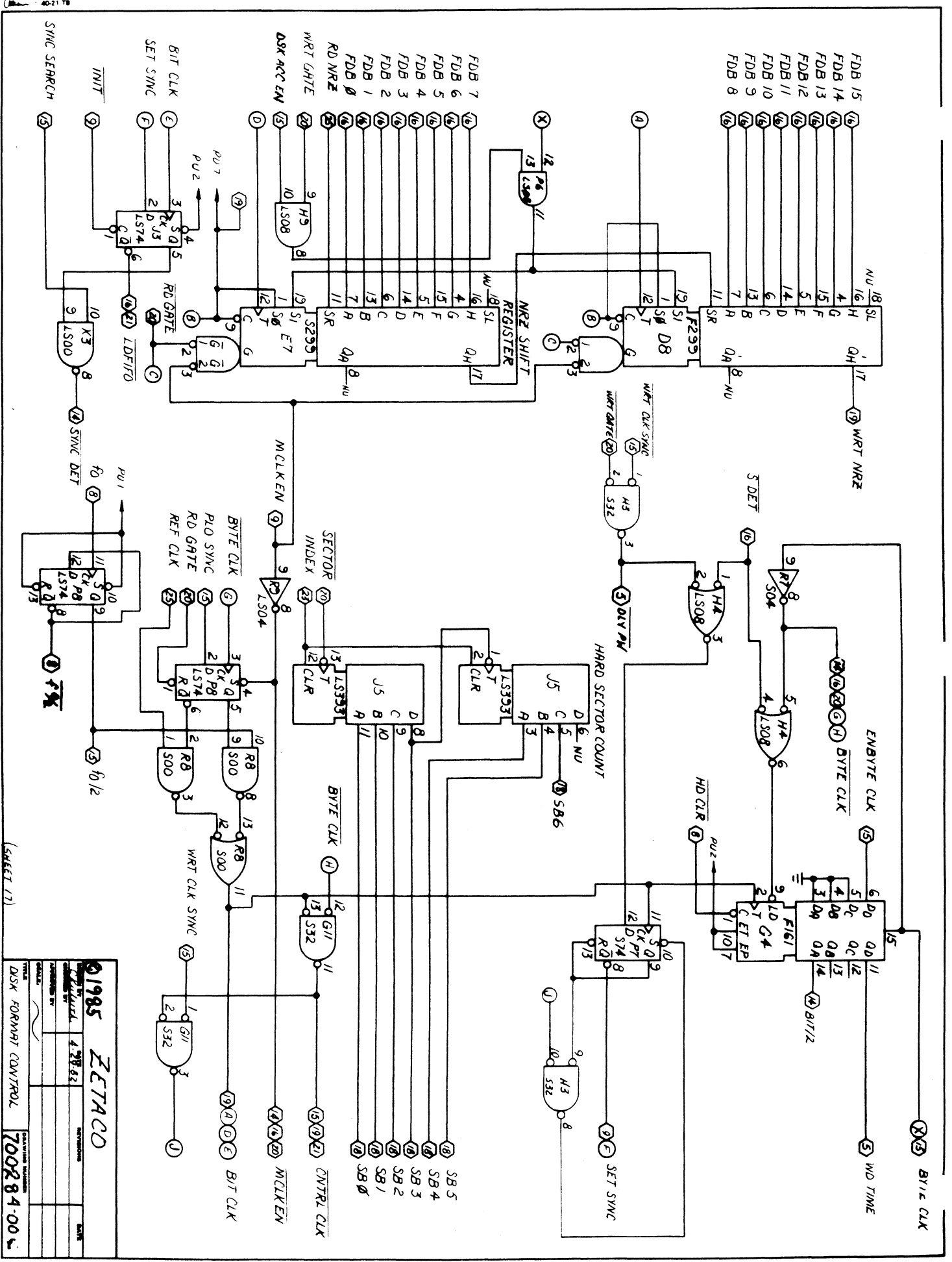
FILE: SYNC DET AND RAM/REG CONTROL SIGNALS

BUS REG 700-284-001

DATE: []

(SHEET 6)

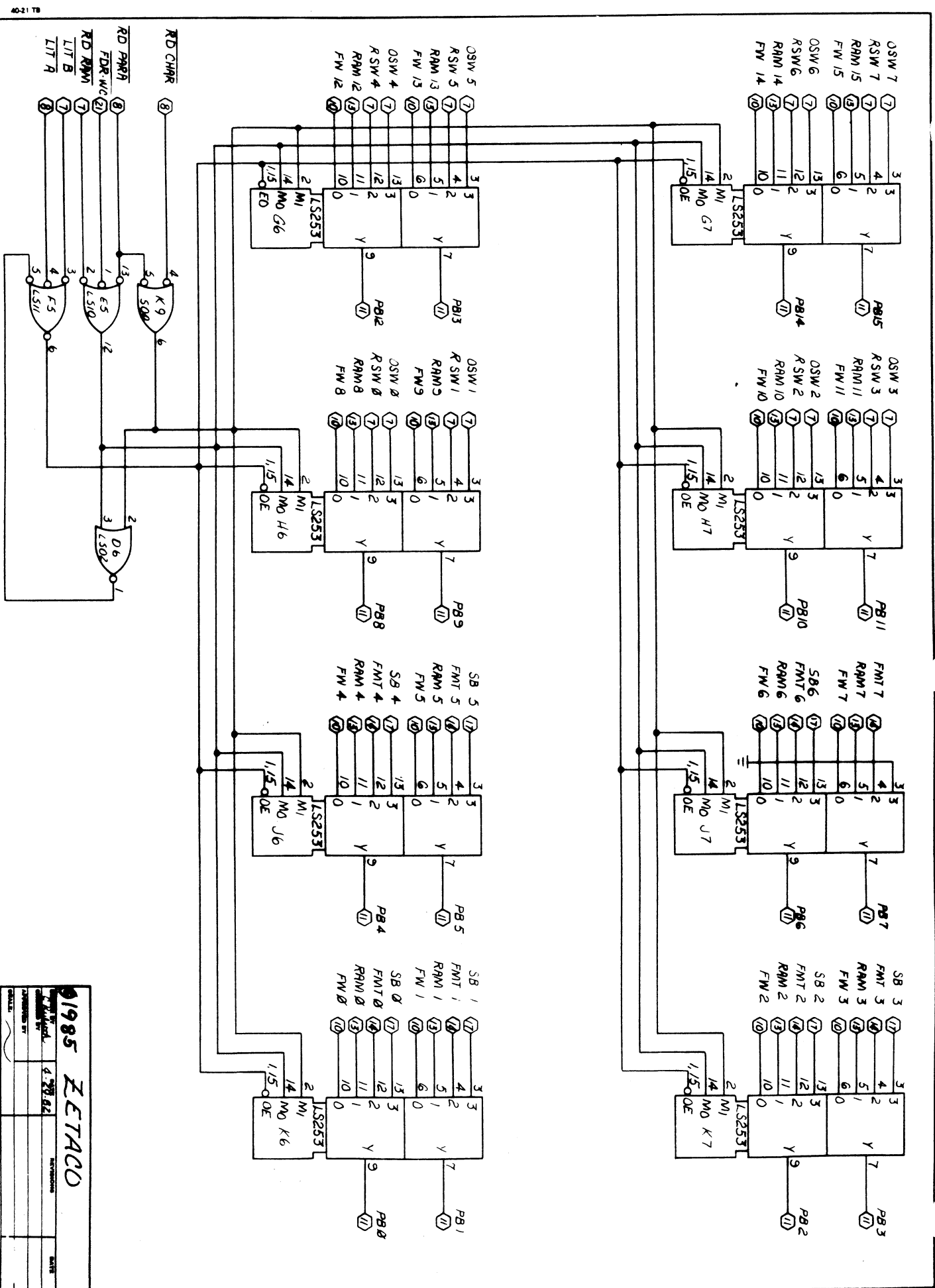
700284-000 B



01985 ZETACO		DRAWING NUMBER	
DATE	4-28-82	700284-000	
DESIGNED BY			
CHECKED BY			
APPROVED BY			
TITLE	DISK FORMAT CONTROL		

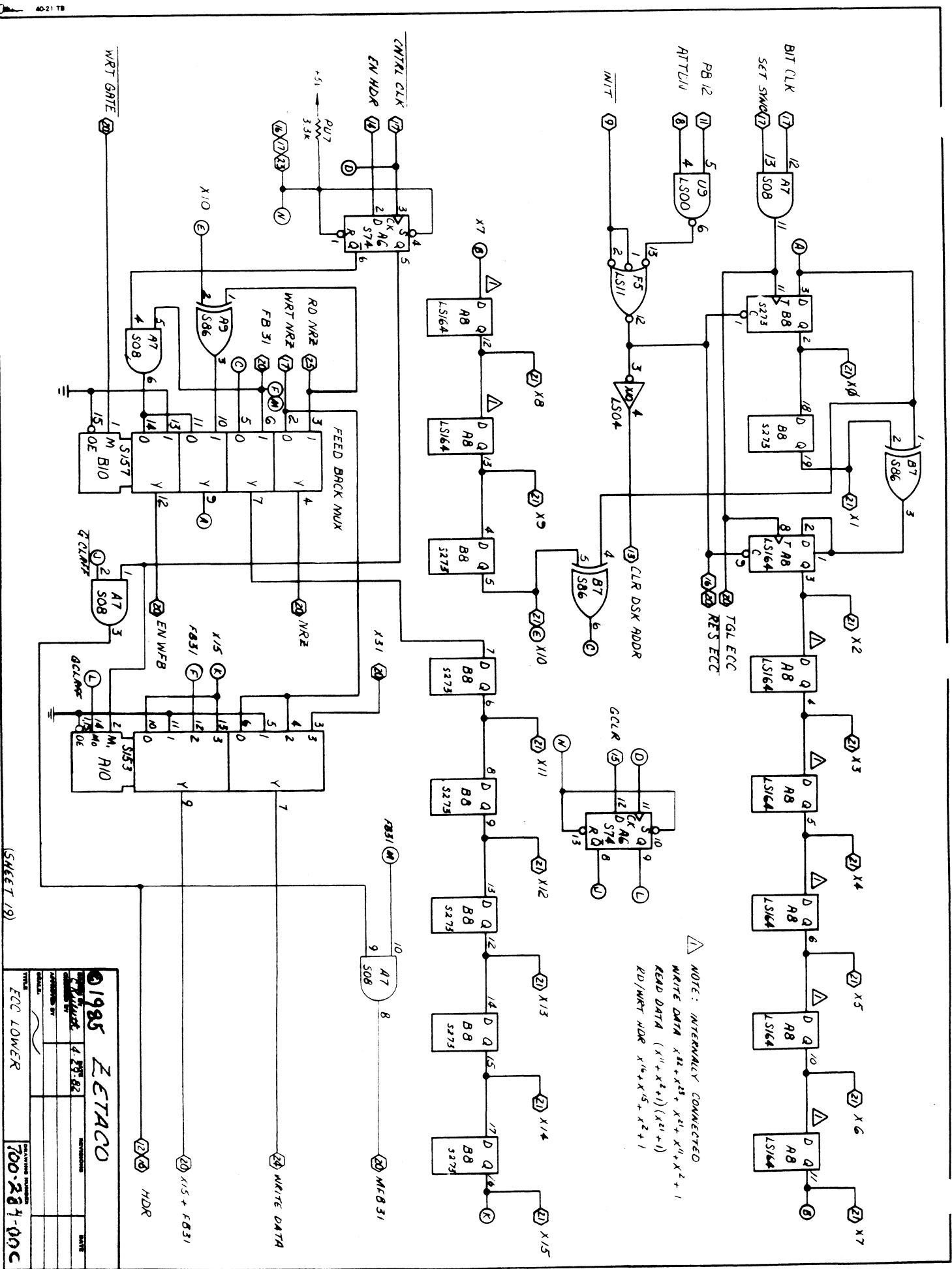
(Sheet 17)

700284-000 B



(SEELET 18)

<p>1985 ZETACO</p>	
<p>DATE: 4-28-82</p>	<p>BY: [Signature]</p>
<p>DESIGNED BY: [Signature]</p>	<p>CHECKED BY: [Signature]</p>
<p>TITLE: PB READ MUX</p>	<p>NO: 700-284-000 C</p>

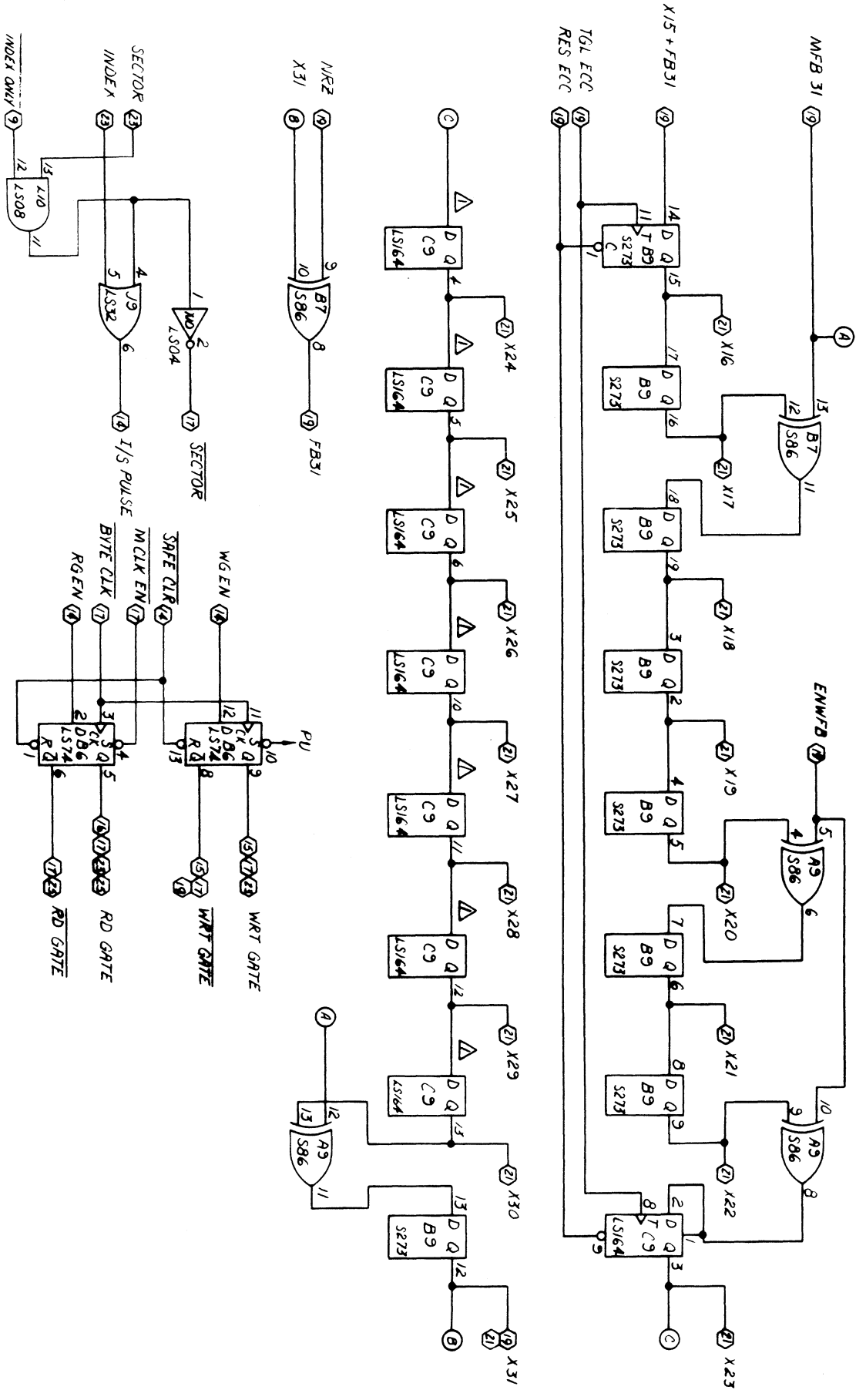


NOTE: INTERNALLY CONNECTED
 WRITE DATA $x^{22} + x^{23} + x^2 + x^{11} + x^2 + 1$
 READ DATA $(x^{11} + x^2 + 1)(x^{21} + 1)$
 RD/WRT HDR $x^{16} + x^{15} + x^2 + 1$

(SHEET 19)

1985 ZETACO	
DATE	4-29-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
REVISIONS	
DATE	
BY	
REASON	
ECC LOWER	
700284-000C	

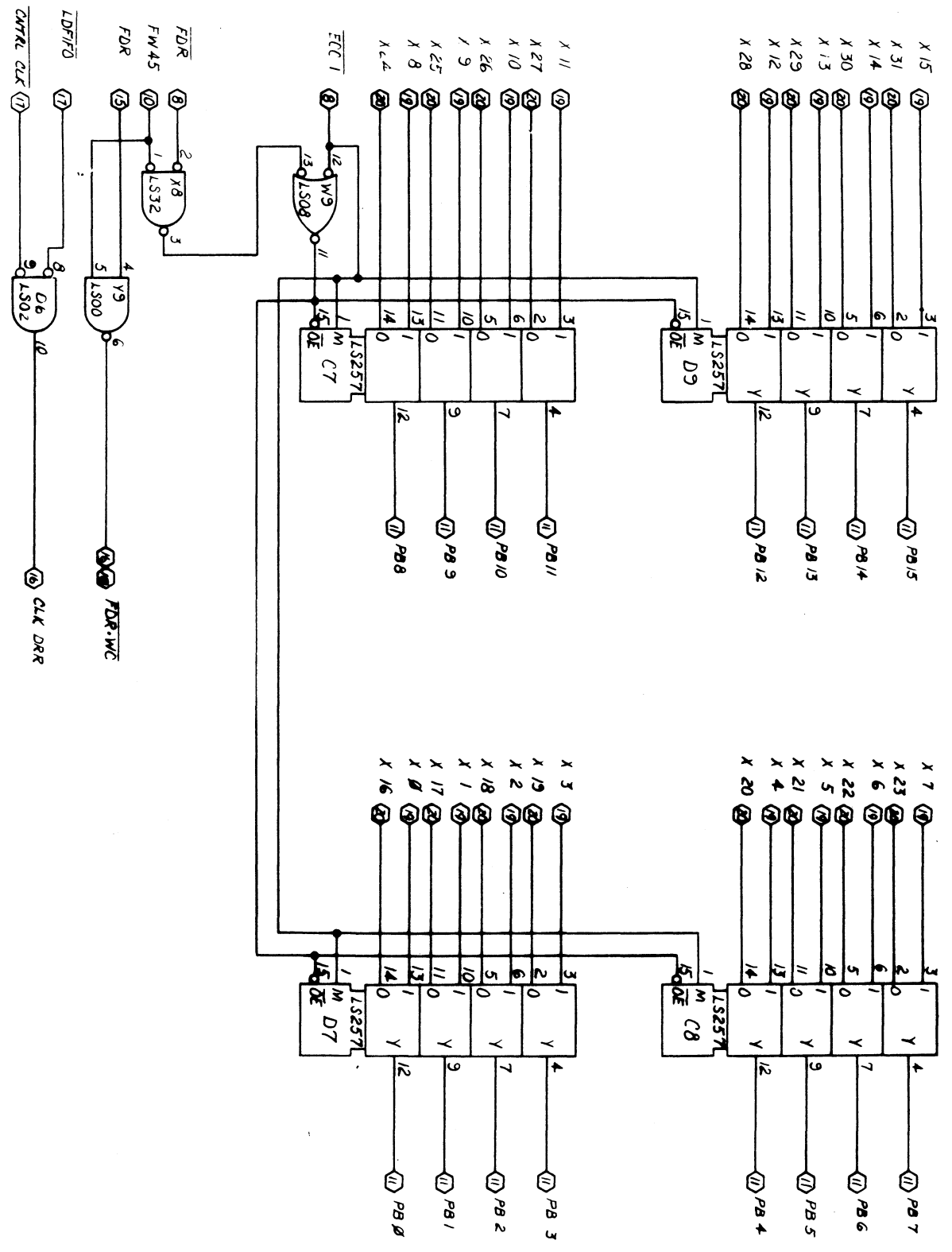
700284-000 B



NOTE: INTERNALLY CONNECTED

(SHEET 20)

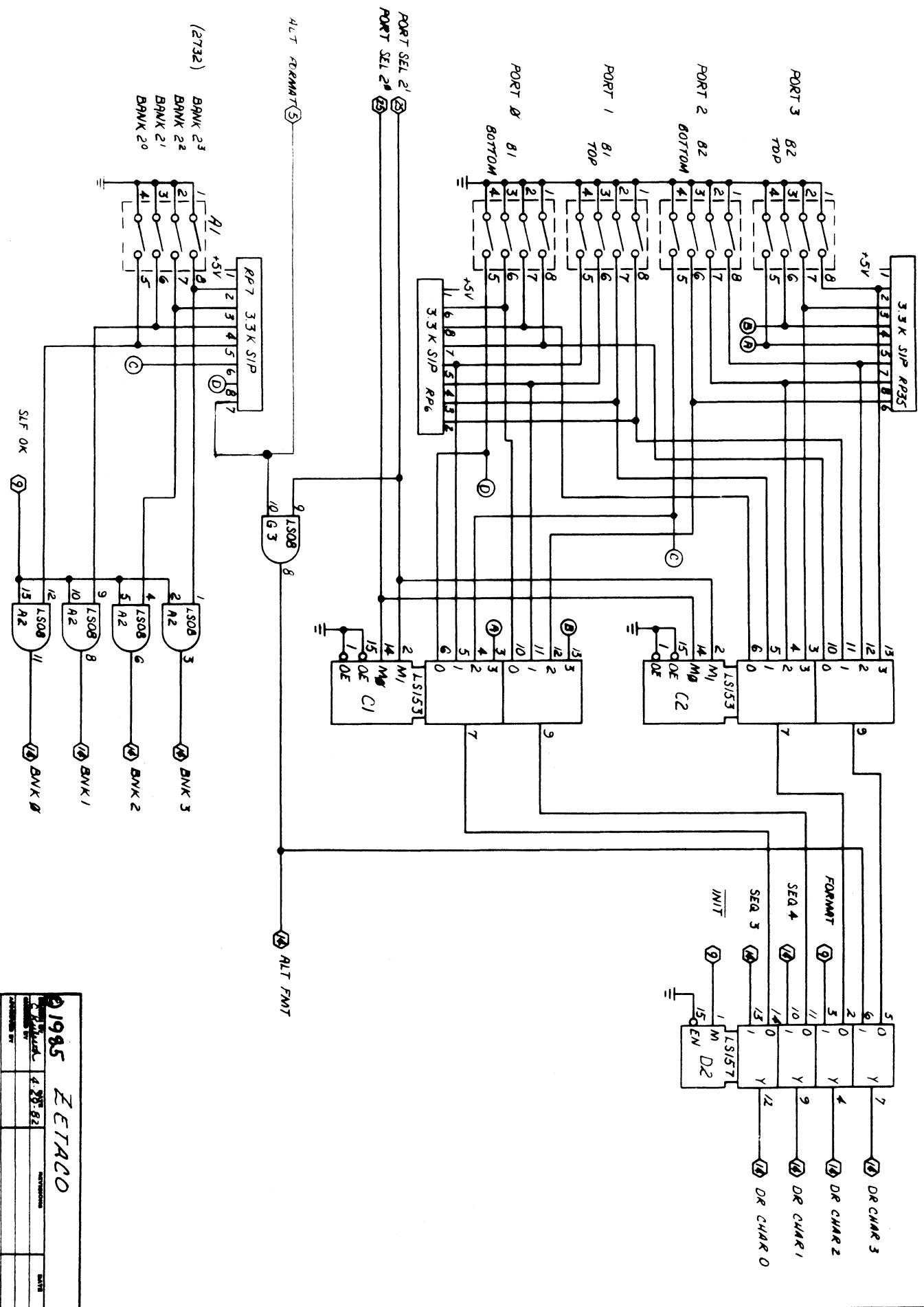
01985 ZETACO		DATE
REVISED	4-28-82	
DESIGNED BY		
CHECKED BY		
TITLE	ECC UPPER	DRAWING NUMBER
		700-284-00C



(SHEET 21)

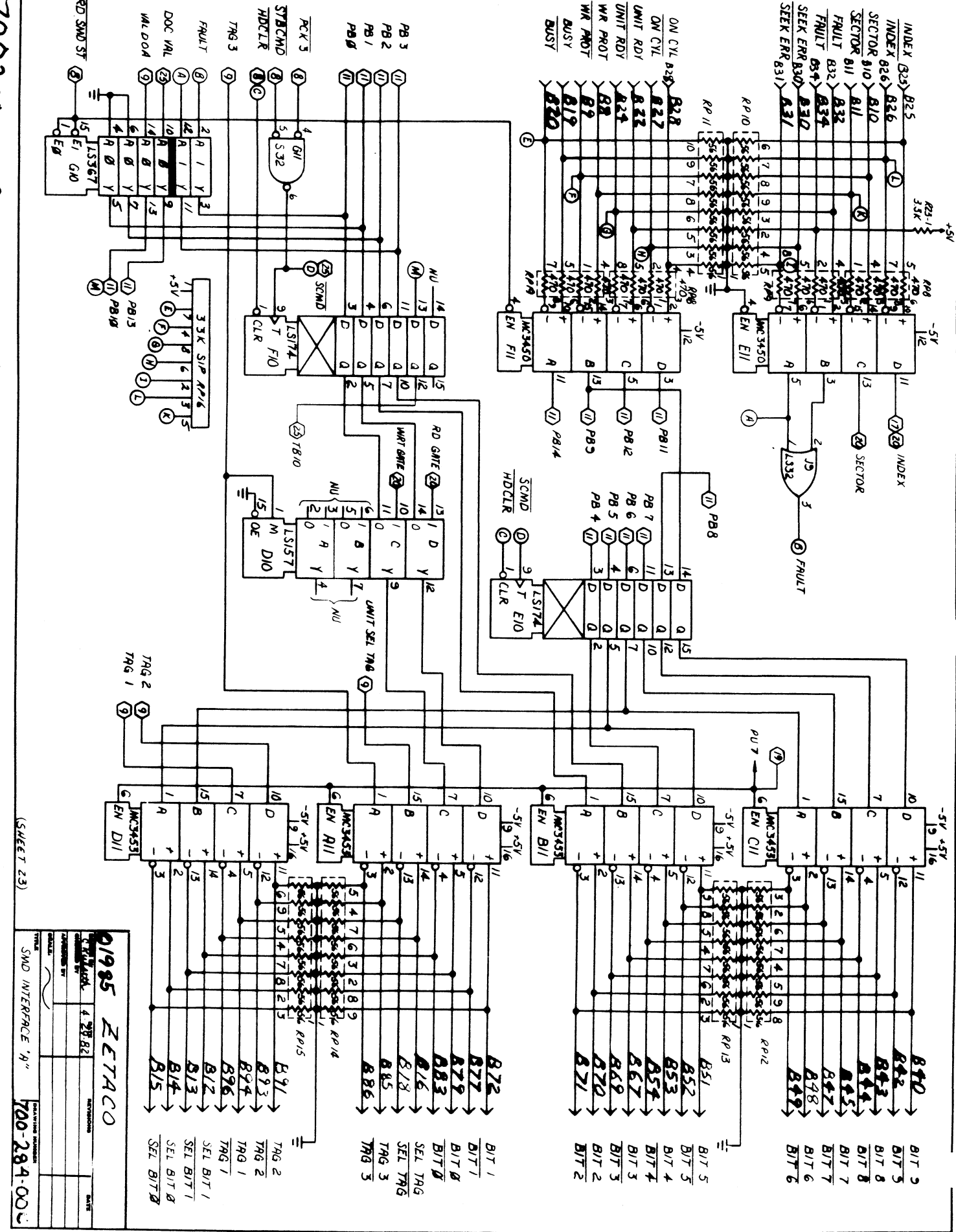
<p>91985 ZETACO</p>	
<p>DATE: 4-28-82</p>	<p>DESIGNED BY: []</p>
<p>DRAWN BY: []</p>	<p>CHECKED BY: []</p>
<p>APPROVED BY: []</p>	<p>DATE: []</p>
<p>REVISIONS:</p>	<p>700-284-00C</p>

700284-000 B



(SHEET 22)

1985 ZETACO		DRAWING NUMBER	
DATE	4-28-82	700-284-000	
DESIGNED BY			
CHECKED			
FORMAT BANK SELECT		DRAWING NUMBER	
		700-284-000	

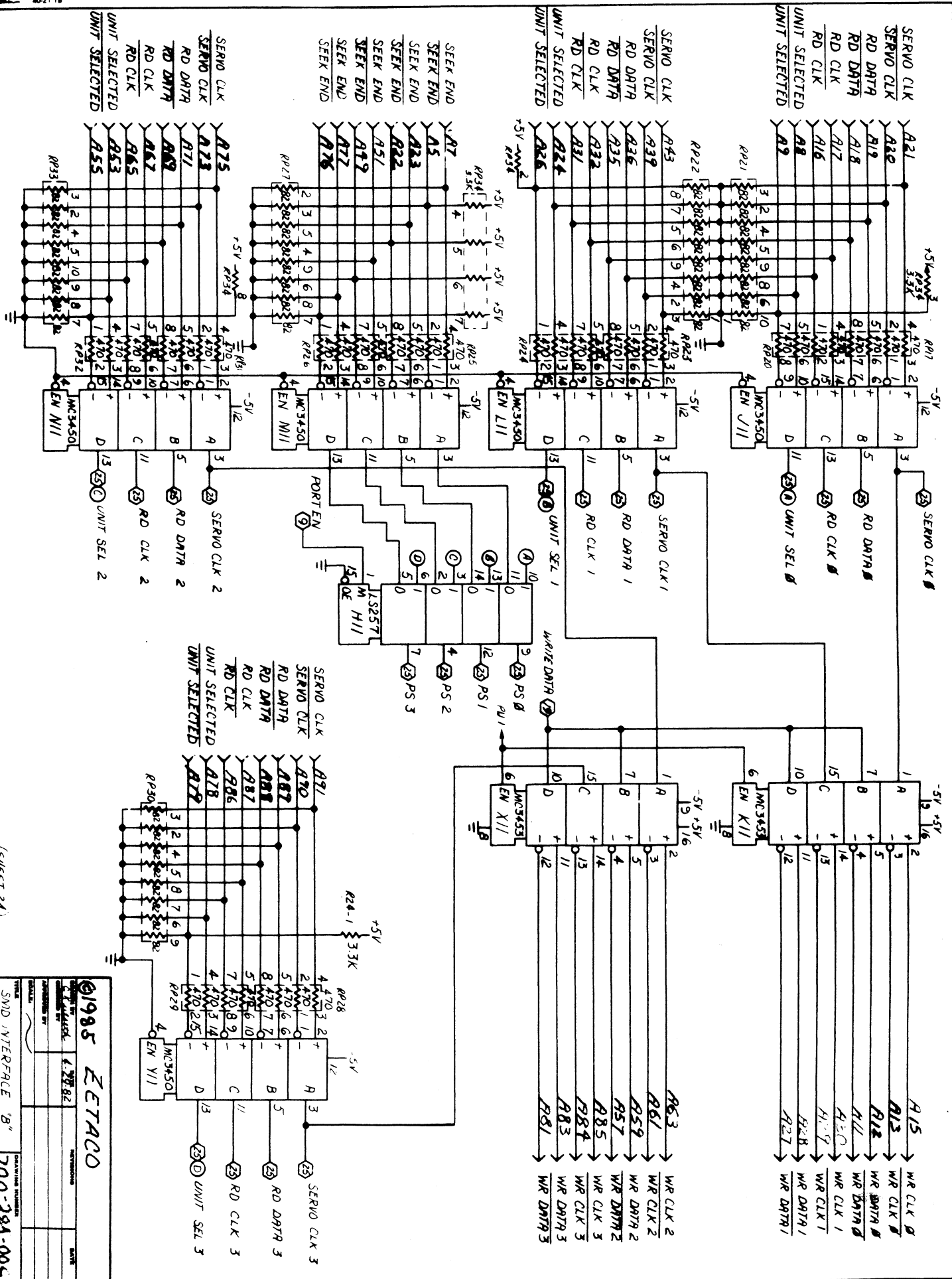


700294-000 B

01985 ZETACCO	
DATE	4-28-82
DESIGNED BY	
CHECKED BY	
APPROVED BY	
REVISION	
SMD INTERFACE 'A'	
700-294-000	

(SHEET 23)

700284-000 B

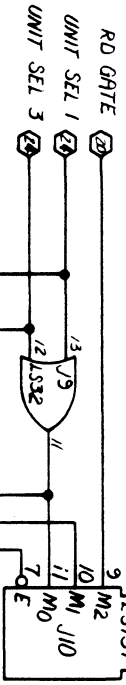
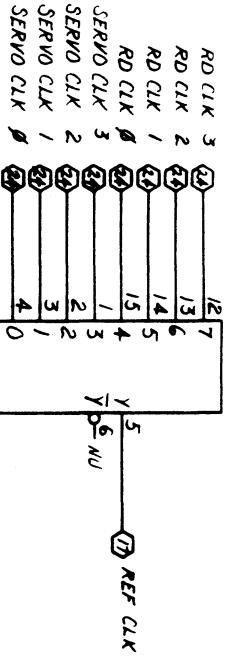


(SHEET 24)

©1985 EETACO

DATE	REV
DESIGNED BY	4/28/82
CHECKED BY	
DATE	

700-284-00C



RD GATE

UNIT SEL 1

UNIT SEL 2

UNIT SEL 3

UNIT SEL 4

UNIT SEL 5

UNIT SEL 6

UNIT SEL 7

UNIT SEL 8

UNIT SEL 9

UNIT SEL 10

UNIT SEL 11

UNIT SEL 12

UNIT SEL 13

UNIT SEL 14

UNIT SEL 15

UNIT SEL 16

UNIT SEL 17

UNIT SEL 18

UNIT SEL 19

UNIT SEL 20

UNIT SEL 21

UNIT SEL 22

UNIT SEL 23

UNIT SEL 24

UNIT SEL 25

UNIT SEL 26

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UNIT SEL 84

UNIT SEL 85

UNIT SEL 86

UNIT SEL 87

UNIT SEL 88

UNIT SEL 89

UNIT SEL 90

UNIT SEL 91

UNIT SEL 92

UNIT SEL 93

UNIT SEL 94

UNIT SEL 95

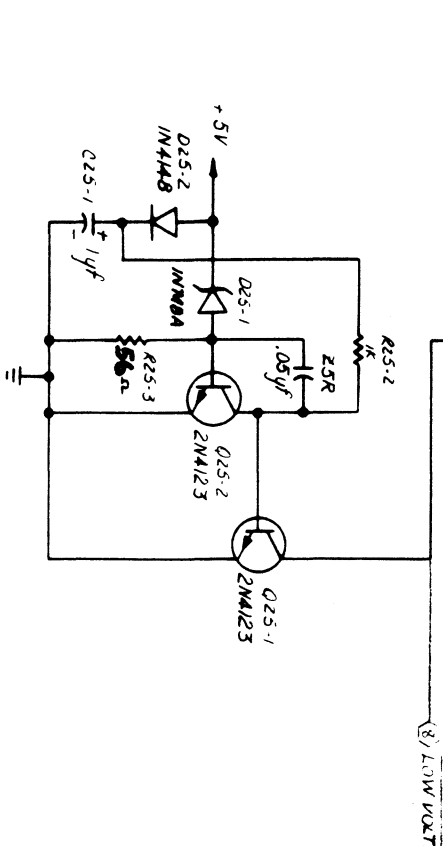
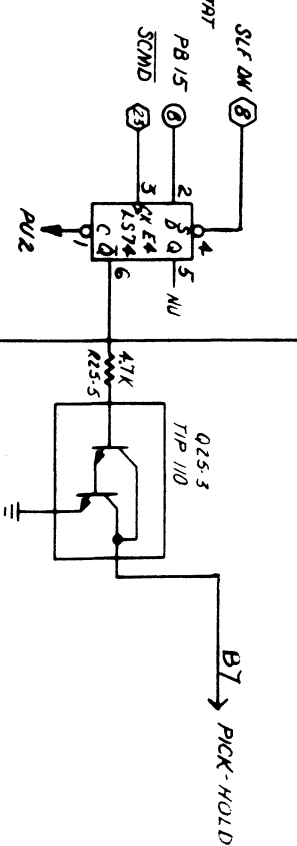
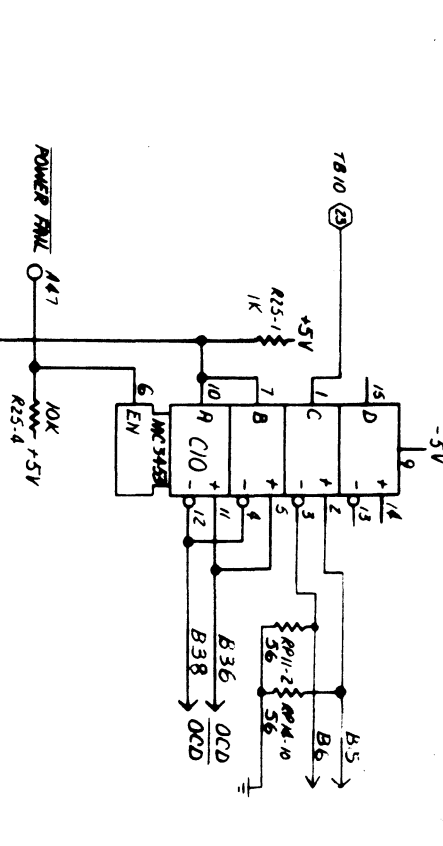
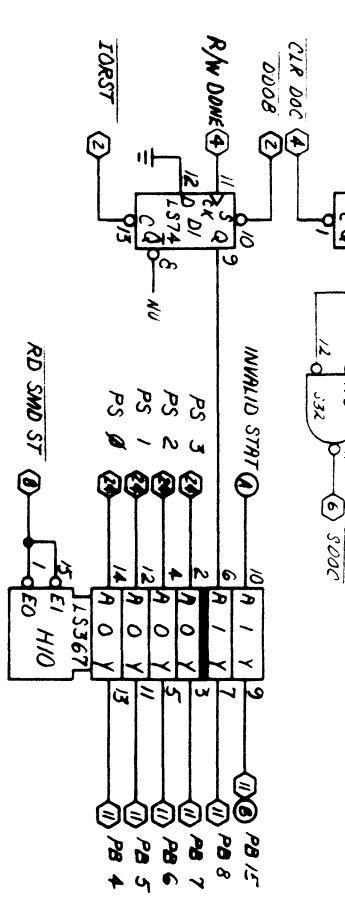
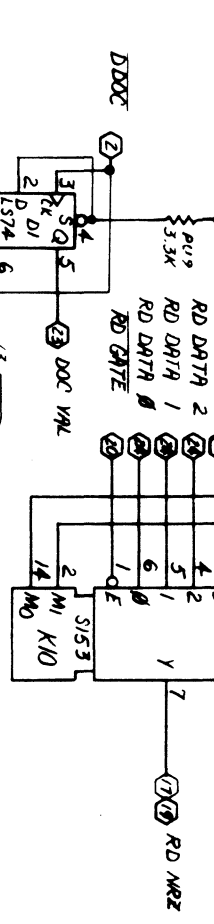
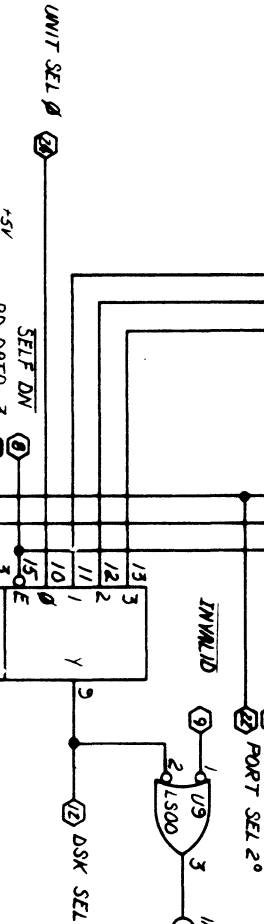
UNIT SEL 96

UNIT SEL 97

UNIT SEL 98

UNIT SEL 99

UNIT SEL 100



[SHEET 25]

1985 ZETACO		DRAWING NUMBER 700-284-00	
DESIGNED BY	DATE	REVISIONS	DATE
CHECKED BY			
SMD INTERFACE CONTROL			

700284-000 B