Model 450

Multi-Device Interface Controller

235-T35-VV0-00

REVISION HISTORY		
ECO #	DATE	DESCRIPTION
0328	6/28/84	New ZETACO Cover

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MULTI-DEVICE INTERFACE CONTROLLER

1.0 General Description

The Multi-Device Interface Controller is a high density printed circuit board which will support the following devices: two serial ports, real time clock, programmable interval timer, and a four channel asynchronous multiplexer.

1.1 Console Terminal Controller

This controller provides interface logic for the system serial console terminal (device code 10/11) which can be either a current loop or RS-232 device operating in a full duplex mode. Baud rates (110 to 19.2K) and data format are switch/jumper selectable on the board. Flexible interface logic permits the use of a CRT, teletype or teleterminal device as the system console.

1.2 Second Console Terminal Controller

This option contains the logic for a second serial terminal device channel with an RS-232C or current loop interface. Baud rates (110 to 19.2K) and data format are switch/jumper selectable on the board. The device code is normally set at 50/51 but is jumper selectable for any device code. This controller is frequently used to control a line printer with a serial interface.

1.3 Programmable Real Time Clock

The Real Time Clock controller provides four frequencies selectable under program control: 60Hz, 10Hz, 100Hz and 1000Hz. Frequency sources are the AC lines for 60Hz and a crystal oscillator for the other frequencies.

1.4 Programmable Interval Timer

The Programmable Interval Timer is a user programmable timer which will generate an interrupt after a specified time delay. Four clocking rates (1usec, 10usec, 100usec, 1msec) are switch selectable.

1.5 Asynchronous Multiplexer

This controller provides control for four asynchronous serial ports which may be teleterminals or CRT's. Baud rates and data formats are selectable, on an individual channel basis, under program control. Full modem control is incorporated into each channel for use in remote communication applications.

1.6 Documentation Package

The controller board is shipped with a complete documentation package, including installation instructions, programming instructions and logic schematics.

2.0 Installation Instructions

2.1 Unpacking

Upon receiving the interface package, unpack the contents and inspect the board for visual damage. If any damage is apparent, do not attempt to install the controller but notify Custom Systems, Inc., immediately.

2.2 Board Installation

The controller board is usually installed in the general input/output slot of the Data General Nova or Eclipse minicomputer. In the case of a Nova 1200 Series or Nova 2, this is the third board slot from the bottom of the computer. For a Nova 3 or an Eclipse, the general I/O slot is slot 4. Install the controller in the desired slot, component side up, and lock into position with the release levers. (See Figure 2)

If with the selection of the I/O slot a vacant slot or slots exist between the controller and the board below it, the DCHP (Data Channel Priority) and INTP (Interrupt Priority) signals must be physically jumpered on the computer backpanel to maintain priority interrupt continuity. Install one end of a wire-wrap jumper to the DCHP - OUT signal at pin 93 at the "A" connector occupied by the device below the controller. Connect the remaining end to the DCHP - IN signal at pin 94 of the "A" connector occupied by the controller, bridging the vacant slot or slots. Similarly, connect the INTP-OUT signal (pin A-95) from the lower device to the INTP-IN signal at pin A-96 of the controller. This will complete the priority interrupt continuity to the card. If vacant slots exist between the controller and the device above the controller, perform similar strapping of the DCHP and INTP signals to maintain interrupt priority.

2.3 Computer Back Panel

The back panel of the computer provides a means for interconnecting the computer, memory, console and various controller boards and cabling to external peripheral equipment. The back panel is the vertical printed circuit board mounted on the left side of the computer chassis when viewed from the front.

On the side of the back panel facing into the chassis are 10 or 12 pairs of printed circuit board female edge connections, one pair for each slot (Figure 2-1). The contact, of these connectors protrude through the back panel to the left side of the minicomputer chassis.

When the male edge connectors of a printed circuit board are inserted into the female edge connectors of a slot, finger contacts on the male edge connectors meet contacts in the female edge connectors. Electrical connections to boards can, therefore, be made to pins on the back panel.

For each controller card slot, there are two horizontal parallel rows of 100 pins on the back plane. The left group of pins is the A connector, and the right group (as viewed from the left side of the computer) is called the B connector. Numbering of each group of 100 pins is as indicated below (shown only for connector A).

BACK PANEL NUMBERING

A1	A3	A5	A7	A9	A11	A13	A15	A17	A19	A21	A23	A25	A27	A29	A31	A33	A35	A37	A39	A41	A43	A45	A47	A49
A2	A4	A6	A8	A10	A12	A14	A16	A18	A20	A22	A24	A26	A28	A30	A32	A34	A36	A38	A40	A42	A44	A46	A48	A50

A51	A53	A55	A57	A59	A61	A63	A65	A67	A69	A71	A73	A75	A77	A79	A81	A83	A85	A87	A89	A91	A93	A95	A97	A99
A52	A54	A56	A58	A60	A62	A64	A66	A68	A70	A72	A74	A76	A78	A80	A82	A84	A86	A88	A90	A92	A94	A96	A98	A100

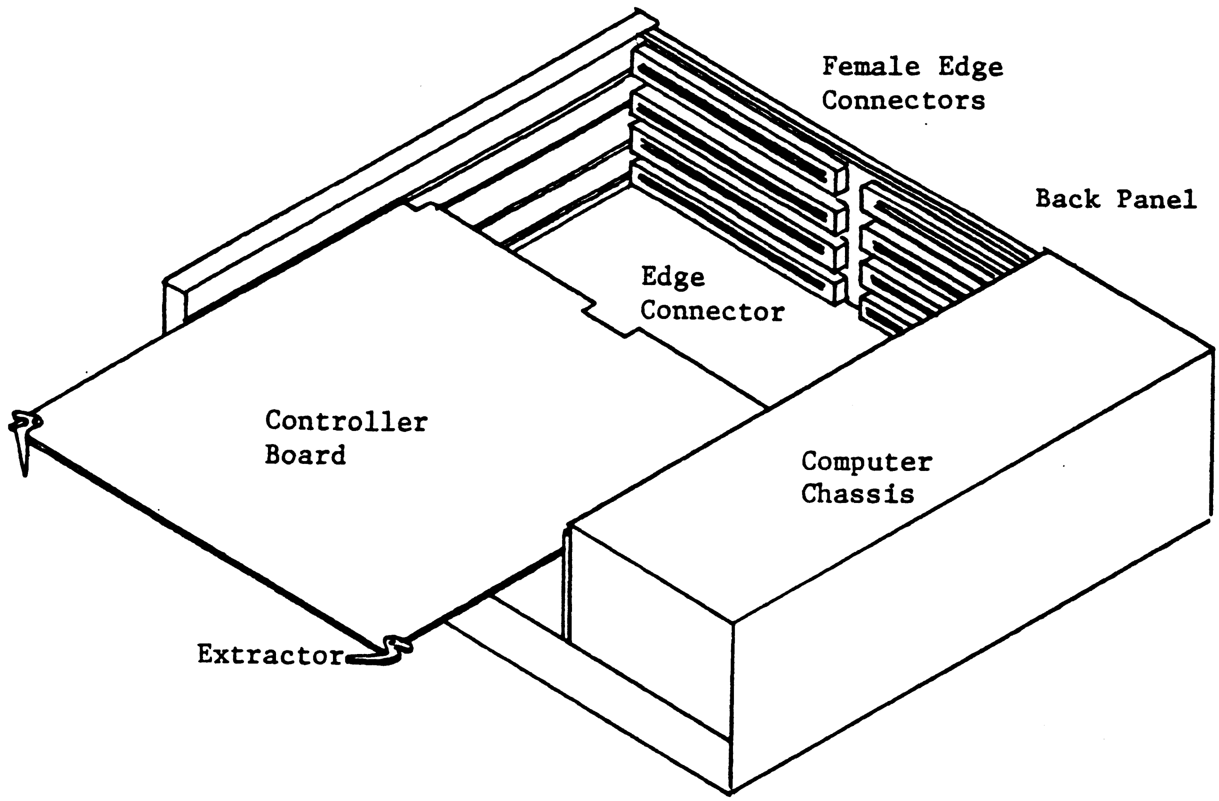


Figure 2-1 : Board Installation

Pin 1 is on the top left of the connector; pin 2 is on the bottom left directly below pin 1. Pin 99 is the top right pin of the connector, and pin 100 is the bottom right.

3.0 Serial Communications Devices

3.1 General Description

The controller can be configured for up to two serial peripheral devices. Most commonly, this will consist of the system console teletype or CRT (device 10/11) and, in larger system, a second CRT (device 50/51). Either of the two channels may be configured for a current loop or RS232C interface. Available baud rates cover the range from 110 baud to 19.2K baud.

3.2 Programmers Reference Information

The Console Serial Device controller is set up to handle full duplex communications with Model ASR-33, KSR-33 or KSR-35 teletypes at a speed of 10 characters per second or a CRT at speeds up to 19.2K baud. Each serial device controller has separate input and output functions and is really two distinct devices. Each has its own device code, BUSY, DONE, and INTERRUPT DISABLE flags.

Output To The Terminal

Output from the computer to the console terminal requires only one I/O instruction. The device code is 11 and the interrupt priority mask bit is 15. A character is transferred to the display terminal with a Data Out A instruction. The ASCII character code is placed in bits 8-15 of the selected accumulator. The START function is used to set BUSY which in turn causes the contents of the controller output buffer to be serially shifted out to the terminal. The terminal displays or prints the character or performs the indicated control function. Completion of transmission clears BUSY, sets DONE and requests an interrupt if the INTERRUPT DISABLE flag is clear.

Input From The Terminal

Input to the computer from the terminal also uses only one I/O instruction. The device code is 10 and the interrupt priority mast bit is 14. The logic of the input controller is slightly different than other input controllers in that striking a key on the keyboard will cause the code from the terminal to be serially shifted into the controller input buffer. This will occur irrespective of whether the program has previously set the BUSY flag or not.

Under normal operation, the BUSY flag is set with a NIOS instruction prior to when data is expected to be received from the terminal. The DONE flag is set, BUSY cleared and an interrupt generated (unless the DISABLE flag is set) when the character has been serially shifted into the teletype controller buffer. The eight bits which comprise the character are brought into the accumulator with a Data In A instruction.

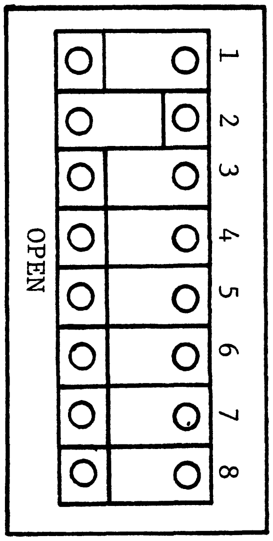
3.3 Selectable Options

The serial console devices can be configured for different baud rates 110 baud to 19.2K and RS232 or 20ma current loop. Also console 2 can be alternately set for a device code other than 50/51 via jumpers.

Baud Rate Selection

Serial Console 1 (Device 10/11) = Switch Pack at Location J6

Serial Console 2 (Device 50/51) = Switch Pack at Location K7



9,600 Baud Shown

S1 Closed = 19,200 Baud
S2 Closed = 9,600 Baud
S3 Closed = 4,800 Baud
S4 Closed = 2,400 Baud
S5 Closed = 1,200 Baud
S6 Closed = 600 Baud
S7 Closed = 300 Baud
S8 Closed = 110 Baud

RS232C/Current Loop Jumpering

Each Console Serial Port may be selected for either RS-232C(EIA) or current loop input/output by jumper changes. (Reference jumper option sheet).

Serial Console Port 1

RS-232C	Current Loop
J6-5 In	J6-5 Out
J6-1 Out	J6-1 In
J6-2 Out	J6-2 In
J6-4 Out	J6-4 In

Serial Console Port 2

RS-232C	Current Loop
J8-4 In	J8-4 Out
J8-1 Out	J8-1 In
J8-2 Out	J8-2 In
J8-5 Out	J8-5 In

Device Code Selection (Serial Channel #2)

The device code for the first serial channel is usually set at 10/11. Unless otherwise specified, the second channel comes wired as 50/51. For special applications, other device codes may be used for the second serial channel. The device code is determined by five hard wire jumpers J9-1 through J9-5. The table provides a guide to selecting non-standard device codes.

Device Code Selection Table

CRTII	J9-1 (DS0)	J9-2 (DS1)	J9-3 (DS2)		J9-4 (DS3)	J9-5 (DS4)
0X	IN	IN	IN	X0+1	IN	IN
1X	IN	IN	OUT	X2+3	IN	OUT
2X	IN	OUT	IN	X4+5	OUT	IN
3X	IN	OUT	OUT	X6+7	OUT	OUT
4X	OUT	IN	IN			
5X	OUT	IN	OUT			
6X	OUT	OUT	IN			
7X	OUT	OUT	OUT			

Jumper OUT = 1 bit; Jumper IN = 0 bit. Reference the assembly drawing for the location of these jumpers.

4.0 Programmable Real Time Clock

4.1 General Description

The Real Time Clock controller provides a series of timing pulses which are independent of the minicomputer processor timing. The clock option consists of four frequencies (10, 60, 100, 1000Hz) which are selectable under program control and can provide program timing and scheduling interrupts at the pre-selected rate.

The 60 cycle frequency is derived from the line frequency which operates the computer. The other three frequencies are derived from a crystal controlled oscillator.

NOTE: If the board is inserted in a slot other than slot 3 or 4 a jumper has to be installed from pin B6 of slot 3 or 4 to pin B6 of the slot the board resides in.

4.2 Programmers Reference Information

The controller for the Real Time Clock options uses the standard clock instruction set as outlined in the Nova Programmers Reference Manual. The Real Time Clock option consists of four frequencies (10, 60, 100, 1000Hz) which are selectable under program control.

One I/O instruction is required to set the clock frequency. BUSY and DONE are controlled or sensed by bits 8 and 9 in all I/O instructions. The device code is 14 and the interrupt priority mask bit is 13.

The clock frequency to be used is selected with a DATA OUT A instruction to the Real Time Clock. The referenced accumulator will contain the desired frequency in bits 14 and 15 as follows:

AC Bits 14-15	Frequency
00	AC Line Frequency
01	10Hz
10	100Hz
11	1000Hz

As with all other peripheral controllers, the BUSY flip flop is set by the START signal (NIOS instruction). The next pulse from the selected clock will then set DONE, requesting an interrupt if INTERRUPT DISABLE is clear. A DOA instruction to select the frequency need be given only once; following each interrupt a NIOS sets up the clock for the next pulse.

When BUSY is first set, the first interrupt can come up at any time up to the clock period. But, once one interrupt has occurred, further interrupts are at the clock frequency selected, provided the program always sets BUSY before the next period expires.

The Real Time Clock option is used for low resolution timing compared to processor speed, but it has high long-term accuracy. Power turn on or the RESET function generated by either the program or the minicomputer console will reset the clock to line frequency. Following power turn on, the line frequency pulses are available immediately, but up to five seconds may elapse before a steady pulse train is available from the crystal for other frequencies.

5.0 Programmable Interval Timing

5.1 General Description

The Programmable Interval Timer (PIT) is a general purpose timer which may be programmed to generate an interrupt after a specific time delay. The PIT allows the user the flexibility of generating an interrupt at a rate of his own choice or at a fixed interval as with the Real Time Clock.

The PIT is selectable to any of the 64 Device Codes, and uses mask bit 6 to inhibit interrupts. Data General software supports a PIT Device Code of 43_8.

The PIT contains a 16 bit counter which must be loaded with the two's complement of the desired time count. If jumper J11-12 is installed the counter must be loaded each time a time delayed interrupt is required by the program. If jumper J11-1 is installed it is only necessary to load the counter once and a time delay interrupt will occur repeatedly at the fixed interval. (Similar operation to RTC).

Counting begins when a start pulse is issued. The current count contained in the 16 bit counter can be read out in two's complement notation.

5.2 Programming Notes

Two instructions in the standard I/O format program the PIT. One of these instructions supplies the controller with the information necessary to begin the counting operation. The second instruction allows the program to determine the current count contained in the TIME COUNT REGISTER.

The device flag commands control the timer's BUSY and DONE flags as follows:

f = S	Initiates the counting sequence by setting the BUSY flag to one and the DONE flag to zero.
f = C	Clears the PIT by setting the DONE flag to one and the BUSY flag to zero. Also resets the TIME COUNT REGISTER.
f = P	Used to set the Diagnostic Mode and then pulse the Commercial I/O Subassembly timing generation circuit.

5.2.1 Load Time Count Register

DOA (f) ac, PIT

0	1	1	ac		0	1	0	f		device code					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

This instruction loads bit 0-15 of the specified AC into the PIT Time Count Register. After the data transfer, the PIT's BUSY and DONE flags are set according to the function specified by F. The specified accumulator must be preloaded with the two's complement of the Starting Time Count.

5.2.2 Read Time Count Register

DIA (f) ac, PIT

0	1	1	ac		0	0	1	f			device code				
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

This instruction places the contents of the PIT Time Count Register into bits 0-15 of the specified AC. After the data transfer, the PIT's BUSY and DONE flags are set according to the function specified by F.

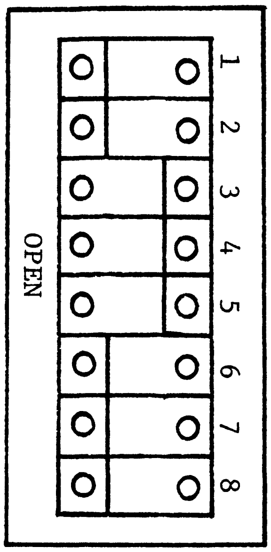
The data placed into the specified AC is the two's complement of the current time count.

5.3 Device Selection Switches

Pit Device Selection is configured as follows:

Open = 1

Closed = 0



S1 = DS5 - Least Significant Bit

S2 = DS4

S3 = DS3

S4 = DS2

S5 - DS1

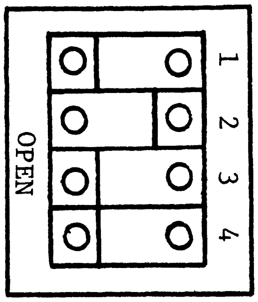
S6 = DS0 - Most Significant Bit

S7, S8 — Not Used

Device Code 43_8 Shown

5.4 Selectable Options

Programmable Interval Timer Clock selection.



100KHz Shown

S1 Closed = 1MHz or 1 uSec
S2 Closed = 100KHz or 10 uSec
S3 Closed = 10KHz or 100 uSec
S4 Closed = 1KHz or 1 mSec

6.0 Programmable Asynchronous Multiplexer

6.1 Introduction

The ZETACO, Inc. Asynchronous Line Multiplexer (Multiplexer) enables any Data General Nova or Eclipse Line Computer to communicate with and control four serial terminal devices (e.g. CRT, Modem). The multiplexer contains all logic necessary to receive, transmit, and control the exchange of data characters between the terminal devices and the computer. The Asynchronous Line Multiplexer is compatible with Data General's operating system and diagnostic software.

6.2 Programming Notes

The Multiplexer is accessed with a single device address (34 primary, 44 secondary) with a unique address (1 of 256) for each specific line Multiplexer. Each line is divided into three sections; Receiver Section, Transmitter Section and Modem Section. Any one of these can generate an interrupt when it requires service (if it is enabled).

The line being controlled is called the "Current Line Address" and can be set by a Set Line and Section instruction or a Read Line and Section Requesting Service instruction which is valid only if the Multiplexer's DONE flag is set.

The Receiver and Transmitter sections of each Multiplexer can be turned on or off. A section which is turned off is operable but cannot set DONE when it requires service. Modems are always turned on and may set DONE when service is required. The Multiplexer may also be in one two modes: online or offline. In offline mode the board is being controlled by diagnostic software. This software can step the internal state clock, monitor signal conditions and control the flags. In online mode the board runs via the internal crystal oscillator.

Interrupts are generated when any of the following conditions occur:

Receiver	- Whenever the receive character buffer is full
Transmitter	- Whenever the transmitter can accept a character
Modem	- Whenever a signal has changed state, or if the signal is a "1" when going online

These devices are arranged in a specific priority which reflect the urgency in which their service requests must be attended. These section priorities are as follows:

Receiver 0

Receiver 1

Receiver 2

Receiver 3

Transmitter 0

Modem 0

:

Transmitter 3

Modem 3

There are three device flag commands (f) which control interval operations on the Multiplexer board. They are as follows:

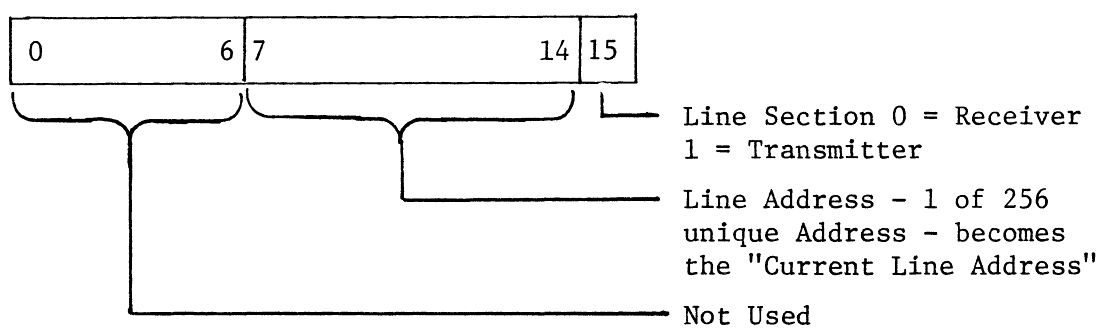
Flag	Function
f = S or IORESET	Set the busy flag to 1, clear the DONE flag, place the current board in offline mode. Initialize all logic, and then clear the BUSY flag.
f = C	Clear the current boards DONE flag, and/or place the board in online mode.
f = P	For use in offline mode only. Will step the internal state counter of the Mutliplexer board.

6.3 Instruction Formats

The Mutliplexer will respond to 9 instructions which control all the funtions required for asynchronous communications. However, some instructions use the same Data Out or Data In commands with the contents of the specified accumulator determining how the Mutliplexer board will function. All instructions affect only the "Current Line Address" once it has been set by a Set Line and Section or a Read Line and Section Requesting Service instruction.

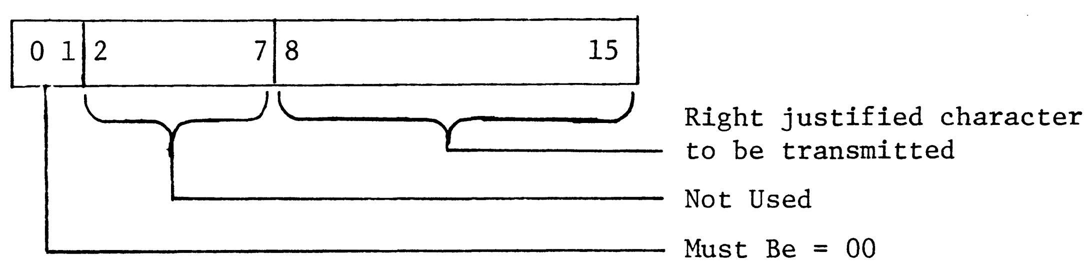
1) Set Line and Section

DOA (f) AC, MUX



2) Transmit Data

DOB (f) AC,MUX



3) Transmit Break

DOB (f) AC, MUX

0 1	2 7	8 15

- Bits 8–15: Must be all Zeros
- Bits 2–7: Not Used
- Bits 0–1: Must be = 01

4) Set Modem Control Status

DOB (f) AC,MUX

0 1	2 13	14	15

- Bit 15: State of "Data Terminal Ready" 0 = Off, 1 = On
- Bit 14: State of "Request to Send" 0 = Off, 1 = On
- Bits 2–13: Not Used
- Bits 0–1: Must be = 10

5) Control Line Section

DOC (f) AC,MUX

0 1	2 6	7	8	9 14	15

- Bit 15: Control Current Line Section 0 = Off, 1 = On
- Bits 9–14: Not Used
- Bits 7–8: For Diagnostic use, in online mode must be = 00, in offline mode Bit 7 = 1 will set the DONE flag, and Bit 8 = 1 will clear all timing logic
- Bits 2–6: Not Used
- Bits 0–1: Must be = 00

6) Set Line Characteristics

DOC (f) AC,MUX

0 1	2 6	7 8	9 10	11 12	13 14	15
Must be = 10	Not Used	Clock Source Select	Stop Bits	Word Size	Parity	Loop Back Mode

- Loop Back Mode (0 = Off, 1 = On)
- Parity
  - 00 = No Parity
  - 01 = Odd Parity
  - 10 = Even Parity
  - 11 = Reserve
- Word Size
  - 00 = 5 Bits
  - 01 = 6 Bits
  - 10 = 7 Bits
  - 11 = 8 Bits
- Stop Bits
  - 00 = One
  - 01 = Two
  - 10 = Reserved
  - 11 = Reserved
- Clock Source Select
  - 00 = Clock 0
  - 01 = Clock 1
  - 10 = Clock 2
  - 11 = Clock 3
- Not Used
- Must be = 10

7) Read Line and Section Requesting Service

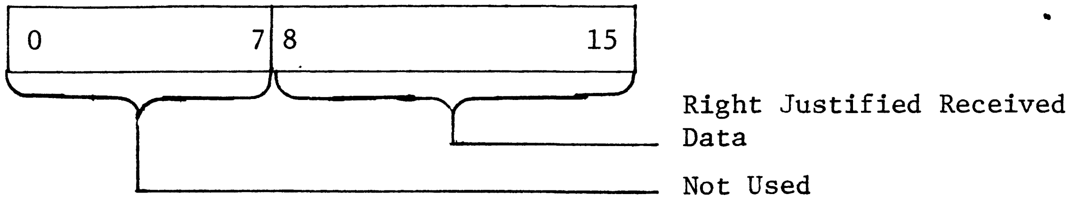
DIA (f) AC,MUX

0 6	7 14	15
Not Used	Highest Priority Line Address requiring service	Line Section

- Line Section 0 = Receiver or Modem, 1 = Transmitter
- Highest Priority Line Address requiring service
- Not Used

8) Receive Data

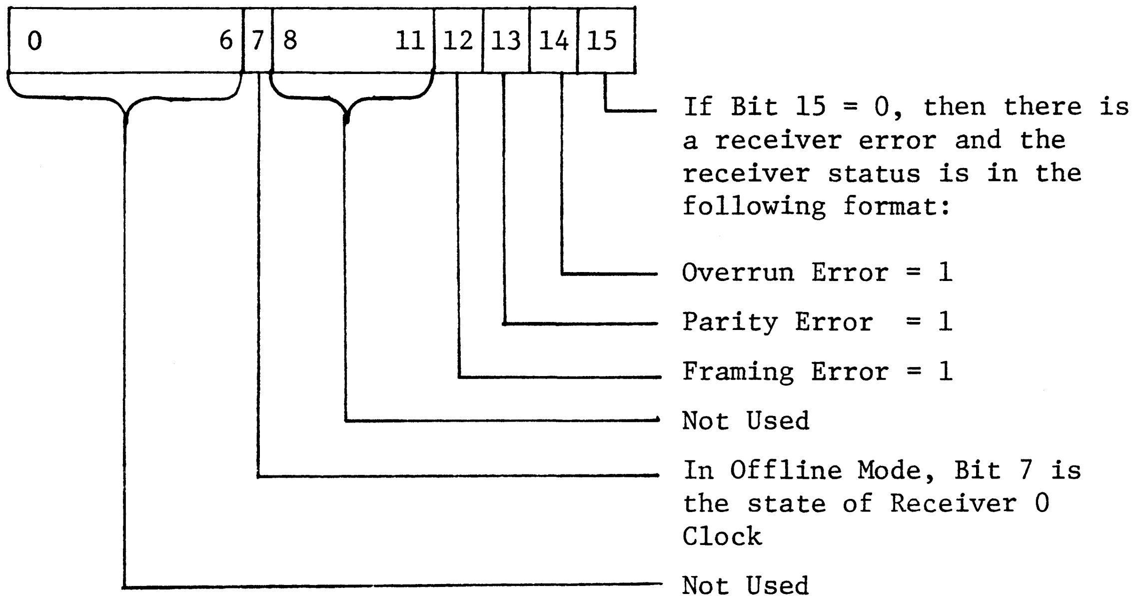
DIB (f) AC,MUX



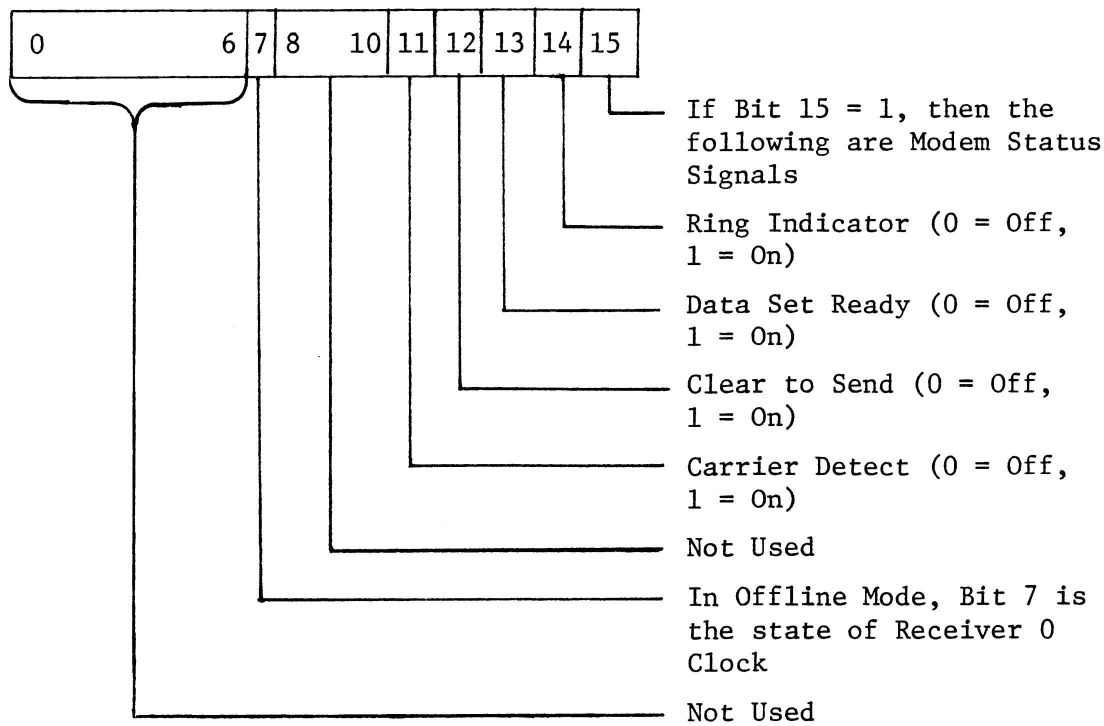
9) Read Receiver or Modem Status

DIC (f) AC,MUX

A)



B)



NOTE:

Status information is irrelevant if the Current Line Section is a transmitter or if the Current Line Section was set with a Set Line and Section rather than a Real Time and Section requesting service instruction

6.4 Selectable Options

6.4.1 Device Address

Switches 1 and 2 of the Switch Pack at Position R3 control the Device Address in the following manner:

Device Address 44_8 = S1 = Open, S2 = Closed

Device Address 34_8 = S1 = Closed, S2 = Open

6.4.2 Line Address

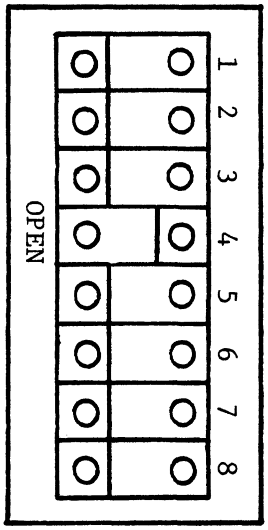
Switches 3-8 of the Switch Pack at Position R3 control the Line Address in the following manner:

ADDRESS RANGE (OCTAL)	SWITCH SETTINGS S3	S4	S5	S6	S7	S8
000 ⟶ 003	C	C	C	C	C	C
004 ⟶ 007	C	C	C	C	C	O
010 ⟶ 013	C	C	C	C	O	C
014 ⟶ 017	C	C	C	C	O	O
020 ⟶ 023	C	C	C	O	C	C
354 ⟶ 357	O	O	O	C	O	O
360 ⟶ 363	O	O	O	O	C	C
364 ⟶ 367	O	O	O	O	C	O
370 ⟶ 373	O	O	O	O	O	C
374 ⟶ 377	O	O	O	O	O	O

C = Closed O = Open

6.4.3 Baud Rate Selection

Clock 0   Switch Pack at Location R11



2,400 Baud Shown

S1 Closed = 19,000 Baud

S2 Closed = 9,600 Baud

S3 Closed = 4,800 Baud

S4 Closed = 2,400 Baud

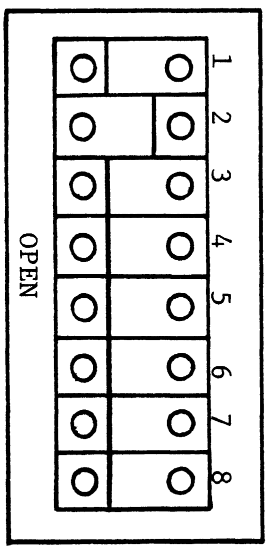
S5 Closed = 1,200 Baud

S6 Closed = 600 Baud

S7 Closed = 300 Baud

S8 Closed = 150 Baud

Clock 1   Switch Pack at Location S11



4,800 Baud Shown

S1 Closed = 9,600 Baud

S2 Closed = 4,800 Baud

S3 Closed = 2,400 Baud

S4 Closed = 1,200 Baud

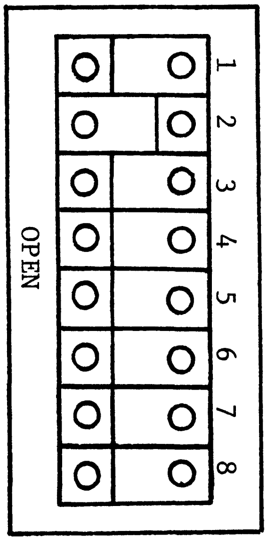
S5 Closed = 600 Baud

S6 Closed = 300 Baud

S7 Closed = 150 Baud

S8 Closed = 75 Baud

Clock 2   Switch Pack at Location T11



2,400 Baud Shown

S1 Closed = 4,800 Baud

S2 Closed = 2,400 Baud

S3 Closed = 1,200 Baud

S4 Closed = 600 Baud

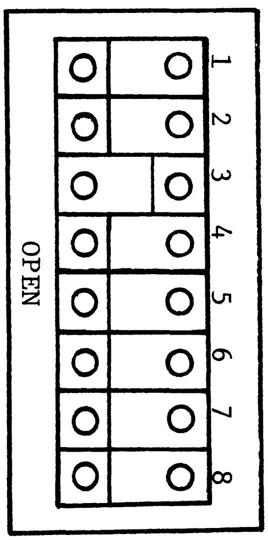
S5 Closed = 300 Baud

S6 Closed = 150 Baud

S7 Closed = 110 Baud

S8 Closed = 75 Baud

Clock 3   Switch Pack at Location W11



1,200 Baud Shown

S1 Closed = 4,800 Baud

S2 Closed = 2,400 Baud

S3 Closed = 1,200 Baud

S4 Closed = 600 Baud

S5 Closed = 300 Baud

S6 Closed = 150 Baud

S7 Closed = 110 Baud

S8 Closed = 75 Baud

Test A: Program To Repeatedly Output A Single Character Using BUSY/DONE Logic

The octal program listed below is entered through the console data switches starting at location 100. The starting address (100) is set in the switches and then the EXAMINE switch is hit to load this address. The console switches can then be reset to the ASCII value of the character to be printed (e.g., octal 100 = @, octal 101 = A, etc.) The program is started by pressing the CONTINUE switch.

The program reads the selected character from the computer data switches, sends out the character to the teletype or CRT and then waits in a SKIP BUSY (or DONE) loop for the serial shifting of the character to the terminal to be completed. The process requires no response from the terminal and will repeatedly send out the same character. If the terminal does not have an automatic line feed, it will be necessary to take the terminal off line to advance the line. If proper transmission is occurring, the console switches can be changed on the fly to change the character sent out.

Memory Location	Octal Program	Symbolic Code	Comments
100	062677	IORST	
101	060477	READS 0,CPU	Reads console switches
102	061111	DOAS 0,TTO	Send out character
103	063511	SKPBZ TTO	
104	000777	JMP .-1	Wait for completion
105	773	JMP .-5	Repeat

To run under DONE logic, change the instruction in location 103 to 063611.

If no output occurs, a problem exists with one of the following:

1. The cable has been improperly installed. Carefully check installation.
2. Terminal not on line.
3. Wrong baud rate selected.
4. A problem exists with the controller. Check that controller and cable are plugged to the same slot.

6.4.4 Board Priorities (For Multiple Boards)

This back panel jumper allows priority assignment for multiple board configurations. Jumper pin A91 of the higher priority board to pin A92 of the lower priority board.

7.0 Interface Signals, I/O Pin Assignments

7.1 Interface Signals

SIGNAL NAME	PIN NUMBER
$\overline{\text{DATA 0}}$	B62
$\overline{\text{DATA 1}}$	B65
$\overline{\text{DATA 2}}$	B82
$\overline{\text{DATA 3}}$	B73
$\overline{\text{DATA 4}}$	B61
$\overline{\text{DATA 5}}$	B57
$\overline{\text{DATA 6}}$	B95
$\overline{\text{DATA 7}}$	B55
$\overline{\text{DATA 8}}$	B60
$\overline{\text{DATA 9}}$	B63
$\overline{\text{DATA 10}}$	B75
$\overline{\text{DATA 11}}$	B58
$\overline{\text{DATA 12}}$	B59
$\overline{\text{DATA 13}}$	B64
$\overline{\text{DATA 14}}$	B56
$\overline{\text{DATA 15}}$	B66
CLR	A50
DATIA	A44
DATIB	A42
DATIC	A54
DATOA	A58
DATOB	A56
DATOC	A48

7.1 Interface Signals (Cont)

SIGNAL NAME	PIN NUMBERS
$\overline{\text{DCHP IN}}$*	A94
$\overline{\text{DCHP OUT}}$*	A93
$\overline{\text{DS0}}$	A72
$\overline{\text{DS1}}$	A68
$\overline{\text{DS2}}$	A66
$\overline{\text{DS3}}$	A46
$\overline{\text{DS4}}$	A62
$\overline{\text{DS5}}$	A64
INTA	A40
$\overline{\text{INTP IN}}$	A96
$\overline{\text{INTP OUT}}$	A95
$\overline{\text{INTR}}$	B29
IOPLS	A74
IORST	A70
$\overline{\text{MSKO}}$	A38
$\overline{\text{RQENB}}$	B41
$\overline{\text{SELB}}$	A82
$\overline{\text{SECD}}$	A80
STRT	A52

*Not used but must be jumpered for signal continuity

7.2 I/O Pin Assignments

Device/Signal Name	Pin Number
Console #1	
- Clear to Send	A90
- EIA and -20MA Data Out	A85
- +20MA Data Out	A83
- EIA and +20MA Data In	A69

Device/Signal Name	Pin Number
Console #2	
- Clear to Send	A67
- EIA and -20MA Data Out	B13
- +20MA Data Out	A77
- EIA and +20MA Data In	B11
Mux Channel 0	
- DSR	A76
- CTS	A75
- CD	A73
- RI	A71
- RTS	A67
- DTR	A65
- S Data In	A69
- S Data Out	A63
Mux Channel 1	
- DSR	A89
- CTS	A88
- CD	A87
- RI	A86
- RTS	A81
- DTR	A79
- S Data In	A84
- S Data Out	A78
Mux Channel 2	
- DSR	B36
- CTS	B34
- CD	B31
- RI	B27
- RTS	A23

Device/Signal Name	Pin Number
Mux Channel 2 (Cont)	
- DTR	B19
- S Data In	B25
- S Data Out	B15
Mux Channel 3	
- DSR	B54
- CTS	B53
- CD	B52
- RI	B51
- RTS	B48
- DTR	B40
- S Data In	B49
- S Data Out	B38
- Priority In	A92
- Priority Out	A91
Real Time Clock	
- 60Hz In	B6

MULTI-DEVICE
INTERFACE
CONTROLLER

NOTES

1. NUMBERS FOUND WITHIN THE HEXAGON SYMBOLS INDICATE SHEETS WHERE CONTINUED LOGIC WILL BE FOUND.
   EXAMPLE: 3 10 = SHEETS 3 & 10

CUSTOM SYSTEMS INC

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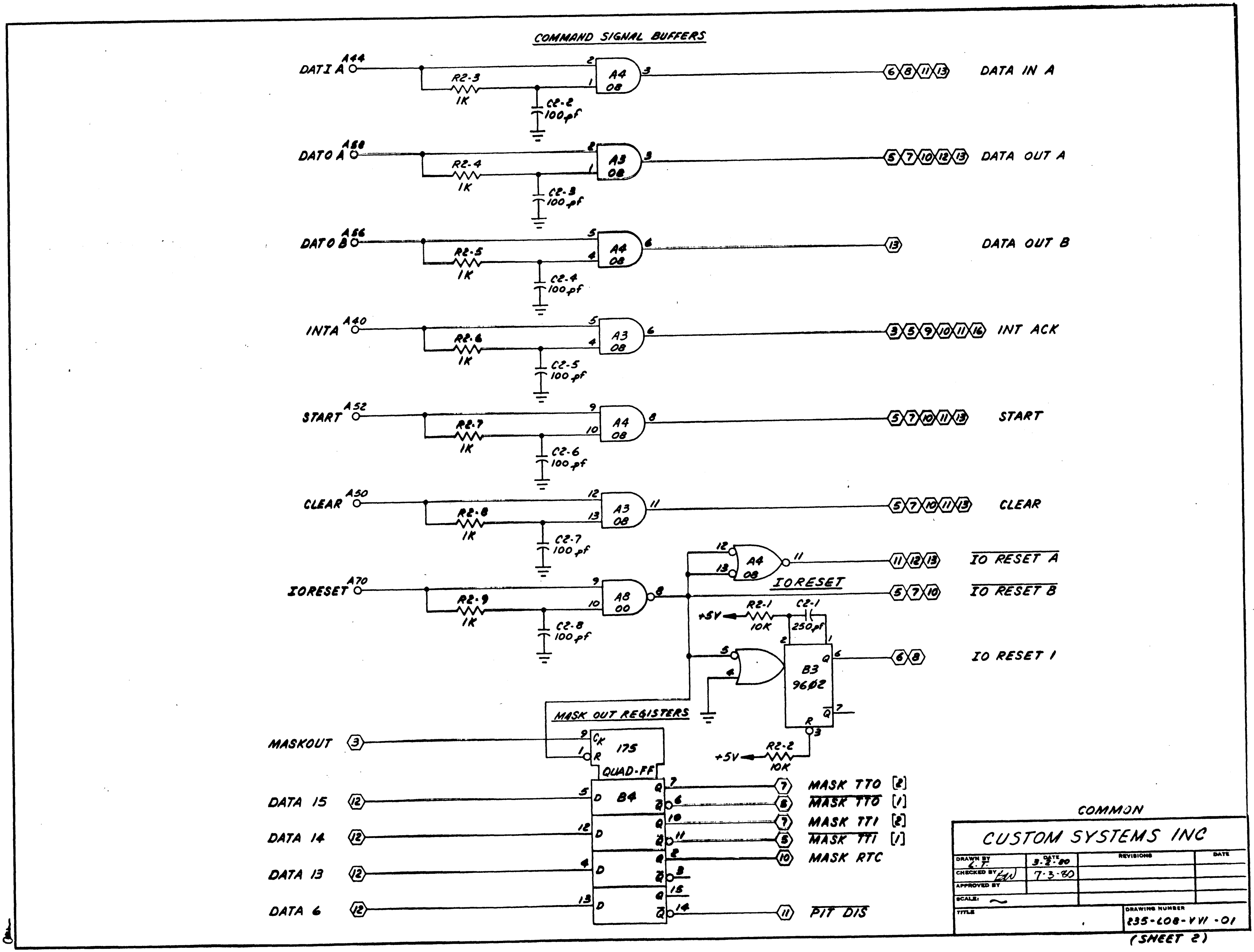
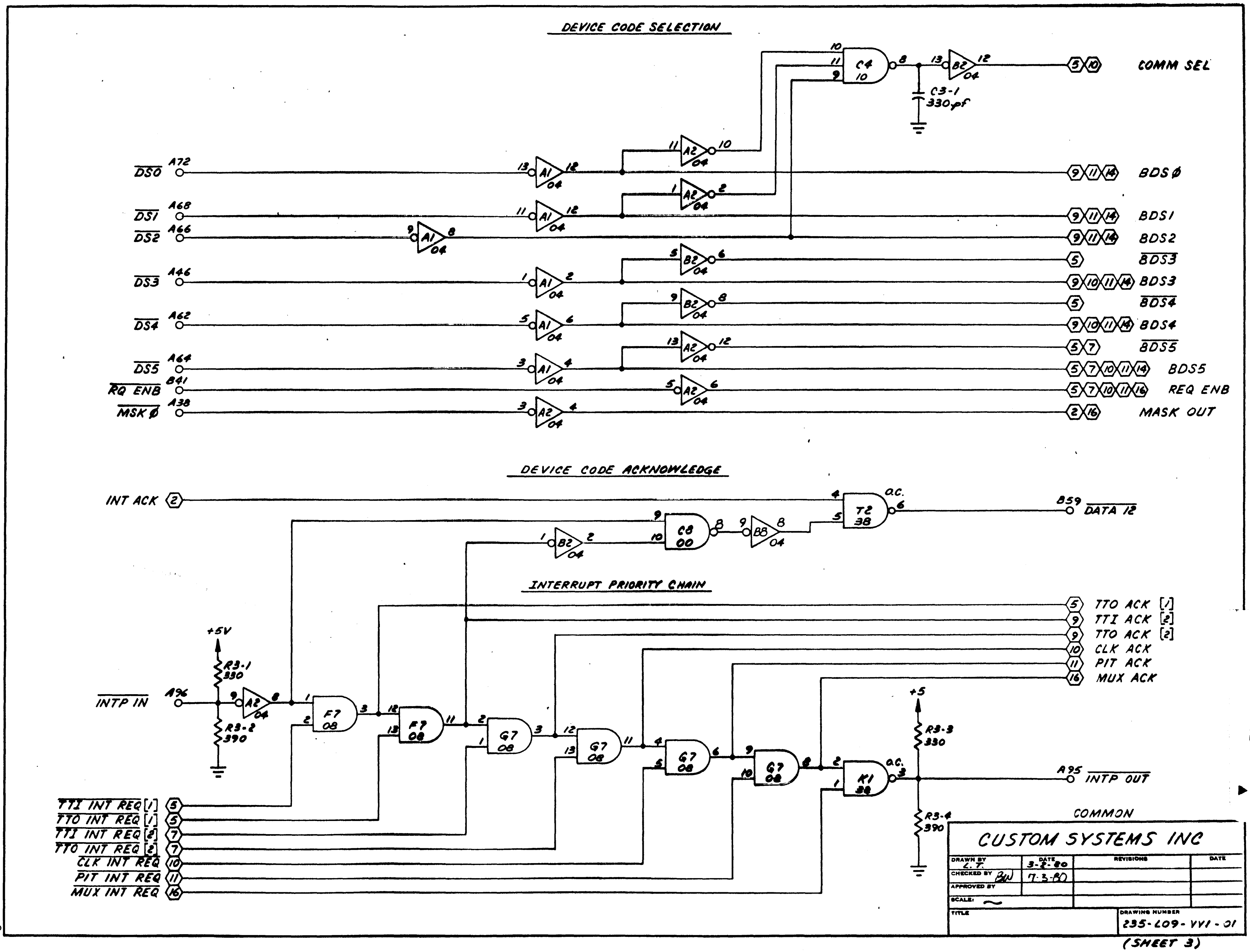
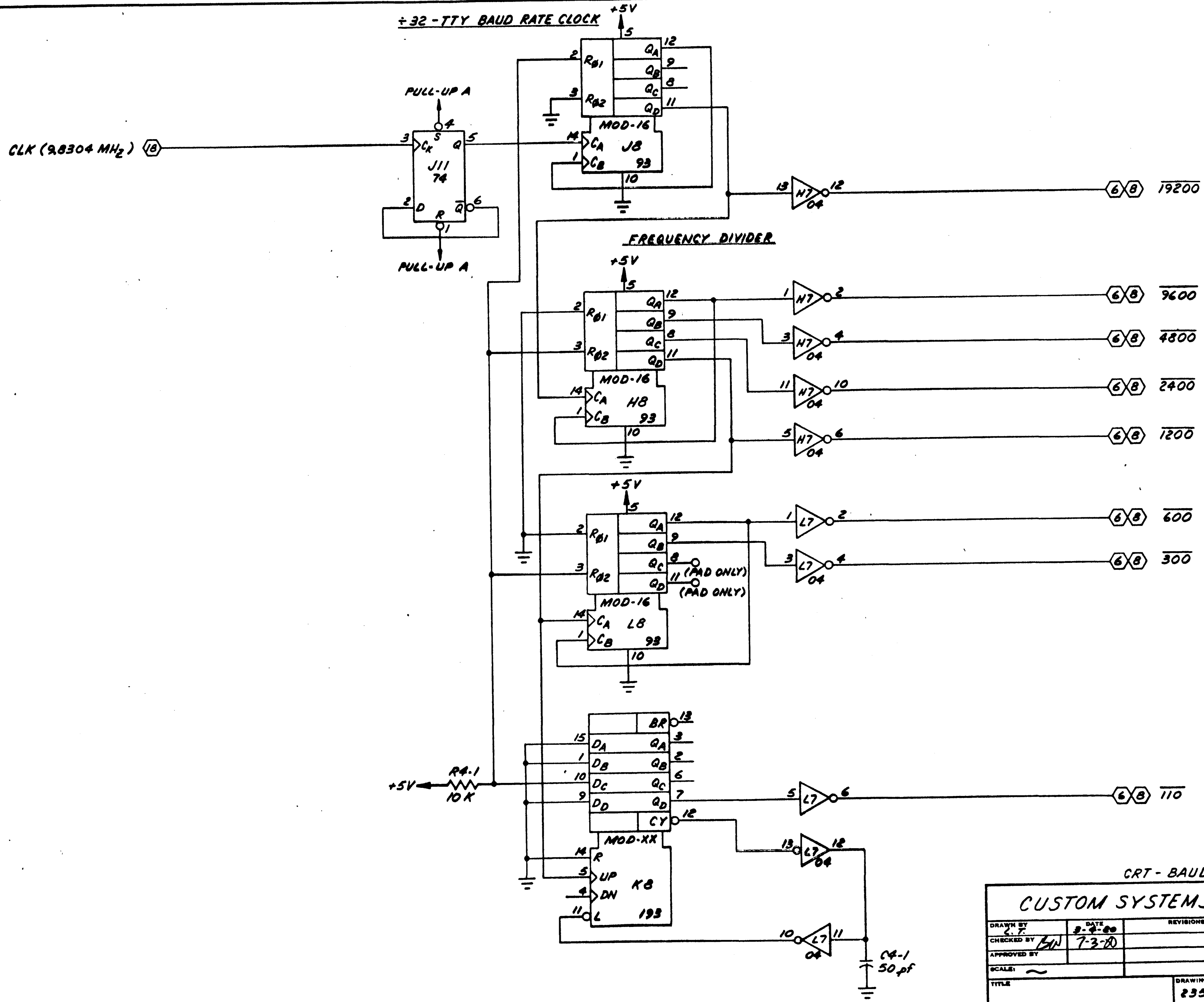
SCALE: ~			
TITLE		DRAWING NUMBER 235-L07-VV1-01	

(SHEET 1 OF)


COMMAND SIGNAL BUFFERS
DATI A
A44
R2-3
1K
C2-2
100pf
A4
08
DATA IN A
DATO A
A58
R2-4
1K
C2-3
100pf
A3
08
DATA OUT A
DATO B
A56
R2-5
1K
C2-4
100pf
A4
08
DATA OUT B
INTA
A40
R2-6
1K
C2-5
100pf
A3
08
INT ACK
START
A52
R2-7
1K
C2-6
100pf
A4
08
START
CLEAR
A50
R2-8
1K
C2-7
100pf
A3
08
CLEAR
IORESET
A70
R2-9
1K
C2-8
100pf
A8
00
A4
08
IO RESET A
IORESET
IO RESET B
+5V
R2-1
10K
C2-1
250pf
B3
9602
IO RESET 1
+5V
R2-2
10K
MASK OUT REGISTERS
MASKOUT
175
QUAD-FF
B4
DATA 15
DATA 14
DATA 13
DATA 6
MASK TTO [2]
MASK TTO [1]
MASK TTI [2]
MASK TTI [1]
MASK RTC
PIT DIS
COMMON
CUSTOM SYSTEMS INC
DRAWN BY C.T.
DATE 3.2.80
CHECKED BY EW 7-3-80
APPROVED BY
SCALE: ~
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L08-VVI-01
(SHEET 2)


DEVICE CODE SELECTION
COMM SEL
C3-1
330pf
DS0
A72
BDS Ø
DS1
A68
BDS1
DS2
A66
BDS2
BDS3
DS3
A46
BDS3
BDS4
DS4
A62
BDS4
BDS5
DS5
A64
BDS5
RQ ENB
B41
REQ ENB
MSK Ø
A38
MASK OUT
DEVICE CODE ACKNOWLEDGE
INT ACK
B59
DATA 12
O.C.
INTERRUPT PRIORITY CHAIN
TTO ACK [1]
TTI ACK [2]
TTO ACK [2]
CLK ACK
PIT ACK
MUX ACK
+5V
R3-1
330
INTP IN
A96
R3-2
390
+5
R3-3
330
A95
INTP OUT
R3-4
390
TTI INT REQ [1]
TTO INT REQ [1]
TTI INT REQ [2]
TTO INT REQ [2]
CLK INT REQ
PIT INT REQ
MUX INT REQ
COMMON
CUSTOM SYSTEMS INC
DRAWN BY L.T.
DATE 3-2-80
CHECKED BY BW
7-3-80
APPROVED BY
SCALE: ~
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-609-VVI-01
(SHEET 3)

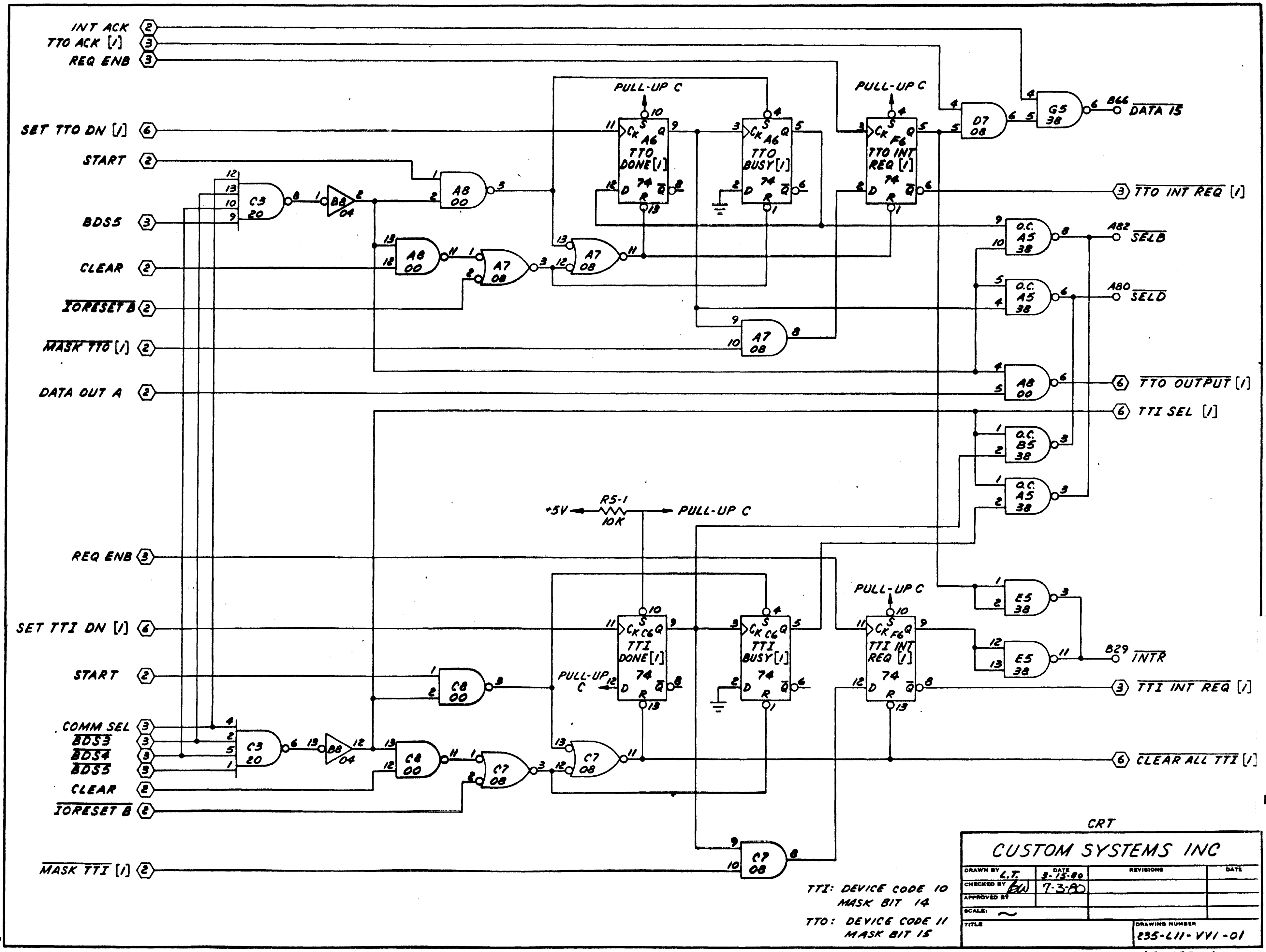


CRT - BAUD RATE CLOCK

CUSTOM SYSTEMS INC

DRAWN BY	C. T.	DATE 3-4-80	REVISIONS	DATE
CHECKED BY	BN	7-3-80		
APPROVED BY				
SCALE:	~			
TITLE			DRAWING NUMBER 235-L10-VVI-01	

(SHEET 4)



CRT

CUSTOM SYSTEMS INC

DRAWN BY L.T.	DATE 3-13-80	REVISIONS	DATE
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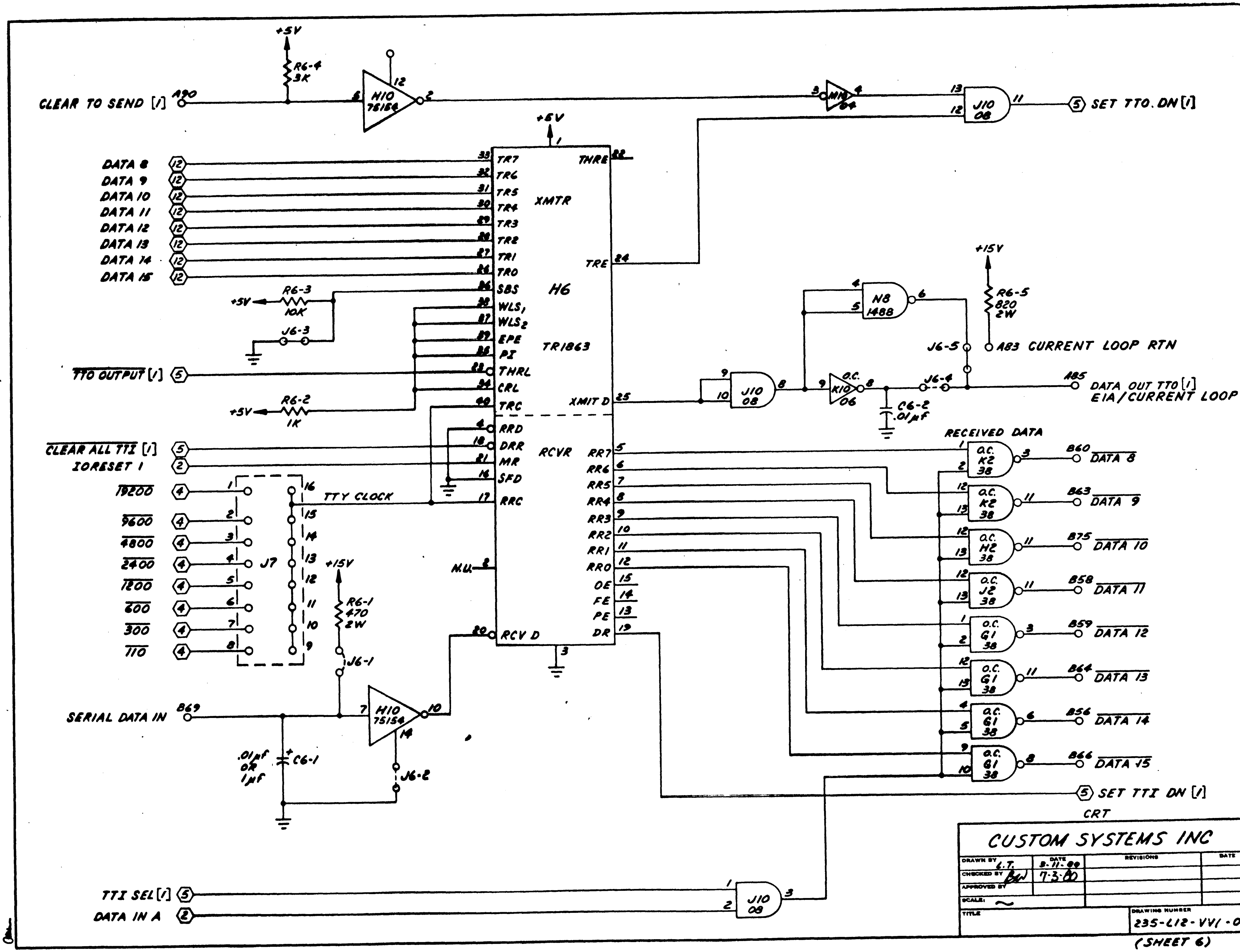
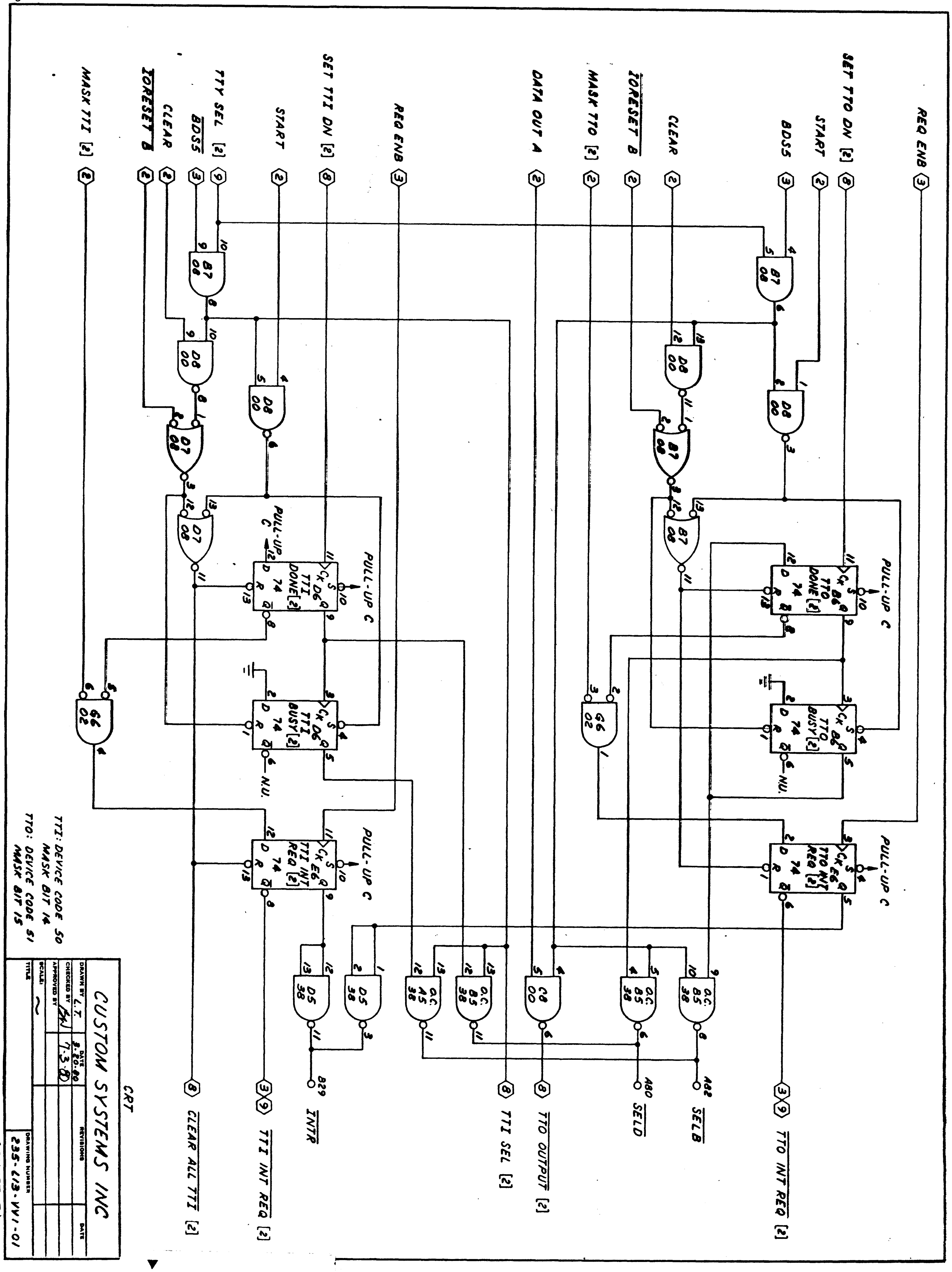
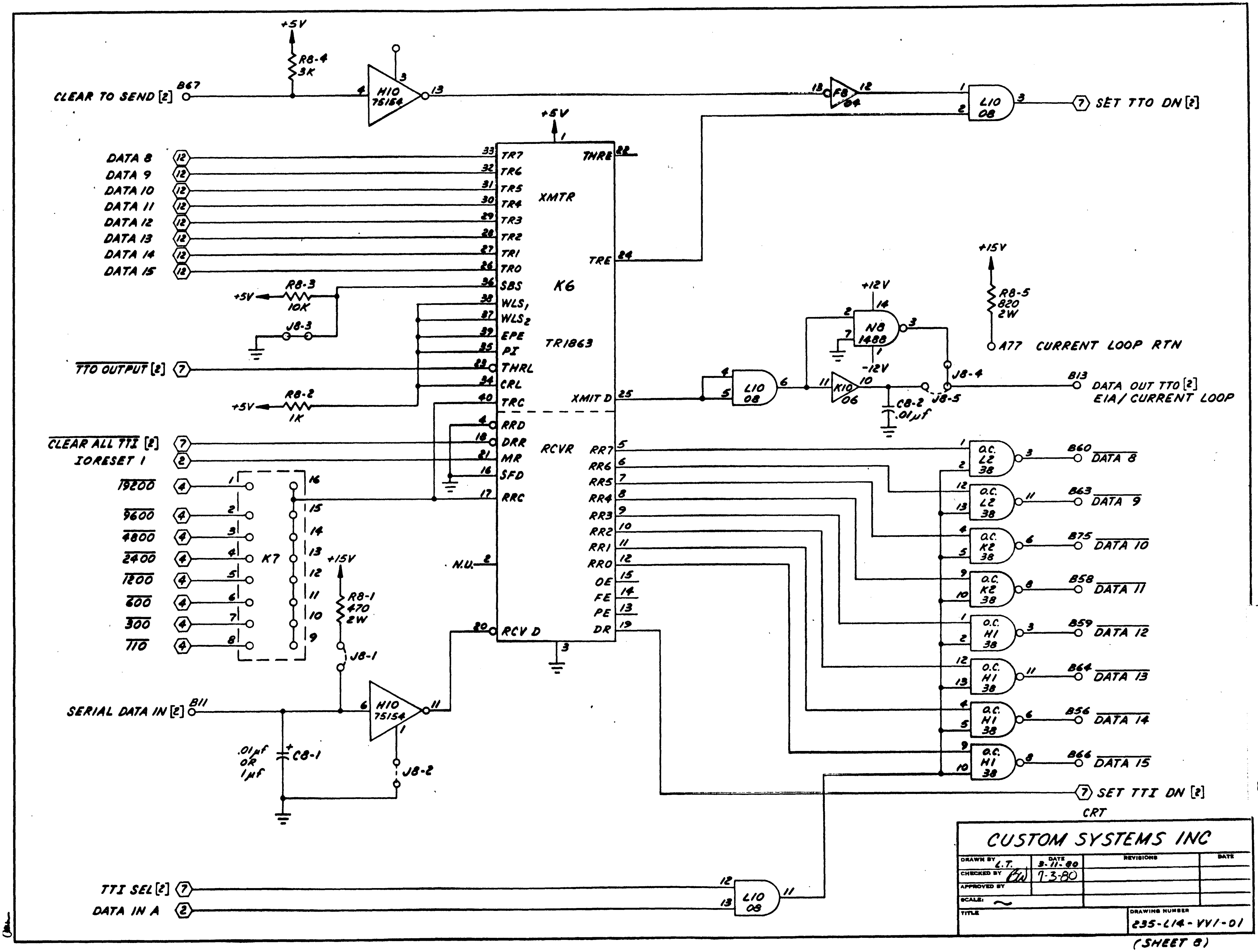
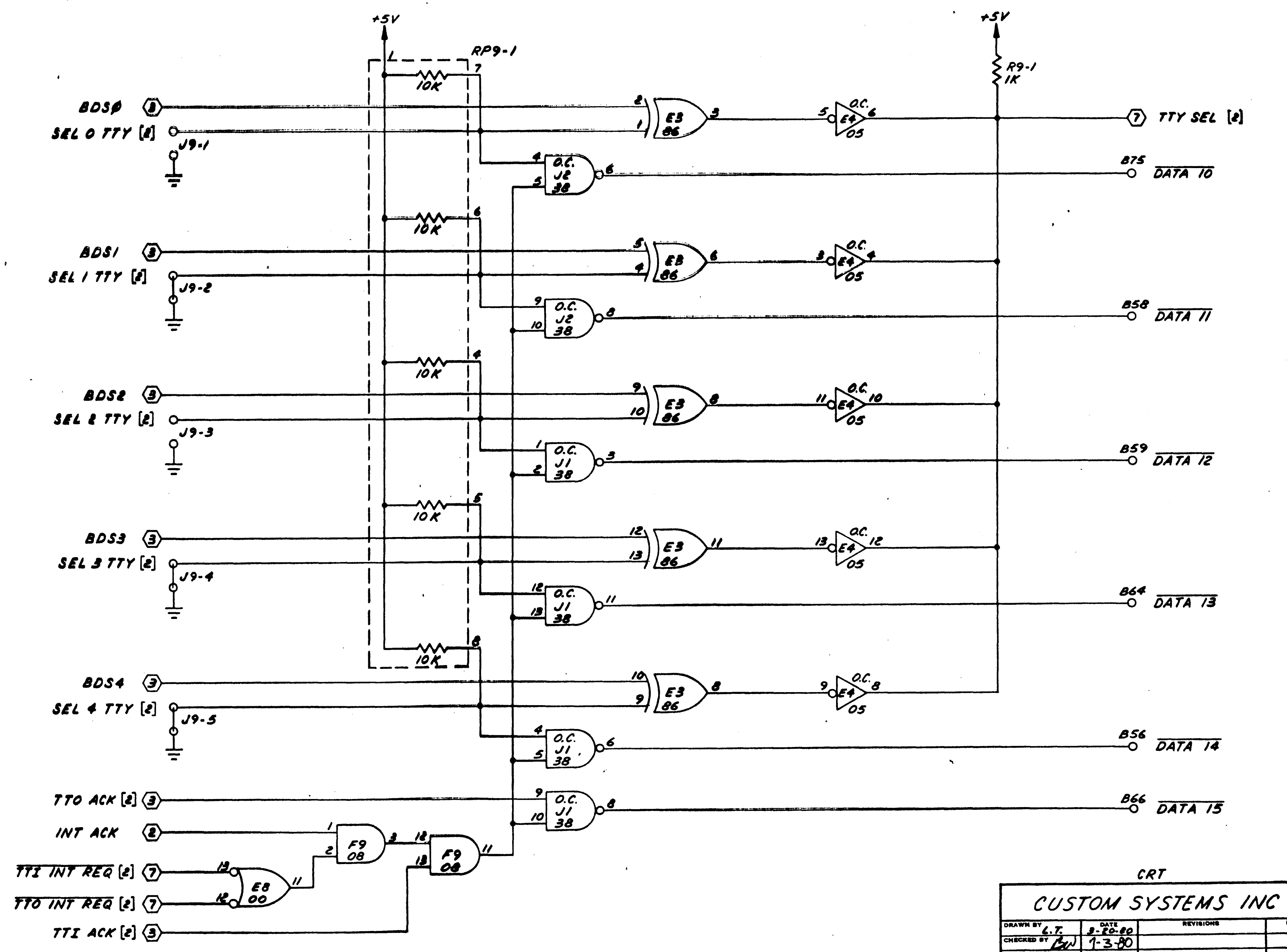
APPROVED BY			
SCALE: ~			
TITLE		DRAWING NUMBER 235-L11-VV1-01	

(SHEET 5)


CLEAR TO SEND [/]
SET TTO. ON [/]
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
TTO OUTPUT [/]
CLEAR ALL TTI [/]
IORESET 1
19200
9600
4800
2400
1200
600
300
110
J7
TTY CLOCK
SERIAL DATA IN
H6
TR1863
XMTR
RCVR
A83 CURRENT LOOP RTN
DATA OUT TTO [/]
EIA/CURRENT LOOP
RECEIVED DATA
SET TTI ON [/]
CRT
TTI SEL [/]
DATA IN A
CUSTOM SYSTEMS INC
235-L12-VV1-01
(SHEET 6)


MASK TTI [2]
IORESET B
CLEAR
BDS5
TTY SEL [2]
START
SET TTI DN [2]
REQ ENB
DATA OUT A
MASK TTO [2]
IORESET B
CLEAR
BDS5
START
SET TTO DN [2]
REQ ENB
PULL-UP C
TTI DONE [2]
TTI BUSY [2]
TTI INT REQ [2]
TTO DONE [2]
TTO BUSY [2]
TTO INT REQ [2]
N.U.
CLEAR ALL TTI [2]
TTI INT REQ [2]
INTR
TTI SEL [2]
TTO OUTPUT [2]
SELD
SELB
TTO INT REQ [2]
TTI: DEVICE CODE 50
MASK BIT 14
TTO: DEVICE CODE 51
MASK BIT 15
CUSTOM SYSTEMS INC
CRT
235-613-VY1-01
(SHEET 7)

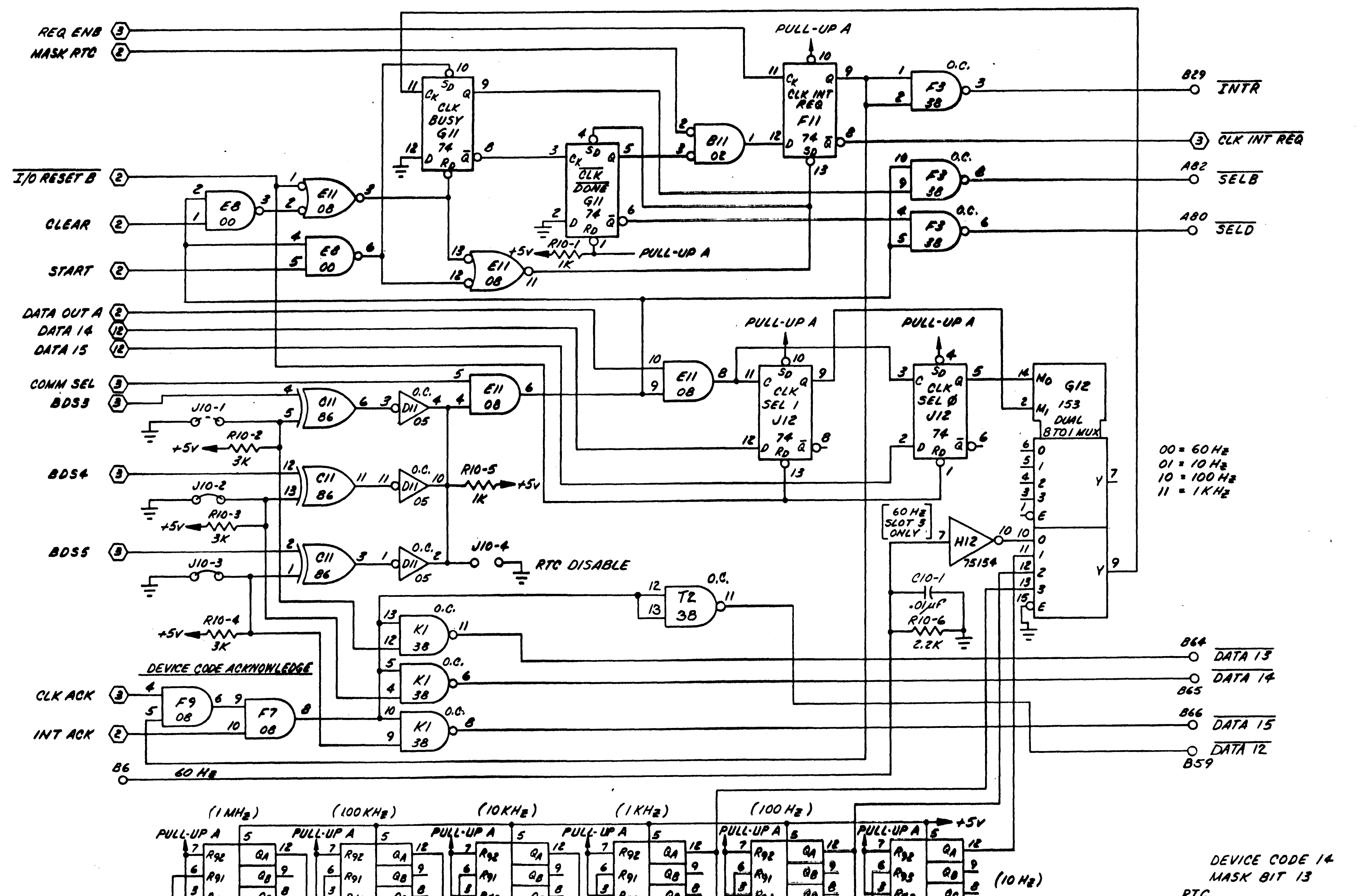

CLEAR TO SEND [2]
B67
+5V
R8-4
3K
H10
75154
F8
04
L10
08
SET TTO DN [2]
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
TR7
TR6
TR5
TR4
TR3
TR2
TR1
TR0
SBS
WLS1
WLS2
EPE
PI
THRL
CRL
TRC
XMTR
K6
TR1863
THRE
TRE
XMIT D
RRD
DRR
MR
SFD
RRC
RCVR
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RR0
OE
FE
PE
DR
RCV D
N.U.
R8-3
10K
J8-3
TTO OUTPUT [2]
R8-2
1K
CLEAR ALL TTI [2]
IORESET 1
19200
9600
4800
2400
1200
600
300
110
K7
+15V
R8-1
470
2W
J8-1
SERIAL DATA IN [2]
B11
.01µf OR 1µf
C8-1
J8-2
N8
1488
+12V
-12V
K10
06
C8-2
.01µf
J8-4
J8-5
R8-5
820
2W
A77 CURRENT LOOP RTN
B13
DATA OUT TTO [2]
EIA/CURRENT LOOP
O.C.
L2
K2
H1
38
B60
B63
B75
B58
B59
B64
B56
B66
SET TTI DN [2]
CRT
TTI SEL [2]
DATA IN A
CUSTOM SYSTEMS INC
DRAWN BY L.T.
DATE 3-11-80
CHECKED BY
7-3-80
APPROVED BY
SCALE: ~
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L14-VV1-01
(SHEET 8)



CRT

CUSTOM SYSTEMS INC			
DRAWN BY L.T.	DATE 3-20-80	REVISIONS	DATE
CHECKED BY BW	1-3-80		
APPROVED BY			
SCALE: ~			
TITLE		DRAWING NUMBER 235-L15-VV1-01	

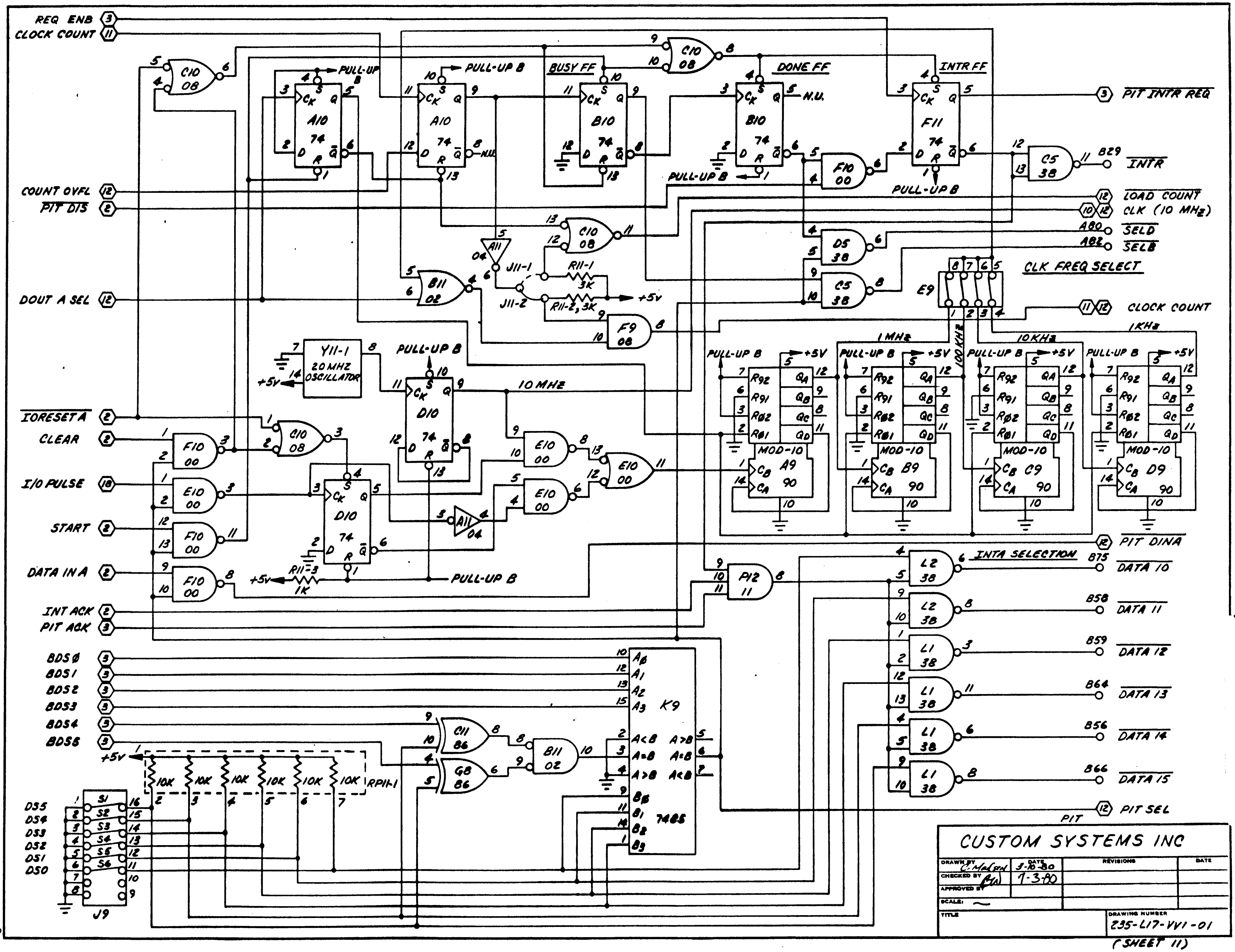
(SHEET 9)

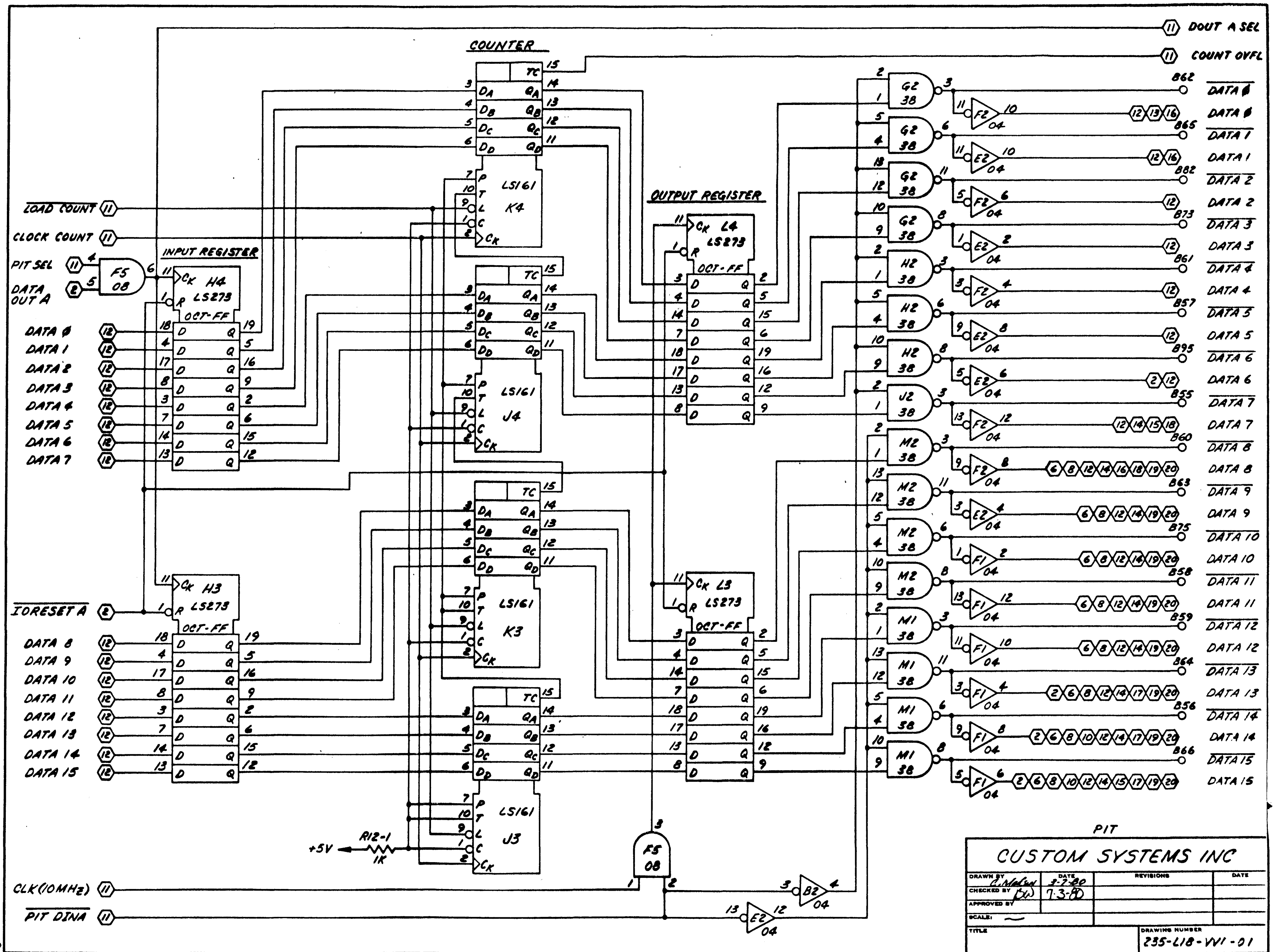


DEVICE CODE 14
MASK BIT 13
RTC

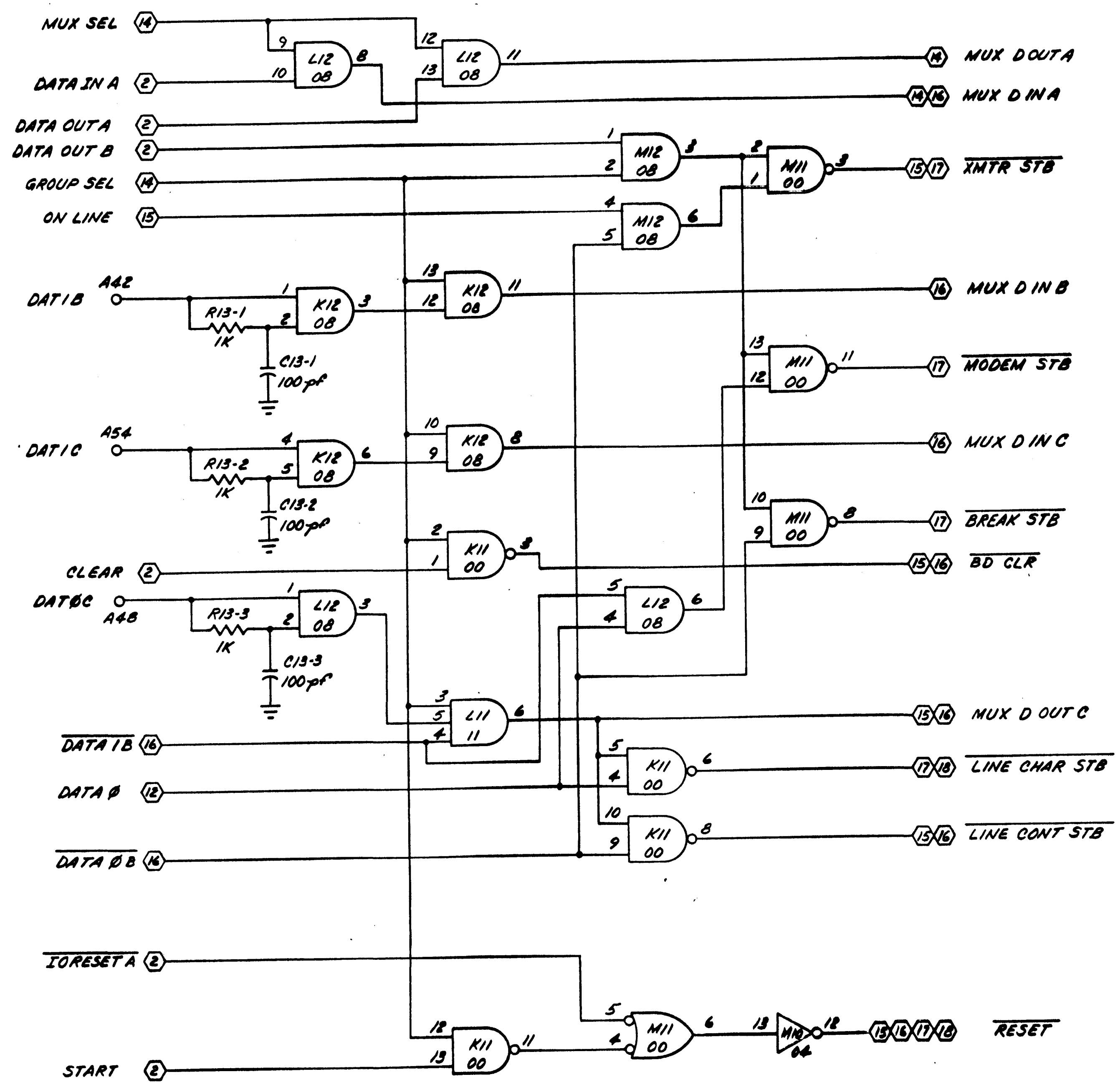
CUSTOM SYSTEMS INC		
DRAWN BY C. Melvin	DATE 6-25-80	REVISIONS
CHECKED BY EW	7-3-80	
APPROVED BY		
SCALE: ~		
TITLE		DRAWING NUMBER 235-L16-VV1-01

(SHEET 10)


REQ ENB
CLOCK COUNT
COUNT OVFL
PIT DIS
DOUT A SEL
IORESET A
CLEAR
I/O PULSE
START
DATA IN A
INT ACK
PIT ACK
BDSØ
BDS1
BDS2
BDS3
BDS4
BDS5
+5V
DS5
DS4
DS3
DS2
DS1
DS0
J9
RP11-1
PULL-UP B
BUSY FF
DONE FF
INTR FF
N.U.
Y11-1
20 MHZ OSCILLATOR
10 MHZ
CLK FREQ SELECT
E9
100 KHZ
1 MHZ
10 KHZ
1 KHZ
MOD-10
PIT INTR REQ
B29 INTR
LOAD COUNT
CLK (10 MHZ)
A80 SELD
A82 SELB
CLOCK COUNT
PIT DINA
INTA SELECTION
B75 DATA 10
B58 DATA 11
B59 DATA 12
B64 DATA 13
B56 DATA 14
B66 DATA 15
PIT SEL
CUSTOM SYSTEMS INC
DRAWN BY C. McLean 3-10-80
CHECKED BY 7-3-80
APPROVED BY
SCALE: ~
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L17-VV1-01
(SHEET 11)

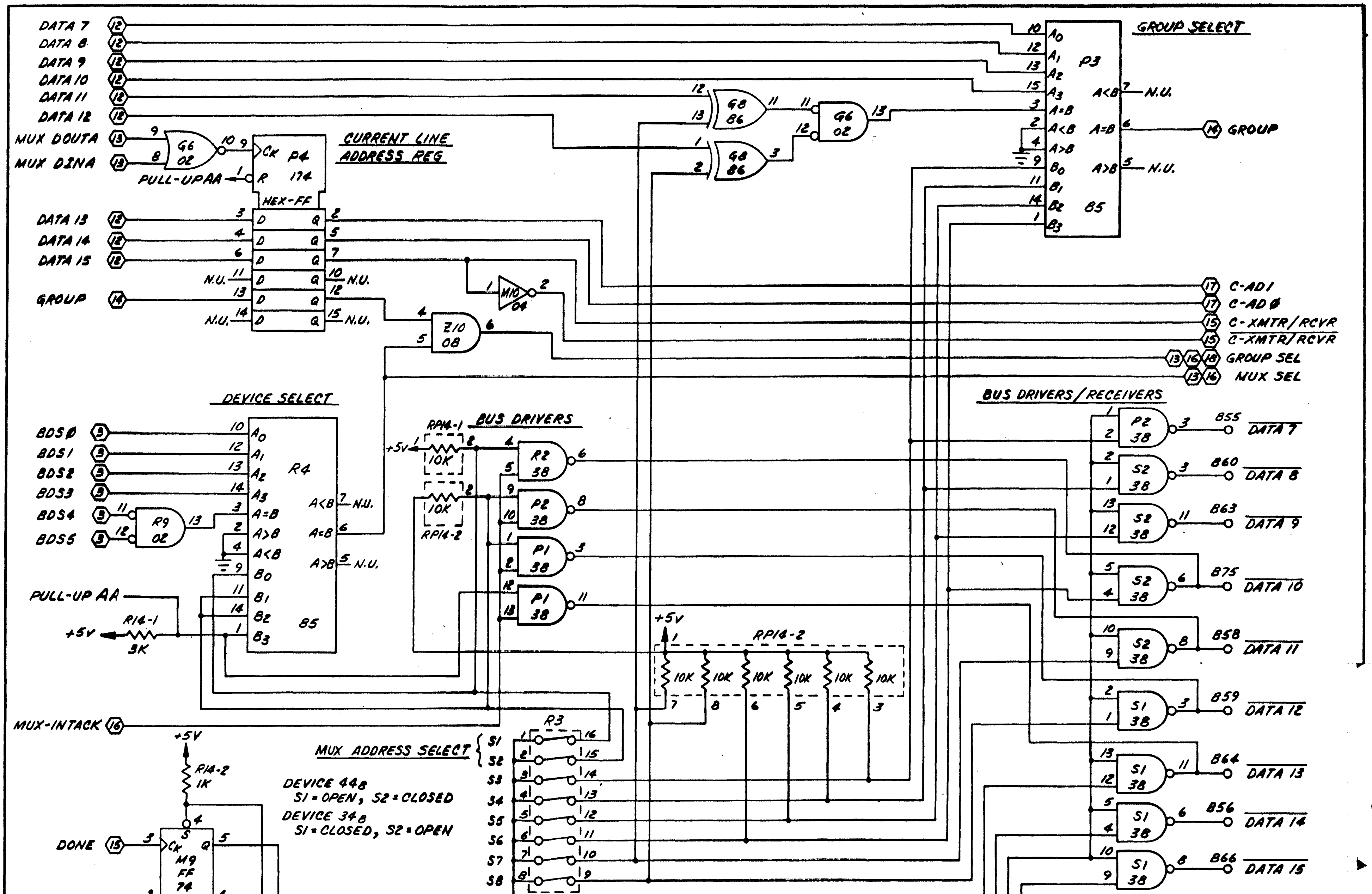


DOUT A SEL
COUNT OVFL
COUNTER
LS161
K4
J4
K3
J3
OUTPUT REGISTER
INPUT REGISTER
L4
L3
H4
H3
LS273
OCT-FF
F5
08
LOAD COUNT
CLOCK COUNT
PIT SEL
DATA OUT A
IORESET A
DATA Ø
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
R12-1
1K
+5V
CLK(10MHz)
PIT DINA
G2
H2
J2
M2
M1
38
F2
E2
F1
B2
04
B62
B65
B82
B73
B61
B57
B95
B55
B60
B63
B75
B58
B59
B64
B56
B66
PIT
CUSTOM SYSTEMS INC
DRAWN BY
DATE
CHECKED BY
APPROVED BY
SCALE:
TITLE
REVISIONS
DATE
7-3-80
DRAWING NUMBER
235-L18-VV1-01
(SHEET 12)



CUSTOM SYSTEMS INC			
DRAWN BY C. Molzen	DATE	REVISIONS	DATE
CHECKED BY CW	7-3-80		
APPROVED BY			
SCALE: ~			
TITLE		DRAWING NUMBER 235-L19-VV1-01	

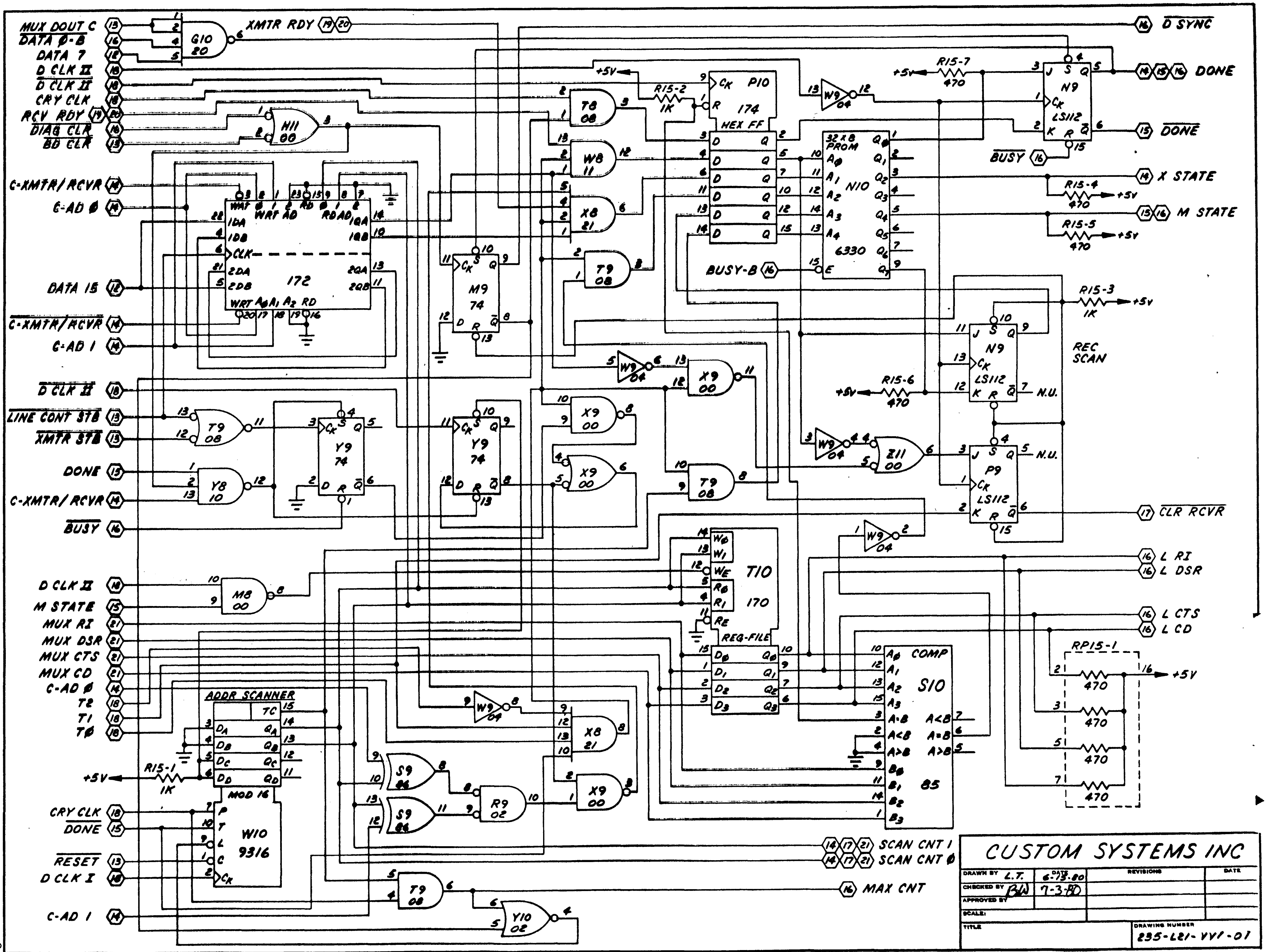
(SHEET 13)



CUSTOM SYSTEMS INC

DRAWN BY	DATE	REVISIONS	DATE
C. Madsen			
CHECKED BY HW	7-3-80		
APPROVED BY			
SCALE: ~			
TITLE		DRAWING NUMBER 235-L20-VW-01	

(SHEET 14)



CUSTOM SYSTEMS INC

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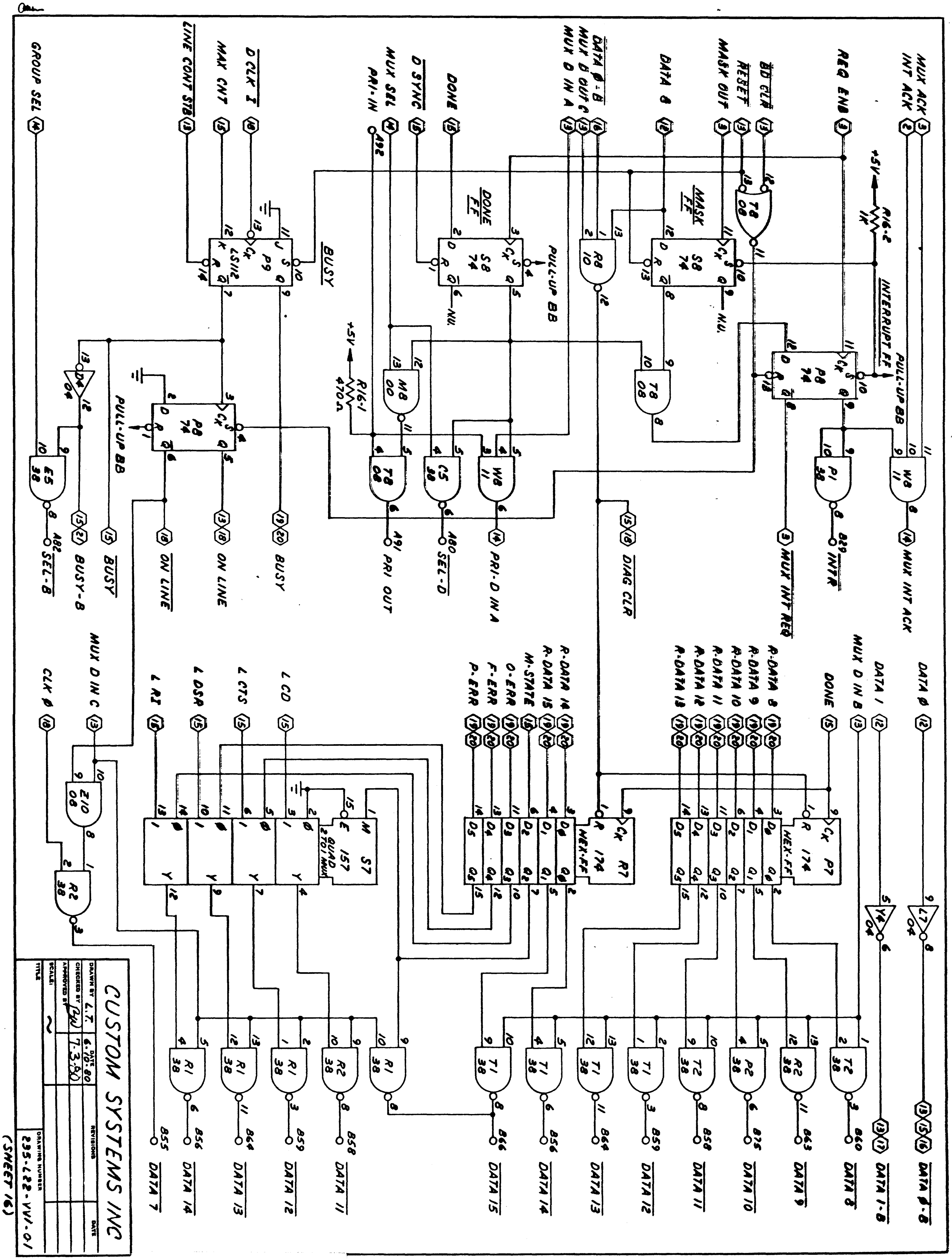
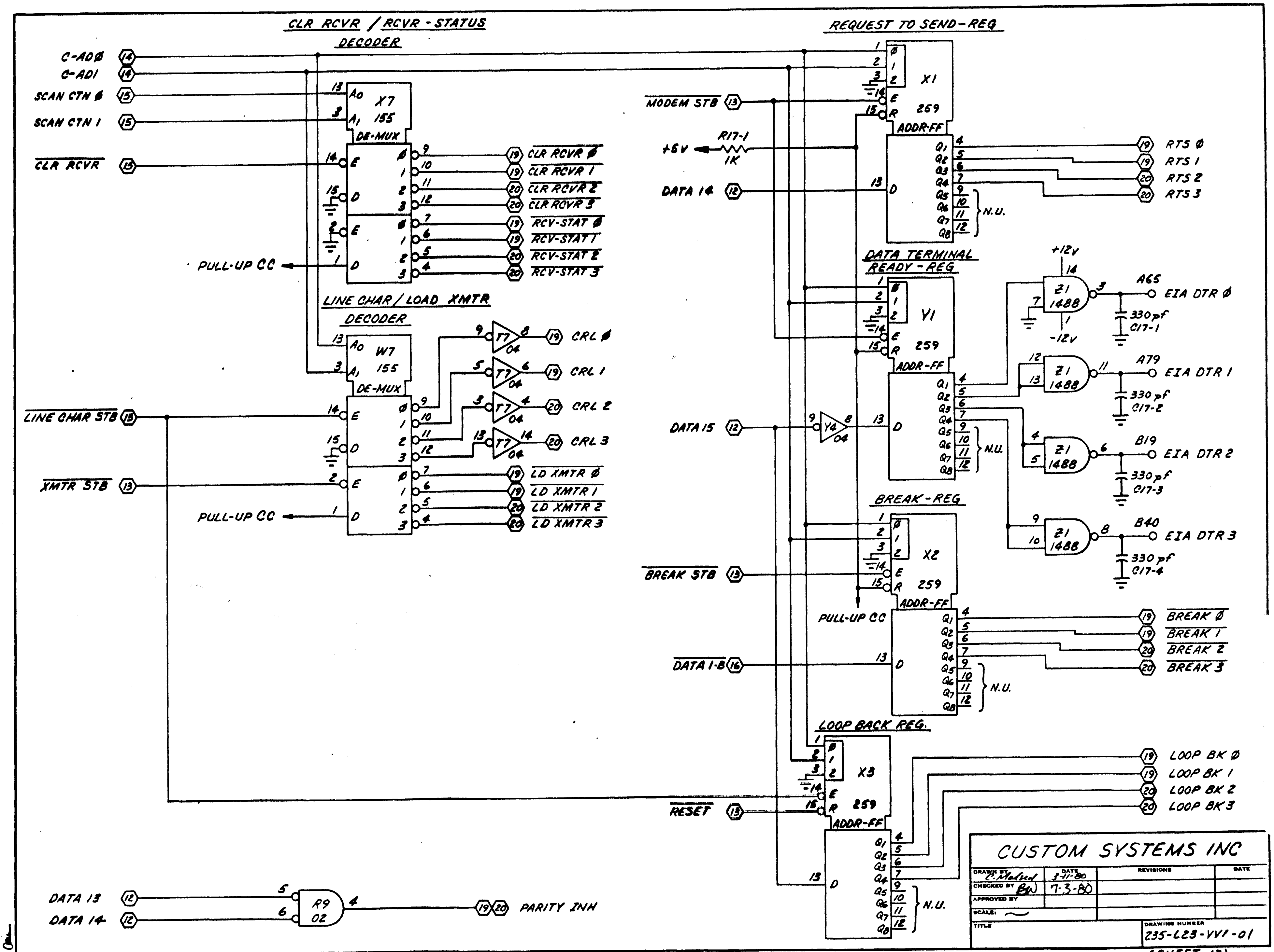
CHECKED BY	BW	7-3-80		
APPROVED BY				
SCALE:				
TITLE			DRAWING NUMBER 235-L21-YY1-01	

(SHEET 15)

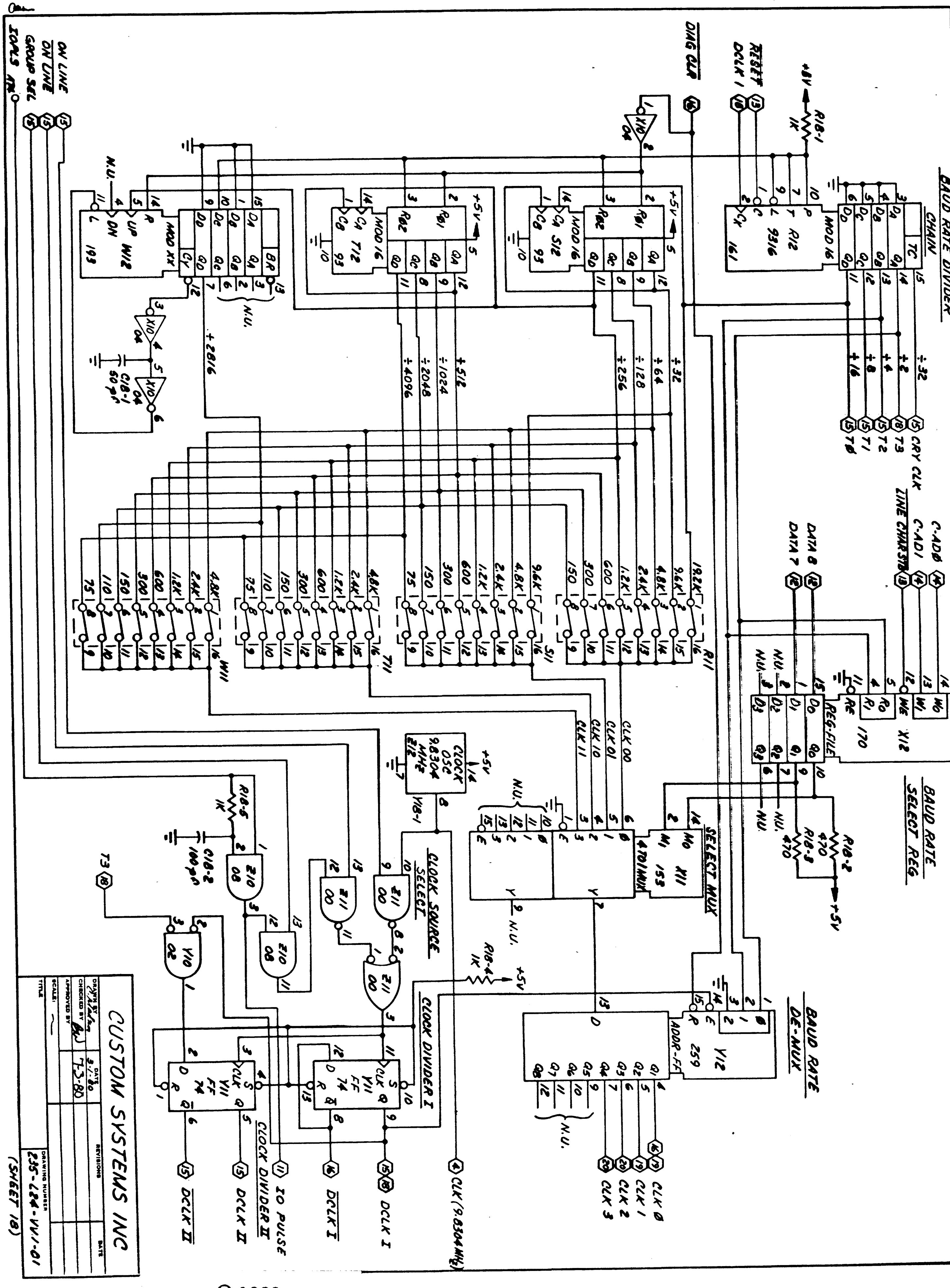

CUSTOM SYSTEMS INC
DRAWN BY L.T.
DATE 6-10-80
CHECKED BY
APPROVED BY
7-3-80
SCALE
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L22-YVI-01
(SHEET 16)
MUX ACK
INT ACK
REQ ENB
BD CLR
RESET
MASK OUT
DATA 8
DATA Ø-B
MUX B OUT C
MUX D IN A
DONE
D SYNC
MUX SEL
PRI-IN
D CLK I
MAX CNT
LINE CONT STB
GROUP SEL
BUSY
DONE FF
MASK FF
INTERRUPT FF
PULL-UP BB
SEL-B
BUSY-B
ON LINE
PRI OUT
SEL-D
PRI-D IN A
DIAG CLR
MUX INT REQ
INTR
MUX INT ACK
DATA Ø
DATA 1
MUX D IN B
R-DATA 8
R-DATA 9
R-DATA 10
R-DATA 11
R-DATA 12
R-DATA 13
R-DATA 14
R-DATA 15
M-STATE
O-ERR
F-ERR
P-ERR
L CD
L CTS
L DSR
L RI
MUX D IN C
CLK Ø
HEX-FF
QUAD 2 TO 1 MUX
DATA Ø-B
DATA 1-B
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
DATA 7



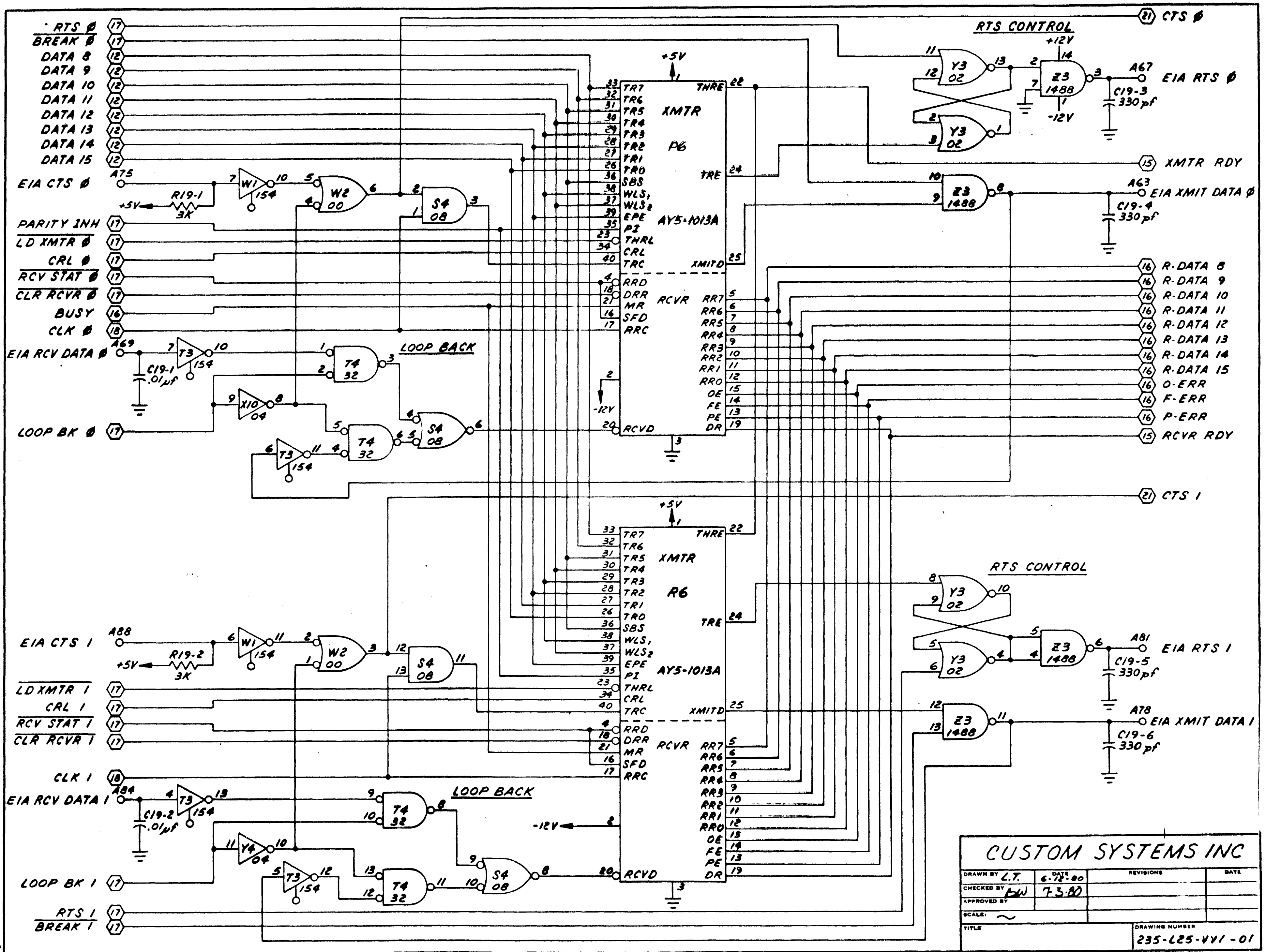
CUSTOM SYSTEMS INC

DRAWN BY C. Madsen	DATE 3-11-80	REVISIONS	DATE
CHECKED BY BW	7-3-80		
APPROVED BY			
SCALE: ~			
TITLE		DRAWING NUMBER 235-L23-VV1-01	

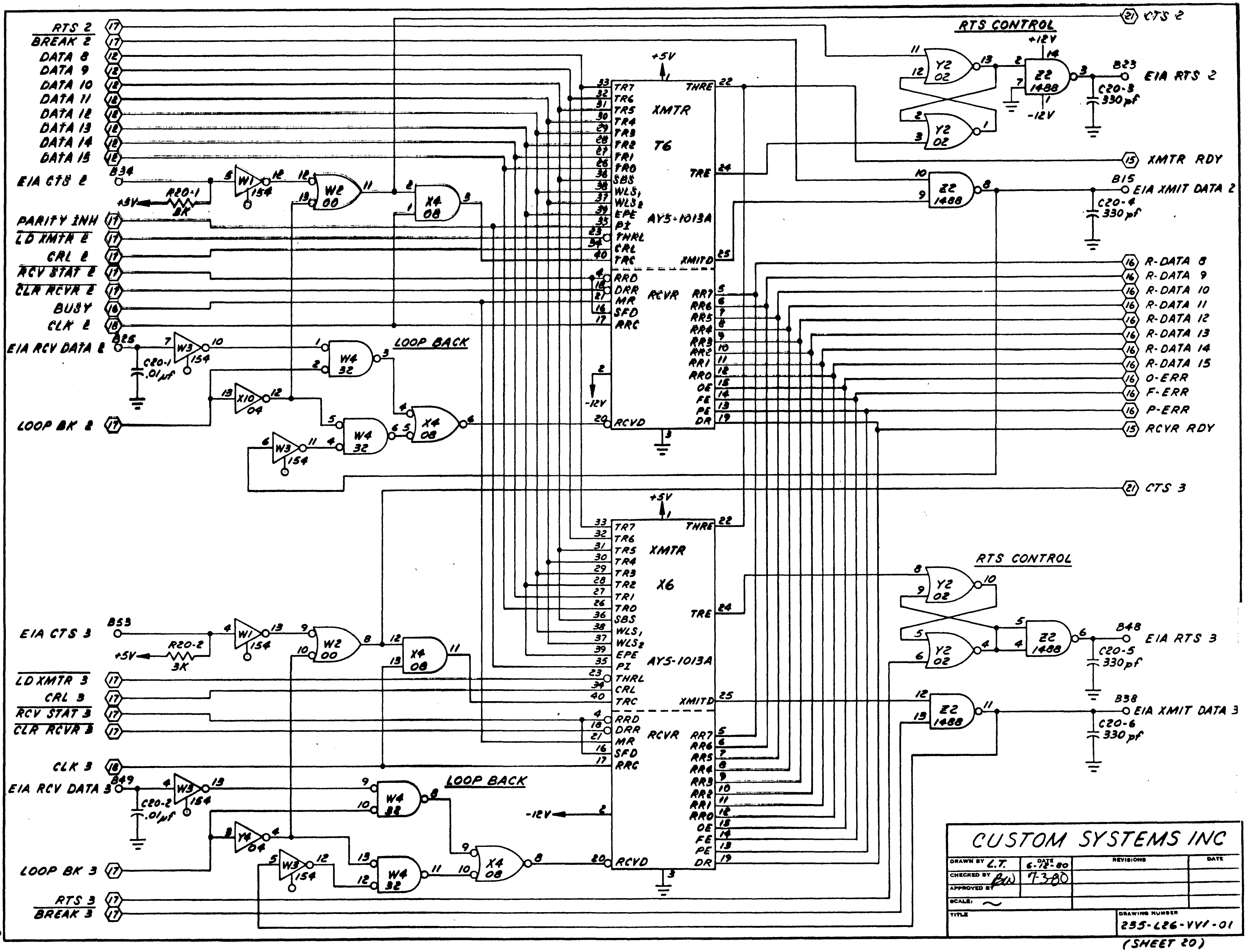
(SHEET 17)

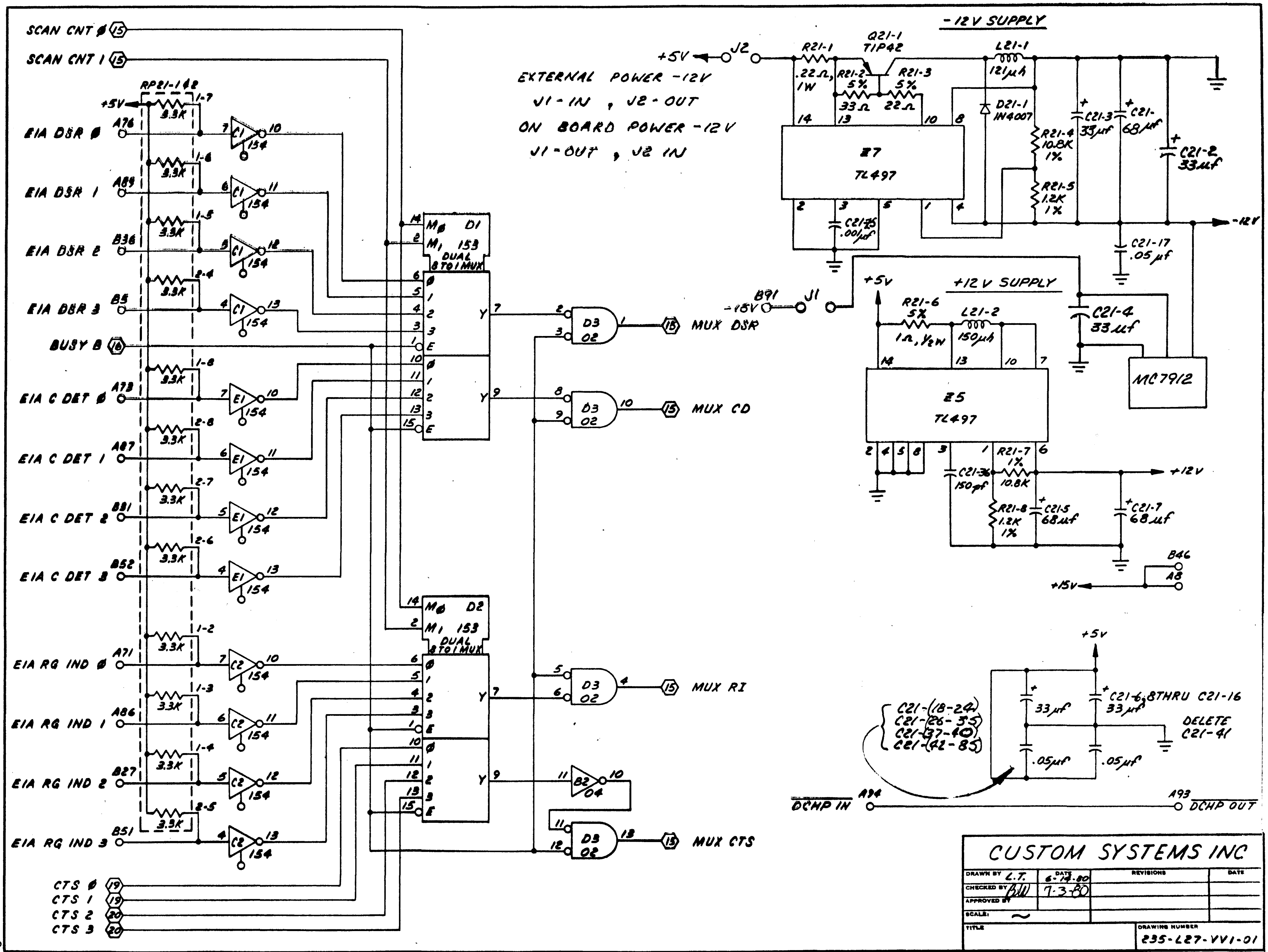


BAUD RATE DIVIDER
CHAIN
BAUD RATE SELECT REG
SELECT MUX
BAUD RATE DE-MUX
CLOCK SOURCE SELECT
CLOCK DIVIDER I
CLOCK DIVIDER II
ON LINE
GROUP SEL
IOPLS
DIAG CLR
RESET
DCLK I
DCLK II
IO PULSE
CLK (9.8304 MHz)
CLK 0
CLK 1
CLK 2
CLK 3
CRY CLK
LINE CHAR STB
DATA 8
DATA 7
CLOCK OSC 9.8304 MHz
CUSTOM SYSTEMS INC
235-L24-VV1-01
(SHEET 18)


RTS Ø
BREAK Ø
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
EIA CTS Ø
PARITY INH
LD XMTR Ø
CRL Ø
RCV STAT Ø
CLR RCVR Ø
BUSY
CLK Ø
EIA RCV DATA Ø
LOOP BK Ø
EIA CTS 1
LD XMTR 1
CRL 1
RCV STAT 1
CLR RCVR 1
CLK 1
EIA RCV DATA 1
LOOP BK 1
RTS 1
BREAK 1
LOOP BACK
RTS CONTROL
XMTR
P6
R6
AY5-1013A
RCVR
CTS Ø
EIA RTS Ø
XMTR RDY
EIA XMIT DATA Ø
R-DATA 8
R-DATA 9
R-DATA 10
R-DATA 11
R-DATA 12
R-DATA 13
R-DATA 14
R-DATA 15
O-ERR
F-ERR
P-ERR
RCVR RDY
CTS 1
EIA RTS 1
EIA XMIT DATA 1
CUSTOM SYSTEMS INC
DRAWN BY L.T. DATE 6-12-80
CHECKED BY 7-3-80
APPROVED BY
SCALE
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L25-VY1-01

(SHEET 19)


RTS 2
BREAK 2
DATA 8
DATA 9
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
EIA CTS 2
PARITY INH
LD XMTR 2
CRL 2
RCV STAT 2
CLR RCVR 2
BUSY
CLK 2
EIA RCV DATA 2
LOOP BK 2
EIA CTS 3
LD XMTR 3
CRL 3
RCV STAT 3
CLR RCVR 3
CLK 3
EIA RCV DATA 3
LOOP BK 3
RTS 3
BREAK 3
LOOP BACK
LOOP BACK
XMTR
T6
AY5-1013A
RCVR
XMTR
X6
AY5-1013A
RCVR
RTS CONTROL
RTS CONTROL
CTS 2
EIA RTS 2
XMTR RDY
EIA XMIT DATA 2
R-DATA 8
R-DATA 9
R-DATA 10
R-DATA 11
R-DATA 12
R-DATA 13
R-DATA 14
R-DATA 15
O-ERR
F-ERR
P-ERR
RCVR RDY
CTS 3
EIA RTS 3
EIA XMIT DATA 3
CUSTOM SYSTEMS INC
DRAWN BY L.T. DATE 6-12-80
CHECKED BY BW 7-3-80
APPROVED BY
SCALE: ~
TITLE
REVISIONS
DATE
DRAWING NUMBER
235-L26-VYI-01
(SHEET 20)


SCAN CNT ∅
SCAN CNT 1
-12V SUPPLY
EXTERNAL POWER -12V
J1 - IN , J2 - OUT
ON BOARD POWER -12V
J1 - OUT , J2 IN
EIA DSR ∅
EIA DSR 1
EIA DSR 2
EIA DSR 3
BUSY B
EIA C DET ∅
EIA C DET 1
EIA C DET 2
EIA C DET 3
EIA RG IND ∅
EIA RG IND 1
EIA RG IND 2
EIA RG IND 3
CTS ∅
CTS 1
CTS 2
CTS 3
RP21-1&2
DUAL 8 TO 1 MUX
MUX DSR
MUX CD
MUX RI
MUX CTS
+12V SUPPLY
TL497
MC7912
C21-(18-24)
C21-(26-35)
C21-(37-40)
C21-(42-85)
C21-6,8 THRU C21-16
DELETE C21-41
DCHP IN
DCHP OUT
CUSTOM SYSTEMS INC
DRAWN BY L.T. 6-14-80
CHECKED BY BW 7-3-80
DRAWING NUMBER
235-L27-VV1-01

(SHEET 21)