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PROGRAM

NOVA 3 LOGIC TEST

TAPE

095-000345-01

ABSTRACT

THE NOVA 3 LOGIC TEST IS A MAINTENANCE PROGRAM DESIGNED TO TEST THE NOVA 3 CENTRAL PROCESSING UNIT. IT IS A GATE BY GATE TEST OF THE LOGIC USED TO IMPLEMENT THE NOVA 3 INSTRUCTION SET. ALSO INCLUDED IS A MINIMUM LEVEL TEST OF THE CPU I/O INSTRUCTIONS, TELETYPE I/O, AND PROGRAM INTERRUPT.

```
 0001 N3LGC MACRO REV 03.00              11:12:26 07/02/76
01
02
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: N3LGCT.SR                          PART NUMBER: 094-000749
10              ;
11              ;
12              ; DESCRIPTION: NOVA 3 LOGIC TEST
13              ;
14              ;
15              ; REVISION HISTORY:
16              ;
17              ;       REV.            DATE
18              ;
19              ;       00              02/26/76
20              ;       01              07/02/76
21              ;
22              ;
23              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1976
24              ; ALL RIGHTS RESERVED.
25              ;*****************************************************************
```

```
!0002 N3LGC
01
                        .TITL N3LGC
03              ;               NOVA 3 LOGIC TEST
04              ;1.     ABSTRACT
05              ;               THE NOVA 3 LOGIC TEST IS A MAINTENANCE PROGRAM
06              ;               DESIGNED TO TEST THE NOVA 3 CENTRAL PROCESSING
07              ;               UNIT.  IT IS A GATE BY GATE TEST OF THE LOGIC
08              ;               USED TO IMPLEMENT THE NOVA 3 INSTRUCTION SET.
09              ;               ALSO INCLUDED IS A MINIMUM LEVEL TEST OF THE
10              ;               CPU I/O INSTRUCTIONS,TELETYPE I/O, AND
11              ;               PROGRAM INTERRUPT.
12
13              ;2.     MACHINE REQUIREMENTS
14              ;2.1            NOVA 3 PROCESSOR
15              ;2.2            4K OF READ/WRITE MEMORY
16              ;2.3            BASIC I/O TELETYPE INTERFACE
17              ;
18              ;
19              ;4.     OPERATING PROCEDURE
20              ;4.1            VERIFY THAT THE NOVA 3 WILL PERFORM ALL
21              ;               CONSOLE FUNCTIONS, I.E. EXAMINE/EXAMINE NEXT
22              ;               DEPOSIT/DEPOSIT NEXT AC'S EXAMINE/DEPOSIT
23              ;4.2            LOAD THE PROGRAM VIA THE BINARY LOADER.
24              ;4.3            SET THE SWITCHES EQUAL TO 200
25              ;4.4            PRESS START
26              ;4.5            MACHINE SHOULD HALT M/A=201, PRESS CONTINUE
27              ;4.6            PROCESSOR SHOULD CONTINUE TO RUN WITHOUT HALTING
28              ;               TELETYPE SHOULD STUTTER FOR 60 CHARACTERS
29              ;               THE TYPEOUT "PASS" SHOULD OCCUR AND THE TEST
30              ;               SHOULD CONTINUE TO LOOP WITH THE TELETYPE RUNNIN
31              ;               AT A SLOWER RATE.
32              ; 4.7           TO RESTART AFTER FIRST PASS, START AT LOC 170
33
34
35              ;5.     ERROR DESCRIPTION
36              ;5.1            DETECTED ERRORS WILL CAUSE THE PROGRAM TO DO A
37              ;               PROCESSOR HALT.
38              ;5.2            RECORD THE STATE OF THE PROCESSOR AND REGISTERS
39              ;               AT THE TIME OF THE HALT.  CONSULT THE LISTING
40              ;               AT THE ADDRESS OF THE ERROR HALT FOR PROB-
41              ;               ABLE CAUSES OF THE FAILURE. CONSTRUCT A LOOP
42              ;               THAT WILL REPEAT THE FAILURE AND SCOPE AS REQUIR
43
44              ;6.     PROGRAM DESCRIPTION
45              ;               THIS PROGRAM IS A COLLECTION OF SMALL TESTS,
46              ;               EACH TEST IN SEQUENCE BASED ON PREVIOUS TESTS
47              ;               WORKING AND DESIGNED TO TEST AS SMALL AN ADDI-
48              ;               TIONAL PIECE OF THE LOGIC AS POSSIBLE.
49              ;
50              ;
51              ; 7.     CAT/KITTEN OPERATION
52              ;
53              ;               IF THE PROGRAM WAS LOADED FROM DTOS WITH CAT
54              ;               OR KITTEN THE PROGRAM WILL RUN IT IN
55              ;               THE BACKGROUND AFTER ONE PASS OF USING THE TTY
56              ;               INTERRUPTS. THE PROGRAM WILL RUN MUCH
57              ;               SLOWER ALLOWING THE CAT/KITTEN AMPLE TIME TO
58              ;               COMPLETE A PASS.
```

```
↓0003 N3LGC
01
02        000000          .LOC 0
03 00000 000147           DIRT
04 00001 100000           #0
05 00002 047503           .TXT ↓COPYRIGHT (C) DGC,1976
06        054520
07        044522
08        044107
09        020124
10        041450
11        020051
12        043504
13        026103
14        034461
15        033067
16 00015 046101 ALL RIGHTS RESERVED↓
17        020114
18        044522
19        044107
20        051524
21        051040
22        051525
23        051105
24        042526
25        000104
26
27        000045          .LOC 45
28 00045 000141           EGGS
29
30        000055          .LOC 55
31 00055 000001 K1: 1
32 00056 000002 K2: 2
33 00057 000003 K3: 3
34 00060 000004 K4: 4
35 00061 000005 K5: 5
36 00062 000006 K6: 6
37 00063 000007 K7: 7
38 00064 000010 K10: 10
39 00065 000020 K20: 20
40 00066 000040 K40: 40
41 00067 000100 K100: 100
42 00070 000200 K200: 200
43 00071 000405 K405: 405
44 00072 000400 K400: 400
45 00073 001000 K1000: 1000
46 00074 002000 K2000: 2000
47 00075 004000 K4000: 4000
48 00076 003300 K3.3K:  3300
49 00077 010000 K10K: 10000
50 00100 020000 K20K: 20000
51 00101 040000 K40K: 40000
52 00102 100000 K100K: 100000
53 00103 077777 K0777:  077777
54 00104 020400 KLDA.:  20400   ;= TO AN LDA 0,, OFF PAGE0
55 00105 000300 K300:   300
56 00106 100300 KD300: #300
57 00107 100011 KD11:   #11
58 00110 100017 KD17:   #17
59 00111 000210 K210:   210
60 00112 177770 KM8:    -8.
```

```
 0004 N3LGC
01 00113 100021 KD21:   #21
02 00114 100037 KD37:   #37
03 00115 125251 KCBE:   125251  ;EVEN # BITS
04 00116 052525 KCBO:   052525  ;ODD # BITS
05 00117 025252 K2525:  25252
06        000116 K5252 = KCBO
07 00120 000420 K420:   420
08 00121 001400 KJRET:  JMP 0,3 ;JSR RETURNS TYPE JMP
09 00122 000000 K0:     0
10 00123 000074 K60:    60.
11 00124 000074 TESTK:  060.
12 00125 000215 K215:   215
13 00126 000212 K212:   212
14 00127 000323 K323:   323
15 00130 000011 KTTO:   TTO
16 00131 000377 K377:   377
17 00132 000320 K320:   320
18 00133 002300 JMP3K:  JMP #300
19 00134 000001 PKR00:  1
20 00135 000001 PKR01:  1
21 00136 001377 K1377:  1377
22 00137 000000 TSTLC:  0
23 00140 000000 KATSW:  0       ;=1 IF USE CAT/KITTEN ON THIS PASS
24 00141 000000 EGGS:   0
25 00142 000000         0
26 00143 000000         0
27 00144 000000         0
28 00145 000000         0
29 00146 000000 SWREG:  0
30
31 00147 031516 DIRT:   .TXTE ↓N3LGCT   011↓
32        043714
33        152303
34        120240
35        030240
36        000261
37 00155 000000         0
38 00156 000201         DTOSB
39 00157 167774         167774
40 00160 000000         0
41 00161 000000         0
42 00162 000000         0
43 00163 000000         0
44 00164 000000         0
```

```
10005 N3LGC
01
02        063077          .DUSR HALTE= HALT
03
04        061001          .DIAC MTSP = DOA 0,1
05        060001          .DIAC MTFP = 060001     ;NIO 0,1
06        061201          .DIAC MFSP = DOAC 0,1
07        060201          .DIAC MFFP = 060201     ;NIOC 0,1
08        061401          .DIAC PSH = DIB 0,1
09        061601          .DIAC POP = DIBC 0,1
10        062401          .DUSR SAVE = DIC 0,1
11        062601          .DUSR RTRN = DICC 0,1
12        100010          .DUSR TRAP = 100010     ;COM# 0,0
13
14
15        063077          EHALT = HALTE
16
17        000046          TPLOC = 46
18        000047          TPADR = 47
```

```
10006 N3LGC
01
02                000170          .LOC 170
03 00170 062677 RESTR:  IORST
04 00171 102400         SUB 0,0
05 00172 040140         STA 0,KATSW
06 00173 101400         INC 0,0
07 00174 040134         STA 0,PKR00
08 00175 040135         STA 0,PKR01
09 00176 000200         JMP START
10                000200          .LOC 200
11 00200 063077 START:  HALT            ;TO TEST CPU HALT
12                      ;THIS TEST WILL VERIFY THAT A ALC
13                      ;INSTRUCTION WILL NOT SKIP/THEN SKIP UNCONDITIONALLY
14                      ;ERR HALT INDICATES EXTRANEOUS SKIP
15                      DTOSB:
16                      A1A:
17 00201 100000         COM 0,0         ;COM SHD NOT CAUSE SKIP IR13,14,15=000
18 00202 100001         COM 0,0,SKP     ;COM SKIP ALWAYS IR13,14,15=001
19 00203 063077         HALTE
20                      ;IF ABOVE FAILS SEE IR15 AND CALC  AT SETSKIP LOGIC
21
22                      ;IF ABOVE CAUSES A JMP 0, SEE IR12 AT SET TRAP AND GATE
```

```
10007 N3LGC
01                ;TEST CARRY (CRY FLOP) AND SKIP LOGIC
02
03 00204 000212           JMP A9A           ;LOCATIONS 207-211 ARE RESERVED
04       000212           .LOC 212
05 00212 102022 A9A:      ADCZ 0,0,SZC      ;NOT NEWCARRY,IR14,NOT IR15
06 00213 063077           HALTE             ;ZERO INPUT TO CARRY FAILED
07
08 00214 102023           ADCZ 0,0,SNC      ;SNC NOT SEE CALC,IR15
09 00215 102002           ADC 0,0,SZC       ;ALSO TEST ZERO HOLD OF CRY
10 00216 063077           HALTE             ;IF CRY=1 SEE NOT IR12 OR
11                ;ABOVE FAILURE IF CRY=1 MIGHT BE IN "NOT SCI" NOT IR10
12 00217 102026 A9B:      ADCZ 0,0,SEZ      ;CARRY=0 NOT NEWCARRY,IR14,NOT IR15
13 00220 063077           HALTE             ;INVOLVES SAME GATES AS SZC
14
15 00221 102043           ADCO 0,0,SNC      ;TEST FOR TRUE CALC=IR15
16 00222 063077           HALTE             ;1'S INPUT TO CRY CALC WAS NOT 1
17
18 00223 102042           ADCO 0,0,SZC      ;TEST FOR CALC,IR15 FALSE
19 00224 102003           ADC 0,0,SNC       ;ALSO TEST ONES HOLD OF CRY
20 00225 063077           HALTE             ;IF CRY=0 SEE NOT IR12
21                ;ABOVE FAILURE IF CRY=0 MIGHT BE IN "NOT SCI" IR11
22
23 00226 102046 A9C:      ADCO 0,0,SEZ      ;AGAIN TEST NOT NOT NEWCARRY,IR14,NOT IR
24 00227 102003           ADC 0,0,SNC       ;SAME GATES AS LAST TEST (SZC)
25 00230 063077           HALTE             ;EXCEPT FOR ZR,IR13
26
27                ;CARRY SHOULD=1 COMING INTO NEXT TEST CHECK
28                ;OF TRANSITION TO 0 ON NOT NEWCARRY
29 00231 102022 A9D:      ADCZ 0,0,SZC      ;SKIP ON NOT NEWCARRY,IR14,NOT IR15
30 00232 063077           HALTE             ;SEE CRY,IR11 THROUGH NOT SCI
31
32 00233 102040           ADCO 0,0          ;SET CRY=1
33 00234 102023           ADCZ 0,0,SNC      ;TRANSITION CRY TO 0
34 00235 102002           ADC 0,0,SZC       ;CHECK 0 REALLY GOT THERE
35 00236 063077           HALTE             ;CRY=0 IS SNC FAILED
36                ;CRY=1 SEE CRY,IR11 IN "NOT SCI" GATES OR NOT NEWCARRY,LOAD CARR
37
38                ;CARRY=0 COMING INTO NEXT TEST CHECK NOT CRY,NOT IR10
39 00237 102023 A9E:      ADCZ 0,0,SNC      ;ALSO NOT (CRY,IR11)
40 00240 102002           ADC 0,0,SZC       ;CRY SHD HAVE STAYED 0
41 00241 063077           HALTE             ;ALSO NOT NEWCARRY AND LOAD CARRY USED
```

726

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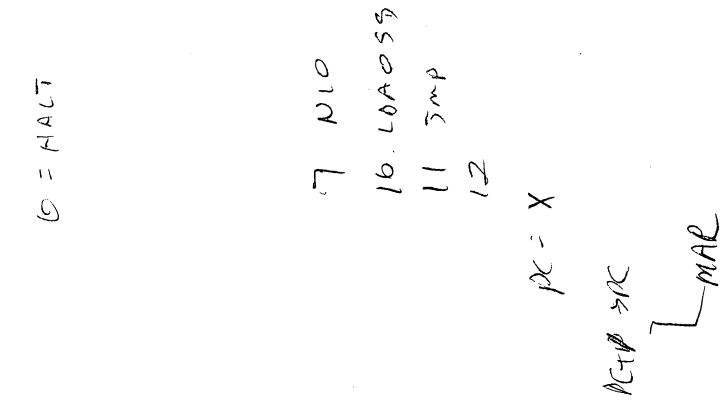
10008 N3LGC
01
02   775
03                ;TEST CARRY TO TRANSITION FROM 0 TO 1
04 00242 102020 A9F:      ADCZ 0,0,         ;SET CRY=1
05 00243 102042           ADCO 0,0,SZC      ;MAKE IT=1 AGAIN NOT CRY,IR10
06 00244 102003           ADC 0,0,SNC       ;DID 1 REALLY GET TO CRY
07 00245 063077           HALTE             ;IF CRY=1 SZC FAILED
08                ;IF CRY=0 SEE CALC,NOT IR12
09
10                ;TEST COMPLIMENT OF CARRY IR11,IR10
11 00246 102020 A9G:      ADCZ 0,0          ;SET CRY=0
12 00247 102062           ADCC 0,0,SZC      ;TRANS CRY 0 TO 1 (SZC NOT)
13 00250 102003           ADC 0,0,SNC       ;CRY SHD=1
14 00251 063077           HALTE             ;CRY=0 SEE CALC,LOAD CARRY
15                ;CARRY=0 SEE NOT SCI
16
17 00252 102040 A9H:      ADCO 0,0          ;SET CRY=1
18 00253 102063           ADCC 0,0,SNC      ;NOT NEWCARRY SHD BE TRUE (NOT SNC)
19 00254 102002           ADC 0,0,SZC       ;CARRY SHD REALLY=0
20 00255 063077           HALTE             ;CRY=1 SEE NOT NEWCARRY AND LOAD CARRY
21
```

```
10009 N3LGC
01
02
03                      ;TEST FOR ADC TO SET AC0=MOSTLY 1'S AND SNR TO SKIP
04                      ;START BUILDING INSTRUCTIONS TO CREATE CONSTANTS
05                      ;VERY LITTLE LOGIC IS VERIFIED YET
06 00256 102005 A20:    ADC 0,0,SNR     ;ANY RESULT IN AC0 SHD CAUSE SKP
07 00257 063077         HALTE           ;AC0 ANYTHING BUT 0 IS SNR FAILED
08                  ;AC0 NOT=0 SEE IR15 IN SKIP CONTROL AND ZR AND GATES
09                  ;AC0=0 ADC MAY=SUB SEE DP1/D ROM NOT IR7 INPUT
10
11                  ;SZR SHOULD NOT SKIP WHEN AC0 NOT=0
12 00260 102004 A21:    ADC 0,0,SZR     ;TEST A2 INDICATES AC0 NOT=0
13 00261 102005         ADC 0,0,SNR     ;AS RESULT OF AN ADC
14 00262 063077         HALTE           ;SZR SKIPPED IF AC0 NOT=0
15
16                  ;ATTEMPT TO GENERATE AN ALL 0'S CONSTANT VIA ADC+COM
17                  ;ALSO TESTS SZR TO SKIP IN GROSS CASE
18 00263 102000 A22:    ADC 0,0         ;ADC MAY NOT YET=-1
19 00264 100004         COM 0,0,SZR     ;OR COM MAY ALSO FAIL
20                  ; RESULT DOES NOT=0
21 00265 063077         HALTE           ;RESULT IN AC0 SHOULD HELP TO
22                  ;ISOLATE PROBLEM TO A BIT OR CARRY GATE THROUGH THE ALU
23                  ;AC0=0 IS SZR FAILED TO SKIP IR15=0 IN SKIP LOGIC
24                  ;IF COM 0,0,=-1 THEN COM MAY=MOV OR ADC IR5+IR6
25
26                  ;TEST ZERO CARRY SKIP FROM COM 0,0
27 00266 102020 A23:    ADCZ 0,0        ;0 TO CARRY=1 TO AC0
28 00267 100002         COM 0,0,SZC     ;CARRY SHD STILL=0
29 00270 063077         HALTE
30
31                  ;TEST SKIP EITHER ZERO WITH BOTH AC AND CARRY=0
32
33 00271 102020 A24:    ADCZ 0,0
34 00272 100006         COM 0,0,SEZ     ;BOTH RESULT AND CARRY=0
35 00273 063077         HALTE           ;SEZ FAILED BOTH=0
36                  ;SEE IR13,ZR+IR14,NOT NEWCARRY,NOT IR15 ((NEG AND) SKIP CONTRO
37
38                  ;TEST SKIP EITHER ZERO WITH AC=0 AND CARRY=1
39
40 00274 000302         JMP A25
41       000302         .LOC 302
42 00302 102040 A25:    ADCO 0,0
43 00303 100006         COM 0,0,SEZ     ;RES=0 BUT CARRY=1
44 00304 063077         HALTE           ;SEE ZR,IR13,NOT IR15
```




```
10010 N3LGC
01
02                  ;THE NEXT SERIES OF TESTS VERIFY
03                  ;THAT REFERENCING ONE AC DOES NOT DISTURB THE OTHERS
04                      .MACRO ACITS    ;AC ISOLATION TEST^1
05                  ;ACI^1:
06                      ADC ^2,^2
07                      COM ^2,^2       ;SET AC^2 TO 0
08                      MOV ^2,^4       ;SET AC^4 TO 0
09                      MOV ^2,^5       ;SET AC^5 TO 0
10                      ADC ^3,^3       ;SET AC^3 TO -1
11                      MOV ^2,^2,SZR   ;TEST AC^2 TO STILL=0
12                      HALTE           ;AC^3 DEST, DISTURBED AC^2
13                      MOV ^4,^4,SZR   ;TEST AC^4 TO=0
14                      HALTE           ;AC^3 DEST, DISTURBED AC^4
15                      MOV ^5,^5,SZR   ;TEST AC^5 TO = 0
16                      HALTE           ;AC^3 DEST, DISTURBED AC^5
17                  %
18
19                      ACITS   00      0       1       2       3
20                  ;ACI00:
21 00305 102000         ADC 0,0
22 00306 100000         COM 0,0 ;SET AC0 TO 0
23 00307 111000         MOV 0,2 ;SET AC2 TO 0
24 00310 115000         MOV 0,3 ;SET AC3 TO 0
25 00311 126000         ADC 1,1 ;SET AC1 TO -1
26 00312 101004         MOV 0,0,SZR     ;TEST AC0 TO STILL=0
27 00313 063077         HALTE           ;AC1 DEST, DISTURBED AC0
28 00314 151004         MOV 2,2,SZR     ;TEST AC2 TO=0
29 00315 063077         HALTE           ;AC1 DEST, DISTURBED AC2
30 00316 175004         MOV 3,3,SZR     ;TEST AC3 TO = 0
31 00317 063077         HALTE           ;AC1 DEST, DISTURBED AC3
32                      ACITS   01      1       2       3       0
33                  ;ACI01:
34 00320 126000         ADC 1,1
35 00321 124000         COM 1,1 ;SET AC1 TO 0
36 00322 135000         MOV 1,3 ;SET AC3 TO 0
37 00323 121000         MOV 1,0 ;SET AC0 TO 0
38 00324 152000         ADC 2,2 ;SET AC2 TO -1
39 00325 125004         MOV 1,1,SZR     ;TEST AC1 TO STILL=0
40 00326 063077         HALTE           ;AC2 DEST, DISTURBED AC1
41 00327 175004         MOV 3,3,SZR     ;TEST AC3 TO=0
42 00330 063077         HALTE           ;AC2 DEST, DISTURBED AC3
43 00331 101004         MOV 0,0,SZR     ;TEST AC0 TO = 0
44 00332 063077         HALTE           ;AC2 DEST, DISTURBED AC0
45                      ACITS   02      2       3       0       1
46                  ;ACI02:
47 00333 152000         ADC 2,2
48 00334 150000         COM 2,2 ;SET AC2 TO 0
49 00335 141000         MOV 2,0 ;SET AC0 TO 0
50 00336 145000         MOV 2,1 ;SET AC1 TO 0
51 00337 176000         ADC 3,3 ;SET AC3 TO -1
52 00340 151004         MOV 2,2,SZR     ;TEST AC2 TO STILL=0
53 00341 063077         HALTE           ;AC3 DEST, DISTURBED AC2
54 00342 101004         MOV 0,0,SZR     ;TEST AC0 TO=0
55 00343 063077         HALTE           ;AC3 DEST, DISTURBED AC0
56 00344 125004         MOV 1,1,SZR     ;TEST AC1 TO = 0
57 00345 063077         HALTE           ;AC3 DEST, DISTURBED AC1
58                      ACITS   03      3       0       1       2
59                  ;ACI03:
60 00346 176000         ADC 3,3
```

```
 0011 N3LGC
01 00347 174000          COM 3,3 ;SET AC3 TO 0
02 00350 165000          MOV 3,1 ;SET AC1 TO 0
03 00351 171000          MOV 3,2 ;SET AC2 TO 0
04 00352 102000          ADC 0,0 ;SET AC0 TO -1
05 00353 175004          MOV 3,3,SZR      ;TEST AC3 TO STILL=0
06 00354 063077          HALTE            ;AC0 DEST, DISTURBED AC3
07 00355 125004          MOV 1,1,SZR      ;TEST AC1 TO=0
08 00356 063077          HALTE            ;AC0 DEST, DISTURBED AC1
09 00357 151004          MOV 2,2,SZR      ;TEST AC2 TO = 0
10 00360 063077          HALTE            ;AC0 DEST, DISTURBED AC2
```

```
 0012 N3LGC
01                ;THE FOLLOWING TESTS INSURE 0'S ISOLATION
02                ;OF AC TO AC
03
04                        .MACRO ACIT2    ;0'S ISOLATION TEST
05                ;ACI^1:
06                        ADC ^2,^2       ;SET AC^2=-1
07                        COM ^2,^3       ;SET 0'S TO AC^3
08                        COM ^2,^2,SZR   ;AC^2 SHD STILL=-1
09                        HALTE           ;0'S TO AC^3 DISTURBED AC^2
10                %
11                        ACIT2   12      0       1
12                ;ACI12:
13 00361 102000           ADC 0,0 ;SET AC0=-1
14 00362 104000           COM 0,1 ;SET 0'S TO AC1
15 00363 100004           COM 0,0,SZR     ;AC0 SHD STILL=-1
16 00364 063077           HALTE           ;0'S TO AC1 DISTURBED AC0
17                        ACIT2   13      0       2
18                ;ACI13:
19 00365 102000           ADC 0,0 ;SET AC0=-1
20 00366 110000           COM 0,2 ;SET 0'S TO AC2
21 00367 100004           COM 0,0,SZR     ;AC0 SHD STILL=-1
22 00370 063077           HALTE           ;0'S TO AC2 DISTURBED AC0
23                        ACIT2   14      0       3
24                ;ACI14:
25 00371 102000           ADC 0,0 ;SET AC0=-1
26 00372 114000           COM 0,3 ;SET 0'S TO AC3
27 00373 100004           COM 0,0,SZR     ;AC0 SHD STILL=-1
28 00374 063077           HALTE           ;0'S TO AC3 DISTURBED AC0
29 00375 000444           JMP XXYZ
30        000441          .LOC 441
31                XXYZ:
32                        ACIT2   15      1       0
33                ;ACI15:
34 00441 126000           ADC 1,1 ;SET AC1=-1
35 00442 120000           COM 1,0 ;SET 0'S TO AC0
36 00443 124004           COM 1,1,SZR     ;AC1 SHD STILL=-1
37 00444 063077           HALTE           ;0'S TO AC0 DISTURBED AC1
38                        ACIT2   16      1       2
39                ;ACI16:
40 00445 126000           ADC 1,1 ;SET AC1=-1
41 00446 130000           COM 1,2 ;SET 0'S TO AC2
42 00447 124004           COM 1,1,SZR     ;AC1 SHD STILL=-1
43 00450 063077           HALTE           ;0'S TO AC2 DISTURBED AC1
44                        ACIT2   17      1       3
45                ;ACI17:
46 00451 126000           ADC 1,1 ;SET AC1=-1
47 00452 134000           COM 1,3 ;SET 0'S TO AC3
48 00453 124004           COM 1,1,SZR     ;AC1 SHD STILL=-1
49 00454 063077           HALTE           ;0'S TO AC3 DISTURBED AC1
50                        ACIT2   18      2       0
51                ;ACI18:
52 00455 152000           ADC 2,2 ;SET AC2=-1
53 00456 140000           COM 2,0 ;SET 0'S TO AC0
54 00457 150004           COM 2,2,SZR     ;AC2 SHD STILL=-1
55 00460 063077           HALTE           ;0'S TO AC0 DISTURBED AC2
56                        ACIT2   19      2       1
57                ;ACI19:
58 00461 152000           ADC 2,2 ;SET AC2=-1
59 00462 144000           COM 2,1 ;SET 0'S TO AC1
60 00463 150004           COM 2,2,SZR     ;AC2 SHD STILL=-1
```

```
 0013 N3LGC
01 00464 063077          HALTE            ;0'S TO AC1 DISTURBED AC2
02                       ACIT2   20       2        3
03                ;ACI20:
04 00465 152000          ADC 2,2 ;SET AC2=-1
05 00466 154000          COM 2,3 ;SET 0'S TO AC3
06 00467 150004          COM 2,2,SZR      ;AC2 SHD STILL=-1
07 00470 063077          HALTE            ;0'S TO AC3 DISTURBED AC2
08                       ACIT2   21       3        0
09                ;ACI21:
10 00471 176000          ADC 3,3 ;SET AC3=-1
11 00472 160000          COM 3,0 ;SET 0'S TO AC0
12 00473 174004          COM 3,3,SZR      ;AC3 SHD STILL=-1
13 00474 063077          HALTE            ;0'S TO AC0 DISTURBED AC3
14                       ACIT2   22       3        1
15                ;ACI22:
16 00475 176000          ADC 3,3 ;SET AC3=-1
17 00476 164000          COM 3,1 ;SET 0'S TO AC1
18 00477 174004          COM 3,3,SZR      ;AC3 SHD STILL=-1
19 00500 063077          HALTE            ;0'S TO AC1 DISTURBED AC3
20                       ACIT2   23       3        2
21                ;ACI23:
22 00501 176000          ADC 3,3 ;SET AC3=-1
23 00502 170000          COM 3,2 ;SET 0'S TO AC2
24 00503 174004          COM 3,3,SZR      ;AC3 SHD STILL=-1
25 00504 063077          HALTE            ;0'S TO AC2 DISTURBED AC3
26
27
28
```

```
;0014 N3LGC
01                ;AT THIS POINT IN THE TEST THE FOLLOWING
02                ;ITEMS HAVE BEEN VERIFIED
03                ;1. NONE OF THE ALC INSTRUCTIONS SKIP EXTRANEOUSLY
04                ;2. CRY CAN BE SET TO 1 OR 0 AND CRY SKIPS
05                     ;FUNCTION CORRECTLY
06                ;3. A CONSTANT OTHER THAN 0 CAN BE GENERATED
07                     ;BY AN ADC ANY AC TO ITSELF
08                ;4. A CONSTANT THAT AT LEAST APPEARS TO=0 CAN
09                     ;BE GENERATED BY AN ADC+COM ANY AC TO ITSELF
10                ;5. ANY AC MAY BE REFERENCED BY EITHER
11                     ;AN ADC OR COM WITHOUT DISTURBING THE OTHERS
12                ;6. SNR SKIPS ON -1 DOES NOT SKIP ON 0
13                ;7. SZR SKIPS ON 0 DOES NOT SKIP ON -1
14                ;8. NO TRANSFER (IR 12=1) INHIBITS CARRY CHANGE
15
16                ;TEST LEFT SHIFT OF A 1 INTO 0 CRY
17              ;TESTS BIT 9=1 ENABLES LEFT SHIFT SHIFT INPUTS
18 00505 102020 A40:     ADCZ 0,0
19 00506 101102          MOVL 0,0,SZC     ;MAKE LEFT SHIFT CRY IN=1
20 00507 101003          MOV 0,0,SNC      ;TEST FOR CRY REALLY=1
21 00510 063077          HALTE            ;LEFT SHIFT IR9 FAILED
22                ;IF GATE IR8=1 AND CALC IS TRUE TEST WILL ALSO FAIL (SWAP)
23                ;TEST LEFT SHIFT OF A 0 INTO A 1 CRY
24
25 00511 102040 A41:     ADCO 0,0
26 00512 100103          COML 0,0,SNC     ;CRY INPUT (ZC)
27 00513 101002          MOV 0,0,SZC      ;DID 0 REALLY GET TO CRY
28 00514 063077          HALTE            ;LEFT SHIFT (IR9) 0 INTO CRY
29
30
```

```
10015 N3LGC
01
02                  ;TEST FOR NO BITS TO PICK UP ON SHIFT LEFT
03
04 00515 102020 A42:    ADCZ 0,0            ;AC0=-1  CRY=0
05 00516 100105          COML 0,0,SNR       ;TEST RESULT LEVELS=0
06 00517 101004          MOV 0,0,SZR        ;AND ACTUAL RESULT=0
07 00520 063077          HALTE              ;AC0 L SHOULD=0
08                  ;TEST THE TRANSFER OF A CRY=1 INTO BIT 15 AC 0
09 00521 102040 A43:    ADCO 0,0
10 00522 100105          COML 0,0,SNR       ;CRY SHOULD=1 TO AC 15
11 00523 063077          HALTE              ;IF AC0=0 SEE ALU 15
12                  ;IF AC0=+1 SEE NOT SUM 15 INTO SKIP LOGIC
13                  ;IN ABOVE TEST ALU LEVEL INPUT IS NOT SCI (FALSE)
14                  ;NOT SUM 15 GOES LOW FOR LEFT SHIFT ALSO
15                  )
16                  ;TEST BIT 15=1 STRAIGHT TRANSFER THROUGH
17
18 00524 102040 A44:    ADCO 0,0
19 00525 100104          COML 0,0,SZR       ;IN CASE LEVEL NOT SUM 15 FAILS
20 00526 101005          MOV 0,0,SNR        ;AC0=+1 RESULT IS NON ZERO
21 00527 063077          HALTE
22                  ;ABOVE FAILURE IS MOST PROBABLY "NOT ALU 15" FALSE WAS TRUE
23                  ;OR "NOT SUM 15" FALSE INTO ZR AND'S IN SKP LOGIC
24
25                  ;TEST RIGHT SHIFT LOGIC INTO CRY
26                  ;TEST ONES SHIFT INTO A 0 CRY
27                  ;TEST OF IR8=1 ENABLES RIGHT SHIFT INPUTS
28 00530 102223 A45:    ADCZR 0,0,SNC      ;TEST INPUT TO CRY=1
29 00531 063077          HALTE
30                  ;IF IR9 AND CALC GATE IS TRUE TEST WILL ALSO FAIL (SWAP)
31
32 00532 102222 A46:    ADCZR 0,0,SZC      ;INPUT TO CRY=1
33 00533 100003          COM 0,0,SNC        ;CRY RIGHT SHD STILL=1
34 00534 063077          HALTE
35                  ;TEST RIGHT 0 INPUT TO CRY=1
36
37 00535 102040 A47:    ADCO 0,0
38 00536 100203          COMR 0,0,SNC
39 00537 100002          COM 0,0,SZC
40 00540 063077          HALTE              ;CRY SHOULD=0
41                  ;TEST OF NOT ALU0 INPUT TO NOT NEWCARRY AND IR8=1
42                  )
```

```
10016 N3LGC
01
02                  ;TEST FOR NO BITS TO PICK UP ON RIGHT SHIFT
03
04 00541 102020 A48:    ADCZ 0,0           ;(AC0)=-1 CRY=0
05 00542 100205          COMR 0,0,SNR       ;SHIFT Q'S RIGHT
06 00543 101004          MOV 0,0,SZR        ;RESULT SHOULD REMAIN=0
07 00544 063077          HALTE              ;RIGHT SHIFT ALL Q'S FAILED
08                  ;EXAMINE AC0 TO DETERMINE BITS PICKED SHIFT RIGHT
09
10                  ;SHIFT CRY=1 RIGHT INTO BIT 0
11                  ;ALSO TEST BIT 0=1 INTO NOT ZR
12 00545 102040 A49:    ADCO 0,0           ;CRY=1 AC0=-1
13 00546 100204          COMR 0,0,SZR       ;RIGHT SHIFT 0'S CRY=1 TO BIT 0
14 00547 101005          MOV 0,0,SNR        ;TEST RESULT TO REALLY HOLD
15 00550 063077          HALTE              ;RIGHT SHIFT CRY=1 FAILED
16                  ;ABOVE HALTE CAN BE NOT SCI INTO NOT SUM 0 (AC0 WILL=0)
17                  ;OR NOT SUM 0 INTO ZR AND GATES  (AC0=100000)
18
19                  ;TEST RIGHT SHIFT OF AC0=0'S INTO AC1
20                  ;START BUILDING DOUBLE REGISTERS FOR TEST USAGE
21
22 00551 102000 A50:    ADC 0,0
23 00552 126020          ADCZ 1,1
24 00553 104200          COMR 0,1
25 00554 125004          MOV 1,1,SZR
26 00555 063077          HALTE              ;RIGHT SHIFT ALL 0'S TO AC1
27
28                  ;TRANSFER CRY=1 INTO AC1 BIT 0 SHIFT RIGHT
29 00556 102000 A51:    ADC 0,0            ;AC0=-1
30 00557 104040          COMO 0,1           ;AC1=0  CRY=1
31 00560 104200          COMR 0,1           ;RIGHT SHIFT NOT(0) TO AC1
32 00561 125005          MOV 1,1,SNR        ;RESULT SHD=NOT 0 BIT 0=1
33 00562 063077          HALTE              ;AC1 SHD=100000
34                  ;ABOVE TESTS WERE TO VERIFY TRANSFER OF AC0 TO AC OCCURS
35                  ;RIGHT SHIFT OF CRY=1 TO BIT 0 WAS PREV. VERIFIED
```

```
01
02                ;DEFINE MACRO TO TEST SHIFTS OF
03                ;A SINGLE ONE BIT INTO THE NEXT POSITION
04                      .MACRO SHIFT
05                ;THIS IS A ^5 SHIFT TEST OF BIT ^2 TO BIT ^3
06                ;AC0 SHD=^4 COMING INTO THE TEST
07              ;AS^1:
08                      MOV^5 0,1,SZR   ;TEST NOT ALU^2 INTO SUM^3
09                      MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
10                      HALTE           ;RESULT IN AC1 SHD=^6
11                      MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
12                      HALTE           ;STRAIGHT TRANSFER BIT ^3 FAILED
13                ;BIT ^3 ^5 SHIFT FAILED IF AC1=0 IF=^6 BIT ^3 INTO ZR AND GATE
14              %
15                ;SETUP NEXT SERIES OF RIGHT SHIFT TESTS
16 00563 102040          ADCO 0,0
17 00564 100200          COMR 0,0
18 00565 101005          MOV 0,0,SNR
19 00566 063077          HALTE           ;BIT 0 SETUP FAILED
20
21                       SHIFT R00,0,1,100000,R,040000
22                ;THIS IS A R SHIFT TEST OF BIT 0 TO BIT 1
23                ;AC0 SHD=100000 COMING INTO THE TEST
24              ;ASR00:
25 00567 105204          MOVR 0,1,SZR    ;TEST NOT ALU0 INTO SUM1
26 00570 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
27 00571 063077          HALTE           ;RESULT IN AC1 SHD=040000
28 00572 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
29 00573 063077          HALTE           ;STRAIGHT TRANSFER BIT 1 FAILED
30                ;BIT 1 R SHIFT FAILED IF AC1=0 IF=040000 BIT 1 INTO ZR AND GAT
31                       SHIFT R01,1,2,040000,R,020000
32                ;THIS IS A R SHIFT TEST OF BIT 1 TO BIT 2
33                ;AC0 SHD=040000 COMING INTO THE TEST
34              ;ASR01:
35 00574 105204          MOVR 0,1,SZR    ;TEST NOT ALU1 INTO SUM2
36 00575 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
37 00576 063077          HALTE           ;RESULT IN AC1 SHD=020000
38 00577 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
39 00600 063077          HALTE           ;STRAIGHT TRANSFER BIT 2 FAILED
40                ;BIT 2 R SHIFT FAILED IF AC1=0 IF=020000 BIT 2 INTO ZR AND GAT
41                       SHIFT R02,2,3,020000,R,010000
42                ;THIS IS A R SHIFT TEST OF BIT 2 TO BIT 3
43                ;AC0 SHD=020000 COMING INTO THE TEST
44              ;ASR02:
45 00601 105204          MOVR 0,1,SZR    ;TEST NOT ALU2 INTO SUM3
46 00602 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
47 00603 063077          HALTE           ;RESULT IN AC1 SHD=010000
48 00604 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
49 00605 063077          HALTE           ;STRAIGHT TRANSFER BIT 3 FAILED
50                ;BIT 3 R SHIFT FAILED IF AC1=0 IF=010000 BIT 3 INTO ZR AND GAT
51                       SHIFT R03,3,4,010000,R,004000
52                ;THIS IS A R SHIFT TEST OF BIT 3 TO BIT 4
53                ;AC0 SHD=010000 COMING INTO THE TEST
54              ;ASR03:
55 00606 105204          MOVR 0,1,SZR    ;TEST NOT ALU3 INTO SUM4
56 00607 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
57 00610 063077          HALTE           ;RESULT IN AC1 SHD=004000
58 00611 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
59 00612 063077          HALTE           ;STRAIGHT TRANSFER BIT 4 FAILED
60                ;BIT 4 R SHIFT FAILED IF AC1=0 IF=004000 BIT 4 INTO ZR AND GAT
```



```
01                       SHIFT R04,4,5,004000,R,002000
02                ;THIS IS A R SHIFT TEST OF BIT 4 TO BIT 5
03                ;AC0 SHD=004000 COMING INTO THE TEST
04              ;ASR04:
05 00613 105204          MOVR 0,1,SZR    ;TEST NOT ALU4 INTO SUM5
06 00614 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
07 00615 063077          HALTE           ;RESULT IN AC1 SHD=002000
08 00616 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
09 00617 063077          HALTE           ;STRAIGHT TRANSFER BIT 5 FAILED
10                ;BIT 5 R SHIFT FAILED IF AC1=0 IF=002000 BIT 5 INTO ZR AND GAT
11                       SHIFT R05,5,6,002000,R,001000
12                ;THIS IS A R SHIFT TEST OF BIT 5 TO BIT 6
13                ;AC0 SHD=002000 COMING INTO THE TEST
14              ;ASR05:
15 00620 105204          MOVR 0,1,SZR    ;TEST NOT ALU5 INTO SUM6
16 00621 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
17 00622 063077          HALTE           ;RESULT IN AC1 SHD=001000
18 00623 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
19 00624 063077          HALTE           ;STRAIGHT TRANSFER BIT 6 FAILED
20                ;BIT 6 R SHIFT FAILED IF AC1=0 IF=001000 BIT 6 INTO ZR AND GAT
21                       SHIFT R06,6,7,001000,R,000400
22                ;THIS IS A R SHIFT TEST OF BIT 6 TO BIT 7
23                ;AC0 SHD=001000 COMING INTO THE TEST
24              ;ASR06:
25 00625 105204          MOVR 0,1,SZR    ;TEST NOT ALU6 INTO SUM7
26 00626 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
27 00627 063077          HALTE           ;RESULT IN AC1 SHD=000400
28 00630 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
29 00631 063077          HALTE           ;STRAIGHT TRANSFER BIT 7 FAILED
30                ;BIT 7 R SHIFT FAILED IF AC1=0 IF=000400 BIT 7 INTO ZR AND GAT
31                       SHIFT R07,7,8,000400,R,000200
32                ;THIS IS A R SHIFT TEST OF BIT 7 TO BIT 8
33                ;AC0 SHD=000400 COMING INTO THE TEST
34              ;ASR07:
35 00632 105204          MOVR 0,1,SZR    ;TEST NOT ALU7 INTO SUM8
36 00633 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
37 00634 063077          HALTE           ;RESULT IN AC1 SHD=000200
38 00635 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
39 00636 063077          HALTE           ;STRAIGHT TRANSFER BIT 8 FAILED
40                ;BIT 8 R SHIFT FAILED IF AC1=0 IF=000200 BIT 8 INTO ZR AND GAT
41                       SHIFT R08,8,9,000200,R,000100
42                ;THIS IS A R SHIFT TEST OF BIT 8 TO BIT 9
43                ;AC0 SHD=000200 COMING INTO THE TEST
44              ;ASR08:
45 00637 105204          MOVR 0,1,SZR    ;TEST NOT ALU8 INTO SUM9
46 00640 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
47 00641 063077          HALTE           ;RESULT IN AC1 SHD=000100
48 00642 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
49 00643 063077          HALTE           ;STRAIGHT TRANSFER BIT 9 FAILED
50                ;BIT 9 R SHIFT FAILED IF AC1=0 IF=000100 BIT 9 INTO ZR AND GAT
51                       SHIFT R09,9,10,000100,R,000040
52                ;THIS IS A R SHIFT TEST OF BIT 9 TO BIT 10
53                ;AC0 SHD=000100 COMING INTO THE TEST
54              ;ASR09:
55 00644 105204          MOVR 0,1,SZR    ;TEST NOT ALU9 INTO SUM10
56 00645 125005          MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
57 00646 063077          HALTE           ;RESULT IN AC1 SHD=000040
58 00647 121005          MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
59 00650 063077          HALTE           ;STRAIGHT TRANSFER BIT 10 FAILED
60                ;BIT 10 R SHIFT FAILED IF AC1=0 IF=000040 BIT 10 INTO ZR AND G
```

```
0019 N3LGC
01                      SHIFT R10,10,11,000040,R,000020
02                    ;THIS IS A R SHIFT TEST OF BIT 10 TO BIT 11
03                    ;AC0 SHD=000040 COMING INTO THE TEST
04                   ;ASR10:
05 00651 105204              MOVR 0,1,SZR     ;TEST NOT ALU10 INTO SUM11
06 00652 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
07 00653 063077              HALTE            ;RESULT IN AC1 SHD=000020
08 00654 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
09 00655 063077              HALTE            ;STRAIGHT TRANSFER BIT 11 FAILED
10                    ;BIT 11 R SHIFT FAILED IF AC1=0 IF=000020 BIT 11 INTO ZR AND G
11                      SHIFT R11,11,12,000020,R,000010
12                    ;THIS IS A R SHIFT TEST OF BIT 11 TO BIT 12
13                    ;AC0 SHD=000020 COMING INTO THE TEST
14                   ;ASR11:
15 00656 105204              MOVR 0,1,SZR     ;TEST NOT ALU11 INTO SUM12
16 00657 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
17 00660 063077              HALTE            ;RESULT IN AC1 SHD=000010
18 00661 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
19 00662 063077              HALTE            ;STRAIGHT TRANSFER BIT 12 FAILED
20                    ;BIT 12 R SHIFT FAILED IF AC1=0 IF=000010 BIT 12 INTO ZR AND G
21                      SHIFT R12,12,13,000010,R,000004
22                    ;THIS IS A R SHIFT TEST OF BIT 12 TO BIT 13
23                    ;AC0 SHD=000010 COMING INTO THE TEST
24                   ;ASR12:
25 00663 105204              MOVR 0,1,SZR     ;TEST NOT ALU12 INTO SUM13
26 00664 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
27 00665 063077              HALTE            ;RESULT IN AC1 SHD=000004
28 00666 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
29 00667 063077              HALTE            ;STRAIGHT TRANSFER BIT 13 FAILED
30                    ;BIT 13 R SHIFT FAILED IF AC1=0 IF=000004 BIT 13 INTO ZR AND G
31                      SHIFT R13,13,14,000004,R,000002
32                    ;THIS IS A R SHIFT TEST OF BIT 13 TO BIT 14
33                    ;AC0 SHD=000004 COMING INTO THE TEST
34                   ;ASR13:
35 00670 105204              MOVR 0,1,SZR     ;TEST NOT ALU13 INTO SUM14
36 00671 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
37 00672 063077              HALTE            ;RESULT IN AC1 SHD=000002
38 00673 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
39 00674 063077              HALTE            ;STRAIGHT TRANSFER BIT 14 FAILED
40                    ;BIT 14 R SHIFT FAILED IF AC1=0 IF=000002 BIT 14 INTO ZR AND G
41                      SHIFT R14,14,15,000002,R,000001
42                    ;THIS IS A R SHIFT TEST OF BIT 14 TO BIT 15
43                    ;AC0 SHD=000002 COMING INTO THE TEST
44                   ;ASR14:
45 00675 105204              MOVR 0,1,SZR     ;TEST NOT ALU14 INTO SUM15
46 00676 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
47 00677 063077              HALTE            ;RESULT IN AC1 SHD=000001
48 00700 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
49 00701 063077              HALTE            ;STRAIGHT TRANSFER BIT 15 FAILED
50                    ;BIT 15 R SHIFT FAILED IF AC1=0 IF=000001 BIT 15 INTO ZR AND G
51
52 00702 105205 ASR15:  MOVR 0,1,SNR     ;TEST BIT 15=1 R TO CRY
53 00703 125004              MOV 1,1,SZR      ;AC1 SHD=0'S
54 00704 063077              HALTE
55 00705 125003              MOV 1,1,SNC      ;AND CRY SHD=1
56 00706 063077              HALTE
```

```
0020 N3LGC
01
02                    ;LEFT SHIFT SINGLE BIT TESTS
03                    ;SET UP A 1 IN BIT 15
04
05 00707 102040              ADCO 0,0
06 00710 100104              COML 0,0,SZR
07 00711 101005              MOV 0,0,SNR
08 00712 063077              HALTE            ;AC0 SHD=1 SETUP FAILED
09
10                      SHIFT L00,15,14,000001,L,000002
11                    ;THIS IS A L SHIFT TEST OF BIT 15 TO BIT 14
12                    ;AC0 SHD=000001 COMING INTO THE TEST
13                   ;ASL00:
14 00713 105104              MOVL 0,1,SZR     ;TEST NOT ALU15 INTO SUM14
15 00714 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
16 00715 063077              HALTE            ;RESULT IN AC1 SHD=000002
17 00716 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
18 00717 063077              HALTE            ;STRAIGHT TRANSFER BIT 14 FAILED
19                    ;BIT 14 L SHIFT FAILED IF AC1=0 IF=000002 BIT 14 INTO ZR AND G
20                      SHIFT L01,14,13,000002,L,000004
21                    ;THIS IS A L SHIFT TEST OF BIT 14 TO BIT 13
22                    ;AC0 SHD=000002 COMING INTO THE TEST
23                   ;ASL01:
24 00720 105104              MOVL 0,1,SZR     ;TEST NOT ALU14 INTO SUM13
25 00721 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
26 00722 063077              HALTE            ;RESULT IN AC1 SHD=000004
27 00723 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
28 00724 063077              HALTE            ;STRAIGHT TRANSFER BIT 13 FAILED
29                    ;BIT 13 L SHIFT FAILED IF AC1=0 IF=000004 BIT 13 INTO ZR AND G
30                      SHIFT L02,13,12,000004,L,000010
31                    ;THIS IS A L SHIFT TEST OF BIT 13 TO BIT 12
32                    ;AC0 SHD=000004 COMING INTO THE TEST
33                   ;ASL02:
34 00725 105104              MOVL 0,1,SZR     ;TEST NOT ALU13 INTO SUM12
35 00726 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
36 00727 063077              HALTE            ;RESULT IN AC1 SHD=000010
37 00730 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
38 00731 063077              HALTE            ;STRAIGHT TRANSFER BIT 12 FAILED
39                    ;BIT 12 L SHIFT FAILED IF AC1=0 IF=000010 BIT 12 INTO ZR AND G
40                      SHIFT L03,12,11,000010,L,000020
41                    ;THIS IS A L SHIFT TEST OF BIT 12 TO BIT 11
42                    ;AC0 SHD=000010 COMING INTO THE TEST
43                   ;ASL03:
44 00732 105104              MOVL 0,1,SZR     ;TEST NOT ALU12 INTO SUM11
45 00733 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
46 00734 063077              HALTE            ;RESULT IN AC1 SHD=000020
47 00735 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
48 00736 063077              HALTE            ;STRAIGHT TRANSFER BIT 11 FAILED
49                    ;BIT 11 L SHIFT FAILED IF AC1=0 IF=000020 BIT 11 INTO ZR AND G
50                      SHIFT L04,11,10,000020,L,000040
51                    ;THIS IS A L SHIFT TEST OF BIT 11 TO BIT 10
52                    ;AC0 SHD=000020 COMING INTO THE TEST
53                   ;ASL04:
54 00737 105104              MOVL 0,1,SZR     ;TEST NOT ALU11 INTO SUM10
55 00740 125005              MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
56 00741 063077              HALTE            ;RESULT IN AC1 SHD=000040
57 00742 121005              MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
58 00743 063077              HALTE            ;STRAIGHT TRANSFER BIT 10 FAILED
59                    ;BIT 10 L SHIFT FAILED IF AC1=0 IF=000040 BIT 10 INTO ZR AND G
60                      SHIFT L05,10,09,000040,L,000100
```

```
 0021 N3LGC
01                ;THIS IS A L SHIFT TEST OF BIT 10 TO BIT 09
02                ;AC0 SHD=000040 COMING INTO THE TEST
03              ;ASL05:
04 00744 105104         MOVL 0,1,SZR      ;TEST NOT ALU10 INTO SUM09
05 00745 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
06 00746 063077         HALTE             ;RESULT IN AC1 SHD=000100
07 00747 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
08 00750 063077         HALTE             ;STRAIGHT TRANSFER BIT 09 FAILED
09                ;BIT 09 L SHIFT FAILED IF AC1=0 IF=000100 BIT 09 INTO ZR AND G
10                      SHIFT L06,09,08,000100,L,000200
11                ;THIS IS A L SHIFT TEST OF BIT 09 TO BIT 08
12                ;AC0 SHD=000100 COMING INTO THE TEST
13              ;ASL06:
14 00751 105104         MOVL 0,1,SZR      ;TEST NOT ALU09 INTO SUM08
15 00752 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
16 00753 063077         HALTE             ;RESULT IN AC1 SHD=000200
17 00754 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
18 00755 063077         HALTE             ;STRAIGHT TRANSFER BIT 08 FAILED
19                ;BIT 08 L SHIFT FAILED IF AC1=0 IF=000200 BIT 08 INTO ZR AND G
20                      SHIFT L07,08,07,000200,L,000400
21                ;THIS IS A L SHIFT TEST OF BIT 08 TO BIT 07
22                ;AC0 SHD=000200 COMING INTO THE TEST
23              ;ASL07:
24 00756 105104         MOVL 0,1,SZR      ;TEST NOT ALU08 INTO SUM07
25 00757 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
26 00760 063077         HALTE             ;RESULT IN AC1 SHD=000400
27 00761 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
28 00762 063077         HALTE             ;STRAIGHT TRANSFER BIT 07 FAILED
29                ;BIT 07 L SHIFT FAILED IF AC1=0 IF=000400 BIT 07 INTO ZR AND G
30                      SHIFT L08,07,06,000400,L,001000
31                ;THIS IS A L SHIFT TEST OF BIT 07 TO BIT 06
32                ;AC0 SHD=000400 COMING INTO THE TEST
33              ;ASL08:
34 00763 105104         MOVL 0,1,SZR      ;TEST NOT ALU07 INTO SUM06
35 00764 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
36 00765 063077         HALTE             ;RESULT IN AC1 SHD=001000
37 00766 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
38 00767 063077         HALTE             ;STRAIGHT TRANSFER BIT 06 FAILED
39                ;BIT 06 L SHIFT FAILED IF AC1=0 IF=001000 BIT 06 INTO ZR AND G
40                      SHIFT L09,06,05,001000,L,002000
41                ;THIS IS A L SHIFT TEST OF BIT 06 TO BIT 05
42                ;AC0 SHD=001000 COMING INTO THE TEST
43              ;ASL09:
44 00770 105104         MOVL 0,1,SZR      ;TEST NOT ALU06 INTO SUM05
45 00771 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
46 00772 063077         HALTE             ;RESULT IN AC1 SHD=002000
47 00773 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
48 00774 063077         HALTE             ;STRAIGHT TRANSFER BIT 05 FAILED
49                ;BIT 05 L SHIFT FAILED IF AC1=0 IF=002000 BIT 05 INTO ZR AND G
50                      SHIFT L10,05,04,002000,L,004000
51                ;THIS IS A L SHIFT TEST OF BIT 05 TO BIT 04
52                ;AC0 SHD=002000 COMING INTO THE TEST
53              ;ASL10:
54 00775 105104         MOVL 0,1,SZR      ;TEST NOT ALU05 INTO SUM04
55 00776 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
56 00777 063077         HALTE             ;RESULT IN AC1 SHD=004000
57 01000 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
58 01001 063077         HALTE             ;STRAIGHT TRANSFER BIT 04 FAILED
59                ;BIT 04 L SHIFT FAILED IF AC1=0 IF=004000 BIT 04 INTO ZR AND G
60                      SHIFT L11,04,03,004000,L,010000
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 0022 N3LGC
01                ;THIS IS A L SHIFT TEST OF BIT 04 TO BIT 03
02                ;AC0 SHD=004000 COMING INTO THE TEST
03              ;ASL11:
04 01002 105104         MOVL 0,1,SZR      ;TEST NOT ALU04 INTO SUM03
05 01003 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
06 01004 063077         HALTE             ;RESULT IN AC1 SHD=010000
07 01005 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
08 01006 063077         HALTE             ;STRAIGHT TRANSFER BIT 03 FAILED
09                ;BIT 03 L SHIFT FAILED IF AC1=0 IF=010000 BIT 03 INTO ZR AND G.
10                      SHIFT L12,03,02,010000,L,020000
11                ;THIS IS A L SHIFT TEST OF BIT 03 TO BIT 02
12                ;AC0 SHD=010000 COMING INTO THE TEST
13              ;ASL12:
14 01007 105104         MOVL 0,1,SZR      ;TEST NOT ALU03 INTO SUM02
15 01010 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
16 01011 063077         HALTE             ;RESULT IN AC1 SHD=020000
17 01012 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
18 01013 063077         HALTE             ;STRAIGHT TRANSFER BIT 02 FAILED
19                ;BIT 02 L SHIFT FAILED IF AC1=0 IF=020000 BIT 02 INTO ZR AND G
20                      SHIFT L13,02,01,020000,L,040000
21                ;THIS IS A L SHIFT TEST OF BIT 02 TO BIT 01
22                ;AC0 SHD=020000 COMING INTO THE TEST
23              ;ASL13:
24 01014 105104         MOVL 0,1,SZR      ;TEST NOT ALU02 INTO SUM01
25 01015 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
26 01016 063077         HALTE             ;RESULT IN AC1 SHD=040000
27 01017 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
28 01020 063077         HALTE             ;STRAIGHT TRANSFER BIT 01 FAILED
29                ;BIT 01 L SHIFT FAILED IF AC1=0 IF=040000 BIT 01 INTO ZR AND G
30                      SHIFT L14,01,00,040000,L,100000
31                ;THIS IS A L SHIFT TEST OF BIT 01 TO BIT 00
32                ;AC0 SHD=040000 COMING INTO THE TEST
33              ;ASL14:
34 01021 105104         MOVL 0,1,SZR      ;TEST NOT ALU01 INTO SUM00
35 01022 125005         MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
36 01023 063077         HALTE             ;RESULT IN AC1 SHD=100000
37 01024 121005         MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
38 01025 063077         HALTE             ;STRAIGHT TRANSFER BIT 00 FAILED
39                ;BIT 00 L SHIFT FAILED IF AC1=0 IF=100000 BIT 00 INTO ZR AND G
40
41 01026 105105 ASL15:  MOVL 0,1,SNR      ;AC0=100000
42 01027 125004         MOV 1,1,SZR       ;RESULT LEFT SHD=0'S
43 01030 063077         HALTE             ;PICKED UP EXTRA BITS LEFT
44 01031 125003         MOV 1,1,SNC
45 01032 063077         HALTE             ;LOST CARRY LAST LEFT SHIFT
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10023 N3LGC
01                      ;SHIFT A 0 BIT IN FIELD OF ONES
02                      ;DEFINITION OF MACRO FOR TESTING SAME
03                              .MACRO2 SHIFZ
04                      ;THIS IS A ^5 SHIFT TEST OF NOT BIT ^2 TO NOT BIT ^3
05                    ;ASA1:
06                              MOVO^5 0,1      ;AC0 SHD=^4 COMING INTO TEST
07                              COMZ^5 0,2,SNR  ;AC2 SHD=COM OF ^6
08                              HALTE
09                              COM 2,2         ;AC2 SHD NOW=AC1
10                              ADC 1,2         ;THE ADDITION OF COM SHD=-1
11                              COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
12                              HALTE           ;BIT ^2 TO BIT ^5 TO BIT ^3 FAILED
13                      ;AC0=^4 ORIGINAL TO ^6 IN AC1 AC2 WAS COM OF AC1
14                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
15                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU^2 INTO NOT SUM^3
16                              MOV 1,0         ;SET UP NEXT TEST
17                    %
18                      ;SET UP SERIES OF RIGHT SHIFT TESTS
19                      ;BY SETTING AC0 TO 077777
20 01033 102000                 ADC 0,0
21 01034 100240                 COMOR 0,0       ;SEQUENCE MOST LIKELY TO
22 01035 100000                 COM 0,0         ;SET AC0=077777
23 01036 110005                 COM 0,2,SNR
24 01037 063077                 HALTE           ;SETUP FAILED CRY=0 TO BIT 0
25 01040 105000                 MOV 0,1
26 01041 150000                 COM 2,2         ;RETEST INSTRUCTION
27 01042 132000                 ADC 1,2         ;CHECK SEQUENCE
28 01043 150004                 COM 2,2,SZR     ;JUST TO MAKE SURE IT WORKS
29 01044 063077                 HALTE           ;COMPARE OF AC0=077777 FAILED
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10024 N3LGC
01
02                              SHIFZ R16,0,1,077777,R,137777
03                      ;THIS IS A R SHIFT TEST OF NOT BIT 0 TO NOT BIT 1
04                    ;ASR16:
05 01045 105240                 MOVOR 0,1       ;AC0 SHD=077777 COMING INTO TEST
06 01046 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 137777
07 01047 063077                 HALTE
08 01050 150000                 COM 2,2         ;AC2 SHD NOW=AC1
09 01051 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
10 01052 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
11 01053 063077                 HALTE           ;BIT 0 R TO BIT 1 FAILED
12                      ;AC0=077777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
13                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU0 INTO NOT SUM1
15 01054 121000                 MOV 1,0         ;SET UP NEXT TEST
16                              SHIFZ R17,1,2,137777,R,157777
17                      ;THIS IS A R SHIFT TEST OF NOT BIT 1 TO NOT BIT 2
18                    ;ASR17:
19 01055 105240                 MOVOR 0,1       ;AC0 SHD=137777 COMING INTO TEST
20 01056 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 157777
21 01057 063077                 HALTE
22 01060 150000                 COM 2,2         ;AC2 SHD NOW=AC1
23 01061 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
24 01062 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
25 01063 063077                 HALTE           ;BIT 1 R TO BIT 2 FAILED
26                      ;AC0=137777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
27                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
28                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU1 INTO NOT SUM2
29 01064 121000                 MOV 1,0         ;SET UP NEXT TEST
30                              SHIFZ R18,2,3,157777,R,167777
31                      ;THIS IS A R SHIFT TEST OF NOT BIT 2 TO NOT BIT 3
32                    ;ASR18:
33 01065 105240                 MOVOR 0,1       ;AC0 SHD=157777 COMING INTO TEST
34 01066 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 167777
35 01067 063077                 HALTE
36 01070 150000                 COM 2,2         ;AC2 SHD NOW=AC1
37 01071 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
38 01072 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
39 01073 063077                 HALTE           ;BIT 2 R TO BIT 3 FAILED
40                      ;AC0=157777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
41                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
42                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU2 INTO NOT SUM3
43 01074 121000                 MOV 1,0         ;SET UP NEXT TEST
44                              SHIFZ R19,3,4,167777,R,173777
45                      ;THIS IS A R SHIFT TEST OF NOT BIT 3 TO NOT BIT 4
46                    ;ASR19:
47 01075 105240                 MOVOR 0,1       ;AC0 SHD=167777 COMING INTO TEST
48 01076 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 173777
49 01077 063077                 HALTE
50 01100 150000                 COM 2,2         ;AC2 SHD NOW=AC1
51 01101 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
52 01102 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
53 01103 063077                 HALTE           ;BIT 3 R TO BIT 4 FAILED
54                      ;AC0=167777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
55                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
56                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU3 INTO NOT SUM4
57 01104 121000                 MOV 1,0         ;SET UP NEXT TEST
58                              SHIFZ R20,4,5,173777,R,175777
59                      ;THIS IS A R SHIFT TEST OF NOT BIT 4 TO NOT BIT 5
60                    ;ASR20:
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01 01105 105240          MOVOR 0,1          ;AC0 SHD=173777 COMING INTO TEST
02 01106 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 175777
03 01107 063077          HALTE
04 01110 150000          COM 2,2            ;AC2 SHD NOW=AC1
05 01111 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
06 01112 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
07 01113 063077          HALTE              ;BIT 4 R TO BIT 5 FAILED
08                  ;AC0=173777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
09                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
10                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU4 INTO NOT SUM5
11 01114 121000          MOV 1,0            ;SET UP NEXT TEST
12                       SHIFZ R21,5,6,175777,R,176777
13                  ;THIS IS A R SHIFT TEST OF NOT BIT 5 TO NOT BIT 6
14                ;ASR21:
15 01115 105240          MOVOR 0,1          ;AC0 SHD=175777 COMING INTO TEST
16 01116 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 176777
17 01117 063077          HALTE
18 01120 150000          COM 2,2            ;AC2 SHD NOW=AC1
19 01121 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
20 01122 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
21 01123 063077          HALTE              ;BIT 5 R TO BIT 6 FAILED
22                  ;AC0=175777 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
23                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
24                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU5 INTO NOT SUM6
25 01124 121000          MOV 1,0            ;SET UP NEXT TEST
26                       SHIFZ R22,6,7,176777,R,177377
27                  ;THIS IS A R SHIFT TEST OF NOT BIT 6 TO NOT BIT 7
28                ;ASR22:
29 01125 105240          MOVOR 0,1          ;AC0 SHD=176777 COMING INTO TEST
30 01126 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177377
31 01127 063077          HALTE
32 01130 150000          COM 2,2            ;AC2 SHD NOW=AC1
33 01131 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
34 01132 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
35 01133 063077          HALTE              ;BIT 6 R TO BIT 7 FAILED
36                  ;AC0=176777 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
37                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
38                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU6 INTO NOT SUM7
39 01134 121000          MOV 1,0            ;SET UP NEXT TEST
40                       SHIFZ R23,7,8,177377,R,177577
41                  ;THIS IS A R SHIFT TEST OF NOT BIT 7 TO NOT BIT 8
42                ;ASR23:
43 01135 105240          MOVOR 0,1          ;AC0 SHD=177377 COMING INTO TEST
44 01136 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177577
45 01137 063077          HALTE
46 01140 150000          COM 2,2            ;AC2 SHD NOW=AC1
47 01141 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
48 01142 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
49 01143 063077          HALTE              ;BIT 7 R TO BIT 8 FAILED
50                  ;AC0=177377 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
51                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
52                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU7 INTO NOT SUM8
53 01144 121000          MOV 1,0            ;SET UP NEXT TEST
54                       SHIFZ R24,8,9,177577,R,177677
55                  ;THIS IS A R SHIFT TEST OF NOT BIT 8 TO NOT BIT 9
56                ;ASR24:
57 01145 105240          MOVOR 0,1          ;AC0 SHD=177577 COMING INTO TEST
58 01146 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177677
59 01147 063077          HALTE
60 01150 150000          COM 2,2            ;AC2 SHD NOW=AC1
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01 01151 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
02 01152 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
03 01153 063077          HALTE              ;BIT 8 R TO BIT 9 FAILED
04                  ;AC0=177577 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
05                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
06                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU8 INTO NOT SUM9
07 01154 121000          MOV 1,0            ;SET UP NEXT TEST
08                       SHIFZ R25,9,10,177677,R,177737
09                  ;THIS IS A R SHIFT TEST OF NOT BIT 9 TO NOT BIT 10
10                ;ASR25:
11 01155 105240          MOVOR 0,1          ;AC0 SHD=177677 COMING INTO TEST
12 01156 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177737
13 01157 063077          HALTE
14 01160 150000          COM 2,2            ;AC2 SHD NOW=AC1
15 01161 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
16 01162 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
17 01163 063077          HALTE              ;BIT 9 R TO BIT 10 FAILED
18                  ;AC0=177677 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
19                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
20                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU9 INTO NOT SUM10
21 01164 121000          MOV 1,0            ;SET UP NEXT TEST
22                       SHIFZ R26,10,11,177737,R,177757
23                  ;THIS IS A R SHIFT TEST OF NOT BIT 10 TO NOT BIT 11
24                ;ASR26:
25 01165 105240          MOVOR 0,1          ;AC0 SHD=177737 COMING INTO TEST
26 01166 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177757
27 01167 063077          HALTE
28 01170 150000          COM 2,2            ;AC2 SHD NOW=AC1
29 01171 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
30 01172 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
31 01173 063077          HALTE              ;BIT 10 R TO BIT 11 FAILED
32                  ;AC0=177737 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
33                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
34                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM11
35 01174 121000          MOV 1,0            ;SET UP NEXT TEST
36                       SHIFZ R27,11,12,177757,R,177767
37                  ;THIS IS A R SHIFT TEST OF NOT BIT 11 TO NOT BIT 12
38                ;ASR27:
39 01175 105240          MOVOR 0,1          ;AC0 SHD=177757 COMING INTO TEST
40 01176 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177767
41 01177 063077          HALTE
42 01200 150000          COM 2,2            ;AC2 SHD NOW=AC1
43 01201 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
44 01202 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
45 01203 063077          HALTE              ;BIT 11 R TO BIT 12 FAILED
46                  ;AC0=177757 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
47                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
48                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM12
49 01204 121000          MOV 1,0            ;SET UP NEXT TEST
50                       SHIFZ R28,12,13,177767,R,177773
51                  ;THIS IS A R SHIFT TEST OF NOT BIT 12 TO NOT BIT 13
52                ;ASR28:
53 01205 105240          MOVOR 0,1          ;AC0 SHD=177767 COMING INTO TEST
54 01206 110225          COMZR 0,2,SNR      ;AC2 SHD=COM OF 177773
55 01207 063077          HALTE
56 01210 150000          COM 2,2            ;AC2 SHD NOW=AC1
57 01211 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
58 01212 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
59 01213 063077          HALTE              ;BIT 12 R TO BIT 13 FAILED
60                  ;AC0=177767 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
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 0027 N3LGC
01                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
02                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM13
03 01214 121000                 MOV 1,0         ;SET UP NEXT TEST
04                              SHIFZ R29,13,14,177773,R,177775
05                      ;THIS IS A R SHIFT TEST OF NOT BIT 13 TO NOT BIT 14
06                    ;ASR29:
07 01215 105240                 MOVOR 0,1       ;AC0 SHD=177773 COMING INTO TEST
08 01216 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 177775
09 01217 063077                 HALTE
10 01220 150000                 COM 2,2         ;AC2 SHD NOW=AC1
11 01221 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
12 01222 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
13 01223 063077                 HALTE           ;BIT 13 R TO BIT 14 FAILED
14                      ;AC0=177773 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
15                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
16                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM14
17 01224 121000                 MOV 1,0         ;SET UP NEXT TEST
18                              SHIFZ R30,14,15,177775,R,177776
19                      ;THIS IS A R SHIFT TEST OF NOT BIT 14 TO NOT BIT 15
20                    ;ASR30:
21 01225 105240                 MOVOR 0,1       ;AC0 SHD=177775 COMING INTO TEST
22 01226 110225                 COMZR 0,2,SNR   ;AC2 SHD=COM OF 177776
23 01227 063077                 HALTE
24 01230 150000                 COM 2,2         ;AC2 SHD NOW=AC1
25 01231 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
26 01232 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
27 01233 063077                 HALTE           ;BIT 14 R TO BIT 15 FAILED
28                      ;AC0=177775 ORIGINAL TO 177776 IN AC1 AC2 WAS COM OF AC1
29                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
30                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM15
31 01234 121000                 MOV 1,0         ;SET UP NEXT TEST
32
33 01235 105240 ASR31:  MOVOR 0,1       ;TEST 177776 TO -1
34 01236 130004                 COM 1,2,SZR     ;ALSO RETEST ABOVE SEQ
35 01237 063077                 HALTE           ;AN R16 TO R30 MAY HAVE LOST
36 01240 101002                 MOV 0,0,SZC
37 01241 063077                 HALTE           ;CRY SHD=0 FROM LAST MOVOR
38
39                      ;SETUP SERIES OF LEFT SHIFT TESTS SET AC0=177776
40 01242 102000                 ADC 0,0         ;AC0=-1
41 01243 100140                 COMOL 0,0       ;SHD NOW=+1
42 01244 100000                 COM 0,0
43 01245 104224                 COMZR 0,1,SZR
44 01246 063077                 HALTE           ;LEFT SHIFT SETUP FAILED
45 01247 125003                 MOV 1,1,SNC
46 01250 063077                 HALTE           ;LEFT SHIFT SETUP FAILED
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10028 N3LGC
01                      ;LEFT SHIFT SINGLE 0 BIT TESTS
02                              SHIFZ L16,15,14,177776,L,177775
03                      ;THIS IS A L SHIFT TEST OF NOT BIT 15 TO NOT BIT 14
04                    ;ASL16:
05 01251 105140                 MOVOL 0,1       ;AC0 SHD=177776 COMING INTO TEST
06 01252 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 177775
07 01253 063077                 HALTE
08 01254 150000                 COM 2,2         ;AC2 SHD NOW=AC1
09 01255 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
10 01256 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
11 01257 063077                 HALTE           ;BIT 15 L TO BIT 14 FAILED
12                      ;AC0=177776 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
13                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU15 INTO NOT SUM14
15 01260 121000                 MOV 1,0         ;SET UP NEXT TEST
16                              SHIFZ L17,14,13,177775,L,177773
17                      ;THIS IS A L SHIFT TEST OF NOT BIT 14 TO NOT BIT 13
18                    ;ASL17:
19 01261 105140                 MOVOL 0,1       ;AC0 SHD=177775 COMING INTO TEST
20 01262 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 177773
21 01263 063077                 HALTE
22 01264 150000                 COM 2,2         ;AC2 SHD NOW=AC1
23 01265 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
24 01266 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
25 01267 063077                 HALTE           ;BIT 14 L TO BIT 13 FAILED
26                      ;AC0=177775 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
27                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
28                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM13
29 01270 121000                 MOV 1,0         ;SET UP NEXT TEST
30                              SHIFZ L18,13,12,177773,L,177767
31                      ;THIS IS A L SHIFT TEST OF NOT BIT 13 TO NOT BIT 12
32                    ;ASL18:
33 01271 105140                 MOVOL 0,1       ;AC0 SHD=177773 COMING INTO TEST
34 01272 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 177767
35 01273 063077                 HALTE
36 01274 150000                 COM 2,2         ;AC2 SHD NOW=AC1
37 01275 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
38 01276 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
39 01277 063077                 HALTE           ;BIT 13 L TO BIT 12 FAILED
40                      ;AC0=177773 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
41                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
42                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM12
43 01300 121000                 MOV 1,0         ;SET UP NEXT TEST
44                              SHIFZ L19,12,11,177767,L,177757
45                      ;THIS IS A L SHIFT TEST OF NOT BIT 12 TO NOT BIT 11
46                    ;ASL19:
47 01301 105140                 MOVOL 0,1       ;AC0 SHD=177767 COMING INTO TEST
48 01302 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 177757
49 01303 063077                 HALTE
50 01304 150000                 COM 2,2         ;AC2 SHD NOW=AC1
51 01305 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
52 01306 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
53 01307 063077                 HALTE           ;BIT 12 L TO BIT 11 FAILED
54                      ;AC0=177767 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
55                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
56                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM11
57 01310 121000                 MOV 1,0         ;SET UP NEXT TEST
58                              SHIFZ L20,11,10,177757,L,177737
59                      ;THIS IS A L SHIFT TEST OF NOT BIT 11 TO NOT BIT 10
60                    ;ASL20:
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 0029 N3LGC
01 01311 105140          MOVOL 0,1          ;AC0 SHD=177757 COMING INTO TEST
02 01312 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 177737
03 01313 063077          HALTE
04 01314 150000          COM 2,2            ;AC2 SHD NOW=AC1
05 01315 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
06 01316 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
07 01317 063077          HALTE              ;BIT 11 L TO BIT 10 FAILED
08                     ;AC0=177757 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
09                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
10                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM10
11 01320 121000          MOV 1,0            ;SET UP NEXT TEST
12                       SHIFZ L21,10,09,177737,L,177677
13                     ;THIS IS A L SHIFT TEST OF NOT BIT 10 TO NOT BIT 09
14                   ;ASL21:
15 01321 105140          MOVOL 0,1          ;AC0 SHD=177737 COMING INTO TEST
16 01322 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 177677
17 01323 063077          HALTE
18 01324 150000          COM 2,2            ;AC2 SHD NOW=AC1
19 01325 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
20 01326 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
21 01327 063077          HALTE              ;BIT 10 L TO BIT 09 FAILED
22                     ;AC0=177737 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
23                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
24                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM09
25 01330 121000          MOV 1,0            ;SET UP NEXT TEST
26                       SHIFZ L22,09,08,077677,L,177577
27                     ;THIS IS A L SHIFT TEST OF NOT BIT 09 TO NOT BIT 08
28                   ;ASL22:
29 01331 105140          MOVOL 0,1          ;AC0 SHD=077677 COMING INTO TEST
30 01332 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 177577
31 01333 063077          HALTE
32 01334 150000          COM 2,2            ;AC2 SHD NOW=AC1
33 01335 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
34 01336 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
35 01337 063077          HALTE              ;BIT 09 L TO BIT 08 FAILED
36                     ;AC0=077677 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
37                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
38                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU09 INTO NOT SUM08
39 01340 121000          MOV 1,0            ;SET UP NEXT TEST
40                       SHIFZ L23,08,07,177577,L,177377
41                     ;THIS IS A L SHIFT TEST OF NOT BIT 08 TO NOT BIT 07
42                   ;ASL23:
43 01341 105140          MOVOL 0,1          ;AC0 SHD=177577 COMING INTO TEST
44 01342 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 177377
45 01343 063077          HALTE
46 01344 150000          COM 2,2            ;AC2 SHD NOW=AC1
47 01345 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
48 01346 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
49 01347 063077          HALTE              ;BIT 08 L TO BIT 07 FAILED
50                     ;AC0=177577 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
51                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
52                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU08 INTO NOT SUM07
53 01350 121000          MOV 1,0            ;SET UP NEXT TEST
54                       SHIFZ L24,07,06,177377,L,176777
55                     ;THIS IS A L SHIFT TEST OF NOT BIT 07 TO NOT BIT 06
56                   ;ASL24:
57 01351 105140          MOVOL 0,1          ;AC0 SHD=177377 COMING INTO TEST
58 01352 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 176777
59 01353 063077          HALTE
60 01354 150000          COM 2,2            ;AC2 SHD NOW=AC1
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 0030 N3LGC
01 01355 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
02 01356 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
03 01357 063077          HALTE              ;BIT 07 L TO BIT 06 FAILED
04                     ;AC0=177377 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
05                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
06                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU07 INTO NOT SUM06
07 01360 121000          MOV 1,0            ;SET UP NEXT TEST
08                       SHIFZ L25,06,05,176777,L,175777
09                     ;THIS IS A L SHIFT TEST OF NOT BIT 06 TO NOT BIT 05
10                   ;ASL25:
11 01361 105140          MOVOL 0,1          ;AC0 SHD=176777 COMING INTO TEST
12 01362 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 175777
13 01363 063077          HALTE
14 01364 150000          COM 2,2            ;AC2 SHD NOW=AC1
15 01365 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
16 01366 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
17 01367 063077          HALTE              ;BIT 06 L TO BIT 05 FAILED
18                     ;AC0=176777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
19                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
20                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU06 INTO NOT SUM05
21 01370 121000          MOV 1,0            ;SET UP NEXT TEST
22                       SHIFZ L26,05,04,175777,L,173777
23                     ;THIS IS A L SHIFT TEST OF NOT BIT 05 TO NOT BIT 04
24                   ;ASL26:
25 01371 105140          MOVOL 0,1          ;AC0 SHD=175777 COMING INTO TEST
26 01372 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 173777
27 01373 063077          HALTE
28 01374 150000          COM 2,2            ;AC2 SHD NOW=AC1
29 01375 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
30 01376 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
31 01377 063077          HALTE              ;BIT 05 L TO BIT 04 FAILED
32                     ;AC0=175777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
33                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
34                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU05 INTO NOT SUM04
35 01400 121000          MOV 1,0            ;SET UP NEXT TEST
36                       SHIFZ L27,04,03,173777,L,167777
37                     ;THIS IS A L SHIFT TEST OF NOT BIT 04 TO NOT BIT 03
38                   ;ASL27:
39 01401 105140          MOVOL 0,1          ;AC0 SHD=173777 COMING INTO TEST
40 01402 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 167777
41 01403 063077          HALTE
42 01404 150000          COM 2,2            ;AC2 SHD NOW=AC1
43 01405 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
44 01406 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
45 01407 063077          HALTE              ;BIT 04 L TO BIT 03 FAILED
46                     ;AC0=173777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
47                     ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
48                     ;WAS PREVIOUSLY VERIFIED SEE NOT ALU04 INTO NOT SUM03
49 01410 121000          MOV 1,0            ;SET UP NEXT TEST
50                       SHIFZ L28,03,02,167777,L,157777
51                     ;THIS IS A L SHIFT TEST OF NOT BIT 03 TO NOT BIT 02
52                   ;ASL28:
53 01411 105140          MOVOL 0,1          ;AC0 SHD=167777 COMING INTO TEST
54 01412 110125          COMZL 0,2,SNR      ;AC2 SHD=COM OF 157777
55 01413 063077          HALTE
56 01414 150000          COM 2,2            ;AC2 SHD NOW=AC1
57 01415 132000          ADC 1,2            ;THE ADDITION OF COM SHD=-1
58 01416 150004          COM 2,2,SZR        ;AND RESULT SHD=0 ALL SHIFTS OK
59 01417 063077          HALTE              ;BIT 03 L TO BIT 02 FAILED
60                     ;AC0=167777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
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 0031 N3LGC
01                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
02                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU03 INTO NOT SUM02
03 01420 121000                 MOV 1,0         ;SET UP NEXT TEST
04                              SHIFZ L29,02,01,157777,L,137777
05                      ;THIS IS A L SHIFT TEST OF NOT BIT 02 TO NOT BIT 01
06                    ;ASL29:
07 01421 105140                 MOVOL 0,1       ;AC0 SHD=157777 COMING INTO TEST
08 01422 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 137777
09 01423 063077                 HALTE
10 01424 150000                 COM 2,2         ;AC2 SHD NOW=AC1
11 01425 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
12 01426 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
13 01427 063077                 HALTE           ;BIT 02 L TO BIT 01 FAILED
14                      ;AC0=157777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
15                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
16                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU02 INTO NOT SUM01
17 01430 121000                 MOV 1,0         ;SET UP NEXT TEST
18                              SHIFZ L30,01,00,137777,L,077777
19                      ;THIS IS A L SHIFT TEST OF NOT BIT 01 TO NOT BIT 00
20                    ;ASL30:
21 01431 105140                 MOVOL 0,1       ;AC0 SHD=137777 COMING INTO TEST
22 01432 110125                 COMZL 0,2,SNR   ;AC2 SHD=COM OF 077777
23 01433 063077                 HALTE
24 01434 150000                 COM 2,2         ;AC2 SHD NOW=AC1
25 01435 132000                 ADC 1,2         ;THE ADDITION OF COM SHD=-1
26 01436 150004                 COM 2,2,SZR     ;AND RESULT SHD=0 ALL SHIFTS OK
27 01437 063077                 HALTE           ;BIT 01 L TO BIT 00 FAILED
28                      ;AC0=137777 ORIGINAL TO 077777 IN AC1 AC2 WAS COM OF AC1
29                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
30                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU01 INTO NOT SUM00
31 01440 121000                 MOV 1,0         ;SET UP NEXT TEST
32                      ;IF AC0 DOES NOT=077777 HERE SOME L16 TO L30 FAILED
33 01441 105140 ASL31:  MOVOL 0,1       ;SHD RESULT IN AC1=-1
34 01442 130004                 COM 1,2,SZR     ;TEST FOR AC2 RESULT=0
35 01443 063077                 HALTE           ;COULD HAVE FAILED L16 TO L30
36 01444 151002                 MOV 2,2,SZC     ;CRY SHD=0 FROM BIT 0
37 01445 063077                 HALTE           ;BIT 0 TO CRY FAILED
38
39
40
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10032 N3LGC
01
02                      ;SINGLE BIT ADD WITHOUT CARRY TESTS
03                      ;DEFINE MACRO ENCOMPASSING SOURCE OR DEST=NON ZERO
04
05                              .MACRO ADDT1
06                      ;TEST ADD INSTRUCTION NO CARRY WHEN ^1 IS NON ZERO
07                      ;^2 IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
08                      ;AC0=^3 COMING INTO THE TEST
09                    ;ANC^7:
10                              MOV 0,^4        ;SET UP ^1 AC^4
11                              ADC ^5,^5
12                              COM ^5,^5       ;SET AC^5 ^2=0
13                              ADD 1,2         ;PERFORM ADD WITH NO CARRIES
14                              MOV 2,3         ;THE ^1 AC WAS NON ZERO
15                              ADC 0,3         ;AC3 SHD NOW=-1
16                              COM 3,3,SZR     ;WITH COM=0
17                              HALTE           ;ADD WITHOUT CARRY FAILED
18                              MOVZL 0,0       ;SET UP NEXT TEST
19                      ;AC2 SHD=^3 AS A RESULT OF ABOVE TEST
20                    .
21                      ;TEST ADD OF ALL 0'S TO GENERATE NO CARRIES
22 01446 102000 ANC00:  ADC 0,0
23 01447 100000                 COM 0,0         ;SETS AC0=0
24 01450 103004                 ADD 0,0,SZR     ;RESULT OF ADD SHD STILL=0
25 01451 063077                 HALTE           ;ADD 0+0 GENERATED A CARRY
26 01452 101002                 MOV 0,0,SZC     ;ABOVE ADD SHD LVE CRY=0
27 01453 063077                 HALTE           ;INTO CRY SEE CARRY OUT
28
29                      ;SET UP AC0 TO=+1 FOR FIRST TEST
30 01454 102000                 ADC 0,0
31 01455 100145                 COMOL 0,0,SNR
32 01456 063077                 HALTE           ;SETUP FAILED
```

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10033 N3LGC
01
02                      ADDT1 SRC,DEST,1,1,2,Z,01
03                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                    ;AC0=1 COMING INTO THE TEST
06                  ;ANC01:
07 01457 105000             MOV 0,1 ;SET UP SRC AC1
08 01460 152000             ADC 2,2
09 01461 150000             COM 2,2 ;SET AC2 DEST=0
10 01462 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 01463 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
12 01464 116000             ADC 0,3          ;AC3 SHD NOW=-1
13 01465 174004             COM 3,3,SZR      ;WITH COM=0
14 01466 063077             HALTE            ;ADD WITHOUT CARRY FAILED
15 01467 101120             MOVZL 0,0        ;SET UP NEXT TEST
16                    ;AC2 SHD=1 AS A RESULT OF ABOVE TEST
17                      ADDT1 SRC,DEST,2,1,2,Z,02
18                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                    ;AC0=2 COMING INTO THE TEST
21                  ;ANC02:
22 01470 105000             MOV 0,1 ;SET UP SRC AC1
23 01471 152000             ADC 2,2
24 01472 150000             COM 2,2 ;SET AC2 DEST=0
25 01473 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 01474 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
27 01475 116000             ADC 0,3          ;AC3 SHD NOW=-1
28 01476 174004             COM 3,3,SZR      ;WITH COM=0
29 01477 063077             HALTE            ;ADD WITHOUT CARRY FAILED
30 01500 101120             MOVZL 0,0        ;SET UP NEXT TEST
31                    ;AC2 SHD=2 AS A RESULT OF ABOVE TEST
32                      ADDT1 SRC,DEST,4,1,2,Z,03
33                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                    ;AC0=4 COMING INTO THE TEST
36                  ;ANC03:
37 01501 105000             MOV 0,1 ;SET UP SRC AC1
38 01502 152000             ADC 2,2
39 01503 150000             COM 2,2 ;SET AC2 DEST=0
40 01504 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 01505 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
42 01506 116000             ADC 0,3          ;AC3 SHD NOW=-1
43 01507 174004             COM 3,3,SZR      ;WITH COM=0
44 01510 063077             HALTE            ;ADD WITHOUT CARRY FAILED
45 01511 101120             MOVZL 0,0        ;SET UP NEXT TEST
46                    ;AC2 SHD=4 AS A RESULT OF ABOVE TEST
47                      ADDT1 SRC,DEST,10,1,2,Z,04
48                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                    ;AC0=10 COMING INTO THE TEST
51                  ;ANC04:
52 01512 105000             MOV 0,1 ;SET UP SRC AC1
53 01513 152000             ADC 2,2
54 01514 150000             COM 2,2 ;SET AC2 DEST=0
55 01515 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 01516 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
57 01517 116000             ADC 0,3          ;AC3 SHD NOW=-1
58 01520 174004             COM 3,3,SZR      ;WITH COM=0
59 01521 063077             HALTE            ;ADD WITHOUT CARRY FAILED
60 01522 101120             MOVZL 0,0        ;SET UP NEXT TEST
```

```
 0034 N3LGC
01                    ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
02                      ADDT1 SRC,DEST,20,1,2,Z,05
03                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                    ;AC0=20 COMING INTO THE TEST
06                  ;ANC05:
07 01523 105000             MOV 0,1 ;SET UP SRC AC1
08 01524 152000             ADC 2,2
09 01525 150000             COM 2,2 ;SET AC2 DEST=0
10 01526 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 01527 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
12 01530 116000             ADC 0,3          ;AC3 SHD NOW=-1
13 01531 174004             COM 3,3,SZR      ;WITH COM=0
14 01532 063077             HALTE            ;ADD WITHOUT CARRY FAILED
15 01533 101120             MOVZL 0,0        ;SET UP NEXT TEST
16                    ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
17                      ADDT1 SRC,DEST,40,1,2,Z,06
18                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                    ;AC0=40 COMING INTO THE TEST
21                  ;ANC06:
22 01534 105000             MOV 0,1 ;SET UP SRC AC1
23 01535 152000             ADC 2,2
24 01536 150000             COM 2,2 ;SET AC2 DEST=0
25 01537 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 01540 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
27 01541 116000             ADC 0,3          ;AC3 SHD NOW=-1
28 01542 174004             COM 3,3,SZR      ;WITH COM=0
29 01543 063077             HALTE            ;ADD WITHOUT CARRY FAILED
30 01544 101120             MOVZL 0,0        ;SET UP NEXT TEST
31                    ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
32                      ADDT1 SRC,DEST,100,1,2,Z,07
33                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                    ;AC0=100 COMING INTO THE TEST
36                  ;ANC07:
37 01545 105000             MOV 0,1 ;SET UP SRC AC1
38 01546 152000             ADC 2,2
39 01547 150000             COM 2,2 ;SET AC2 DEST=0
40 01550 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 01551 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
42 01552 116000             ADC 0,3          ;AC3 SHD NOW=-1
43 01553 174004             COM 3,3,SZR      ;WITH COM=0
44 01554 063077             HALTE            ;ADD WITHOUT CARRY FAILED
45 01555 101120             MOVZL 0,0        ;SET UP NEXT TEST
46                    ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
47                      ADDT1 SRC,DEST,200,1,2,Z,08
48                    ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                    ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                    ;AC0=200 COMING INTO THE TEST
51                  ;ANC08:
52 01556 105000             MOV 0,1 ;SET UP SRC AC1
53 01557 152000             ADC 2,2
54 01560 150000             COM 2,2 ;SET AC2 DEST=0
55 01561 133000             ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 01562 155000             MOV 2,3          ;THE SRC AC WAS NON ZERO
57 01563 116000             ADC 0,3          ;AC3 SHD NOW=-1
58 01564 174004             COM 3,3,SZR      ;WITH COM=0
59 01565 063077             HALTE            ;ADD WITHOUT CARRY FAILED
60 01566 101120             MOVZL 0,0        ;SET UP NEXT TEST
```

```
0035 N3LGC
01                      ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
02                           ADDT1 SRC,DEST,400,1,2,Z,09
03                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                      ;AC0=400 COMING INTO THE TEST
06                    ;ANC09:
07 01567 105000               MOV 0,1 ;SET UP SRC AC1
08 01570 152000               ADC 2,2
09 01571 150000               COM 2,2 ;SET AC2 DEST=0
10 01572 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 01573 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
12 01574 116000               ADC 0,3          ;AC3 SHD NOW=-1
13 01575 174004               COM 3,3,SZR      ;WITH COM=0
14 01576 063077               HALTE            ;ADD WITHOUT CARRY FAILED
15 01577 101120               MOVZL 0,0        ;SET UP NEXT TEST
16                      ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
17                           ADDT1 SRC,DEST,1000,1,2,Z,10
18                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                      ;AC0=1000 COMING INTO THE TEST
21                    ;ANC10:
22 01600 105000               MOV 0,1 ;SET UP SRC AC1
23 01601 152000               ADC 2,2
24 01602 150000               COM 2,2 ;SET AC2 DEST=0
25 01603 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 01604 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
27 01605 116000               ADC 0,3          ;AC3 SHD NOW=-1
28 01606 174004               COM 3,3,SZR      ;WITH COM=0
29 01607 063077               HALTE            ;ADD WITHOUT CARRY FAILED
30 01610 101120               MOVZL 0,0        ;SET UP NEXT TEST
31                      ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
32                           ADDT1 SRC,DEST,2000,1,2,Z,11
33                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                      ;AC0=2000 COMING INTO THE TEST
36                    ;ANC11:
37 01611 105000               MOV 0,1 ;SET UP SRC AC1
38 01612 152000               ADC 2,2
39 01613 150000               COM 2,2 ;SET AC2 DEST=0
40 01614 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 01615 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
42 01616 116000               ADC 0,3          ;AC3 SHD NOW=-1
43 01617 174004               COM 3,3,SZR      ;WITH COM=0
44 01620 063077               HALTE            ;ADD WITHOUT CARRY FAILED
45 01621 101120               MOVZL 0,0        ;SET UP NEXT TEST
46                      ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
47                           ADDT1 SRC,DEST,4000,1,2,Z,12
48                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                      ;AC0=4000 COMING INTO THE TEST
51                    ;ANC12:
52 01622 105000               MOV 0,1 ;SET UP SRC AC1
53 01623 152000               ADC 2,2
54 01624 150000               COM 2,2 ;SET AC2 DEST=0
55 01625 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 01626 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
57 01627 116000               ADC 0,3          ;AC3 SHD NOW=-1
58 01630 174004               COM 3,3,SZR      ;WITH COM=0
59 01631 063077               HALTE            ;ADD WITHOUT CARRY FAILED
60 01632 101120               MOVZL 0,0        ;SET UP NEXT TEST
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0036 N3LGC
01                      ;AC2 SHD=4000 AS A RESULT OF ABOVE TEST
02                           ADDT1 SRC,DEST,10000,1,2,Z,13
03                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                      ;AC0=10000 COMING INTO THE TEST
06                    ;ANC13:
07 01633 105000               MOV 0,1 ;SET UP SRC AC1
08 01634 152000               ADC 2,2
09 01635 150000               COM 2,2 ;SET AC2 DEST=0
10 01636 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 01637 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
12 01640 116000               ADC 0,3          ;AC3 SHD NOW=-1
13 01641 174004               COM 3,3,SZR      ;WITH COM=0
14 01642 063077               HALTE            ;ADD WITHOUT CARRY FAILED
15 01643 101120               MOVZL 0,0        ;SET UP NEXT TEST
16                      ;AC2 SHD=10000 AS A RESULT OF ABOVE TEST
17                           ADDT1 SRC,DEST,20000,1,2,Z,14
18                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                      ;AC0=20000 COMING INTO THE TEST
21                    ;ANC14:
22 01644 105000               MOV 0,1 ;SET UP SRC AC1
23 01645 152000               ADC 2,2
24 01646 150000               COM 2,2 ;SET AC2 DEST=0
25 01647 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 01650 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
27 01651 116000               ADC 0,3          ;AC3 SHD NOW=-1
28 01652 174004               COM 3,3,SZR      ;WITH COM=0
29 01653 063077               HALTE            ;ADD WITHOUT CARRY FAILED
30 01654 101120               MOVZL 0,0        ;SET UP NEXT TEST
31                      ;AC2 SHD=20000 AS A RESULT OF ABOVE TEST
32                           ADDT1 SRC,DEST,40000,1,2,Z,15
33                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                      ;AC0=40000 COMING INTO THE TEST
36                    ;ANC15:
37 01655 105000               MOV 0,1 ;SET UP SRC AC1
38 01656 152000               ADC 2,2
39 01657 150000               COM 2,2 ;SET AC2 DEST=0
40 01660 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 01661 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
42 01662 116000               ADC 0,3          ;AC3 SHD NOW=-1
43 01663 174004               COM 3,3,SZR      ;WITH COM=0
44 01664 063077               HALTE            ;ADD WITHOUT CARRY FAILED
45 01665 101120               MOVZL 0,0        ;SET UP NEXT TEST
46                      ;AC2 SHD=40000 AS A RESULT OF ABOVE TEST
47                           ADDT1 SRC,DEST,100000,1,2,Z,16
48                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                      ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                      ;AC0=100000 COMING INTO THE TEST
51                    ;ANC16:
52 01666 105000               MOV 0,1 ;SET UP SRC AC1
53 01667 152000               ADC 2,2
54 01670 150000               COM 2,2 ;SET AC2 DEST=0
55 01671 133000               ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 01672 155000               MOV 2,3          ;THE SRC AC WAS NON ZERO
57 01673 116000               ADC 0,3          ;AC3 SHD NOW=-1
58 01674 174004               COM 3,3,SZR      ;WITH COM=0
59 01675 063077               HALTE            ;ADD WITHOUT CARRY FAILED
60 01676 101120               MOVZL 0,0        ;SET UP NEXT TEST
```

```
 0037 N3LGC
01                      ;AC2 SHD=100000 AS A RESULT OF ABOVE TEST
02
03                      ;RESET UP AC0 FOR DEST NOT=0 ADD TEST
04 01677 102000                 ADC 0,0
05 01700 100145                 COMOL 0,0,SNR
06 01701 063077                 HALTE
07
08                              ADDT1 DEST,SRC,1,2,1,Z,17
09                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
11                      ;AC0=1 COMING INTO THE TEST
12                    ;ANC17:
13 01702 111000                 MOV 0,2 ;SET UP DEST AC2
14 01703 126000                 ADC 1,1
15 01704 124000                 COM 1,1 ;SET AC1 SRC=0
16 01705 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
17 01706 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
18 01707 116000                 ADC 0,3         ;AC3 SHD NOW=-1
19 01710 174004                 COM 3,3,SZR     ;WITH COM=0
20 01711 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
21 01712 101120                 MOVZL 0,0       ;SET UP NEXT TEST
22                      ;AC2 SHD=1 AS A RESULT OF ABOVE TEST
23                              ADDT1 DEST,SRC,2,2,1,Z,18
24                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
26                      ;AC0=2 COMING INTO THE TEST
27                    ;ANC18:
28 01713 111000                 MOV 0,2 ;SET UP DEST AC2
29 01714 126000                 ADC 1,1
30 01715 124000                 COM 1,1 ;SET AC1 SRC=0
31 01716 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
32 01717 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
33 01720 116000                 ADC 0,3         ;AC3 SHD NOW=-1
34 01721 174004                 COM 3,3,SZR     ;WITH COM=0
35 01722 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
36 01723 101120                 MOVZL 0,0       ;SET UP NEXT TEST
37                      ;AC2 SHD=2 AS A RESULT OF ABOVE TEST
38                              ADDT1 DEST,SRC,4,2,1,Z,19
39                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
41                      ;AC0=4 COMING INTO THE TEST
42                    ;ANC19:
43 01724 111000                 MOV 0,2 ;SET UP DEST AC2
44 01725 126000                 ADC 1,1
45 01726 124000                 COM 1,1 ;SET AC1 SRC=0
46 01727 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
47 01730 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
48 01731 116000                 ADC 0,3         ;AC3 SHD NOW=-1
49 01732 174004                 COM 3,3,SZR     ;WITH COM=0
50 01733 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
51 01734 101120                 MOVZL 0,0       ;SET UP NEXT TEST
52                      ;AC2 SHD=4 AS A RESULT OF ABOVE TEST
53                              ADDT1 DEST,SRC,10,2,1,Z,20
54                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
56                      ;AC0=10 COMING INTO THE TEST
57                    ;ANC20:
58 01735 111000                 MOV 0,2 ;SET UP DEST AC2
59 01736 126000                 ADC 1,1
60 01737 124000                 COM 1,1 ;SET AC1 SRC=0
```

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 0038 N3LGC
01 01740 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
02 01741 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
03 01742 116000                 ADC 0,3         ;AC3 SHD NOW=-1
04 01743 174004                 COM 3,3,SZR     ;WITH COM=0
05 01744 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
06 01745 101120                 MOVZL 0,0       ;SET UP NEXT TEST
07                      ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
08                              ADDT1 DEST,SRC,20,2,1,Z,21
09                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
11                      ;AC0=20 COMING INTO THE TEST
12                    ;ANC21:
13 01746 111000                 MOV 0,2 ;SET UP DEST AC2
14 01747 126000                 ADC 1,1
15 01750 124000                 COM 1,1 ;SET AC1 SRC=0
16 01751 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
17 01752 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
18 01753 116000                 ADC 0,3         ;AC3 SHD NOW=-1
19 01754 174004                 COM 3,3,SZR     ;WITH COM=0
20 01755 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
21 01756 101120                 MOVZL 0,0       ;SET UP NEXT TEST
22                      ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
23                              ADDT1 DEST,SRC,40,2,1,Z,22
24                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
26                      ;AC0=40 COMING INTO THE TEST
27                    ;ANC22:
28 01757 111000                 MOV 0,2 ;SET UP DEST AC2
29 01760 126000                 ADC 1,1
30 01761 124000                 COM 1,1 ;SET AC1 SRC=0
31 01762 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
32 01763 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
33 01764 116000                 ADC 0,3         ;AC3 SHD NOW=-1
34 01765 174004                 COM 3,3,SZR     ;WITH COM=0
35 01766 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
36 01767 101120                 MOVZL 0,0       ;SET UP NEXT TEST
37                      ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
38                              ADDT1 DEST,SRC,100,2,1,Z,23
39                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
41                      ;AC0=100 COMING INTO THE TEST
42                    ;ANC23:
43 01770 111000                 MOV 0,2 ;SET UP DEST AC2
44 01771 126000                 ADC 1,1
45 01772 124000                 COM 1,1 ;SET AC1 SRC=0
46 01773 133000                 ADD 1,2         ;PERFORM ADD WITH NO CARRIES
47 01774 155000                 MOV 2,3         ;THE DEST AC WAS NON ZERO
48 01775 116000                 ADC 0,3         ;AC3 SHD NOW=-1
49 01776 174004                 COM 3,3,SZR     ;WITH COM=0
50 01777 063077                 HALTE           ;ADD WITHOUT CARRY FAILED
51 02000 101120                 MOVZL 0,0       ;SET UP NEXT TEST
52                      ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
53                              ADDT1 DEST,SRC,200,2,1,Z,24
54                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                      ;SRC IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
56                      ;AC0=200 COMING INTO THE TEST
57                    ;ANC24:
58 02001 111000                 MOV 0,2 ;SET UP DEST AC2
59 02002 126000                 ADC 1,1
60 02003 124000                 COM 1,1 ;SET AC1 SRC=0
```

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0039 N3LGC
02004 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02005 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02006 116000          ADC 0,3          ;AC3 SHD NOW=-1
02007 174004          COM 3,3,SZR      ;WITH COM=0
02010 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02011 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,400,2,1,Z,25
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=400 COMING INTO THE TEST
                   ;ANC25:
02012 111000          MOV 0,2 ;SET UP DEST AC2
02013 126000          ADC 1,1
02014 124000          COM 1,1 ;SET AC1 SRC=0
02015 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02016 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02017 116000          ADC 0,3          ;AC3 SHD NOW=-1
02020 174004          COM 3,3,SZR      ;WITH COM=0
02021 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02022 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,1000,2,1,Z,26
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=1000 COMING INTO THE TEST
                   ;ANC26:
02023 111000          MOV 0,2 ;SET UP DEST AC2
02024 126000          ADC 1,1
02025 124000          COM 1,1 ;SET AC1 SRC=0
02026 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02027 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02030 116000          ADC 0,3          ;AC3 SHD NOW=-1
02031 174004          COM 3,3,SZR      ;WITH COM=0
02032 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02033 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,2000,2,1,Z,27
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=2000 COMING INTO THE TEST
                   ;ANC27:
02034 111000          MOV 0,2 ;SET UP DEST AC2
02035 126000          ADC 1,1
02036 124000          COM 1,1 ;SET AC1 SRC=0
02037 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02040 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02041 116000          ADC 0,3          ;AC3 SHD NOW=-1
02042 174004          COM 3,3,SZR      ;WITH COM=0
02043 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02044 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,4000,2,1,Z,28
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=4000 COMING INTO THE TEST
                   ;ANC28:
02045 111000          MOV 0,2 ;SET UP DEST AC2
02046 126000          ADC 1,1
02047 124000          COM 1,1 ;SET AC1 SRC=0
```

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0040 N3LGC
02050 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02051 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02052 116000          ADC 0,3          ;AC3 SHD NOW=-1
02053 174004          COM 3,3,SZR      ;WITH COM=0
02054 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02055 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=4000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,10000,2,1,Z,29
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=10000 COMING INTO THE TEST
                   ;ANC29:
02056 111000          MOV 0,2 ;SET UP DEST AC2
02057 126000          ADC 1,1
02060 124000          COM 1,1 ;SET AC1 SRC=0
02061 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02062 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02063 116000          ADC 0,3          ;AC3 SHD NOW=-1
02064 174004          COM 3,3,SZR      ;WITH COM=0
02065 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02066 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=10000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,20000,2,1,Z,30
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=20000 COMING INTO THE TEST
                   ;ANC30:
02067 111000          MOV 0,2 ;SET UP DEST AC2
02070 126000          ADC 1,1
02071 124000          COM 1,1 ;SET AC1 SRC=0
02072 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02073 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02074 116000          ADC 0,3          ;AC3 SHD NOW=-1
02075 174004          COM 3,3,SZR      ;WITH COM=0
02076 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02077 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=20000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,40000,2,1,Z,31
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=40000 COMING INTO THE TEST
                   ;ANC31:
02100 111000          MOV 0,2 ;SET UP DEST AC2
02101 126000          ADC 1,1
02102 124000          COM 1,1 ;SET AC1 SRC=0
02103 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02104 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
02105 116000          ADC 0,3          ;AC3 SHD NOW=-1
02106 174004          COM 3,3,SZR      ;WITH COM=0
02107 063077          HALTE            ;ADD WITHOUT CARRY FAILED
02110 101120          MOVZL 0,0        ;SET UP NEXT TEST
                    ;AC2 SHD=40000 AS A RESULT OF ABOVE TEST
                          ADDT1 DEST,SRC,100000,2,1,Z,32
                    ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
                    ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
                    ;AC0=100000 COMING INTO THE TEST
                   ;ANC32:
02111 111000          MOV 0,2 ;SET UP DEST AC2
02112 126000          ADC 1,1
02113 124000          COM 1,1 ;SET AC1 SRC=0
```

```
 0041 N3LGC
01 02114 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02 02115 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
03 02116 116000          ADC 0,3          ;AC3 SHD NOW=-1
04 02117 174004          COM 3,3,SZR      ;WITH COM=0
05 02120 063077          HALTE            ;ADD WITHOUT CARRY FAILED
06 02121 101120          MOVZL 0,0        ;SET UP NEXT TEST
07                ;AC2 SHD=100000 AS A RESULT OF ABOVE TEST
```

```
10042 N3LGC
01
02                ;SINGLE BIT CARRY TESTS DEFINE MACRO
03                ;CONSTANTS ARE SET UP BY ALREADY TESTED SHIFT
04
05                      .MACRO ADDT0
06                ;TEST SINGLE BIT CARRY ADD BIT ^2 TO ITSELF
07                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT ^3
08                ;AND SUM BIT ^2 TO GO TO 0 RESULT SHD=^5
09              ;AC^1:
10                      MOV 0,1          ;AC0=^^4 COMING INTO TEST
11                      ADD 1,1          ;USE IT TO SET UP AC1+AC1
12                      MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
13                      ADC 1,2          ;AC2 SHD NOW=-1
14                      COM 2,2,SZR      ;NOT 0 IS BIT ^2 CARRY FAILED
15                      HALTE            ;BIT ^2+^2 FAILED ADD SEE ALU^3
16                                         ;AND ALU^2
17                      MOVZL 0,0        ;SET UP NEXT TEST
18                %
19                ;SET UP BIT 15 FOR ADD TESTS
20 02122 102000          ADC 0,0
21 02123 100145          COMOL 0,0,SNR
22 02124 063077          HALTE            ;AC0 SHD=+1
23
24                      ADDT0 00,15,14,1,2
25                ;TEST SINGLE BIT CARRY ADD BIT 15 TO ITSELF
26                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 14
27                ;AND SUM BIT 15 TO GO TO 0 RESULT SHD=2
28              ;AC00:
29 02125 105000          MOV 0,1          ;AC0=1 COMING INTO TEST
30 02126 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
31 02127 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
32 02130 132000          ADC 1,2          ;AC2 SHD NOW=-1
33 02131 150004          COM 2,2,SZR      ;NOT 0 IS BIT 15 CARRY FAILED
34 02132 063077          HALTE            ;BIT 15+15 FAILED ADD SEE ALU14
35                                         ;AND ALU15
36 02133 101120          MOVZL 0,0        ;SET UP NEXT TEST
37                      ADDT0 01,14,13,2,4
38                ;TEST SINGLE BIT CARRY ADD BIT 14 TO ITSELF
39                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 13
40                ;AND SUM BIT 14 TO GO TO 0 RESULT SHD=4
41              ;AC01:
42 02134 105000          MOV 0,1          ;AC0=2 COMING INTO TEST
43 02135 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
44 02136 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
45 02137 132000          ADC 1,2          ;AC2 SHD NOW=-1
46 02140 150004          COM 2,2,SZR      ;NOT 0 IS BIT 14 CARRY FAILED
47 02141 063077          HALTE            ;BIT 14+14 FAILED ADD SEE ALU13
48                                         ;AND ALU14
49 02142 101120          MOVZL 0,0        ;SET UP NEXT TEST
50                      ADDT0 02,13,12,4,10
51                ;TEST SINGLE BIT CARRY ADD BIT 13 TO ITSELF
52                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 12
53                ;AND SUM BIT 13 TO GO TO 0 RESULT SHD=10
54              ;AC02:
55 02143 105000          MOV 0,1          ;AC0=4 COMING INTO TEST
56 02144 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
57 02145 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
58 02146 132000          ADC 1,2          ;AC2 SHD NOW=-1
59 02147 150004          COM 2,2,SZR      ;NOT 0 IS BIT 13 CARRY FAILED
60 02150 063077          HALTE            ;BIT 13+13 FAILED ADD SEE ALU12
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```
0043 N3LGC
01                                      ;AND ALU13
02 02151 101120         MOVZL 0,0       ;SET UP NEXT TEST
03                      ADDT0 03,12,11,10,20
04                  ;TEST SINGLE BIT CARRY ADD BIT 12 TO ITSELF
05                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 11
06                  ;AND SUM BIT 12 TO GO TO 0 RESULT SHD=20
07                ;AC03:
08 02152 105000         MOV 0,1         ;AC0=10 COMING INTO TEST
09 02153 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
10 02154 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
11 02155 132000         ADC 1,2         ;AC2 SHD NOW=-1
12 02156 150004         COM 2,2,SZR     ;NOT 0 IS BIT 12 CARRY FAILED
13 02157 063077         HALTE           ;BIT 12+12 FAILED ADD SEE ALU11
14                                      ;AND ALU12
15 02160 101120         MOVZL 0,0       ;SET UP NEXT TEST
16                  ;IF ABOVE TEST FAILS ALSO SEE CN2 IF AC1=0
17                      ADDT0 04,11,10,20,40
18                  ;TEST SINGLE BIT CARRY ADD BIT 11 TO ITSELF
19                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 10
20                  ;AND SUM BIT 11 TO GO TO 0 RESULT SHD=40
21                ;AC04:
22 02161 105000         MOV 0,1         ;AC0=20 COMING INTO TEST
23 02162 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
24 02163 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
25 02164 132000         ADC 1,2         ;AC2 SHD NOW=-1
26 02165 150004         COM 2,2,SZR     ;NOT 0 IS BIT 11 CARRY FAILED
27 02166 063077         HALTE           ;BIT 11+11 FAILED ADD SEE ALU10
28                                      ;AND ALU11
29 02167 101120         MOVZL 0,0       ;SET UP NEXT TEST
30                      ADDT0 05,10,9,40,100
31                  ;TEST SINGLE BIT CARRY ADD BIT 10 TO ITSELF
32                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 9
33                  ;AND SUM BIT 10 TO GO TO 0 RESULT SHD=100
34                ;AC05:
35 02170 105000         MOV 0,1         ;AC0=40 COMING INTO TEST
36 02171 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
37 02172 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
38 02173 132000         ADC 1,2         ;AC2 SHD NOW=-1
39 02174 150004         COM 2,2,SZR     ;NOT 0 IS BIT 10 CARRY FAILED
40 02175 063077         HALTE           ;BIT 10+10 FAILED ADD SEE ALU9
41                                      ;AND ALU10
42 02176 101120         MOVZL 0,0       ;SET UP NEXT TEST
43                      ADDT0 06,9,8,100,200
44                  ;TEST SINGLE BIT CARRY ADD BIT 9 TO ITSELF
45                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 8
46                  ;AND SUM BIT 9 TO GO TO 0 RESULT SHD=200
47                ;AC06:
48 02177 105000         MOV 0,1         ;AC0=100 COMING INTO TEST
49 02200 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
50 02201 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
51 02202 132000         ADC 1,2         ;AC2 SHD NOW=-1
52 02203 150004         COM 2,2,SZR     ;NOT 0 IS BIT 9 CARRY FAILED
53 02204 063077         HALTE           ;BIT 9+9 FAILED ADD SEE ALU8
54                                      ;AND ALU9
55 02205 101120         MOVZL 0,0       ;SET UP NEXT TEST
56                      ADDT0 07,8,7,200,400
57                  ;TEST SINGLE BIT CARRY ADD BIT 8 TO ITSELF
58                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 7
59                  ;AND SUM BIT 8 TO GO TO 0 RESULT SHD=400
60                ;AC07:
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0044 N3LGC
01 02206 105000         MOV 0,1         ;AC0=200 COMING INTO TEST
02 02207 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
03 02210 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
04 02211 132000         ADC 1,2         ;AC2 SHD NOW=-1
05 02212 150004         COM 2,2,SZR     ;NOT 0 IS BIT 8 CARRY FAILED
06 02213 063077         HALTE           ;BIT 8+8 FAILED ADD SEE ALU7
07                                      ;AND ALU8
08 02214 101120         MOVZL 0,0       ;SET UP NEXT TEST
09                  ;IF ABOVE TEST FAILS ALSO SEE CN1 IF AC1=0
10                      ADDT0 08,7,6,400,1000
11                  ;TEST SINGLE BIT CARRY ADD BIT 7 TO ITSELF
12                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 6
13                  ;AND SUM BIT 7 TO GO TO 0 RESULT SHD=1000
14                ;AC08:
15 02215 105000         MOV 0,1         ;AC0=400 COMING INTO TEST
16 02216 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
17 02217 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
18 02220 132000         ADC 1,2         ;AC2 SHD NOW=-1
19 02221 150004         COM 2,2,SZR     ;NOT 0 IS BIT 7 CARRY FAILED
20 02222 063077         HALTE           ;BIT 7+7 FAILED ADD SEE ALU6
21                                      ;AND ALU7
22 02223 101120         MOVZL 0,0       ;SET UP NEXT TEST
23                      ADDT0 09,6,5,1000,2000
24                  ;TEST SINGLE BIT CARRY ADD BIT 6 TO ITSELF
25                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 5
26                  ;AND SUM BIT 6 TO GO TO 0 RESULT SHD=2000
27                ;AC09:
28 02224 105000         MOV 0,1         ;AC0=1000 COMING INTO TEST
29 02225 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
30 02226 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
31 02227 132000         ADC 1,2         ;AC2 SHD NOW=-1
32 02230 150004         COM 2,2,SZR     ;NOT 0 IS BIT 6 CARRY FAILED
33 02231 063077         HALTE           ;BIT 6+6 FAILED ADD SEE ALU5
34                                      ;AND ALU6
35 02232 101120         MOVZL 0,0       ;SET UP NEXT TEST
36                      ADDT0 10,5,4,2000,4000
37                  ;TEST SINGLE BIT CARRY ADD BIT 5 TO ITSELF
38                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 4
39                  ;AND SUM BIT 5 TO GO TO 0 RESULT SHD=4000
40                ;AC10:
41 02233 105000         MOV 0,1         ;AC0=2000 COMING INTO TEST
42 02234 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
43 02235 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
44 02236 132000         ADC 1,2         ;AC2 SHD NOW=-1
45 02237 150004         COM 2,2,SZR     ;NOT 0 IS BIT 5 CARRY FAILED
46 02240 063077         HALTE           ;BIT 5+5 FAILED ADD SEE ALU4
47                                      ;AND ALU5
48 02241 101120         MOVZL 0,0       ;SET UP NEXT TEST
49                      ADDT0 11,4,3,4000,10000
50                  ;TEST SINGLE BIT CARRY ADD BIT 4 TO ITSELF
51                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 3
52                  ;AND SUM BIT 4 TO GO TO 0 RESULT SHD=10000
53                ;AC11:
54 02242 105000         MOV 0,1         ;AC0=4000 COMING INTO TEST
55 02243 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
56 02244 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
57 02245 132000         ADC 1,2         ;AC2 SHD NOW=-1
58 02246 150004         COM 2,2,SZR     ;NOT 0 IS BIT 4 CARRY FAILED
59 02247 063077         HALTE           ;BIT 4+4 FAILED ADD SEE ALU3
60                                      ;AND ALU4
```

```
 0045 N3LGC
01 02250 101120          MOVZL 0,0        ;SET UP NEXT TEST
02                  ;IF ABOVE TEST FAILS SEE ALSO CN0 IF AC1=0
03                       ADDT0 12,3,2,10000,20000
04                  ;TEST SINGLE BIT CARRY ADD BIT 3 TO ITSELF
05                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 2
06                  ;AND SUM BIT 3 TO GO TO 0 RESULT SHD=20000
07                ;AC12:
08 02251 105000          MOV 0,1          ;AC0=10000 COMING INTO TEST
09 02252 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
10 02253 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
11 02254 132000          ADC 1,2          ;AC2 SHD NOW=-1
12 02255 150004          COM 2,2,SZR      ;NOT 0 IS BIT 3 CARRY FAILED
13 02256 063077          HALTE            ;BIT 3+3 FAILED ADD SEE ALU2
14                                          ;AND ALU3
15 02257 101120          MOVZL 0,0        ;SET UP NEXT TEST
16                       ADDT0 13,2,1,20000,40000
17                  ;TEST SINGLE BIT CARRY ADD BIT 2 TO ITSELF
18                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 1
19                  ;AND SUM BIT 2 TO GO TO 0 RESULT SHD=40000
20                ;AC13:
21 02260 105000          MOV 0,1          ;AC0=20000 COMING INTO TEST
22 02261 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
23 02262 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
24 02263 132000          ADC 1,2          ;AC2 SHD NOW=-1
25 02264 150004          COM 2,2,SZR      ;NOT 0 IS BIT 2 CARRY FAILED
26 02265 063077          HALTE            ;BIT 2+2 FAILED ADD SEE ALU1
27                                          ;AND ALU2
28 02266 101120          MOVZL 0,0        ;SET UP NEXT TEST
29                       ADDT0 14,1,0,40000,100000
30                  ;TEST SINGLE BIT CARRY ADD BIT 1 TO ITSELF
31                  ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 0
32                  ;AND SUM BIT 1 TO GO TO 0 RESULT SHD=100000
33                ;AC14:
34 02267 105000          MOV 0,1          ;AC0=40000 COMING INTO TEST
35 02270 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
36 02271 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
37 02272 132000          ADC 1,2          ;AC2 SHD NOW=-1
38 02273 150004          COM 2,2,SZR      ;NOT 0 IS BIT 1 CARRY FAILED
39 02274 063077          HALTE            ;BIT 1+1 FAILED ADD SEE ALU0
40                                          ;AND ALU1
41 02275 101120          MOVZL 0,0        ;SET UP NEXT TEST
42
43                ;TEST ADD BIT 0 TO BIT0 AC0=100000
44                ;SEE THAT CRYOUT GETS TO CRY
45 02276 105020 AC15:    MOVZ 0,1
46 02277 127004          ADD 1,1,SZR      ;ADD BIT 0 TO 0 FAILED
47 02300 063077          HALTE
48 02301 125003          MOV 1,1,SNC      ;BIT 0+BIT 0 DID NOT CRY OUT
49 02302 063077          HALTE
```

```
 0046 N3LGC
01
02                ;TEST AND INSTRUCTION AND VARIATIONS
03                ;FIRST TEST GROSS CASE AND -1 TO -1
04
05 02303 102000 AND00:   ADC 0,0          ;SET AC0=-1
06 02304 103405          AND 0,0,SNR      ;FIRST USE OF "AND"
07 02305 063077          HALTE            ;RESULT SHD STILL BE NON 0
08                ;IF RESULT=0 "AND" LOOKS LIKE "SUB" OR "INC"
09                ;SEE NOT IR6 OR NOT IR5 AT ALU ROM
10 02306 104004          COM 0,1,SZR
11 02307 063077          HALTE            ;RESULT OF PREV AND NOT=-1
12                ;IF RESULT IN AC0=-2 "AND" LOOKS LIKE "ADD"
13                ;SEE NOT IR7 AT ALU ROM
14
15                ;TEST AND 0'S TO 0'S RESULT SHD REMAIN=0
16 02310 102000 AND01:   ADC 0,0
17 02311 100000          COM 0,0          ;AC0=0
18 02312 103404          AND 0,0,SZR      ;RESULT OF AND SHD=0
19 02313 063077          HALTE
20 02314 101004          MOV 0,0,SZR      ;RECHECK RESULT
21 02315 063077          HALTE
22                ;SEE RESULT IN AC0 TO DETERMINE ALU BIT(S) IN ERR
23
24                ;AND -1 TO 0 WITH 0 AS DESTINATION
25                ;RESULT SHOULD AGAIN=0'S
26 02316 102000 AND02:   ADC 0,0
27 02317 104000          COM 0,1
28 02320 107404          AND 0,1,SZR      ;DEST REG AC1=0'S
29 02321 063077          HALTE            ;RESULT OF ABOVE AND NOT=0
30 02322 125004          MOV 1,1,SZR      ;RECHECK RESULT
31 02323 063077          HALTE
32                ;EXAMINE AC1 TO DETERMINE ALU BIT(S) IN ERROR
33
34                ;TEST AND OF 0 TO -1 WITH -1 ORIGINAL DESTINATION
35 02324 102000 AND03:   ADC 0,0
36 02325 104000          COM 0,1
37 02326 123404          AND 1,0,SZR      ;DEST=-1  SRC=0  RES SHD=0
38 02327 063077          HALTE
39 02330 101004          MOV  0,0,SZR     ;RECHECK RESULT
40 02331 063077          HALTE
41                ;EXAMINE AC0 TO DETERMINE ALU BIT(S) IN ERROR
```

```
10047 N3LGC
01
02                ;DEFINE BIT TEST MACRO FOR AND INSTRUCTION
03                  .MACRO ANDTS
04                ;THE NEXT SERIES IS AN AND TST OF BIT ^2
05                ;AC0=^3 COMING INTO THE TEST
06              ;AND^1:
07                      MOV 0,1           ;AC0=^3
08                      AND 0,1,SNR       ;BIT ^2 SHD REMAIN=1
09                      HALTE
10                      MOV 1,2
11                      ADC 0,2
12                      COM 2,2,SZR       ;TEST FOR EXTRA BITS
13                      HALTE             ;MORE THAN 1 BIT IN AND OF ^3
14                ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=^3
15
16
17                ;NOW TEST AND OF COMPLIMENTS
18                ;SOURCE WILL=^3 DEST WILL=COMPLIMENT
19              ;AN^1A:
20                      COM 0,1
21                      AND 0,1,SZR
22                      HALTE             ;AND OF ^3 AND ITS COM FAILED
23                ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
24
25
26                ;TEST AND OF COMPLIMENTS WITH DEST=^3 AND SRC=COM
27              ;AN^1B:
28                      MOV 0,1
29                      COM 1,2
30                      AND 2,1,SZR
31                      HALTE             ;AND OF ^3 AND ITS COM FAILED
32                ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
33                      MOVZL 0,0         ;SET UP NEXT TEST
34              %
35
36
37                ;SET UP AC0=1 FOR FIRST AND TEST
38
39 02332 102000          ADC 0,0
40 02333 100145          COMOL 0,0,SNR
41 02334 063077          HALTE
```

```
10048 N3LGC
01
02                      ANDTS 04,15,1
03                ;THE NEXT SERIES IS AN AND TST OF BIT 15
04                ;AC0=1 COMING INTO THE TEST
05              ;AND04:
06 02335 105000          MOV 0,1           ;AC0=1
07 02336 107405          AND 0,1,SNR       ;BIT 15 SHD REMAIN=1
08 02337 063077          HALTE
09 02340 131000          MOV 1,2
10 02341 112000          ADC 0,2
11 02342 150004          COM 2,2,SZR       ;TEST FOR EXTRA BITS
12 02343 063077          HALTE             ;MORE THAN 1 BIT IN AND OF 1
13                ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1
14
15
16                ;NOW TEST AND OF COMPLIMENTS
17                ;SOURCE WILL=1 DEST WILL=COMPLIMENT
18              ;AN04A:
19 02344 104000          COM 0,1
20 02345 107404          AND 0,1,SZR
21 02346 063077          HALTE             ;AND OF 1 AND ITS COM FAILED
22                ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
23
24
25                ;TEST AND OF COMPLIMENTS WITH DEST=1 AND SRC=COM
26              ;AN04B:
27 02347 105000          MOV 0,1
28 02350 130000          COM 1,2
29 02351 147404          AND 2,1,SZR
30 02352 063077          HALTE             ;AND OF 1 AND ITS COM FAILED
31                ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
32 02353 101120          MOVZL 0,0         ;SET UP NEXT TEST
33                       ANDTS 05,14,2
34                ;THE NEXT SERIES IS AN AND TST OF BIT 14
35                ;AC0=2 COMING INTO THE TEST
36              ;AND05:
37 02354 105000          MOV 0,1           ;AC0=2
38 02355 107405          AND 0,1,SNR       ;BIT 14 SHD REMAIN=1
39 02356 063077          HALTE
40 02357 131000          MOV 1,2
41 02360 112000          ADC 0,2
42 02361 150004          COM 2,2,SZR       ;TEST FOR EXTRA BITS
43 02362 063077          HALTE             ;MORE THAN 1 BIT IN AND OF 2
44                ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2
45
46
47                ;NOW TEST AND OF COMPLIMENTS
48                ;SOURCE WILL=2 DEST WILL=COMPLIMENT
49              ;AN05A:
50 02363 104000          COM 0,1
51 02364 107404          AND 0,1,SZR
52 02365 063077          HALTE             ;AND OF 2 AND ITS COM FAILED
53                ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
54
55
56                ;TEST AND OF COMPLIMENTS WITH DEST=2 AND SRC=COM
57              ;AN05B:
58 02366 105000          MOV 0,1
59 02367 130000          COM 1,2
60 02370 147404          AND 2,1,SZR
```

```
 0049 N3LGC
01 02371 063077          HALTE              ;AND OF 2 AND ITS COM FAILED
02                  ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03 02372 101120          MOVZL 0,0          ;SET UP NEXT TEST
04                       ANDTS 06,13,4
05                  ;THE NEXT SERIES IS AN AND TST OF BIT 13
06                  ;AC0=4 COMING INTO THE TEST
07                ;AND06:
08 02373 105000          MOV 0,1            ;AC0=4
09 02374 107405          AND 0,1,SNR        ;BIT 13 SHD REMAIN=1
10 02375 063077          HALTE
11 02376 131000          MOV 1,2
12 02377 112000          ADC 0,2
13 02400 150004          COM 2,2,SZR        ;TEST FOR EXTRA BITS
14 02401 063077          HALTE              ;MORE THAN 1 BIT IN AND OF 4
15                  ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4
16
17
18                  ;NOW TEST AND OF COMPLIMENTS
19                  ;SOURCE WILL=4 DEST WILL=COMPLIMENT
20                ;AN06A:
21 02402 104000          COM 0,1
22 02403 107404          AND 0,1,SZR
23 02404 063077          HALTE              ;AND OF 4 AND ITS COM FAILED
24                  ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
25
26
27                  ;TEST AND OF COMPLIMENTS WITH DEST=4 AND SRC=COM
28                ;AN06B:
29 02405 105000          MOV 0,1
30 02406 130000          COM 1,2
31 02407 147404          AND 2,1,SZR
32 02410 063077          HALTE              ;AND OF 4 AND ITS COM FAILED
33                  ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
34 02411 101120          MOVZL 0,0          ;SET UP NEXT TEST
35                       ANDTS 07,12,10
36                  ;THE NEXT SERIES IS AN AND TST OF BIT 12
37                  ;AC0=10 COMING INTO THE TEST
38                ;AND07:
39 02412 105000          MOV 0,1            ;AC0=10
40 02413 107405          AND 0,1,SNR        ;BIT 12 SHD REMAIN=1
41 02414 063077          HALTE
42 02415 131000          MOV 1,2
43 02416 112000          ADC 0,2
44 02417 150004          COM 2,2,SZR        ;TEST FOR EXTRA BITS
45 02420 063077          HALTE              ;MORE THAN 1 BIT IN AND OF 10
46                  ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10
47
48
49                  ;NOW TEST AND OF COMPLIMENTS
50                  ;SOURCE WILL=10 DEST WILL=COMPLIMENT
51                ;AN07A:
52 02421 104000          COM 0,1
53 02422 107404          AND 0,1,SZR
54 02423 063077          HALTE              ;AND OF 10 AND ITS COM FAILED
55                  ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
56
57
58                  ;TEST AND OF COMPLIMENTS WITH DEST=10 AND SRC=COM
59                ;AN07B:
60 02424 105000          MOV 0,1
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 0050 N3LGC
01 02425 130000          COM 1,2
02 02426 147404          AND 2,1,SZR
03 02427 063077          HALTE              ;AND OF 10 AND ITS COM FAILED
04                  ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
05 02430 101120          MOVZL 0,0          ;SET UP NEXT TEST
06                       ANDTS 08,11,20
07                  ;THE NEXT SERIES IS AN AND TST OF BIT 11
08                  ;AC0=20 COMING INTO THE TEST
09                ;AND08:
10 02431 105000          MOV 0,1            ;AC0=20
11 02432 107405          AND 0,1,SNR        ;BIT 11 SHD REMAIN=1
12 02433 063077          HALTE
13 02434 131000          MOV 1,2
14 02435 112000          ADC 0,2
15 02436 150004          COM 2,2,SZR        ;TEST FOR EXTRA BITS
16 02437 063077          HALTE              ;MORE THAN 1 BIT IN AND OF 20
17                  ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20
18
19
20                  ;NOW TEST AND OF COMPLIMENTS
21                  ;SOURCE WILL=20 DEST WILL=COMPLIMENT
22                ;AN08A:
23 02440 104000          COM 0,1
24 02441 107404          AND 0,1,SZR
25 02442 063077          HALTE              ;AND OF 20 AND ITS COM FAILED
26                  ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
27
28
29                  ;TEST AND OF COMPLIMENTS WITH DEST=20 AND SRC=COM
30                ;AN08B:
31 02443 105000          MOV 0,1
32 02444 130000          COM 1,2
33 02445 147404          AND 2,1,SZR
34 02446 063077          HALTE              ;AND OF 20 AND ITS COM FAILED
35                  ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
36 02447 101120          MOVZL 0,0          ;SET UP NEXT TEST
37                       ANDTS 09,10,40
38                  ;THE NEXT SERIES IS AN AND TST OF BIT 10
39                  ;AC0=40 COMING INTO THE TEST
40                ;AND09:
41 02450 105000          MOV 0,1            ;AC0=40
42 02451 107405          AND 0,1,SNR        ;BIT 10 SHD REMAIN=1
43 02452 063077          HALTE
44 02453 131000          MOV 1,2
45 02454 112000          ADC 0,2
46 02455 150004          COM 2,2,SZR        ;TEST FOR EXTRA BITS
47 02456 063077          HALTE              ;MORE THAN 1 BIT IN AND OF 40
48                  ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40
49
50
51                  ;NOW TEST AND OF COMPLIMENTS
52                  ;SOURCE WILL=40 DEST WILL=COMPLIMENT
53                ;AN09A:
54 02457 104000          COM 0,1
55 02460 107404          AND 0,1,SZR
56 02461 063077          HALTE              ;AND OF 40 AND ITS COM FAILED
57                  ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
58
59
60                  ;TEST AND OF COMPLIMENTS WITH DEST=40 AND SRC=COM
```

```
01                      ;AN09B:
02 02462 105000                 MOV 0,1
03 02463 130000                 COM 1,2
04 02464 147404                 AND 2,1,SZR
05 02465 063077                 HALTE           ;AND OF 40 AND ITS COM FAILED
06                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
07 02466 101120                 MOVZL 0,0       ;SET UP NEXT TEST
08                              ANDTS 10,9,100
09                      ;THE NEXT SERIES IS AN AND TST OF BIT 9
10                      ;AC0=100 COMING INTO THE TEST
11                      ;AND10:
12 02467 105000                 MOV 0,1         ;AC0=100
13 02470 107405                 AND 0,1,SNR     ;BIT 9 SHD REMAIN=1
14 02471 063077                 HALTE
15 02472 131000                 MOV 1,2
16 02473 112000                 ADC 0,2
17 02474 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
18 02475 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 100
19                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100
20
21
22                      ;NOW TEST AND OF COMPLIMENTS
23                      ;SOURCE WILL=100 DEST WILL=COMPLIMENT
24                      ;AN10A:
25 02476 104000                 COM 0,1
26 02477 107404                 AND 0,1,SZR
27 02500 063077                 HALTE           ;AND OF 100 AND ITS COM FAILED
28                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
29
30
31                      ;TEST AND OF COMPLIMENTS WITH DEST=100 AND SRC=COM
32                      ;AN10B:
33 02501 105000                 MOV 0,1
34 02502 130000                 COM 1,2
35 02503 147404                 AND 2,1,SZR
36 02504 063077                 HALTE           ;AND OF 100 AND ITS COM FAILED
37                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
38 02505 101120                 MOVZL 0,0       ;SET UP NEXT TEST
39                              ANDTS 11,8,200
40                      ;THE NEXT SERIES IS AN AND TST OF BIT 8
41                      ;AC0=200 COMING INTO THE TEST
42                      ;AND11:
43 02506 105000                 MOV 0,1         ;AC0=200
44 02507 107405                 AND 0,1,SNR     ;BIT 8 SHD REMAIN=1
45 02510 063077                 HALTE
46 02511 131000                 MOV 1,2
47 02512 112000                 ADC 0,2
48 02513 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
49 02514 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 200
50                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=200
51
52
53                      ;NOW TEST AND OF COMPLIMENTS
54                      ;SOURCE WILL=200 DEST WILL=COMPLIMENT
55                      ;AN11A:
56 02515 104000                 COM 0,1
57 02516 107404                 AND 0,1,SZR
58 02517 063077                 HALTE           ;AND OF 200 AND ITS COM FAILED
59                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
60
```



```
01
02                      ;TEST AND OF COMPLIMENTS WITH DEST=200 AND SRC=COM
03                      ;AN11B:
04 02520 105000                 MOV 0,1
05 02521 130000                 COM 1,2
06 02522 147404                 AND 2,1,SZR
07 02523 063077                 HALTE           ;AND OF 200 AND ITS COM FAILED
08                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
09 02524 101120                 MOVZL 0,0       ;SET UP NEXT TEST
10                              ANDTS 12,7,400
11                      ;THE NEXT SERIES IS AN AND TST OF BIT 7
12                      ;AC0=400 COMING INTO THE TEST
13                      ;AND12:
14 02525 105000                 MOV 0,1         ;AC0=400
15 02526 107405                 AND 0,1,SNR     ;BIT 7 SHD REMAIN=1
16 02527 063077                 HALTE
17 02530 131000                 MOV 1,2
18 02531 112000                 ADC 0,2
19 02532 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
20 02533 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 400
21                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=400
22
23
24                      ;NOW TEST AND OF COMPLIMENTS
25                      ;SOURCE WILL=400 DEST WILL=COMPLIMENT
26                      ;AN12A:
27 02534 104000                 COM 0,1
28 02535 107404                 AND 0,1,SZR
29 02536 063077                 HALTE           ;AND OF 400 AND ITS COM FAILED
30                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
31
32
33                      ;TEST AND OF COMPLIMENTS WITH DEST=400 AND SRC=COM
34                      ;AN12B:
35 02537 105000                 MOV 0,1
36 02540 130000                 COM 1,2
37 02541 147404                 AND 2,1,SZR
38 02542 063077                 HALTE           ;AND OF 400 AND ITS COM FAILED
39                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
40 02543 101120                 MOVZL 0,0       ;SET UP NEXT TEST
41                              ANDTS 13,6,1000
42                      ;THE NEXT SERIES IS AN AND TST OF BIT 6
43                      ;AC0=1000 COMING INTO THE TEST
44                      ;AND13:
45 02544 105000                 MOV 0,1         ;AC0=1000
46 02545 107405                 AND 0,1,SNR     ;BIT 6 SHD REMAIN=1
47 02546 063077                 HALTE
48 02547 131000                 MOV 1,2
49 02550 112000                 ADC 0,2
50 02551 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
51 02552 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 1000
52                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1000
53
54
55                      ;NOW TEST AND OF COMPLIMENTS
56                      ;SOURCE WILL=1000 DEST WILL=COMPLIMENT
57                      ;AN13A:
58 02553 104000                 COM 0,1
59 02554 107404                 AND 0,1,SZR
60 02555 063077                 HALTE           ;AND OF 1000 AND ITS COM FAILED
```

```
01                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
02
03
04                      ;TEST AND OF COMPLIMENTS WITH DEST=1000 AND SRC=COM
05                    ;AN13B:
06 02556 105000               MOV 0,1
07 02557 130000               COM 1,2
08 02560 147404               AND 2,1,SZR
09 02561 063077               HALTE           ;AND OF 1000 AND ITS COM FAILED
10                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
11 02562 101120               MOVZL 0,0       ;SET UP NEXT TEST
12                            ANDTS 14,5,2000
13                      ;THE NEXT SERIES IS AN AND TST OF BIT 5
14                      ;AC0=2000 COMING INTO THE TEST
15                    ;AND14:
16 02563 105000               MOV 0,1         ;AC0=2000
17 02564 107405               AND 0,1,SNR     ;BIT 5 SHD REMAIN=1
18 02565 063077               HALTE
19 02566 131000               MOV 1,2
20 02567 112000               ADC 0,2
21 02570 150004               COM 2,2,SZR     ;TEST FOR EXTRA BITS
22 02571 063077               HALTE           ;MORE THAN 1 BIT IN AND OF 2000
23                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2000
24
25
26                      ;NOW TEST AND OF COMPLIMENTS
27                      ;SOURCE WILL=2000 DEST WILL=COMPLIMENT
28                    ;AN14A:
29 02572 104000               COM 0,1
30 02573 107404               AND 0,1,SZR
31 02574 063077               HALTE           ;AND OF 2000 AND ITS COM FAILED
32                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
33
34
35                      ;TEST AND OF COMPLIMENTS WITH DEST=2000 AND SRC=COM
36                    ;AN14B:
37 02575 105000               MOV 0,1
38 02576 130000               COM 1,2
39 02577 147404               AND 2,1,SZR
40 02600 063077               HALTE           ;AND OF 2000 AND ITS COM FAILED
41                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
42 02601 101120               MOVZL 0,0       ;SET UP NEXT TEST
43                            ANDTS 15,4,4000
44                      ;THE NEXT SERIES IS AN AND TST OF BIT 4
45                      ;AC0=4000 COMING INTO THE TEST
46                    ;AND15:
47 02602 105000               MOV 0,1         ;AC0=4000
48 02603 107405               AND 0,1,SNR     ;BIT 4 SHD REMAIN=1
49 02604 063077               HALTE
50 02605 131000               MOV 1,2
51 02606 112000               ADC 0,2
52 02607 150004               COM 2,2,SZR     ;TEST FOR EXTRA BITS
53 02610 063077               HALTE           ;MORE THAN 1 BIT IN AND OF 4000
54                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4000
55
56
57                      ;NOW TEST AND OF COMPLIMENTS
58                      ;SOURCE WILL=4000 DEST WILL=COMPLIMENT
59                    ;AN15A:
60 02611 104000               COM 0,1
```



```
01 02612 107404               AND 0,1,SZR
02 02613 063077               HALTE           ;AND OF 4000 AND ITS COM FAILED
03                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
04
05
06                      ;TEST AND OF COMPLIMENTS WITH DEST=4000 AND SRC=COM
07                    ;AN15B:
08 02614 105000               MOV 0,1
09 02615 130000               COM 1,2
10 02616 147404               AND 2,1,SZR
11 02617 063077               HALTE           ;AND OF 4000 AND ITS COM FAILED
12                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
13 02620 101120               MOVZL 0,0       ;SET UP NEXT TEST
14                            ANDTS 16,3,10000
15                      ;THE NEXT SERIES IS AN AND TST OF BIT 3
16                      ;AC0=10000 COMING INTO THE TEST
17                    ;AND16:
18 02621 105000               MOV 0,1         ;AC0=10000
19 02622 107405               AND 0,1,SNR     ;BIT 3 SHD REMAIN=1
20 02623 063077               HALTE
21 02624 131000               MOV 1,2
22 02625 112000               ADC 0,2
23 02626 150004               COM 2,2,SZR     ;TEST FOR EXTRA BITS
24 02627 063077               HALTE           ;MORE THAN 1 BIT IN AND OF 10000
25                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10000
26
27
28                      ;NOW TEST AND OF COMPLIMENTS
29                      ;SOURCE WILL=10000 DEST WILL=COMPLIMENT
30                    ;AN16A:
31 02630 104000               COM 0,1
32 02631 107404               AND 0,1,SZR
33 02632 063077               HALTE           ;AND OF 10000 AND ITS COM FAILED
34                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
35
36
37                      ;TEST AND OF COMPLIMENTS WITH DEST=10000 AND SRC=COM
38                    ;AN16B:
39 02633 105000               MOV 0,1
40 02634 130000               COM 1,2
41 02635 147404               AND 2,1,SZR
42 02636 063077               HALTE           ;AND OF 10000 AND ITS COM FAILED
43                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
44 02637 101120               MOVZL 0,0       ;SET UP NEXT TEST
45                            ANDTS 17,2,20000
46                      ;THE NEXT SERIES IS AN AND TST OF BIT 2
47                      ;AC0=20000 COMING INTO THE TEST
48                    ;AND17:
49 02640 105000               MOV 0,1         ;AC0=20000
50 02641 107405               AND 0,1,SNR     ;BIT 2 SHD REMAIN=1
51 02642 063077               HALTE
52 02643 131000               MOV 1,2
53 02644 112000               ADC 0,2
54 02645 150004               COM 2,2,SZR     ;TEST FOR EXTRA BITS
55 02646 063077               HALTE           ;MORE THAN 1 BIT IN AND OF 20000
56                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20000
57
58
59                      ;NOW TEST AND OF COMPLIMENTS
60                      ;SOURCE WILL=20000 DEST WILL=COMPLIMENT
```

```
0055 N3LGC
01                      ;AN17A:
02 02647 104000                 COM 0,1
03 02650 107404                 AND 0,1,SZR
04 02651 063077                 HALTE           ;AND OF 20000 AND ITS COM FAILED
05                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
06
07
08                      ;TEST AND OF COMPLIMENTS WITH DEST=20000 AND SRC=COM
09                      ;AN17B:
10 02652 105000                 MOV 0,1
11 02653 130000                 COM 1,2
12 02654 147404                 AND 2,1,SZR
13 02655 063077                 HALTE           ;AND OF 20000 AND ITS COM FAILED
14                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
15 02656 101120                 MOVZL 0,0       ;SET UP NEXT TEST
16                              ANDTS 18,1,40000
17                      ;THE NEXT SERIES IS AN AND TST OF BIT 1
18                      ;AC0=40000 COMING INTO THE TEST
19                      ;AND18:
20 02657 105000                 MOV 0,1         ;AC0=40000
21 02660 107405                 AND 0,1,SNR     ;BIT 1 SHD REMAIN=1
22 02661 063077                 HALTE
23 02662 131000                 MOV 1,2
24 02663 112000                 ADC 0,2
25 02664 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
26 02665 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 40000
27                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40000
28
29
30                      ;NOW TEST AND OF COMPLIMENTS
31                      ;SOURCE WILL=40000 DEST WILL=COMPLIMENT
32                      ;AN18A:
33 02666 104000                 COM 0,1
34 02667 107404                 AND 0,1,SZR
35 02670 063077                 HALTE           ;AND OF 40000 AND ITS COM FAILED
36                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
37
38
39                      ;TEST AND OF COMPLIMENTS WITH DEST=40000 AND SRC=COM
40                      ;AN18B:
41 02671 105000                 MOV 0,1
42 02672 130000                 COM 1,2
43 02673 147404                 AND 2,1,SZR
44 02674 063077                 HALTE           ;AND OF 40000 AND ITS COM FAILED
45                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
46 02675 101120                 MOVZL 0,0       ;SET UP NEXT TEST
47                              ANDTS 19,0,100000
48                      ;THE NEXT SERIES IS AN AND TST OF BIT 0
49                      ;AC0=100000 COMING INTO THE TEST
50                      ;AND19:
51 02676 105000                 MOV 0,1         ;AC0=100000
52 02677 107405                 AND 0,1,SNR     ;BIT 0 SHD REMAIN=1
53 02700 063077                 HALTE
54 02701 131000                 MOV 1,2
55 02702 112000                 ADC 0,2
56 02703 150004                 COM 2,2,SZR     ;TEST FOR EXTRA BITS
57 02704 063077                 HALTE           ;MORE THAN 1 BIT IN AND OF 100000
58                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100000
59
60
```

```
0056 N3LGC
01                      ;NOW TEST AND OF COMPLIMENTS
02                      ;SOURCE WILL=100000 DEST WILL=COMPLIMENT
03                      ;AN19A:
04 02705 104000                 COM 0,1
05 02706 107404                 AND 0,1,SZR
06 02707 063077                 HALTE           ;AND OF 100000 AND ITS COM FAILED
07                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
08
09
10                      ;TEST AND OF COMPLIMENTS WITH DEST=100000 AND SRC=COM
11                      ;AN19B:
12 02710 105000                 MOV 0,1
13 02711 130000                 COM 1,2
14 02712 147404                 AND 2,1,SZR
15 02713 063077                 HALTE           ;AND OF 100000 AND ITS COM FAILED
16                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
17 02714 101120                 MOVZL 0,0       ;SET UP NEXT TEST
```

```
10057 N3LGC
01
02                ;THE NEXT SERIES OF TESTS VERIFY THAT "AND"
03                ;DOES NOT EFFECT "CRY"
04
05 02715 102020 AND20:  ADCZ 0,0          ;CRY=0  AC0=-1
06 02716 103402         AND 0,0,SZC       ;CRY SHD STILL=0
07 02717 063077         HALTE             ;AND SET CRY=1
08                ;SEE "NOT AND" AND WITH ALUCARRYOUT
09
10 02720 102040 AND21:  ADCO 0,0          ;AND=1 WITH CRY=1
11 02721 103403         AND 0,0,SNC       ;CRY SHD STILL=1
12 02722 063077         HALTE             ;AND OF -1,-1 CLEARED CARRY
13
14                ;TEST AND WITH 00 TO NOT CHNG CRY 0 TO 1
15
16 02723 102000 AND22:  ADC 0,0
17 02724 100020         COMZ 0,0
18 02725 103402         AND 0,0,SZC
19 02726 063077         HALTE
20                ;TEST AND WITH 00 TO NOT CHNG CRY 1 TO 0
21 02727 102000 AND23:  ADC 0,0
22 02730 100040         COMO 0,0
23 02731 103403         AND 0,0,SNC
24 02732 063077         HALTE
25
26                ;REPEAT TESTS CHANGING STATE OF CRY DURING AND
27
28 02733 102040 AND24:  ADCO 0,0
29 02734 103422         ANDZ 0,0,SZC
30 02735 063077         HALTE             ;SEE IR11 NOT IR10 IN NOT SCI
31                ;POSSIBLY TRANSITION TIMING AS AND DID NOT PREV CHNG CRY
32 02736 102020 AND25:  ADCZ 0,0
33 02737 103443         ANDO 0,0,SNC      ;SEE NOT OF ABOVE TEST IR10=11
34 02740 063077         HALTE             ;CRY WENT TO 0 AND -1 TO -1
35
36 02741 102000 AND26:  ADC 0,0
37 02742 100040         COMO 0,0
38 02743 103422         ANDZ 0,0,SZC      ;FURTHER TEST AND IN SCI LOGIC
39 02744 063077         HALTE             ;CRY WENT TO 1 AND 0 TO 0
40
41 02745 102000 AND27:  ADC 0,0
42 02746 100020         COMZ 0,0
43 02747 103443         ANDO 0,0,SNC
44 02750 063077         HALT              ;CRY WENT 1 TO 0 AND OF 0 TO 0
45
46
```

```
10058 N3LGC
01                ;VERIFY THE EXISTENCE OF INC INSTRUCTION
02                ;FIRST TIME FOR "INC" INSTRUCTION
03 02751 102000 INC00:  ADC 0,0
04 02752 100000         COM 0,0
05 02753 101405         INC 0,0,SNR       ;RESULT=0 POSSIBLY ALU CRY NOT
06 02754 063077         HALTE             ;AC0 SHD=+1
07 02755 101005         MOV 0,0,SNR
08 02756 063077         HALTEE            ;MAKE SURE RESULT GOT BACK TO AC0
09 02757 105224         MOVZR 0,1,SZR     ;MAKE SURE ONLY +1 NO EXTRAS
10 02760 063077         HALT              ;EXAMINE AC0 FOR EXTRA BITS INC
11                ;AC0=0 POSSIBLY "NOT" IR6 INC LOOKS LIKE NEG
12                ;OR "NOT" IR7 INC LOOKS LIKE MOV SEE ALU ROM
13                ;OR IR5 INTO  ALC ROM INC LOOKS LIKE AND
14
15                ;TEST INC OF +1 TO +2 (2ND TIME FOR INC)
16 02761 102000 INC01:  ADC 0,0
17 02762 100140         COMOL 0,0         ;AC0=+1
18 02763 105120         MOVZL 0,1         ;AC1=+2
19 02764 101405         INC 0,0,SNR       ;1+1 SHD=2
20 02765 063077         HALTE             ;BIT 15 CARRY TO BIT 14(?)
21 02766 105000         ADC 0,1           ;AC1 SHD NOW=-1 (IF INC WORKED)
22 02767 124004         COM 1,1,SZR       ;AND COM SHD BE 0
23 02770 063077         HALTE             ;AC0 INC!D+1 INCORRECT
24                ;EXAMINE AC0 FOR ALU FAILURE IT SHD=+2
25                ;IF AC0 DOES=+2 EXAMINE AC1 FOR ADC+COM FAILURE
26
27                ;TEST TO INSURE ONLY SRC REG IS INVOLVED IN INC
28 02771 102000 INC02:  ADC 0,0
29 02772 100000         COM 0,0           ;AC0=0
30 02773 104140         COMOL 0,1         ;AC1=1
31 02774 125140         MOVOL 1,1         ;=3
32 02775 105405         INC 0,1,SNR       ;0+1 SHD=1
33 02776 063077         HALTE             ;ALU CRY FAILED (?) ALRDY TESTED
34 02777 131224         MOVZR 1,2,SZR     ;AC1 SHD ONLY=1
35 03000 063077         HALTE             ;PROBABLY DESTINATION REG ALSO ADDED
36                ;SEE NOT 2REN  ALC ROM INC ALSO CAUSES ADD OR AND
```

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10059 N3LGC
01
02                ;TEST INC TO CARRY THROUGH ALL 1 BITS
03                ;DEFINE MACRO FOR CARRY TESTS
04                      .MACRO INCTS
05                ;AC0=^A4 COMING INTO TEST,+1=AC1=^A5
06                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
07                ;BIT^A2 INTO BIT^A3 WITH RESULT=AC1
08              ;INC^A1:
09                      INC 0,2,SNR     ;AC0=^A4+1 AND BE NON ZERO
10                      HALTE           ;INC RESULT SHD=^A5
11                      MOV 2,3
12                      ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
13                      COM 3,3,SZR     ;THEN 0
14                      HALTE
15                      MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
16                      MOVZL 1,1       ;SET UP RESULT NEXT TEST
17              %
18
19                ;SET UP FIRST CARRY TEST
20 03001 102000         ADC 0,0
21 03002 100000         COM 0,0
22 03003 105140         MOVOL 0,1
23
24                      INCTS 03,ALUCRY,15,0,1
25                ;AC0=0 COMING INTO TEST,+1=AC1=1
26                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
27                ;BITALUCRY INTO BIT15 WITH RESULT=AC1
28              ;INC03:
29 03004 111405         INC 0,2,SNR     ;AC0=0+1 AND BE NON ZERO
30 03005 063077         HALTE           ;INC RESULT SHD=1
31 03006 155000         MOV 2,3
32 03007 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
33 03010 174004         COM 3,3,SZR     ;THEN 0
34 03011 063077         HALTE
35 03012 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
36 03013 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
37                      INCTS 04,15,14,1,2
38                ;AC0=1 COMING INTO TEST,+1=AC1=2
39                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
40                ;BIT15 INTO BIT14 WITH RESULT=AC1
41              ;INC04:
42 03014 111405         INC 0,2,SNR     ;AC0=1+1 AND BE NON ZERO
43 03015 063077         HALTE           ;INC RESULT SHD=2
44 03016 155000         MOV 2,3
45 03017 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
46 03020 174004         COM 3,3,SZR     ;THEN 0
47 03021 063077         HALTE
48 03022 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
49 03023 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
50                      INCTS 05,14,13,3,4
51                ;AC0=3 COMING INTO TEST,+1=AC1=4
52                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
53                ;BIT14 INTO BIT13 WITH RESULT=AC1
54              ;INC05:
55 03024 111405         INC 0,2,SNR     ;AC0=3+1 AND BE NON ZERO
56 03025 063077         HALTE           ;INC RESULT SHD=4
57 03026 155000         MOV 2,3
58 03027 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
59 03030 174004         COM 3,3,SZR     ;THEN 0
60 03031 063077         HALTE
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 0060 N3LGC
01 03032 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
02 03033 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
03                      INCTS 06,13,12,7,10
04                ;AC0=7 COMING INTO TEST,+1=AC1=10
05                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
06                ;BIT13 INTO BIT12 WITH RESULT=AC1
07              ;INC06:
08 03034 111405         INC 0,2,SNR     ;AC0=7+1 AND BE NON ZERO
09 03035 063077         HALTE           ;INC RESULT SHD=10
10 03036 155000         MOV 2,3
11 03037 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
12 03040 174004         COM 3,3,SZR     ;THEN 0
13 03041 063077         HALTE
14 03042 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
15 03043 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
16                      INCTS 07,12,11,17,20
17                ;AC0=17 COMING INTO TEST,+1=AC1=20
18                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
19                ;BIT12 INTO BIT11 WITH RESULT=AC1
20              ;INC07:
21 03044 111405         INC 0,2,SNR     ;AC0=17+1 AND BE NON ZERO
22 03045 063077         HALTE           ;INC RESULT SHD=20
23 03046 155000         MOV 2,3
24 03047 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
25 03050 174004         COM 3,3,SZR     ;THEN 0
26 03051 063077         HALTE
27 03052 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
28 03053 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
29                      INCTS 08,11,10,37,40
30                ;AC0=37 COMING INTO TEST,+1=AC1=40
31                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
32                ;BIT11 INTO BIT10 WITH RESULT=AC1
33              ;INC08:
34 03054 111405         INC 0,2,SNR     ;AC0=37+1 AND BE NON ZERO
35 03055 063077         HALTE           ;INC RESULT SHD=40
36 03056 155000         MOV 2,3
37 03057 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
38 03060 174004         COM 3,3,SZR     ;THEN 0
39 03061 063077         HALTE
40 03062 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
41 03063 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
42                      INCTS 09,10,9,77,100
43                ;AC0=77 COMING INTO TEST,+1=AC1=100
44                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
45                ;BIT10 INTO BIT9 WITH RESULT=AC1
46              ;INC09:
47 03064 111405         INC 0,2,SNR     ;AC0=77+1 AND BE NON ZERO
48 03065 063077         HALTE           ;INC RESULT SHD=100
49 03066 155000         MOV 2,3
50 03067 136000         ADC 1,3         ;ADC SUM OF 1+3 SHD=-1
51 03070 174004         COM 3,3,SZR     ;THEN 0
52 03071 063077         HALTE
53 03072 101140         MOVOL 0,0       ;SET UP CONSTANTS NEXT TEST
54 03073 125120         MOVZL 1,1       ;SET UP RESULT NEXT TEST
55                      INCTS 10,9,8,177,200
56                ;AC0=177 COMING INTO TEST,+1=AC1=200
57                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
58                ;BIT9 INTO BIT8 WITH RESULT=AC1
59              ;INC10:
60 03074 111405         INC 0,2,SNR     ;AC0=177+1 AND BE NON ZERO
```

```
 0061 N3LGC
01 03075 063077          HALTE              ;INC RESULT SHD=200
02 03076 155000          MOV 2,3
03 03077 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
04 03100 174004          COM 3,3,SZR        ;THEN 0
05 03101 063077          HALTE
06 03102 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
07 03103 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
08                       INCTS 11,8,7,377,400
09                    ;AC0=377 COMING INTO TEST,+1=AC1=400
10                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
11                    ;BIT8 INTO BIT7 WITH RESULT=AC1
12                 ;INC11:
13 03104 111405          INC 0,2,SNR        ;AC0=377+1 AND BE NON ZERO
14 03105 063077          HALTE              ;INC RESULT SHD=400
15 03106 155000          MOV 2,3
16 03107 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
17 03110 174004          COM 3,3,SZR        ;THEN 0
18 03111 063077          HALTE
19 03112 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
20 03113 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
21                       INCTS 12,7,6,777,1000
22                    ;AC0=777 COMING INTO TEST,+1=AC1=1000
23                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
24                    ;BIT7 INTO BIT6 WITH RESULT=AC1
25                 ;INC12:
26 03114 111405          INC 0,2,SNR        ;AC0=777+1 AND BE NON ZERO
27 03115 063077          HALTE              ;INC RESULT SHD=1000
28 03116 155000          MOV 2,3
29 03117 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
30 03120 174004          COM 3,3,SZR        ;THEN 0
31 03121 063077          HALTE
32 03122 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
33 03123 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
34                       INCTS 13,6,5,1777,2000
35                    ;AC0=1777 COMING INTO TEST,+1=AC1=2000
36                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
37                    ;BIT6 INTO BIT5 WITH RESULT=AC1
38                 ;INC13:
39 03124 111405          INC 0,2,SNR        ;AC0=1777+1 AND BE NON ZERO
40 03125 063077          HALTE              ;INC RESULT SHD=2000
41 03126 155000          MOV 2,3
42 03127 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
43 03130 174004          COM 3,3,SZR        ;THEN 0
44 03131 063077          HALTE
45 03132 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
46 03133 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
47                       INCTS 14,5,4,3777,4000
48                    ;AC0=3777 COMING INTO TEST,+1=AC1=4000
49                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                    ;BIT5 INTO BIT4 WITH RESULT=AC1
51                 ;INC14:
52 03134 111405          INC 0,2,SNR        ;AC0=3777+1 AND BE NON ZERO
53 03135 063077          HALTE              ;INC RESULT SHD=4000
54 03136 155000          MOV 2,3
55 03137 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
56 03140 174004          COM 3,3,SZR        ;THEN 0
57 03141 063077          HALTE
58 03142 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
59 03143 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
60                       INCTS 15,4,3,7777,10000
```

```
 0062 N3LGC
01                    ;AC0=7777 COMING INTO TEST,+1=AC1=10000
02                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
03                    ;BIT4 INTO BIT3 WITH RESULT=AC1
04                 ;INC15:
05 03144 111405          INC 0,2,SNR        ;AC0=7777+1 AND BE NON ZERO
06 03145 063077          HALTE              ;INC RESULT SHD=10000
07 03146 155000          MOV 2,3
08 03147 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
09 03150 174004          COM 3,3,SZR        ;THEN 0
10 03151 063077          HALTE
11 03152 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
12 03153 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
13                       INCTS 16,3,2,17777,20000
14                    ;AC0=17777 COMING INTO TEST,+1=AC1=20000
15                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
16                    ;BIT3 INTO BIT2 WITH RESULT=AC1
17                 ;INC16:
18 03154 111405          INC 0,2,SNR        ;AC0=17777+1 AND BE NON ZERO
19 03155 063077          HALTE              ;INC RESULT SHD=20000
20 03156 155000          MOV 2,3
21 03157 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
22 03160 174004          COM 3,3,SZR        ;THEN 0
23 03161 063077          HALTE
24 03162 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
25 03163 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
26                       INCTS 17,2,1,37777,40000
27                    ;AC0=37777 COMING INTO TEST,+1=AC1=40000
28                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
29                    ;BIT2 INTO BIT1 WITH RESULT=AC1
30                 ;INC17:
31 03164 111405          INC 0,2,SNR        ;AC0=37777+1 AND BE NON ZERO
32 03165 063077          HALTE              ;INC RESULT SHD=40000
33 03166 155000          MOV 2,3
34 03167 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
35 03170 174004          COM 3,3,SZR        ;THEN 0
36 03171 063077          HALTE
37 03172 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
38 03173 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
39                       INCTS 18,1,0,77777,100000
40                    ;AC0=77777 COMING INTO TEST,+1=AC1=100000
41                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
42                    ;BIT1 INTO BIT0 WITH RESULT=AC1
43                 ;INC18:
44 03174 111405          INC 0,2,SNR        ;AC0=77777+1 AND BE NON ZERO
45 03175 063077          HALTE              ;INC RESULT SHD=100000
46 03176 155000          MOV 2,3
47 03177 136000          ADC 1,3            ;ADC SUM OF 1+3 SHD=-1
48 03200 174004          COM 3,3,SZR        ;THEN 0
49 03201 063077          HALTE
50 03202 101140          MOVOL 0,0          ;SET UP CONSTANTS NEXT TEST
51 03203 125120          MOVZL 1,1          ;SET UP RESULT NEXT TEST
```

```
10063 N3LGC
01
02                ;TEST INC OF -1 AC TO=0 WITH CRY COMP 0 TO 1
03 03204 102040 INC20:  ADCO 0,0
04 03205 101424         INCZ 0,0,SZR
05 03206 063077         HALTE           ;INC=1 DID NOT=0
06 03207 101003         MOV 0,0,SNC
07 03210 063077         HALTE           ;CRY OUT DID NOT COM 0 TO 1
08                ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
09
10
11                ;TEST INC OF=1 AC TO=0 AND CRY TO COMP 1 TO 0
12
13 03211 102020 INC21:  ADCZ 0,0
14 03212 101444         INCO 0,0,SZR
15 03213 063077         HALTE           ;INC=1 DID NOT=0
16 03214 101002         MOV 0,0,SZC
17 03215 063077         HALTE           ;CRY OUT DID NOT COM 1 TO 0
18                ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALTE
```

```
10064 N3LGC
01
02                ;FIRST USE OF NEG INSTRUCTION
03                ;NEG=1 TO =1 TO VERIFY CORRECT INSTR REF
04
05 03216 102000 NEG00:  ADC 0,0
06 03217 100405         NEG 0,0,SNR
07 03220 063077         HALTE           ;NEG MAY=COM+INC+SUB
08 03221 105224         MOVZR 0,1,SZR
09 03222 063077         HALTE           ;NEG OF =1 SOMETHING OTHER THAN +1
10                ;EXAMINE AC0 FOR ALU ERROR
11
12                ;THE NEGATION OF +1 SHD=-1
13
14 03223 102000 NEG01:  ADC 0,0         ;SET=-1
15 03224 100140         COMOL 0,0       ;MAKES AC0=1
16 03225 100405         NEG 0,0,SNR     ;MAKES AC0=-1
17 03226 063077         HALTE           ;(?)
18 03227 104004         COM 0,1,SZR     ;RESULT REALLY=+1
19 03230 063077         HALTE           ;NEG OF +1 SOMETHING OTHER THAN -1
20                ;EXAMINE AC0 FOR ALU ERROR OR AC1 FOR COM
21
22                ;DEFINE MACRO FOR FURTHER TESTS OF NEG
23                      .MACRO NEGTS
24                ;AC0=^4 COMING INTO TEST IT SHD NEG TO=^5
25                ;NEG IS EQUIVALENT TO COM+INC
26                ;CARRY IS THROUGH BIT ^2 BUT SHOULD STORE AT BIT ^3
27                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
28              ;NEG^1:
29                      NEG 0,2,SNR     ;^4+1 SHD=^5
30                      HALTE           ;CARRY WENT THROUGH BIT ^3
31                      MOV 2,3
32                      ADC 1,3         ;AC1=COM OF ^5 AC3 SHD=-1
33                      COM 3,3,SZR     ;RESULT COM =1 SHD=0
34                      HALTE           ;EXAM AC2 FOR ALU ERR SHD=^5
35                ;AC2=^5 IT SHOULD NEG AGAIN TO=AC0 OR ^4
36              ;NG^1A:
37                      NEG 2,3         ;AC2=^5 3 SHD=^4
38                      ADC 0,3         ;AC3 SHD NOW=-1
39                      COM 3,2,SZR     ;AND ITS COM=0
40                      HALTE           ;^5 DID NOT NEG TO ^4
41                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF ^4
42                      MOVZL 0,0
43                      MOVZL 1,1       ;SET UP NEXT TEST
44              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
45              %
```

```
10065 N3LGC
01
02                      ;SET UP NEG TESTS
03                      ;START WITH AC0=1 AC1=0
04                      ;2ND TEST AC0=2 AC1=1
05
06 03231 126000                 ADC 1,1         ;SET UP AC1=-1
07 03232 120140                 COMOL 1,0       ;AC0=+1
08
09                              NEGTS 03,ALUCRY,15,1,177777
10                      ;AC0=1 COMING INTO TEST IT SHD NEG TO=177777
11                      ;NEG IS EQUIVALENT TO COM+INC
12                      ;CARRY IS THROUGH BIT ALUCRY BUT SHOULD STORE AT BIT 15
13                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
14                    ;NEG03:
15 03233 110405                 NEG 0,2,SNR     ;1+1 SHD=177777
16 03234 063077                 HALTE           ;CARRY WENT THROUGH BIT 15
17 03235 155000                 MOV 2,3
18 03236 136000                 ADC 1,3         ;AC1=COM OF 177777 AC3 SHD=-1
19 03237 174004                 COM 3,3,SZR     ;RESULT COM =1 SHD=0
20 03240 063077                 HALTE           ;EXAM AC2 FOR ALU ERR SHD=177777
21                      ;AC2=177777 IT SHOULD NEG AGAIN TO=AC0 OR 1
22                    ;NG03A:
23 03241 154400                 NEG 2,3         ;AC2=177777 3 SHD=1
24 03242 116000                 ADC 0,3         ;AC3 SHD NOW=-1
25 03243 170004                 COM 3,2,SZR     ;AND ITS COM=0
26 03244 063077                 HALTE           ;177777 DID NOT NEG TO 1
27                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 1
28 03245 101120                 MOVZL 0,0
29 03246 125120                 MOVZL 1,1       ;SET UP NEXT TEST
30                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
31                              NEGTS 04,15,14,2,177776
32                      ;AC0=2 COMING INTO TEST IT SHD NEG TO=177776
33                      ;NEG IS EQUIVALENT TO COM+INC
34                      ;CARRY IS THROUGH BIT 15 BUT SHOULD STORE AT BIT 14
35                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
36                    ;NEG04:
37 03247 110405                 NEG 0,2,SNR     ;2+1 SHD=177776
38 03250 063077                 HALTE           ;CARRY WENT THROUGH BIT 14
39 03251 155000                 MOV 2,3
40 03252 136000                 ADC 1,3         ;AC1=COM OF 177776 AC3 SHD=-1
41 03253 174004                 COM 3,3,SZR     ;RESULT COM =1 SHD=0
42 03254 063077                 HALTE           ;EXAM AC2 FOR ALU ERR SHD=177776
43                      ;AC2=177776 IT SHOULD NEG AGAIN TO=AC0 OR 2
44                    ;NG04A:
45 03255 154400                 NEG 2,3         ;AC2=177776 3 SHD=2
46 03256 116000                 ADC 0,3         ;AC3 SHD NOW=-1
47 03257 170004                 COM 3,2,SZR     ;AND ITS COM=0
48 03260 063077                 HALTE           ;177776 DID NOT NEG TO 2
49                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2
50 03261 101120                 MOVZL 0,0
51 03262 125120                 MOVZL 1,1       ;SET UP NEXT TEST
52                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
53                              NEGTS 05,14,13,4,177774
54                      ;AC0=4 COMING INTO TEST IT SHD NEG TO=177774
55                      ;NEG IS EQUIVALENT TO COM+INC
56                      ;CARRY IS THROUGH BIT 14 BUT SHOULD STORE AT BIT 13
57                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
58                    ;NEG05:
59 03263 110405                 NEG 0,2,SNR     ;4+1 SHD=177774
60 03264 063077                 HALTE           ;CARRY WENT THROUGH BIT 13
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```
 0066 N3LGC
01 03265 155000                 MOV 2,3
02 03266 136000                 ADC 1,3         ;AC1=COM OF 177774 AC3 SHD=-1
03 03267 174004                 COM 3,3,SZR     ;RESULT COM =1 SHD=0
04 03270 063077                 HALTE           ;EXAM AC2 FOR ALU ERR SHD=177774
05                      ;AC2=177774 IT SHOULD NEG AGAIN TO=AC0 OR 4
06                    ;NG05A:
07 03271 154400                 NEG 2,3         ;AC2=177774 3 SHD=4
08 03272 116000                 ADC 0,3         ;AC3 SHD NOW=-1
09 03273 170004                 COM 3,2,SZR     ;AND ITS COM=0
10 03274 063077                 HALTE           ;177774 DID NOT NEG TO 4
11                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4
12 03275 101120                 MOVZL 0,0
13 03276 125120                 MOVZL 1,1       ;SET UP NEXT TEST
14                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
15                              NEGTS 06,13,12,10,177770
16                      ;AC0=10 COMING INTO TEST IT SHD NEG TO=177770
17                      ;NEG IS EQUIVALENT TO COM+INC
18                      ;CARRY IS THROUGH BIT 13 BUT SHOULD STORE AT BIT 12
19                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
20                    ;NEG06:
21 03277 110405                 NEG 0,2,SNR     ;10+1 SHD=177770
22 03300 063077                 HALTE           ;CARRY WENT THROUGH BIT 12
23 03301 155000                 MOV 2,3
24 03302 136000                 ADC 1,3         ;AC1=COM OF 177770 AC3 SHD=-1
25 03303 174004                 COM 3,3,SZR     ;RESULT COM =1 SHD=0
26 03304 063077                 HALTE           ;EXAM AC2 FOR ALU ERR SHD=177770
27                      ;AC2=177770 IT SHOULD NEG AGAIN TO=AC0 OR 10
28                    ;NG06A:
29 03305 154400                 NEG 2,3         ;AC2=177770 3 SHD=10
30 03306 116000                 ADC 0,3         ;AC3 SHD NOW=-1
31 03307 170004                 COM 3,2,SZR     ;AND ITS COM=0
32 03310 063077                 HALTE           ;177770 DID NOT NEG TO 10
33                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10
34 03311 101120                 MOVZL 0,0
35 03312 125120                 MOVZL 1,1       ;SET UP NEXT TEST
36                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
37                              NEGTS 07,12,11,20,177760
38                      ;AC0=20 COMING INTO TEST IT SHD NEG TO=177760
39                      ;NEG IS EQUIVALENT TO COM+INC
40                      ;CARRY IS THROUGH BIT 12 BUT SHOULD STORE AT BIT 11
41                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
42                    ;NEG07:
43 03313 110405                 NEG 0,2,SNR     ;20+1 SHD=177760
44 03314 063077                 HALTE           ;CARRY WENT THROUGH BIT 11
45 03315 155000                 MOV 2,3
46 03316 136000                 ADC 1,3         ;AC1=COM OF 177760 AC3 SHD=-1
47 03317 174004                 COM 3,3,SZR     ;RESULT COM =1 SHD=0
48 03320 063077                 HALTE           ;EXAM AC2 FOR ALU ERR SHD=177760
49                      ;AC2=177760 IT SHOULD NEG AGAIN TO=AC0 OR 20
50                    ;NG07A:
51 03321 154400                 NEG 2,3         ;AC2=177760 3 SHD=20
52 03322 116000                 ADC 0,3         ;AC3 SHD NOW=-1
53 03323 170004                 COM 3,2,SZR     ;AND ITS COM=0
54 03324 063077                 HALTE           ;177760 DID NOT NEG TO 20
55                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20
56 03325 101120                 MOVZL 0,0
57 03326 125120                 MOVZL 1,1       ;SET UP NEXT TEST
58                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
59                              NEGTS 08,11,10,40,177740
60                      ;AC0=40 COMING INTO TEST IT SHD NEG TO=177740
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0067 N3LGC
01                ;NEG IS EQUIVALENT TO COM+INC
02                ;CARRY IS THROUGH BIT 11 BUT SHOULD STORE AT BIT 10
03                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
04              ;NEG08:
05 03327 110405         NEG 0,2,SNR       ;40+1 SHD=177740
06 03330 063077         HALTE             ;CARRY WENT THROUGH BIT 10
07 03331 155000         MOV 2,3
08 03332 136000         ADC 1,3           ;AC1=COM OF 177740 AC3 SHD=-1
09 03333 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
10 03334 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=177740
11                ;AC2=177740 IT SHOULD NEG AGAIN TO=AC0 OR 40
12              ;NG08A:
13 03335 154400         NEG 2,3           ;AC2=177740 3 SHD=40
14 03336 116000         ADC 0,3           ;AC3 SHD NOW=-1
15 03337 170004         COM 3,2,SZR       ;AND ITS COM=0
16 03340 063077         HALTE             ;177740 DID NOT NEG TO 40
17                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40
18 03341 101120         MOVZL 0,0
19 03342 125120         MOVZL 1,1         ;SET UP NEXT TEST
20              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
21                      NEGTS 09,10,9,100,177700
22                ;AC0=100 COMING INTO TEST IT SHD NEG TO=177700
23                ;NEG IS EQUIVALENT TO COM+INC
24                ;CARRY IS THROUGH BIT 10 BUT SHOULD STORE AT BIT 9
25                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
26              ;NEG09:
27 03343 110405         NEG 0,2,SNR       ;100+1 SHD=177700
28 03344 063077         HALTE             ;CARRY WENT THROUGH BIT 9
29 03345 155000         MOV 2,3
30 03346 136000         ADC 1,3           ;AC1=COM OF 177700 AC3 SHD=-1
31 03347 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
32 03350 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=177700
33                ;AC2=177700 IT SHOULD NEG AGAIN TO=AC0 OR 100
34              ;NG09A:
35 03351 154400         NEG 2,3           ;AC2=177700 3 SHD=100
36 03352 116000         ADC 0,3           ;AC3 SHD NOW=-1
37 03353 170004         COM 3,2,SZR       ;AND ITS COM=0
38 03354 063077         HALTE             ;177700 DID NOT NEG TO 100
39                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
40 03355 101120         MOVZL 0,0
41 03356 125120         MOVZL 1,1         ;SET UP NEXT TEST
42              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
43                      NEGTS 10,9,8,200,177600
44                ;AC0=200 COMING INTO TEST IT SHD NEG TO=177600
45                ;NEG IS EQUIVALENT TO COM+INC
46                ;CARRY IS THROUGH BIT 9 BUT SHOULD STORE AT BIT 8
47                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
48              ;NEG10:
49 03357 110405         NEG 0,2,SNR       ;200+1 SHD=177600
50 03360 063077         HALTE             ;CARRY WENT THROUGH BIT 8
51 03361 155000         MOV 2,3
52 03362 136000         ADC 1,3           ;AC1=COM OF 177600 AC3 SHD=-1
53 03363 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
54 03364 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=177600
55                ;AC2=177600 IT SHOULD NEG AGAIN TO=AC0 OR 200
56              ;NG10A:
57 03365 154400         NEG 2,3           ;AC2=177600 3 SHD=200
58 03366 116000         ADC 0,3           ;AC3 SHD NOW=-1
59 03367 170004         COM 3,2,SZR       ;AND ITS COM=0
60 03370 063077         HALTE             ;177600 DID NOT NEG TO 200
```

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0068 N3LGC
01                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 200
02 03371 101120         MOVZL 0,0
03 03372 125120         MOVZL 1,1         ;SET UP NEXT TEST
04              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
05                      NEGTS 11,8,7,400,177400
06                ;AC0=400 COMING INTO TEST IT SHD NEG TO=177400
07                ;NEG IS EQUIVALENT TO COM+INC
08                ;CARRY IS THROUGH BIT 8 BUT SHOULD STORE AT BIT 7
09                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
10              ;NEG11:
11 03373 110405         NEG 0,2,SNR       ;400+1 SHD=177400
12 03374 063077         HALTE             ;CARRY WENT THROUGH BIT 7
13 03375 155000         MOV 2,3
14 03376 136000         ADC 1,3           ;AC1=COM OF 177400 AC3 SHD=-1
15 03377 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
16 03400 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=177400
17                ;AC2=177400 IT SHOULD NEG AGAIN TO=AC0 OR 400
18              ;NG11A:
19 03401 154400         NEG 2,3           ;AC2=177400 3 SHD=400
20 03402 116000         ADC 0,3           ;AC3 SHD NOW=-1
21 03403 170004         COM 3,2,SZR       ;AND ITS COM=0
22 03404 063077         HALTE             ;177400 DID NOT NEG TO 400
23                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 400
24 03405 101120         MOVZL 0,0
25 03406 125120         MOVZL 1,1         ;SET UP NEXT TEST
26              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
27                      NEGTS 12,7,6,100,177000
28                ;AC0=100 COMING INTO TEST IT SHD NEG TO=177000
29                ;NEG IS EQUIVALENT TO COM+INC
30                ;CARRY IS THROUGH BIT 7 BUT SHOULD STORE AT BIT 6
31                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
32              ;NEG12:
33 03407 110405         NEG 0,2,SNR       ;100+1 SHD=177000
34 03410 063077         HALTE             ;CARRY WENT THROUGH BIT 6
35 03411 155000         MOV 2,3
36 03412 136000         ADC 1,3           ;AC1=COM OF 177000 AC3 SHD=-1
37 03413 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
38 03414 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=177000
39                ;AC2=177000 IT SHOULD NEG AGAIN TO=AC0 OR 100
40              ;NG12A:
41 03415 154400         NEG 2,3           ;AC2=177000 3 SHD=100
42 03416 116000         ADC 0,3           ;AC3 SHD NOW=-1
43 03417 170004         COM 3,2,SZR       ;AND ITS COM=0
44 03420 063077         HALTE             ;177000 DID NOT NEG TO 100
45                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
46 03421 101120         MOVZL 0,0
47 03422 125120         MOVZL 1,1         ;SET UP NEXT TEST
48              ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
49                      NEGTS 13,6,5,2000,176000
50                ;AC0=2000 COMING INTO TEST IT SHD NEG TO=176000
51                ;NEG IS EQUIVALENT TO COM+INC
52                ;CARRY IS THROUGH BIT 6 BUT SHOULD STORE AT BIT 5
53                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
54              ;NEG13:
55 03423 110405         NEG 0,2,SNR       ;2000+1 SHD=176000
56 03424 063077         HALTE             ;CARRY WENT THROUGH BIT 5
57 03425 155000         MOV 2,3
58 03426 136000         ADC 1,3           ;AC1=COM OF 176000 AC3 SHD=-1
59 03427 174004         COM 3,3,SZR       ;RESULT COM =1 SHD=0
60 03430 063077         HALTE             ;EXAM AC2 FOR ALU ERR SHD=176000
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```
0069 N3LGC
01                      ;AC2=176000 IT SHOULD NEG AGAIN TO=AC0 OR 2000
02                    ;NG13A:
03 03431 154400               NEG 2,3           ;AC2=176000 3 SHD=2000
04 03432 116000               ADC 0,3           ;AC3 SHD NOW=-1
05 03433 170004               COM 3,2,SZR       ;AND ITS COM=0
06 03434 063077               HALTE             ;176000 DID NOT NEG TO 2000
07                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2000
08 03435 101120               MOVZL 0,0
09 03436 125120               MOVZL 1,1         ;SET UP NEXT TEST
10                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
11                            NEGTS 14,5,4,4000,174000
12                      ;AC0=4000 COMING INTO TEST IT SHD NEG TO=174000
13                      ;NEG IS EQUIVALENT TO COM+INC
14                      ;CARRY IS THROUGH BIT 5 BUT SHOULD STORE AT BIT 4
15                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
16                    ;NEG14:
17 03437 110405               NEG 0,2,SNR       ;4000+1 SHD=174000
18 03440 063077               HALTE             ;CARRY WENT THROUGH BIT 4
19 03441 155000               MOV 2,3
20 03442 136000               ADC 1,3           ;AC1=COM OF 174000 AC3 SHD=-1
21 03443 174004               COM 3,3,SZR       ;RESULT COM =1 SHD=0
22 03444 063077               HALTE             ;EXAM AC2 FOR ALU ERR SHD=174000
23                      ;AC2=174000 IT SHOULD NEG AGAIN TO=AC0 OR 4000
24                    ;NG14A:
25 03445 154400               NEG 2,3           ;AC2=174000 3 SHD=4000
26 03446 116000               ADC 0,3           ;AC3 SHD NOW=-1
27 03447 170004               COM 3,2,SZR       ;AND ITS COM=0
28 03450 063077               HALTE             ;174000 DID NOT NEG TO 4000
29                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4000
30 03451 101120               MOVZL 0,0
31 03452 125120               MOVZL 1,1         ;SET UP NEXT TEST
32                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
33                            NEGTS 15,4,3,10000,170000
34                      ;AC0=10000 COMING INTO TEST IT SHD NEG TO=170000
35                      ;NEG IS EQUIVALENT TO COM+INC
36                      ;CARRY IS THROUGH BIT 4 BUT SHOULD STORE AT BIT 3
37                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
38                    ;NEG15:
39 03453 110405               NEG 0,2,SNR       ;10000+1 SHD=170000
40 03454 063077               HALTE             ;CARRY WENT THROUGH BIT 3
41 03455 155000               MOV 2,3
42 03456 136000               ADC 1,3           ;AC1=COM OF 170000 AC3 SHD=-1
43 03457 174004               COM 3,3,SZR       ;RESULT COM =1 SHD=0
44 03460 063077               HALTE             ;EXAM AC2 FOR ALU ERR SHD=170000
45                      ;AC2=170000 IT SHOULD NEG AGAIN TO=AC0 OR 10000
46                    ;NG15A:
47 03461 154400               NEG 2,3           ;AC2=170000 3 SHD=10000
48 03462 116000               ADC 0,3           ;AC3 SHD NOW=-1
49 03463 170004               COM 3,2,SZR       ;AND ITS COM=0
50 03464 063077               HALTE             ;170000 DID NOT NEG TO 10000
51                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10000
52 03465 101120               MOVZL 0,0
53 03466 125120               MOVZL 1,1         ;SET UP NEXT TEST
54                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
55                            NEGTS 16,3,1,20000,160000
56                      ;AC0=20000 COMING INTO TEST IT SHD NEG TO=160000
57                      ;NEG IS EQUIVALENT TO COM+INC
58                      ;CARRY IS THROUGH BIT 3 BUT SHOULD STORE AT BIT 1
59                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
60                    ;NEG16:
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0070 N3LGC
01 03467 110405               NEG 0,2,SNR       ;20000+1 SHD=160000
02 03470 063077               HALTE             ;CARRY WENT THROUGH BIT 1
03 03471 155000               MOV 2,3
04 03472 136000               ADC 1,3           ;AC1=COM OF 160000 AC3 SHD=-1
05 03473 174004               COM 3,3,SZR       ;RESULT COM =1 SHD=0
06 03474 063077               HALTE             ;EXAM AC2 FOR ALU ERR SHD=160000
07                      ;AC2=160000 IT SHOULD NEG AGAIN TO=AC0 OR 20000
08                    ;NG16A:
09 03475 154400               NEG 2,3           ;AC2=160000 3 SHD=20000
10 03476 116000               ADC 0,3           ;AC3 SHD NOW=-1
11 03477 170004               COM 3,2,SZR       ;AND ITS COM=0
12 03500 063077               HALTE             ;160000 DID NOT NEG TO 20000
13                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20000
14 03501 101120               MOVZL 0,0
15 03502 125120               MOVZL 1,1         ;SET UP NEXT TEST
16                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
17                            NEGTS 17,2,1,40000,140000
18                      ;AC0=40000 COMING INTO TEST IT SHD NEG TO=140000
19                      ;NEG IS EQUIVALENT TO COM+INC
20                      ;CARRY IS THROUGH BIT 2 BUT SHOULD STORE AT BIT 1
21                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
22                    ;NEG17:
23 03503 110405               NEG 0,2,SNR       ;40000+1 SHD=140000
24 03504 063077               HALTE             ;CARRY WENT THROUGH BIT 1
25 03505 155000               MOV 2,3
26 03506 136000               ADC 1,3           ;AC1=COM OF 140000 AC3 SHD=-1
27 03507 174004               COM 3,3,SZR       ;RESULT COM =1 SHD=0
28 03510 063077               HALTE             ;EXAM AC2 FOR ALU ERR SHD=140000
29                      ;AC2=140000 IT SHOULD NEG AGAIN TO=AC0 OR 40000
30                    ;NG17A:
31 03511 154400               NEG 2,3           ;AC2=140000 3 SHD=40000
32 03512 116000               ADC 0,3           ;AC3 SHD NOW=-1
33 03513 170004               COM 3,2,SZR       ;AND ITS COM=0
34 03514 063077               HALTE             ;140000 DID NOT NEG TO 40000
35                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40000
36 03515 101120               MOVZL 0,0
37 03516 125120               MOVZL 1,1         ;SET UP NEXT TEST
38                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
39                            NEGTS 18,1,0,100000,100000
40                      ;AC0=100000 COMING INTO TEST IT SHD NEG TO=100000
41                      ;NEG IS EQUIVALENT TO COM+INC
42                      ;CARRY IS THROUGH BIT 1 BUT SHOULD STORE AT BIT 0
43                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
44                    ;NEG18:
45 03517 110405               NEG 0,2,SNR       ;100000+1 SHD=100000
46 03520 063077               HALTE             ;CARRY WENT THROUGH BIT 0
47 03521 155000               MOV 2,3
48 03522 136000               ADC 1,3           ;AC1=COM OF 100000 AC3 SHD=-1
49 03523 174004               COM 3,3,SZR       ;RESULT COM =1 SHD=0
50 03524 063077               HALTE             ;EXAM AC2 FOR ALU ERR SHD=100000
51                      ;AC2=100000 IT SHOULD NEG AGAIN TO=AC0 OR 100000
52                    ;NG18A:
53 03525 154400               NEG 2,3           ;AC2=100000 3 SHD=100000
54 03526 116000               ADC 0,3           ;AC3 SHD NOW=-1
55 03527 170004               COM 3,2,SZR       ;AND ITS COM=0
56 03530 063077               HALTE             ;100000 DID NOT NEG TO 100000
57                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100000
58 03531 101120               MOVZL 0,0
59 03532 125120               MOVZL 1,1         ;SET UP NEXT TEST
60                    ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE IR13 AT SETTRAP AND GATE
```

```
 0071 N3LGC
01                ;AC0=0 COMING INTO TEST IT SHD NEG TO =0
02                ;CARRY IS THROUGH BIT 0 AND SHOULD COM CRY
03 03533 110404 NEG19:  NEG 0,2,SZR       ;-0+1=0
04 03534 063077         HALTE             ;SEE AC2 NOT=0
05 03535 155000         MOV 2,3
06 03536 136000         ADC 1,3
07 03537 174004         COM 3,3,SZR       ;SKP AC2 REALLY=0
08 03540 063077         HALTE             ;SEE AC2 SHD =0
09                ;AC2 =0 IT SHD NEGATE TO =0 IN AC3
10 03541 154400 NG19A:  NEG 2,3
11 03542 116000         ADC 0,3
12 03543 170004         COM 3,2,SZR
13 03544 063077         HALTE             ;0 DID NOT NEG TO 0
14                ;EXAMINE AC3 FOR ALU FAILURE SHD =-1 CREATED BY ADC OF 0
15
16                  ;NEGATING 0 SHOULD COMPLIMENT CRY 0 TO 1
17
18 03545 102000 NEG20:  ADC 0,0
19 03546 100040         COMO 0,0
20 03547 100423         NEGZ 0,0,SNC
21 03550 063077         HALTE             ;NEG 0 DID NOT SET CRY
22
23                  ;NEGATING 0 SHOULD COM CRY 1 TO 0
24
25 03551 102000 NEG21:  ADC 0,0
26 03552 100020         COMZ 0,0
27 03553 100442         NEGO 0,0,SZC
28 03554 063077         HALTE             ;NEG 0 DID NOT CLR CRY
```

```
;0072 N3LGC
01
02                  ;TEST FOR EXISTANCE OF SUB INSTRUCTION
03                  ;FIRST TIME FOR SUB
04
05 03555 102000 SUB00:  ADC 0,0           ;AC0=-1
06 03556 102404         SUB 0,0,SZR       ;SUB -1 FROM -1
07 03557 063077         HALTE             ;EXAMINE AC0 FOR ERR SHD=0
08                ;SUBTRACT +1 FROM +1 CHECK FOR 0 RESULT (2ND SUB)
09 03560 102000 SUB01:  ADC 0,0
10 03561 100405         NEG 0,0,SNR       ;SET AC0=+1
11 03562 063077         HALTE             ;SET UP FAILED AC0 SHD=+1
12 03563 102404         SUB 0,0,SZR       ;+1-+1 SHD=0
13 03564 063077         HALTE             ;SUB +1-+1 FAILED SEE AC0
14
15                  ;DEFINE SUBTRACT "SUB" TEST MACRO
16
17                      ,MACRO SUBTS
18                ;AC0=^A2 COMING INTO THIS TEST ^A2-^A2 SHOULD=0 RESULT
19                ;0-^A2 NEGATED-^A2 SHD=0 INTO AC3
20              ;SUB^A1:
21                      MOVO 0,1
22                      SUBZ 0,1,SZR
23                      HALTE             ;^A2-^A2 SEE AC1 SHD=0
24                      MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
25                      HALTE   ;AC0=^A2(?) CRY SHD=1
26                      ADC 2,2
27                      COM 2,2 ;MAKE AC2=0 FOR TEST
28                ;0-^A2 SHOULD=-^A2 NEGATED TO AC3
29                      SUB 0,2           ;0-^A2
30                      NEGZ 2,3          ;NEGATED SHD=^A2
31                      SUBO 0,3,SZR      ;^A2-^A2 SHD=0 AGAIN
32                      HALTE
33                      MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
34                      HALTE             ;CRY OUT FAILED
35                      MOVZL 0,0         ;SET UP NEXT TEST
36              %
37
38                  ;SET UP SUBTRACT TESTS
39 03565 102000         ADC 0,0
40 03566 100140         COMOL 0,0
```

```
10073 N3LGC
01
02                      SUBTS 02,1
03                    ;AC0=1 COMING INTO THIS TEST 1-1 SHOULD=0 RESULT
04                    ;0-1 NEGATED-1 SHD=0 INTO AC3
05                  ;SUB02:
06 03567 105040             MOVO 0,1
07 03570 106424             SUBZ 0,1,SZR
08 03571 063077             HALTE           ;1-1 SEE AC1 SHD=0
09 03572 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
10 03573 063077             HALTE   ;AC0=1(?) CRY SHD=1
11 03574 152000             ADC 2,2
12 03575 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
13                    ;0-1 SHOULD=-1 NEGATED TO AC3
14 03576 112400             SUB 0,2         ;0-1
15 03577 154420             NEGZ 2,3        ;NEGATED SHD=1
16 03600 116444             SUBO 0,3,SZR    ;1-1 SHD=0 AGAIN
17 03601 063077             HALTE
18 03602 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
19 03603 063077             HALTE           ;CRY OUT FAILED
20 03604 101120             MOVZL 0,0       ;SET UP NEXT TEST
21                          SUBTS 03,2
22                    ;AC0=2 COMING INTO THIS TEST 2-2 SHOULD=0 RESULT
23                    ;0-2 NEGATED-2 SHD=0 INTO AC3
24                  ;SUB03:
25 03605 105040             MOVO 0,1
26 03606 106424             SUBZ 0,1,SZR
27 03607 063077             HALTE           ;2-2 SEE AC1 SHD=0
28 03610 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
29 03611 063077             HALTE   ;AC0=2(?) CRY SHD=1
30 03612 152000             ADC 2,2
31 03613 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
32                    ;0-2 SHOULD=-2 NEGATED TO AC3
33 03614 112400             SUB 0,2         ;0-2
34 03615 154420             NEGZ 2,3        ;NEGATED SHD=2
35 03616 116444             SUBO 0,3,SZR    ;2-2 SHD=0 AGAIN
36 03617 063077             HALTE
37 03620 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
38 03621 063077             HALTE           ;CRY OUT FAILED
39 03622 101120             MOVZL 0,0       ;SET UP NEXT TEST
40                          SUBTS 04,4
41                    ;AC0=4 COMING INTO THIS TEST 4-4 SHOULD=0 RESULT
42                    ;0-4 NEGATED-4 SHD=0 INTO AC3
43                  ;SUB04:
44 03623 105040             MOVO 0,1
45 03624 106424             SUBZ 0,1,SZR
46 03625 063077             HALTE           ;4-4 SEE AC1 SHD=0
47 03626 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
48 03627 063077             HALTE   ;AC0=4(?) CRY SHD=1
49 03630 152000             ADC 2,2
50 03631 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
51                    ;0-4 SHOULD=-4 NEGATED TO AC3
52 03632 112400             SUB 0,2         ;0-4
53 03633 154420             NEGZ 2,3        ;NEGATED SHD=4
54 03634 116444             SUBO 0,3,SZR    ;4-4 SHD=0 AGAIN
55 03635 063077             HALTE
56 03636 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
57 03637 063077             HALTE           ;CRY OUT FAILED
58 03640 101120             MOVZL 0,0       ;SET UP NEXT TEST
59                          SUBTS 05,10
60                    ;AC0=10 COMING INTO THIS TEST 10-10 SHOULD=0 RESULT
```

```
0074 N3LGC
01                    ;0-10 NEGATED-10 SHD=0 INTO AC3
02                  ;SUB05:
03 03641 105040             MOVO 0,1
04 03642 106424             SUBZ 0,1,SZR
05 03643 063077             HALTE           ;10-10 SEE AC1 SHD=0
06 03644 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
07 03645 063077             HALTE   ;AC0=10(?) CRY SHD=1
08 03646 152000             ADC 2,2
09 03647 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
10                    ;0-10 SHOULD=-10 NEGATED TO AC3
11 03650 112400             SUB 0,2         ;0-10
12 03651 154420             NEGZ 2,3        ;NEGATED SHD=10
13 03652 116444             SUBO 0,3,SZR    ;10-10 SHD=0 AGAIN
14 03653 063077             HALTE
15 03654 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
16 03655 063077             HALTE           ;CRY OUT FAILED
17 03656 101120             MOVZL 0,0       ;SET UP NEXT TEST
18                          SUBTS 06,20
19                    ;AC0=20 COMING INTO THIS TEST 20-20 SHOULD=0 RESULT
20                    ;0-20 NEGATED-20 SHD=0 INTO AC3
21                  ;SUB06:
22 03657 105040             MOVO 0,1
23 03660 106424             SUBZ 0,1,SZR
24 03661 063077             HALTE           ;20-20 SEE AC1 SHD=0
25 03662 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
26 03663 063077             HALTE   ;AC0=20(?) CRY SHD=1
27 03664 152000             ADC 2,2
28 03665 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
29                    ;0-20 SHOULD=-20 NEGATED TO AC3
30 03666 112400             SUB 0,2         ;0-20
31 03667 154420             NEGZ 2,3        ;NEGATED SHD=20
32 03670 116444             SUBO 0,3,SZR    ;20-20 SHD=0 AGAIN
33 03671 063077             HALTE
34 03672 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
35 03673 063077             HALTE           ;CRY OUT FAILED
36 03674 101120             MOVZL 0,0       ;SET UP NEXT TEST
37                          SUBTS 07,40
38                    ;AC0=40 COMING INTO THIS TEST 40-40 SHOULD=0 RESULT
39                    ;0-40 NEGATED-40 SHD=0 INTO AC3
40                  ;SUB07:
41 03675 105040             MOVO 0,1
42 03676 106424             SUBZ 0,1,SZR
43 03677 063077             HALTE           ;40-40 SEE AC1 SHD=0
44 03700 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
45 03701 063077             HALTE   ;AC0=40(?) CRY SHD=1
46 03702 152000             ADC 2,2
47 03703 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
48                    ;0-40 SHOULD=-40 NEGATED TO AC3
49 03704 112400             SUB 0,2         ;0-40
50 03705 154420             NEGZ 2,3        ;NEGATED SHD=40
51 03706 116444             SUBO 0,3,SZR    ;40-40 SHD=0 AGAIN
52 03707 063077             HALTE
53 03710 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
54 03711 063077             HALTE           ;CRY OUT FAILED
55 03712 101120             MOVZL 0,0       ;SET UP NEXT TEST
56                          SUBTS 08,100
57                    ;AC0=100 COMING INTO THIS TEST 100-100 SHOULD=0 RESULT
58                    ;0-100 NEGATED-100 SHD=0 INTO AC3
59                  ;SUB08:
60 03713 105040             MOVO 0,1
```

```
 0075 N3LGC
01 03714 106424          SUBZ 0,1,SZR
02 03715 063077          HALTE              ;100-100 SEE AC1 SHD=0
03 03716 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
04 03717 063077          HALTE    ;AC0=100(?) CRY SHD=1
05 03720 152000          ADC 2,2
06 03721 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
07                    ;0-100 SHOULD=-100 NEGATED TO AC3
08 03722 112400          SUB 0,2            ;0-100
09 03723 154420          NEGZ 2,3           ;NEGATED SHD=100
10 03724 116444          SUBO 0,3,SZR       ;100-100 SHD=0 AGAIN
11 03725 063077          HALTE
12 03726 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
13 03727 063077          HALTE              ;CRY OUT FAILED
14 03730 101120          MOVZL 0,0          ;SET UP NEXT TEST
15                       SUBTS 09,200
16                  ;AC0=200 COMING INTO THIS TEST 200-200 SHOULD=0 RESULT
17                  ;0-200 NEGATED-200 SHD=0 INTO AC3
18                ;SUB09:
19 03731 105040          MOVO 0,1
20 03732 106424          SUBZ 0,1,SZR
21 03733 063077          HALTE              ;200-200 SEE AC1 SHD=0
22 03734 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
23 03735 063077          HALTE    ;AC0=200(?) CRY SHD=1
24 03736 152000          ADC 2,2
25 03737 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
26                    ;0-200 SHOULD=-200 NEGATED TO AC3
27 03740 112400          SUB 0,2            ;0-200
28 03741 154420          NEGZ 2,3           ;NEGATED SHD=200
29 03742 116444          SUBO 0,3,SZR       ;200-200 SHD=0 AGAIN
30 03743 063077          HALTE
31 03744 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
32 03745 063077          HALTE              ;CRY OUT FAILED
33 03746 101120          MOVZL 0,0          ;SET UP NEXT TEST
34                       SUBTS 10,400
35                  ;AC0=400 COMING INTO THIS TEST 400-400 SHOULD=0 RESULT
36                  ;0-400 NEGATED-400 SHD=0 INTO AC3
37                ;SUB10:
38 03747 105040          MOVO 0,1
39 03750 106424          SUBZ 0,1,SZR
40 03751 063077          HALTE              ;400-400 SEE AC1 SHD=0
41 03752 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
42 03753 063077          HALTE    ;AC0=400(?) CRY SHD=1
43 03754 152000          ADC 2,2
44 03755 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
45                    ;0-400 SHOULD=-400 NEGATED TO AC3
46 03756 112400          SUB 0,2            ;0-400
47 03757 154420          NEGZ 2,3           ;NEGATED SHD=400
48 03760 116444          SUBO 0,3,SZR       ;400-400 SHD=0 AGAIN
49 03761 063077          HALTE
50 03762 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
51 03763 063077          HALTE              ;CRY OUT FAILED
52 03764 101120          MOVZL 0,0          ;SET UP NEXT TEST
53                       SUBTS 11,1000
54                  ;AC0=1000 COMING INTO THIS TEST 1000-1000 SHOULD=0 RESULT
55                  ;0-1000 NEGATED-1000 SHD=0 INTO AC3
56                ;SUB11:
57 03765 105040          MOVO 0,1
58 03766 106424          SUBZ 0,1,SZR
59 03767 063077          HALTE              ;1000-1000 SEE AC1 SHD=0
60 03770 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
```

```
 0076 N3LGC
01 03771 063077          HALTE    ;AC0=1000(?) CRY SHD=1
02 03772 152000          ADC 2,2
03 03773 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
04                    ;0-1000 SHOULD=-1000 NEGATED TO AC3
05 03774 112400          SUB 0,2            ;0-1000
06 03775 154420          NEGZ 2,3           ;NEGATED SHD=1000
07 03776 116444          SUBO 0,3,SZR       ;1000-1000 SHD=0 AGAIN
08 03777 063077          HALTE
09 04000 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
10 04001 063077          HALTE              ;CRY OUT FAILED
11 04002 101120          MOVZL 0,0          ;SET UP NEXT TEST
12                       SUBTS 12,2000
13                  ;AC0=2000 COMING INTO THIS TEST 2000-2000 SHOULD=0 RESULT
14                  ;0-2000 NEGATED-2000 SHD=0 INTO AC3
15                ;SUB12:
16 04003 105040          MOVO 0,1
17 04004 106424          SUBZ 0,1,SZR
18 04005 063077          HALTE              ;2000-2000 SEE AC1 SHD=0
19 04006 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
20 04007 063077          HALTE    ;AC0=2000(?) CRY SHD=1
21 04010 152000          ADC 2,2
22 04011 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
23                    ;0-2000 SHOULD=-2000 NEGATED TO AC3
24 04012 112400          SUB 0,2            ;0-2000
25 04013 154420          NEGZ 2,3           ;NEGATED SHD=2000
26 04014 116444          SUBO 0,3,SZR       ;2000-2000 SHD=0 AGAIN
27 04015 063077          HALTE
28 04016 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
29 04017 063077          HALTE              ;CRY OUT FAILED
30 04020 101120          MOVZL 0,0          ;SET UP NEXT TEST
31                       SUBTS 13,4000
32                  ;AC0=4000 COMING INTO THIS TEST 4000-4000 SHOULD=0 RESULT
33                  ;0-4000 NEGATED-4000 SHD=0 INTO AC3
34                ;SUB13:
35 04021 105040          MOVO 0,1
36 04022 106424          SUBZ 0,1,SZR
37 04023 063077          HALTE              ;4000-4000 SEE AC1 SHD=0
38 04024 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
39 04025 063077          HALTE    ;AC0=4000(?) CRY SHD=1
40 04026 152000          ADC 2,2
41 04027 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
42                    ;0-4000 SHOULD=-4000 NEGATED TO AC3
43 04030 112400          SUB 0,2            ;0-4000
44 04031 154420          NEGZ 2,3           ;NEGATED SHD=4000
45 04032 116444          SUBO 0,3,SZR       ;4000-4000 SHD=0 AGAIN
46 04033 063077          HALTE
47 04034 101002          MOV 0,0,SZC        ;CRY SHD COMP 1 TO 0
48 04035 063077          HALTE              ;CRY OUT FAILED
49 04036 101120          MOVZL 0,0          ;SET UP NEXT TEST
50                       SUBTS 14,10000
51                  ;AC0=10000 COMING INTO THIS TEST 10000-10000 SHOULD=0 RESULT
52                  ;0-10000 NEGATED-10000 SHD=0 INTC AC3
53                ;SUB14:
54 04037 105040          MOVO 0,1
55 04040 106424          SUBZ 0,1,SZR
56 04041 063077          HALTE              ;10000-10000 SEE AC1 SHD=0
57 04042 101007          MOV 0,0,SBN        ;0 CRY SHD =1 FROM CRYOUT
58 04043 063077          HALTE    ;AC0=10000(?) CRY SHD=1
59 04044 152000          ADC 2,2
60 04045 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
```

```
 0077 N3LGC
01                      ;0-10000 SHOULD=-10000 NEGATED TO AC3
02 04046 112400         SUB 0,2         ;0-10000
03 04047 154420         NEGZ 2,3        ;NEGATED SHD=10000
04 04050 116444         SUBO 0,3,SZR    ;10000-10000 SHD=0 AGAIN
05 04051 063077         HALTE
06 04052 101002         MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
07 04053 063077         HALTE           ;CRY OUT FAILED
08 04054 101120         MOVZL 0,0       ;SET UP NEXT TEST
09                      SUBTS 15,20000
10                    ;AC0=20000 COMING INTO THIS TEST 20000-20000 SHOULD=0 RESULT
11                    ;0-20000 NEGATED-20000 SHD=0 INTO AC3
12                    ;SUB15:
13 04055 105040         MOVO 0,1
14 04056 106424         SUBZ 0,1,SZR
15 04057 063077         HALTE           ;20000-20000 SEE AC1 SHD=0
16 04060 101007         MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
17 04061 063077         HALTE   ;AC0=20000(?) CRY SHD=1
18 04062 152000         ADC 2,2
19 04063 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
20                    ;0-20000 SHOULD=-20000 NEGATED TO AC3
21 04064 112400         SUB 0,2         ;0-20000
22 04065 154420         NEGZ 2,3        ;NEGATED SHD=20000
23 04066 116444         SUBO 0,3,SZR    ;20000-20000 SHD=0 AGAIN
24 04067 063077         HALTE
25 04070 101002         MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
26 04071 063077         HALTE           ;CRY OUT FAILED
27 04072 101120         MOVZL 0,0       ;SET UP NEXT TEST
28                      SUBTS 16,40000
29                    ;AC0=40000 COMING INTO THIS TEST 40000-40000 SHOULD=0 RESULT
30                    ;0-40000 NEGATED-40000 SHD=0 INTO AC3
31                    ;SUB16:
32 04073 105040         MOVO 0,1
33 04074 106424         SUBZ 0,1,SZR
34 04075 063077         HALTE           ;40000-40000 SEE AC1 SHD=0
35 04076 101007         MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
36 04077 063077         HALTE   ;AC0=40000(?) CRY SHD=1
37 04100 152000         ADC 2,2
38 04101 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
39                    ;0-40000 SHOULD=-40000 NEGATED TO AC3
40 04102 112400         SUB 0,2         ;0-40000
41 04103 154420         NEGZ 2,3        ;NEGATED SHD=40000
42 04104 116444         SUBO 0,3,SZR    ;40000-40000 SHD=0 AGAIN
43 04105 063077         HALTE
44 04106 101002         MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
45 04107 063077         HALTE           ;CRY OUT FAILED
46 04110 101120         MOVZL 0,0       ;SET UP NEXT TEST
47                      SUBTS 17,100000
48                    ;AC0=100000 COMING INTO THIS TEST 100000-100000 SHOULD=0 RESUL
49                    ;0-100000 NEGATED-100000 SHD=0 INTO AC3
50                    ;SUB17:
51 04111 105040         MOVO 0,1
52 04112 106424         SUBZ 0,1,SZR
53 04113 063077         HALTE           ;100000-100000 SEE AC1 SHD=0
54 04114 101007         MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
55 04115 063077         HALTE   ;AC0=100000(?) CRY SHD=1
56 04116 152000         ADC 2,2
57 04117 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
58                    ;0-100000 SHOULD=-100000 NEGATED TO AC3
59 04120 112400         SUB 0,2         ;0-100000
60 04121 154420         NEGZ 2,3        ;NEGATED SHD=100000
```

```
 0078 N3LGC
01 04122 116444         SUBO 0,3,SZR    ;100000-100000 SHD=0 AGAIN
02 04123 063077         HALTE
03 04124 101002         MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
04 04125 063077         HALTE           ;CRY OUT FAILED
05 04126 101120         MOVZL 0,0       ;SET UP NEXT TEST
06
07
```

```
10079 N3LGC
01                      ;LOAD ACCUMULATOR TESTS FIRST MRI FIRST LDA
02 04127 102400 LDA00:  SUB 0,0
03 04130 105040         MOVO 0,1
04 04131 020055         LDA 0,K1        ;K1=1
05 04132 101005         MOV 0,0,SNR     ;AC IS AT LEAST NON ZERO
06 04133 063077         HALTE           ;DID NOT LOAD AC0 WITH+1
07 04134 105224         MOVZR 0,1,SZR   ;CHECK AC0 TO REALLY=+1
08 04135 063077         HALTE           ;SEE AC0 NOT=+1
09                      ;FIRST USE OF MRI OR LDA INSTRUCTION
10                      ;INCORRECT RESULT IN AC0 COULD BE DUE TO ANY OF
11                      ;A VARIETY OF PROBLEMS INCLUDING EFA
12                      ;IF IR0=1  LDA INSTRUCTION DECODES AS COMZ 1,0
13                      ;AC0 WILL=-1 AND CARRY WILL=0
14                      ;IF INSTRUCTION DECODES AS I/O IT'S NIO 40(AC0=0)
15                    ;IF DP2 DOESN'T SET THEN AC0 WILL = 0
16                      ;IF DATA IN AC0 IS OTHER THAN 0 OR -1 EFA
17
18                      ;DEFINE MACRO TO VERIFY LDA DOES NOT DISTURB OTHER AC'S
19                            .MACRO LDAT1
20                    ;LDA^1:
21                            ADC ^3,^3       ;SET AC^3=-1
22                            LDA ^2,K1       ;LOAD +1 TO AC^2
23                            COM ^3,^3,SZR   ;AC^3 SHD STILL=-1
24                            HALTE           ;LDA OF ^2 DIST AC^3
25                    %
26
27                            LDAT1 01,0,1
28                    ;LDA01:
29 04136 126000               ADC 1,1 ;SET AC1=-1
30 04137 020055               LDA 0,K1        ;LOAD +1 TO AC0
31 04140 124004               COM 1,1,SZR     ;AC1 SHD STILL=-1
32 04141 063077               HALTE           ;LDA OF 0 DIST AC1
33                            LDAT1 02,0,2
34                    ;LDA02:
35 04142 152000               ADC 2,2 ;SET AC2=-1
36 04143 020055               LDA 0,K1        ;LOAD +1 TO AC0
37 04144 150004               COM 2,2,SZR     ;AC2 SHD STILL=-1
38 04145 063077               HALTE           ;LDA OF 0 DIST AC2
39                            LDAT1 03,0,3
40                    ;LDA03:
41 04146 176000               ADC 3,3 ;SET AC3=-1
42 04147 020055               LDA 0,K1        ;LOAD +1 TO AC0
43 04150 174004               COM 3,3,SZR     ;AC3 SHD STILL=-1
44 04151 063077               HALTE           ;LDA OF 0 DIST AC3
45                            LDAT1 04,1,0
46                    ;LDA04:
47 04152 102000               ADC 0,0 ;SET AC0=-1
48 04153 024055               LDA 1,K1        ;LOAD +1 TO AC1
49 04154 100004               COM 0,0,SZR     ;AC0 SHD STILL=-1
50 04155 063077               HALTE           ;LDA OF 1 DIST AC0
51                            LDAT1 05,1,2
52                    ;LDA05:
53 04156 152000               ADC 2,2 ;SET AC2=-1
54 04157 024055               LDA 1,K1        ;LOAD +1 TO AC1
55 04160 150004               COM 2,2,SZR     ;AC2 SHD STILL=-1
56 04161 063077               HALTE           ;LDA OF 1 DIST AC2
57                            LDAT1 06,1,3
58                    ;LDA06:
59 04162 176000               ADC 3,3 ;SET AC3=-1
60 04163 024055               LDA 1,K1        ;LOAD +1 TO AC1
```

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 0080 N3LGC
01 04164 174004               COM 3,3,SZR     ;AC3 SHD STILL=-1
02 04165 063077               HALTE           ;LDA OF 1 DIST AC3
03                            LDAT1 07,2,0
04                    ;LDA07:
05 04166 102000               ADC 0,0 ;SET AC0=-1
06 04167 030055               LDA 2,K1        ;LOAD +1 TO AC2
07 04170 100004               COM 0,0,SZR     ;AC0 SHD STILL=-1
08 04171 063077               HALTE           ;LDA OF 2 DIST AC0
09                            LDAT1 08,2,1
10                    ;LDA08:
11 04172 126000               ADC 1,1 ;SET AC1=-1
12 04173 030055               LDA 2,K1        ;LOAD +1 TO AC2
13 04174 124004               COM 1,1,SZR     ;AC1 SHD STILL=-1
14 04175 063077               HALTE           ;LDA OF 2 DIST AC1
15                            LDAT1 09,2,3
16                    ;LDA09:
17 04176 176000               ADC 3,3 ;SET AC3=-1
18 04177 030055               LDA 2,K1        ;LOAD +1 TO AC2
19 04200 174004               COM 3,3,SZR     ;AC3 SHD STILL=-1
20 04201 063077               HALTE           ;LDA OF 2 DIST AC3
21                            LDAT1 10,3,0
22                    ;LDA10:
23 04202 102000               ADC 0,0 ;SET AC0=-1
24 04203 034055               LDA 3,K1        ;LOAD +1 TO AC3
25 04204 100004               COM 0,0,SZR     ;AC0 SHD STILL=-1
26 04205 063077               HALTE           ;LDA OF 3 DIST AC0
27                            LDAT1 11,3,1
28                    ;LDA11:
29 04206 126000               ADC 1,1 ;SET AC1=-1
30 04207 034055               LDA 3,K1        ;LOAD +1 TO AC3
31 04210 124004               COM 1,1,SZR     ;AC1 SHD STILL=-1
32 04211 063077               HALTE           ;LDA OF 3 DIST AC1
33                            LDAT1 12,3,2
34                    ;LDA12:
35 04212 152000               ADC 2,2 ;SET AC2=-1
36 04213 034055               LDA 3,K1        ;LOAD +1 TO AC3
37 04214 150004               COM 2,2,SZR     ;AC2 SHD STILL=-1
38 04215 063077               HALTE           ;LDA OF 3 DIST AC2
```

```
10081 N3LGC
01
02
03                  ;DEFINE MACRO TO FURTHER TEST LDA INST
04
05                          .MACRO LDAT2
06                  ;LDA^1:
07                          LDA 1,^2        ;GET ^3 TO AC1
08                          MOV 1,2
09                          SUB 0,2,SZR     ;AC0=^3 COMING INTO TEST
10                          HALTE
11                          MOVZL 0,0       ;POSITION FOR NEXT TEST
12                  %
13
14 04216 102525             SUBZL 0,0,SNR   ;SET UP LDA TESTS
15 04217 063077             HALTE           ;SET UP FAILED SEE AC0
16
17                          LDAT2 13,K1,1
18                  ;LDA13:
19 04220 024055             LDA 1,K1        ;GET 1 TO AC1
20 04221 131000             MOV 1,2
21 04222 112404             SUB 0,2,SZR     ;AC0=1 COMING INTO TEST
22 04223 063077             HALTE
23 04224 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
24                          LDAT2 14,K2,2
25                  ;LDA14:
26 04225 024056             LDA 1,K2        ;GET 2 TO AC1
27 04226 131000             MOV 1,2
28 04227 112404             SUB 0,2,SZR     ;AC0=2 COMING INTO TEST
29 04230 063077             HALTE
30 04231 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
31                          LDAT2 15,K4,4
32                  ;LDA15:
33 04232 024060             LDA 1,K4        ;GET 4 TO AC1
34 04233 131000             MOV 1,2
35 04234 112404             SUB 0,2,SZR     ;AC0=4 COMING INTO TEST
36 04235 063077             HALTE
37 04236 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
38                          LDAT2 16,K10,10
39                  ;LDA16:
40 04237 024064             LDA 1,K10       ;GET 10 TO AC1
41 04240 131000             MOV 1,2
42 04241 112404             SUB 0,2,SZR     ;AC0=10 COMING INTO TEST
43 04242 063077             HALTE
44 04243 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
45                          LDAT2 17,K20,20
46                  ;LDA17:
47 04244 024065             LDA 1,K20       ;GET 20 TO AC1
48 04245 131000             MOV 1,2
49 04246 112404             SUB 0,2,SZR     ;AC0=20 COMING INTO TEST
50 04247 063077             HALTE
51 04250 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
52                          LDAT2 18,K40,40
53                  ;LDA18:
54 04251 024066             LDA 1,K40       ;GET 40 TO AC1
55 04252 131000             MOV 1,2
56 04253 112404             SUB 0,2,SZR     ;AC0=40 COMING INTO TEST
57 04254 063077             HALTE
58 04255 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
59                          LDAT2 19,K100,100
60                  ;LDA19:
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 0082 N3LGC
01 04256 024067             LDA 1,K100      ;GET 100 TO AC1
02 04257 131000             MOV 1,2
03 04260 112404             SUB 0,2,SZR     ;AC0=100 COMING INTO TEST
04 04261 063077             HALTE
05 04262 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
06                          LDAT2 20,K200,200
07                  ;LDA20:
08 04263 024070             LDA 1,K200      ;GET 200 TO AC1
09 04264 131000             MOV 1,2
10 04265 112404             SUB 0,2,SZR     ;AC0=200 COMING INTO TEST
11 04266 063077             HALTE
12 04267 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
13                          LDAT2 21,K400,400
14                  ;LDA21:
15 04270 024072             LDA 1,K400      ;GET 400 TO AC1
16 04271 131000             MOV 1,2
17 04272 112404             SUB 0,2,SZR     ;AC0=400 COMING INTO TEST
18 04273 063077             HALTE
19 04274 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
20                          LDAT2 22,K1000,1000
21                  ;LDA22:
22 04275 024073             LDA 1,K1000     ;GET 1000 TO AC1
23 04276 131000             MOV 1,2
24 04277 112404             SUB 0,2,SZR     ;AC0=1000 COMING INTO TEST
25 04300 063077             HALTE
26 04301 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
27                          LDAT2 23,K2000,2000
28                  ;LDA23:
29 04302 024074             LDA 1,K2000     ;GET 2000 TO AC1
30 04303 131000             MOV 1,2
31 04304 112404             SUB 0,2,SZR     ;AC0=2000 COMING INTO TEST
32 04305 063077             HALTE
33 04306 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
34                          LDAT2 24,K4000,4000
35                  ;LDA24:
36 04307 024075             LDA 1,K4000     ;GET 4000 TO AC1
37 04310 131000             MOV 1,2
38 04311 112404             SUB 0,2,SZR     ;AC0=4000 COMING INTO TEST
39 04312 063077             HALTE
40 04313 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
41                          LDAT2 25,K10K,10000
42                  ;LDA25:
43 04314 024077             LDA 1,K10K      ;GET 10000 TO AC1
44 04315 131000             MOV 1,2
45 04316 112404             SUB 0,2,SZR     ;AC0=10000 COMING INTO TEST
46 04317 063077             HALTE
47 04320 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
48                          LDAT2 26,K20K,20000
49                  ;LDA26:
50 04321 024100             LDA 1,K20K      ;GET 20000 TO AC1
51 04322 131000             MOV 1,2
52 04323 112404             SUB 0,2,SZR     ;AC0=20000 COMING INTO TEST
53 04324 063077             HALTE
54 04325 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
55                          LDAT2 27,K40K,40000
56                  ;LDA27:
57 04326 024101             LDA 1,K40K      ;GET 40000 TO AC1
58 04327 131000             MOV 1,2
59 04330 112404             SUB 0,2,SZR     ;AC0=40000 COMING INTO TEST
60 04331 063077             HALTE
```

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 0083 N3LGC
01 04332 101120          MOVZL 0,0        ;POSITION FOR NEXT TEST
02                       LDAT2 28,K100K,100000
03               ;LDA28:
04 04333 024102          LDA 1,K100K      ;GET 100000 TO AC1
05 04334 131000          MOV 1,2
06 04335 112404          SUB 0,2,SZR      ;AC0=100000 COMING INTO TEST
07 04336 063077          HALTE
08 04337 101120          MOVZL 0,0        ;POSITION FOR NEXT TEST
```

```
 0084 N3LGC
01
02
03                 ;FIRST TEST OF BYTE SWAP "S"
04                 ;IR0,IR8,IR9 INTO DP1/D ROM
05
06 04340 102745 SWP00:  SUBOS 0,0,SNR
07 04341 101324          MOVZS 0,0,SZR    ;FIRST USE OF "S" AC0=0
08 04342 063077          HALTE            ;EXAMINE AC0 FOR "SWAP" ERR
09 04343 102323 SWP01:   ADCZS 0,0,SNC    ;CRY SHD REMAIN=0
10 04344 101302          MOVS 0,0,SZC     ;SAME
11 04345 063077          HALTE            ;SEE NEWCARRY SHIFTER
12 04346 102722 SWP02:   SUBZS 0,0,SZC    ;CRY SHD REMAIN=1
13 04347 101303          MOVS 0,0,SNC     ;SAME
14 04350 063077          HALTE            ;SEE NEWCARRY SHIFTER
15 04351 102725 SWP03:   SUBZS 0,0,SNR    ;A 1 IN CRY SHD NOT AFFECT "S"
16 04352 101344          MOVOS 0,0,SZR    ;TRY SWAP 0'S WITH CRY=1
17 04353 063077          HALTEE           ;EXAMINE AC0 FOR CRY "S"
18                 ;ERROR DEPENDS ON A 1 IN BIT 0 OR 15 SEE ALU SHIFTER
19
20                 ;DEFINE SWAP TEST MACRO
21                       .MACRO SWPTS
22                 ;TEST SWAP BIT ^4 TO BIT ^5
23                 ;AC0=^6 AC1=^7 EXPECTED RESULT IN AC2 IS ^7
24               ;SWP^1:
25                       LDA 0,^2         ;GET ^6
26                       LDA 1,^3         ;^7 EXPECTED RESULT
27                       MOVZS 0,2,SZR    ;"S" BIT ^4 TO BIT ^5
28                       MOV 2,3,SNR
29                       HALTE    ;POSS. "ZR" AND FAILURE "S"
30                       SUB 1,3,SZR
31                       HALTE            ;"S" BIT ^4 TO ^5 FAILED EX AC2
32               ;SW^1A:
33                       COMOS 0,2        ;REPEAT TEST WITH A0
34                       COM 2,3          ;EXPECTED RESULT HERE IS ^7
35                       SUB 1,3,SZR
36                       HALT             ;"S" A0 IN BIT ^4 TO ^5 SEE AC2
37                 ;SW^1A TESTS SWAP OF COM ^6
38               %
39
40
41
42                       SWPTS 04,K1,K400,15,7,1,400
43                 ;TEST SWAP BIT 15 TO BIT 7
44                 ;AC0=1 AC1=400 EXPECTED RESULT IN AC2 IS 400
45               ;SWP04:
46 04354 020055          LDA 0,K1         ;GET 1
47 04355 024072          LDA 1,K400       ;400 EXPECTED RESULT
48 04356 111324          MOVZS 0,2,SZR    ;"S" BIT 15 TO BIT 7
49 04357 155005          MOV 2,3,SNR
50 04360 063077          HALTE    ;POSS. "ZR" AND FAILURE "S"
51 04361 136404          SUB 1,3,SZR
52 04362 063077          HALTE            ;"S" BIT 15 TO 7 FAILED Ex AC2
53               ;SW04A:
54 04363 110340          COMOS 0,2        ;REPEAT TEST WITH A0
55 04364 154000          COM 2,3          ;EXPECTED RESULT HERE IS 400
56 04365 136404          SUB 1,3,SZR
57 04366 063077          HALT             ;"S" A0 IN BIT 15 TO 7 SEE AC2
58                 ;SW04A TESTS SWAP OF COM 1
59                       SWPTS 05,K2,K1000,14,6,2,1000
60                 ;TEST SWAP BIT 14 TO BIT 6
```

```
01                      ;AC0=2 AC1=1000 EXPECTED RESULT IN AC2 IS 1000
02                    ;SWP05:
03 04367 020056               LDA 0,K2          ;GET 2
04 04370 024073               LDA 1,K1000       ;1000 EXPECTED RESULT
05 04371 111324               MOVZS 0,2,SZR     ;"S" BIT 14 TO BIT 6
06 04372 155005               MOV 2,3,SNR
07 04373 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
08 04374 136404               SUB 1,3,SZR
09 04375 063077               HALTE             ;"S" BIT 14 TO 6 FAILED EX AC2
10                    ;SW05A:
11 04376 110340               COMOS 0,2         ;REPEAT TEST WITH A0
12 04377 154000               COM 2,3           ;EXPECTED RESULT HERE IS 1000
13 04400 136404               SUB 1,3,SZR
14 04401 063077               HALT              ;"S" A0 IN BIT 14 TO 6 SEE AC2
15                      ;SW05A TESTS SWAP OF COM 2
16                            SWPTS 06,K4,K2000,13,5,4,2000
17                      ;TEST SWAP BIT 13 TO BIT 5
18                      ;AC0=4 AC1=2000 EXPECTED RESULT IN AC2 IS 2000
19                    ;SWP06:
20 04402 020060               LDA 0,K4          ;GET 4
21 04403 024074               LDA 1,K2000       ;2000 EXPECTED RESULT
22 04404 111324               MOVZS 0,2,SZR     ;"S" BIT 13 TO BIT 5
23 04405 155005               MOV 2,3,SNR
24 04406 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
25 04407 136404               SUB 1,3,SZR
26 04410 063077               HALTE             ;"S" BIT 13 TO 5 FAILED EX AC2
27                    ;SW06A:
28 04411 110340               COMOS 0,2         ;REPEAT TEST WITH A0
29 04412 154000               COM 2,3           ;EXPECTED RESULT HERE IS 2000
30 04413 136404               SUB 1,3,SZR
31 04414 063077               HALT              ;"S" A0 IN BIT 13 TO 5 SEE AC2
32                      ;SW06A TESTS SWAP OF COM 4
33                            SWPTS 07,K10,K4000,12,4,10,4000
34                      ;TEST SWAP BIT 12 TO BIT 4
35                      ;AC0=10 AC1=4000 EXPECTED RESULT IN AC2 IS 4000
36                    ;SWP07:
37 04415 020064               LDA 0,K10         ;GET 10
38 04416 024075               LDA 1,K4000       ;4000 EXPECTED RESULT
39 04417 111324               MOVZS 0,2,SZR     ;"S" BIT 12 TO BIT 4
40 04420 155005               MOV 2,3,SNR
41 04421 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
42 04422 136404               SUB 1,3,SZR
43 04423 063077               HALTE             ;"S" BIT 12 TO 4 FAILED EX AC2
44                    ;SW07A:
45 04424 110340               COMOS 0,2         ;REPEAT TEST WITH A0
46 04425 154000               COM 2,3           ;EXPECTED RESULT HERE IS 4000
47 04426 136404               SUB 1,3,SZR
48 04427 063077               HALT              ;"S" A0 IN BIT 12 TO 4 SEE AC2
49                      ;SW07A TESTS SWAP OF COM 10
50                            SWPTS 08,K20,K10K,11,3,20,10000
51                      ;TEST SWAP BIT 11 TO BIT 3
52                      ;AC0=20 AC1=10000 EXPECTED RESULT IN AC2 IS 10000
53                    ;SWP08:
54 04430 020065               LDA 0,K20         ;GET 20
55 04431 024077               LDA 1,K10K        ;10000 EXPECTED RESULT
56 04432 111324               MOVZS 0,2,SZR     ;"S" BIT 11 TO BIT 3
57 04433 155005               MOV 2,3,SNR
58 04434 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
59 04435 136404               SUB 1,3,SZR
60 04436 063077               HALTE             ;"S" BIT 11 TO 3 FAILED EX AC2
```



```
01                    ;SW08A:
02 04437 110340               COMOS 0,2         ;REPEAT TEST WITH A0
03 04440 154000               COM 2,3           ;EXPECTED RESULT HERE IS 10000
04 04441 136404               SUB 1,3,SZR
05 04442 063077               HALT              ;"S" A0 IN BIT 11 TO 3 SEE AC2
06                      ;SW08A TESTS SWAP OF COM 20
07                            SWPTS 09,K40,K20K,10,2,40,20000
08                      ;TEST SWAP BIT 10 TO BIT 2
09                      ;AC0=40 AC1=20000 EXPECTED RESULT IN AC2 IS 20000
10                    ;SWP09:
11 04443 020066               LDA 0,K40         ;GET 40
12 04444 024100               LDA 1,K20K        ;20000 EXPECTED RESULT
13 04445 111324               MOVZS 0,2,SZR     ;"S" BIT 10 TO BIT 2
14 04446 155005               MOV 2,3,SNR
15 04447 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
16 04450 136404               SUB 1,3,SZR
17 04451 063077               HALTE             ;"S" BIT 10 TO 2 FAILED EX AC2
18                    ;SW09A:
19 04452 110340               COMOS 0,2         ;REPEAT TEST WITH A0
20 04453 154000               COM 2,3           ;EXPECTED RESULT HERE IS 20000
21 04454 136404               SUB 1,3,SZR
22 04455 063077               HALT              ;"S" A0 IN BIT 10 TO 2 SEE AC2
23                      ;SW09A TESTS SWAP OF COM 40
24                            SWPTS 10,K100,K40K,9,1,100,40000
25                      ;TEST SWAP BIT 9 TO BIT 1
26                      ;AC0=100 AC1=40000 EXPECTED RESULT IN AC2 IS 40000
27                    ;SWP10:
28 04456 020067               LDA 0,K100        ;GET 100
29 04457 024101               LDA 1,K40K        ;40000 EXPECTED RESULT
30 04460 111324               MOVZS 0,2,SZR     ;"S" BIT 9 TO BIT 1
31 04461 155005               MOV 2,3,SNR
32 04462 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
33 04463 136404               SUB 1,3,SZR
34 04464 063077               HALTE             ;"S" BIT 9 TO 1 FAILED EX AC2
35                    ;SW10A:
36 04465 110340               COMOS 0,2         ;REPEAT TEST WITH A0
37 04466 154000               COM 2,3           ;EXPECTED RESULT HERE IS 40000
38 04467 136404               SUB 1,3,SZR
39 04470 063077               HALT              ;"S" A0 IN BIT 9 TO 1 SEE AC2
40                      ;SW10A TESTS SWAP OF COM 100
41                            SWPTS 11,K200,K100K,8,0,200,100000
42                      ;TEST SWAP BIT 8 TO BIT 0
43                      ;AC0=200 AC1=100000 EXPECTED RESULT IN AC2 IS 100000
44                    ;SWP11:
45 04471 020070               LDA 0,K200        ;GET 200
46 04472 024102               LDA 1,K100K       ;100000 EXPECTED RESULT
47 04473 111324               MOVZS 0,2,SZR     ;"S" BIT 8 TO BIT 0
48 04474 155005               MOV 2,3,SNR
49 04475 063077               HALTE   ;POSS, "ZR" AND FAILURE "S"
50 04476 136404               SUB 1,3,SZR
51 04477 063077               HALTE             ;"S" BIT 8 TO 0 FAILED EX AC2
52                    ;SW11A:
53 04500 110340               COMOS 0,2         ;REPEAT TEST WITH A0
54 04501 154000               COM 2,3           ;EXPECTED RESULT HERE IS 100000
55 04502 136404               SUB 1,3,SZR
56 04503 063077               HALT              ;"S" A0 IN BIT 8 TO 0 SEE AC2
57                      ;SW11A TESTS SWAP OF COM 200
58                            SWPTS 12,K400,K1,7,15,400,1
59                      ;TEST SWAP BIT 7 TO BIT 15
60                      ;AC0=400 AC1=1 EXPECTED RESULT IN AC2 IS 1
```

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0087 N3LGC
                        ;SWP12:
04504 020072                    LDA 0,K400      ;GET 400
04505 024055                    LDA 1,K1        ;1 EXPECTED RESULT
04506 111324                    MOVZS 0,2,SZR   ;"S" BIT 7 TO BIT 15
04507 155005                    MOV 2,3,SNR
04510 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04511 136404                    SUB 1,3,SZR
04512 063077                    HALTE           ;"S" BIT 7 TO 15 FAILED EX AC2
                        ;SW12A:
04513 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04514 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 1
04515 136404                    SUB 1,3,SZR
04516 063077                    HALT            ;"S" A0 IN BIT 7 TO 15 SEE AC2
                          ;SW12A TESTS SWAP OF COM 400
                                SWPTS 13,K1000,K2,6,14,1000,2
                          ;TEST SWAP BIT 6 TO BIT 14
                          ;AC0=1000 AC1=2 EXPECTED RESULT IN AC2 IS 2
                        ;SWP13:
04517 020073                    LDA 0,K1000     ;GET 1000
04520 024056                    LDA 1,K2        ;2 EXPECTED RESULT
04521 111324                    MOVZS 0,2,SZR   ;"S" BIT 6 TO BIT 14
04522 155005                    MOV 2,3,SNR
04523 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04524 136404                    SUB 1,3,SZR
04525 063077                    HALTE           ;"S" BIT 6 TO 14 FAILED EX AC2
                        ;SW13A:
04526 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04527 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 2
04530 136404                    SUB 1,3,SZR
04531 063077                    HALT            ;"S" A0 IN BIT 6 TO 14 SEE AC2
                          ;SW13A TESTS SWAP OF COM 1000
                                SWPTS 14,K2000,K4,5,13,2000,4
                          ;TEST SWAP BIT 5 TO BIT 13
                          ;AC0=2000 AC1=4 EXPECTED RESULT IN AC2 IS 4
                        ;SWP14:
04532 020074                    LDA 0,K2000     ;GET 2000
04533 024060                    LDA 1,K4        ;4 EXPECTED RESULT
04534 111324                    MOVZS 0,2,SZR   ;"S" BIT 5 TO BIT 13
04535 155005                    MOV 2,3,SNR
04536 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04537 136404                    SUB 1,3,SZR
04540 063077                    HALTE           ;"S" BIT 5 TO 13 FAILED EX AC2
                        ;SW14A:
04541 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04542 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 4
04543 136404                    SUB 1,3,SZR
04544 063077                    HALT            ;"S" A0 IN BIT 5 TO 13 SEE AC2
                          ;SW14A TESTS SWAP OF COM 2000
                                SWPTS 15,K4000,K10,4,12,4000,10
                          ;TEST SWAP BIT 4 TO BIT 12
                          ;AC0=4000 AC1=10 EXPECTED RESULT IN AC2 IS 10
                        ;SWP15:
04545 020075                    LDA 0,K4000     ;GET 4000
04546 024064                    LDA 1,K10       ;10 EXPECTED RESULT
04547 111324                    MOVZS 0,2,SZR   ;"S" BIT 4 TO BIT 12
04550 155005                    MOV 2,3,SNR
04551 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04552 136404                    SUB 1,3,SZR
04553 063077                    HALTE           ;"S" BIT 4 TO 12 FAILED EX AC2
                        ;SW15A:
```

```
0088 N3LGC
04554 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04555 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 10
04556 136404                    SUB 1,3,SZR
04557 063077                    HALT            ;"S" A0 IN BIT 4 TO 12 SEE AC2
                          ;SW15A TESTS SWAP OF COM 4000
                                SWPTS 16,K10K,K20,3,11,10000,20
                          ;TEST SWAP BIT 3 TO BIT 11
                          ;AC0=10000 AC1=20 EXPECTED RESULT IN AC2 IS 20
                        ;SWP16:
04560 020077                    LDA 0,K10K      ;GET 10000
04561 024065                    LDA 1,K20       ;20 EXPECTED RESULT
04562 111324                    MOVZS 0,2,SZR   ;"S" BIT 3 TO BIT 11
04563 155005                    MOV 2,3,SNR
04564 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04565 136404                    SUB 1,3,SZR
04566 063077                    HALTE           ;"S" BIT 3 TO 11 FAILED EX AC2
                        ;SW16A:
04567 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04570 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 20
04571 136404                    SUB 1,3,SZR
04572 063077                    HALT            ;"S" A0 IN BIT 3 TO 11 SEE AC2
                          ;SW16A TESTS SWAP OF COM 10000
                                SWPTS 17,K20K,K40,2,10,20000,40
                          ;TEST SWAP BIT 2 TO BIT 10
                          ;AC0=20000 AC1=40 EXPECTED RESULT IN AC2 IS 40
                        ;SWP17:
04573 020100                    LDA 0,K20K      ;GET 20000
04574 024066                    LDA 1,K40       ;40 EXPECTED RESULT
04575 111324                    MOVZS 0,2,SZR   ;"S" BIT 2 TO BIT 10
04576 155005                    MOV 2,3,SNR
04577 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04600 136404                    SUB 1,3,SZR
04601 063077                    HALTE           ;"S" BIT 2 TO 10 FAILED EX AC2
                        ;SW17A:
04602 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04603 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 40
04604 136404                    SUB 1,3,SZR
04605 063077                    HALT            ;"S" A0 IN BIT 2 TO 10 SEE AC2
                          ;SW17A TESTS SWAP OF COM 20000
                                SWPTS 18,K40K,K100,1,9,40000,100
                          ;TEST SWAP BIT 1 TO BIT 9
                          ;AC0=40000 AC1=100 EXPECTED RESULT IN AC2 IS 100
                        ;SWP18:
04606 020101                    LDA 0,K40K      ;GET 40000
04607 024067                    LDA 1,K100      ;100 EXPECTED RESULT
04610 111324                    MOVZS 0,2,SZR   ;"S" BIT 1 TO BIT 9
04611 155005                    MOV 2,3,SNR
04612 063077                    HALTE   ;POSS. "ZR" AND FAILURE "S"
04613 136404                    SUB 1,3,SZR
04614 063077                    HALTE           ;"S" BIT 1 TO 9 FAILED EX AC2
                        ;SW18A:
04615 110340                    COMOS 0,2       ;REPEAT TEST WITH A0
04616 154000                    COM 2,3         ;EXPECTED RESULT HERE IS 100
04617 136404                    SUB 1,3,SZR
04620 063077                    HALT            ;"S" A0 IN BIT 1 TO 9 SEE AC2
                          ;SW18A TESTS SWAP OF COM 40000
                                SWPTS 19,K100K,K200,0,8,100000,200
                          ;TEST SWAP BIT 0 TO BIT 8
                          ;AC0=100000 AC1=200 EXPECTED RESULT IN AC2 IS 200
                        ;SWP19:
```

```
 0089 N3LGC
01 04621 020102          LDA 0,K100K      ;GET 100000
02 04622 024070          LDA 1,K200       ;200 EXPECTED RESULT
03 04623 111324          MOVZS 0,2,SZR    ;"S" BIT 0 TO BIT 8
04 04624 155005          MOV 2,3,SNR
05 04625 063077          HALTE    ;POSS. "ZR" AND FAILURE "S"
06 04626 136404          SUB 1,3,SZR
07 04627 063077          HALTE            ;"S" BIT 0 TO 8 FAILED EX AC2
08               ;SW19A:
09 04630 110340          COMOS 0,2        ;REPEAT TEST WITH A0
10 04631 154000          COM 2,3          ;EXPECTED RESULT HERE IS 200
11 04632 136404          SUB 1,3,SZR
12 04633 063077          HALT             ;"S" A0 IN BIT 0 TO 8 SEE AC2
13                ;SW19A TESTS SWAP OF COM 100000
```

```
10090 N3LGC
01
02
03                ;FIRST USE OF NO-LOAD (IR12=1)
04                ;DEFINE MACRO FOR NO LOAD TESTS (IR12=1)
05                        .MACRO NOLOD
06                NLDA1:  ADC ^2,^2        ;AC^2=-1
07                        COM# ^2,^2,SNR   ;ATTEMPT TO MAKE ZEROS
08                        COM ^2,^2,SZR    ;AC^2 SHD HAVE =-1
09                        HALTE            ;AC^2 ALTERED IR12=1
10                        ADC# ^2,^2,SZR ;NOLOAD 1'S
11                        MOV ^2,^2,SZR    ;AC^2 SHD STILL=0'S
12                        HALTE            ;IR12=1 DID NOT BLOCK 1'S
13                %
14                        NOLOD 1,0
15 04634 102000 NLD1:   ADC 0,0 ;AC0=-1
16 04635 100015          COM# 0,0,SNR     ;ATTEMPT TO MAKE ZEROS
17 04636 100004          COM 0,0,SZR      ;AC0 SHD HAVE =-1
18 04637 063077          HALTE            ;AC0 ALTERED IR12=1
19 04640 102014          ADC# 0,0,SZR ;NOLOAD 1'S
20 04641 101004          MOV 0,0,SZR      ;AC0 SHD STILL=0'S
21 04642 063077          HALTE            ;IR12=1 DID NOT BLOCK 1'S
22                        NOLOD 2,1
23 04643 126000 NLD2:   ADC 1,1 ;AC1=-1
24 04644 124015          COM# 1,1,SNR     ;ATTEMPT TO MAKE ZEROS
25 04645 124004          COM 1,1,SZR      ;AC1 SHD HAVE =-1
26 04646 063077          HALTE            ;AC1 ALTERED IR12=1
27 04647 126014          ADC# 1,1,SZR ;NOLOAD 1'S
28 04650 125004          MOV 1,1,SZR      ;AC1 SHD STILL=0'S
29 04651 063077          HALTE            ;IR12=1 DID NOT BLOCK 1'S
30                        NOLOD 3,2
31 04652 152000 NLD3:   ADC 2,2 ;AC2=-1
32 04653 150015          COM# 2,2,SNR     ;ATTEMPT TO MAKE ZEROS
33 04654 150004          COM 2,2,SZR      ;AC2 SHD HAVE =-1
34 04655 063077          HALTE            ;AC2 ALTERED IR12=1
35 04656 152014          ADC# 2,2,SZR ;NOLOAD 1'S
36 04657 151004          MOV 2,2,SZR      ;AC2 SHD STILL=0'S
37 04660 063077          HALTE            ;IR12=1 DID NOT BLOCK 1'S
38                        NOLOD 4,3
39 04661 176000 NLD4:   ADC 3,3 ;AC3=-1
40 04662 174015          COM# 3,3,SNR     ;ATTEMPT TO MAKE ZEROS
41 04663 174004          COM 3,3,SZR      ;AC3 SHD HAVE =-1
42 04664 063077          HALTE            ;AC3 ALTERED IR12=1
43 04665 176014          ADC# 3,3,SZR ;NOLOAD 1'S
44 04666 175004          MOV 3,3,SZR      ;AC3 SHD STILL=0'S
45 04667 063077          HALTE            ;IR12=1 DID NOT BLOCK 1'S
```

```
↓0091 N3LGC
01
02
03                ;TEST CARRY NO LOAD IR12= 1 TO PREVENT CARRY LOAD
04
05 04670 102020 A9I:    ADCZ 0,0
06 04671 102052         ADCO# 0,0,SZC    ;NO LOAD CARRY IR12=1
07 04672 102002         ADC 0,0,SZC
08 04673 063077         HALTE            ;CALC,IR12
09                ;IF ABOVE NO LOAD CAUSES A JMP 0, SEE BIT 14 AT SETTRAP AND GATE
10
11
12 04674 102040 A9J:    ADCO 0,0
13 04675 102033         ADCZ# 0,0,SNC    ;CRY SHD STAY=1 IR12=1
14 04676 102003         ADC 0,0,SNC
15 04677 063077         HALTE            ;NOT NEWCARRY,NOT LOADCARRY
16                ;IF ABOVE NOLOAD CAUSES A JMP 0,SEE BIT 15 AT SETTRAP AND GATE
17
18
19                  ;FIRST USE OF STA INSTRUCTION
20                  ;ALSO, FIRST LDA WITH 10 AS EFFECTIVE ADDRESS
21
22 04700 102000 STA00:  ADC 0,0
23 04701 040010         STA 0,10                 ;FIRST USE OF STA
24 04702 024010         LDA 1,10                 ;FIRST LDA OF LOC "10"
25 04703 130004         COM 1,2,SZR      ;SKIP IF LDA GOT -1 BACK
26 04704 063077         HALTE            ;LDA FROM LOC "0" IS IN AC1
27                ;NOW STORE 0'S IN LOC 10 RETRY LDA 0,10
28 04705 102400 STA01:  SUB 0,0
29 04706 040010         STA 0,10                 ;2ND STA IN LOC "10"
30 04707 024010         LDA 1,10                 ;2ND LDA OF LOC "10"
31 04710 125004         MOV 1,1,SZR      ;SKP IS LDA GOT 0'S BACK
32 04711 063077         HALTE
33                  ;IF EITHER OF ABOVE HALTS EXAMINE LOC CONTAINING STA
34                  ;IN CASE ADDRESSING MODE 1 ENABLED
35                  ;IF STA0,10+1=-1 OR STA0,10+1=0 SEE IR7 ALU ROM(DP1/D)
```

```
↓0092 N3LGC
01
02
03                ;CONTINUATION OF LDA TESTS
04                ;ADDRESSING MODE 01 (IR7=1 IR6=0)
05
06 04712 102000 LDA29:  ADC 0,0          ;SET AC0=-1
07 04713 020400         LDA 0,.          ;FIRST LDA WITH IR7=1
08 04714 024104         LDA 1,KLDA.      ;GET LDA 0,. FROM PAGE 0
09 04715 106404         SUB 0,1,SZR      ;RESULT LAST 2 LOADS SHD BE=
10 04716 063077         HALTE            ;LDA 0 IR7=1 FAILED
11                ;EXPECTED RESULT IN AC0 PROBABLY LOADED LOC "0" INSTEAD
12
13                ;NOW TEST FORWARD "LDA .+1" +1 OFFSET
14 04717 126000 LDA30:  ADC 1,1
15 04720 024401         LDA 1,.+1        ;GET NEXT MEM LOC
16 04721 020400         LDA 0,.+0        ;ALSO 0=LDA 0,.
17 04722 131000         MOV 1,2          ;SAVE LDA RESULTS
18 04723 112404         SUB 0,2,SZR      ;SKP BOTH LDA'S CORRECT
19 04724 063077         HALTE            ;AC0 AND 1 SHD BOTH=LDA 0,.
20                ;USE NEGATIVE OFFEST FOR THE FIRST TIME
21                ;NOW TEST MODE 01 NEGATIVE OFFSET OF=1
22 04725 126000 LDA31:  ADC 1,1          ;SEE DISPXTND IF TEST FAILS
23 04726 020400         LDA 0,.          ;GET THIS INST TO AC0
24 04727 024777         LDA 1,.-1        ;FIRST USE - OFFSET TO AC1
25 04730 131000         MOV 1,2          ;SAVE LDA RESULTS
26 04731 112404         SUB 0,2,SZR      ;SKP BOTH LDA'S CORRECT
27 04732 063077         HALTE            ;SEE NOT DISPEXTEND AT DP1/D ROM
28                ;LDA ALL AC'S WITH LDA 0,. USING FORWARD OFFSETS
29 04733 034403 LDA32:  LDA 3,.+3
30 04734 030402         LDA 2,.+2
31 04735 024401         LDA 1,.+1
32 04736 020400         LDA 0,.
33 04737 106414         SUB# 0,1,SZR
34 04740 063077         HALTE            ;LDA 1,.+1 FAILED
35 04741 112414         SUB# 0,2,SZR
36 04742 063077         HALTE            ;LDA 2,.+2 FAILED
37 04743 116414         SUB# 0,3,SZR
38 04744 063077         HALTE            ;LDA 3,.+3 FAILED
39
40                ;TEST LDA SEQUENCE OF - OFFSETS
41 04745 020400 LDA33:  LDA 0,.
42 04746 024777         LDA 1,.-1
43 04747 030776         LDA 2,.-2
44 04750 034775         LDA 3,.-3
45 04751 106414         SUB# 0,1,SZR
46 04752 063077         HALTE            ;LDA .-1 FAILED
47 04753 112414         SUB# 0,2,SZR
48 04754 063077         HALTE            ;LDA .-2 FAILED
49 04755 116414         SUB# 0,3,SZR
50 04756 063077         HALTE            ;LDA .-3 FAILED
51
52
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10093 N3LGC
01                ;TEST FOR EXISTENCE OF ISZ INSTR
02                ;FIRST USE OF ISZ INSTRUCTION
03 04757 102400 ISZ00:  SUB 0,0
04 04760 040010         STA 0,10
05 04761 152000         ADC 2,2          ;SET AC2=-1 ISZ COULD=LDA OR STA
06 04762 010010         ISZ 10           ;+1 LOC 10 SHD NOW=+1
07 04763 105001         MOV 0,1,SKP      ;ALU CRY MIGHT NOT=1
08 04764 063077         HALTE            ;ISZ (0+1) SKIPPED
09 04765 024010         LDA 1,10                 ;SEE SETSKP,RMW,DP2,ZR  IN SKIP
10 04766 121225         MOVZR 1,0,SNR    ;MAKE SURE ISZ RESULT
11 04767 101003         MOV 0,0,SNC      ;IS=TO+1
12 04770 063077         HALTE            ;0+1 DID NOT=+1
13 04771 154004         COM 2,3,SZR
14 04772 063077         HALTE            ;ISZ CHANGED AC2
15
16                ;TEST FOR EXISTENCE OF DSZ INSTRUCTION
17                ;-1 TO 0 IN LOC 10 SHD=-1
18                ;FIRST USE OF DSZ INST
19 04773 176400 DSZ00:  SUB 3,3
20 04774 040010         STA 0,10
21 04775 014010         DSZ 10           ;-1 TO 0 IN LOC 10
22 04776 105001         MOV 0,1,SKP
23 04777 063077         HALTE            ;DSZ SKIPPED 0-1
24 05000 024010         LDA 1,10                 ;GET DSZ RESULTS SHD=-1
25 05001 120004         COM 1,0,SZR
26 05002 063077         HALTE            ;DSZ RESULT NOT=-1
27 05003 175004         MOV 3,3,SZR      ;AC3 SHD NOT BE DISTURBED
28 05004 063077         HALTE            ;DSZ CHANGED AC3
29
30                ;RETEST ISZ TO SKIP AND NOT CHNGE CRY
31                ;+1 TO -1 IN LOC 10
32 05005 102000 ISZ01:  ADC 0,0
33 05006 040010         STA 0,10         ;(10)=-1
34 05007 111120         MOVZL 0,2        ;(AC2=-2) CRY=1
35 05010 010010         ISZ 10           ;+1-1=SETSKIP,ZR
36 05011 063077         HALTE            ;ISZ=1 DID NOT SKIP
37 05012 101003         MOV 0,0,SNC      ;TEST CALC
38 05013 063077         HALTE            ;CARRY OUT CHANGED CRY
39 05014 020010         LDA 0,10
40 05015 101004         MOV 0,0,SZR
41 05016 063077         HALTE            ;(LOC 10) DID NOT=0 AFTER ISZ
42 05017 140225         COMZR 2,0,SNR    ;MAKE SURE AC2 STILL=-2
43 05020 101003         MOV 0,0,SNC
44 05021 063077         HALTE            ;ISZ CHANGED AC2
```

```
10094 N3LGC
01
02
03                ;TEST DSZ  IN SKIP LOGIC
04 05022 102520 DSZ01:  SUBZL 0,0
05 05023 040010         STA 0,10         ;(LOC 10=+1)
06 05024 114000         COM 0,3          ;(AC3=-2)
07 05025 014010         DSZ 10           ;+1-1=ZR,RMW,DP2,NOT AUTO = SETSKIP
08 05026 063077         HALTE            ;DSZ DID NOT SKIP
09 05027 101002         MOV 0,0,SZC      ;TEST NOT CALC TO STOP ALUCARRYOUT
10 05030 063077         HALTEE           ;ALUCARRYOUT CHANGED CARRY
11 05031 160225         COMZR 3,0,SNR
12 05032 101003         MOV 0,0,SNC      ;AC3 SHD STILL=-2
13 05033 063077         HALT             ;DSZ CHANGED AC3
14
15                ;FIRST USE OF JMP INSTRUCTION JMP .+2
16                ;ADDRS OF JMP TESTS ARE STORED IN LOC 10
17 05034 020402 JMP00:  LDA 0,.+2
18 05035 115001         MOV 0,3,SKP
19 05036 005034         JMP00
20 05037 040010         STA 0,10                 ;ADDRS OF JMP TST TO LOC 10
21 05040 000402         JMP .+2
22 05041 063077         HALTE            ;JMP DID NOT JMP
23 05042 116414         SUB# 0,3,SZR     ;AC0 AND AC3 SHD BE=
24 05043 063077         HALTE            ;JMP CHANGED AC3 (JSR?)
25                ;TEST JMP WITH A NEG OFFSET
26 05044 020402 JMP01:  LDA 0,.+2
27 05045 115001         MOV 0,3,SKP
28 05046 005044         JMP01
29 05047 040010         STA 0,10         ;LOC 10=ADDRS JMP TEST
30 05050 111001         MOV 0,2,SKP      ;GET TO JMP -
31 05051 000403         JMP .+3
32 05052 000777         JMP .-1
33 05053 063077         HALTE
34 05054 116414         SUB# 0,3,SZR
35 05055 063077         HALTE            ;JMP CHNGED AC0 OR AC3
```

```
;0095 N3LGC
01
02
03                ;FIRST USE OF JSR INSTRUCTION
04
05 05056 020402 JSR00:  LDA 0,.+2
06 05057 115001         MOV 0,3,SKP
07 05060 005056         JSR00           ;ADRS THIS TEST
08 05061 040010         STA 0,10                ;TO LOC 10
09 05062 004402         JSR .+2         ;FIRST USE JSR
10 05063 063077         HALTE           ;JSR DID NOT CHNG PC
11 05064 024061         LDA 1,K5
12 05065 123000         ADD 1,0         ;NOW AC0 AND AC3 SHD BE=
13 05066 116414         SUB# 0,3,SZR
14 05067 063077         HALTE           ;JSR FAILED TO LOAD AC3
15                ;TEST JSR WITH NEG OFFSET
16 05070 020402 JSR01:  LDA 0,.+2
17 05071 115001         MOV 0,3,SKP
18 05072 005070         JSR01           ;ADRS THIS TEST
19 05073 040010         STA 0,10                ;TO LOC 10
20 05074 111001         MOV 0,2,SKP
21 05075 000403         JMP .+3
22 05076 004777         JSR .-1         ;FIRST JSR - OFFSET
23 05077 063077         HALTE           ;JSR DID NOT CHNG PC
24 05100 024063         LDA 1,K7
25 05101 123000         ADD 1,0
26 05102 116414         SUB# 0,3,SZR
27 05103 063077         HALTE
28
29                ;NOW TEST LDA USING INDEX MODE 2
30                 ;FIRST USE OF INDEXING OFFSET AND INDEX=0
31 05104 020064 LDA34:  LDA 0,K10
32 05105 040010         STA 0,10
33 05106 111000         MOV 0,2         ;  AC2=10
34 05107 100400         NEG 0,0         ;AC0=-10
35 05110 105000         MOV 0,1         ;AC1=-10
36 05111 040011         STA 0,11        ;(LOC 11)=-10
37 05112 155400         INC 2,3
38 05113 025000         LDA 1,0,2
39 05114 123014         ADD# 1,0,SZR    ;AC1=10 (AC0)=-10 IF LDA CORRECT
40 05115 063077         HALTE           ;LDA 1,0,2 FAILED
41                ;MAY HAVE USED AC3 AS INDEX (AC1) WILL=(LOC 11)
42
```

```
;0096 N3LGC
01
02
03                ;NOW USE STA MODE 2 INDEXED
04                ;ALSO FIRST USE OF AN LDA PAGE 0 BIT 8=1
05
06 05116 030111 STA02:  LDA 2,K210      ;THIS LDA PREV TESTED
07 05117 051000         STA 2,0,2       ;STORE 210 IN LOC 210
08 05120 024210         LDA 1,210       ;DIRECT ACCESS 210
09 05121 132414         SUB# 1,2,SZR    ;NOT=LDA OR STA
10 05122 063077         HALTE           ;COULD FAIL EFA DISPEXTEND
11                ;IR8=1 SHD BE BLOCKED BY ALU ROM IR6,7=0 ,EFA
12
13                ;TRY STA AGAIN WITH + OFFSET
14                ;CONTENTS OF LOC 210 STILL=210
15 05123 030111 STA03:  LDA 2,K210
16 05124 141400         INC 2,0
17 05125 041001         STA 0,1,2       ;211 TO LOC 211
18 05126 024211         LDA 1,211       ;GET 211 DIRECT
19 05127 122414         SUB# 1,0,SZR    ;
20 05130 063077         HALTE           ;STA 0,1,2 FAILED
21
22                ;TRY STA AGAIN WITH - OFFSET
23 05131 030111 STA04:  LDA 2,K210
24 05132 144000         COM 2,1
25 05133 045377         STA 1,-1,2      ;COM 210 TO LOC 207
26 05134 020207         LDA 0,207       ;GET IT BACK
27 05135 106414         SUB# 0,1,SZR    ;(LOC 207) SHD=COM 210
28 05136 063077         HALTE           ;STA 1,-1,2 FAILED
29                ;DISPEXTEND MAY HAVE FAILED EFA IR8=1 AND NOT INDEX 00
30                ;ALU ROM IR6=1 AND EFA
31
32                ;USE STA DIRECT TO 300
33                ;AND LDA INDEXED MODE 3 TO RETRIEVE
34
35 05137 034070 STA05:  LDA 3,K200      ;PREP AC2 AND AC3 FOR
36 05140 030067         LDA 2,K100      ;TESTING INDEX 3 GETS AC3
37 05141 054300         STA 3,300       ;DOUBTFUL THAT DISPXTND FAILS
38 05142 160000         COM 3,0
39 05143 040200         STA 0,200       ;PREP LOC 200 IN CASE INDEXS AC2
40 05144 025500         LDA 1,100,3     ;FIRST USE OF INDEX 3
41 05145 136414         SUB# 1,3,SZR    ;AC1 AND AC3 SHD=200
42 05146 063077         HALTE           ;LDA DIDN'T GET (LOC 300)
43                ;IF (AC1)=COM OF 200 INDEX 2 WAS USED INSTEAD
44
45                ;TEST LDA INDEXED AC3 WITH - OFFSET
46
47 05147 034105 STA06:  LDA 3,K300
48 05150 030070         LDA 2,K200
49 05151 160400         NEG 3,0
50 05152 040277         STA 0,277       ;-300 TO LOC 277
51 05153 025777         LDA 1,-1,3      ;LOC 277 TO AC1
52 05154 122414         SUB# 1,0,SZR    ;AC1 SHD=AC0
53 05155 063077         HALTE           ;LDA 1,-1,3 FAILED
```

```
10097 N3LGC
01                ;START TESTING AUTO INDEX AND INDIRECTS
02                ;USING MODE 2 SAFEST WAY TO LOAD LOC 20
03                ;AND AVOID "AUTO"
04
05 05156 030065 STA07:  LDA 2,K20
06 05157 020072         LDA 0,K400
07 05160 114400         NEG 0,3
08 05161 041000         STA 0,0,2       ;FIRST REF MEM LOC 20
09 05162 055001         STA 3,1,2       ;LOC 21
10 05163 024020         LDA 1,20        ;FIRST DIRECT REF LOC 20
11 05164 122414         SUB# 1,0,SZR    ;AC1 0 AND LOC 20 SHD=400
12 05165 063077         HALTE           ;REFERENCE LOC 20 FAILED
13                ;AUTO ENABLED INTO SET AUTO COULD FAIL IR11=1
14                ;(20) AC1 AND AC0 SHOULD ALL=400
15
16                ;FIRST USE OF DEFER FOLLOWS
17                ;NOT AUTO INDEXED COULD HANG UP VIA NOT CPB0
18 05166 024111 STA08:  LDA 1,K210      ;PREPARE REGISTERS
19 05167 044010         STA 1,10        ;FOR TEST
20 05170 130400         NEG 1,2
21 05171 050210         STA 2,210       ;210=-210
22 05172 044207         STA 1,207       ;207 AND 211
23 05173 044211         STA 1,211       ;=+210
24 05174 022010         LDA 0,@10       ;FIRST TIME IR5=1
25 05175 112414         SUB# 0,2,SZR    ;AC2 AND AC0 SHD=-210
26 05176 063077         HALTE           ;FIRST DEFER FAILED
27 05177 020010         LDA 0,10
28 05200 106414         SUB# 0,1,SZR    ;LOC 10 SHD=210
29 05201 063077         HALTE           ;AUTO INC OR DEC LOC 10
30                ;SEE NOT IR11 INTO SET AUTO
31                ;AC0=211 AUTO SET PREMATURELY
```

```
10098 N3LGC
01
02
03                ;NOW TEST DEFER VIA AUTO LOC 20
04                ;FIRST TIME FOR AUTO
05                ;IF IT DOESNIT CLEAR GOOD LUCK +1 INST!S STARTS
06 05202 024105 STA09:  LDA 1,K300
07 05203 044020         STA 1,20        ;PREPARE REG!S
08 05204 120400         NEG 1,0         ;(20) 300 AND 277=300
09 05205 040301         STA 0,301       ;(301)=-300
10 05206 044300         STA 1,300
11 05207 044277         STA 1,277
12 05210 036020         LDA 3,@20       ;FIRST TIME AUTO
13 05211 116414         SUB# 0,3,SZR    ;(301) 0 AND AC3 SHD=-300
14 05212 063077         HALTE           ;AUTO (@20) FAILED LDA
15 05213 030020         LDA 2,20
16 05214 125400         INC 1,1
17 05215 146414         SUB# 2,1,SZR    ;(20) SHD +1 TO=301
18 05216 063077         HALTE           ;@20 DID NOT +1
19                ;AUTO DEC COULD HAVE SET SEE "NOT ALU12" AND SET AUTO
20                ;CONTENTS OF LOC 20 WILL=277
21                ;OR IF DEFER CLRS PREMATURE AC3 WILL=301
22                ;SEE "SET AUTO" INTO CLR DEFER TO BLOCK 0 TO DEFER
23
24                ;NOW TEST AUTO DEC @30
25                ;FIRST TIME FOR AUTO DEC
26 05217 024111 STA10:  LDA 1,K210      ;NEXT STA COULD HURT IR12=1
27 05220 044030         STA 1,30        ;NO SET AUTO SO AUTO DEC SHD=0
28 05221 134400         NEG 1,3         ;ALU 12 HAS=1 PREVIOUSLY THOUGH
29 05222 054207         STA 3,207       ;207=-210
30 05223 044210         STA 1,210       ;210,211=+210
31 05224 044211         STA 1,211
32 05225 022030         LDA 0,@30       ;FIRST AUTO DEC
33 05226 116414         SUB# 0,3,SZR    ;AC0 AND 3 SHD=-210
34 05227 063077         HALTE           ;FIRST AUTO DEC FAILED
35 05230 020030         LDA 0,30
36 05231 115400         INC 0,3
37 05232 136414         SUB# 1,3,SZR
38 05233 063077         HALTE           ;(30) NOT=207 AUTO DEC
39                ;IF CONTENTS 30=211 SEE ALU12 INTO AUTO DEC
40              ;AND NOT AUTODECEN,NOT AUTODEC INTO NOT DECA
```

```
10099 N3LGC
01
02
03                ;CASCADE DEFERS THROUGH 10 AND 11
04                ;FIRST DEFER DEFERRED
05 05234 020107 STA11:  LDA 0,KD11
06 05235 040010         STA 0,10        ;(LOC 10)=#11
07 05236 024105         LDA 1,K300      ;(LOC 11)=300
08 05237 044011         STA 1,11
09 05240 134400         NEG 1,3
10 05241 054300         STA 3,300       ;(300)=-300
11 05242 044301         STA 1,301       ;(301)=300
12 05243 044277         STA 1,277       ;(277)=300
13 05244 032010         LDA 2,#10       ;SHD ALSO DEFER #11 TO LOC 300
14 05245 156414         SUB# 2,3,SZR    ;AC2,3 SHD BOTH=-300
15 05246 063077         HALTE           ;DEFER DEFERRED FAILED
16                ;IF AC2=300 SEE NOT CPB0 INTO CLEAR DEFER
17                ;CPB0=1 SHD INHIBIT CLR DEFER
18
19                ;CASCADE DEFERS THROUGH 20 TO 37
20                ;20 TO 27 START=#17+1 TO #20  (20) EVENT=#37
21                ;30 TO 36=#21-1 TO #20
22                ;37=300-1 TO 277
23
24 05247 030065 STA12:  LDA 2,K20       ;SET UP
25 05250 020110         LDA 0,KD17      ;AUTO REGISTERS
26 05251 176400         SUB 3,3         ;20 TO 37
27 05252 024112         LDA 1,KM8
28 05253 041000         STA 0,0,2       ;FIRST 20 TO 27=#17
29 05254 151400         INC 2,2         ;THEN 30 TO 37=#21
30 05255 125404         INC 1,1,SZR
31 05256 000775         JMP STA12+4
32 05257 174005         COM 3,3,SNR
33 05260 000403         JMP .+3
34 05261 020113         LDA 0,KD21
35 05262 000770         JMP STA12+3
36 05263 020105         LDA 0,K300
37 05264 041377         STA 0,-1,2      ;(37)=300
38 05265 040300         STA 0,300
39 05266 040301         STA 0,301
40 05267 040017         STA 0,17
41 05270 114400         NEG 0,3
42 05271 054277         STA 3,277
43 05272 027360         LDA 1,#-20,2    ;EFA #20=#'S THROUGH 37 TO 300
44 05273 136414         SUB# 1,3,SZR    ;AC1 AND 3 SHD=-300
45 05274 063077         HALTE           ;CASCADED DEFERS AUTO FAILED
46 05275 021360         LDA 0,-20,2     ;GET (20)AGAIN
47 05276 024114         LDA 1,KD37      ;GET #37
```

```
10100 N3LGC
01
02
03
04
05                ;TEST JMP "#" TO BLOCK SETUP2 AND 2WRADR1
06
07 05277 020402 JMP02:  LDA 0,.+2
08 05300 115001          MOV 0,3,SKP
09 05301 005277          JMP#2
10 05302 040010          STA 0,10               ;ADRS OF JMPTST TO LOC 10
11 05303 002403          JMP #JMP2L
12 05304 063077          HALTE          ;JMP # FAILED TO
13 05305 063077          HALTE          ;JMP AT ALL
14 05306 105311 JMP2L:   #,+3
15 05307 063077          HALTE          ;# WAS IGNORED
16 05310 063077          HALTE          ;#,+3 MAY BE SKIP ALSO
17 05311 005312          .+1
18 05312 116414          SUB# 0,3,SZR   ;AC0 OR 3 CHANGED ON A JMP#
19 05313 063077          HALTE
20
21
22                ;LDA INDEXED WITH BIT 0=1
23                ;SHOULD NOT DEFER
24
25 05314 030105 LDA36:   LDA 2,K300
26 05315 144400          NEG 2,1
27 05316 044301          STA 1,301
28 05317 044277          STA 1,277
29 05320 141400          INC 2,0
30 05321 040300          STA 0,300      ;# WILL GET 301 IN ERRCR
31 05322 153240          ADDOR 2,2      ;SET BIT 0=1
32 05323 035000          LDA 3,0,2      ;IR5=0 SHD NOT DEFER
33 05324 116414          SUB# 0,3,SZR
34 05325 063077          HALTE          ;INDEX "CPB0" DEFERRED
```

```
;0101 N3LGC
01
02
03                      ;LDA AUTO REG 20 SHOULD NOT DEFER
04                      ;WHEN IR5=0 AND (20) BIT 0=1
05
06 05326 030065 LDA37:  LDA 2,K20
07 05327 034105         LDA 3,K300
08 05330 054300         STA 3,300
09 05331 054301         STA 3,301
10 05332 177240         ADDOR 3,3
11 05333 055000         STA 3,0,2
12 05334 153240         ADDOR 2,2
13 05335 021000         LDA 0,0,2
14 05336 116414         SUB# 0,3,SZR    ;AC0,3 SHD = 100300
15 05337 063077         HALTE           ;BIT 0 CAUSED A DEFER
16
17                      ;JSR WITH BIT 0=1 IN INDEX REG
18                      ;SHOULD NOT DEFER AND SHD NOT
19                      ;ALLOW BIT 0 INTO AC3
20
21 05340 020403 JSR02:  LDA 0,.+3
22 05341 030064         LDA 2,K10
23 05342 153241         ADDOR 2,2,SKP
24 05343 005356         JS02K
25 05344 151400         INC 2,2         ;COM# 0,0,SKP
26 05345 050010         STA 2,10                ;TO LOC 10=0+11
27 05346 024105         LDA 1,K300
28 05347 137240         ADDOR 1,3
29 05350 044011         STA 1,11                ;0300 (TO KEEP INVALID 0)
30 05351 040300         STA 0,300       ;DEFER INCORRECT RETURN
31 05352 034121         LDA 3,KJRET     ;(JMP 0,3)
32 05353 054012         STA 3,12                ;TO GET US BACK
33 05354 005377         JSR -1,2        ;(AC2) BIT 0=1 IR5=0 (JSR 0)
34                      ;ABOVE JSR SHD NOT DEFER JMP 0,3 IN LOC 12
35                      ;SHD BRING US BACK TO JSR +1
36 05355 175112         MOVL# 3,3,SZC   ;AC3 BIT 0 SHD=0
37 05356 063077 JS02K:  HALTE           ;DEFERRED OR AC3 BIT 0=1
38 05357 126000         ADC 1,1
39 05360 107000         ADD 0,1         ;AC1=JS02K-1
40 05361 136414         SUB# 1,3,SZR    ;AC3 SHD=JSR+1
41 05362 063077         HALTE           ;WRONG ADDRS IN AC3
42
43                      ;TEST ISZ TO NOT ALTER AC'S
44 05363 102120 ISZ02:  ADCZL 0,0
45 05364 040010         STA 0,10                ;(10)=-1
46 05365 102400         SUB 0,0
47 05366 126400         SUB 1,1         ;AC'S ALL=0
48 05367 152400         SUB 2,2
49 05370 176400         SUB 3,3
50 05371 010010         ISZ 10
51 05372 101004         MOV 0,0,SZR
52 05373 063077         HALTE           ;AC0 NOT=0 OR ISZ SKPD
53 05374 123000         ADD 1,0
54 05375 143000         ADD 2,0
55 05376 163014         ADD# 3,0,SZR
56 05377 063077         HALTE           ;AC1+2+OR 3 ALTERED "ISZ"
57 05400 020010         LDA 0,10
58 05401 100004         COM 0,0,SZR     ;(10) SHD = -1 (SEE RMW)
59 05402 063077         HALTE           ;ISZ 10 DID NOT CHNG (10)
```

```
;0102 N3LGC
01
02                      ;TEST AGAIN 0'S TO NOT ALTER ONES
03 05403 102400 ISZ03:  SUB 0,0
04 05404 040010         STA 0,10
05 05405 100000         COM 0,0
06 05406 126000         ADC 1,1
07 05407 152000         ADC 2,2
08 05410 176040         ADCO 3,3
09 05411 010010         ISZ 10
10 05412 175404         INC 3,3,SZR
11 05413 063077         HALTE
12 05414 136000         ADC 1,3
13 05415 156003         ADC 2,3,SNC
14 05416 116014         ADC# 0,3,SZR
15 05417 063077         HALTE           ;AC1=2 OR 3
16
17                      ;TEST DSZ TO NOT ALTER AC'S
18 05420 102000 DSZ02:  ADC 0,0
19 05421 040010         STA 0,10
20 05422 100000         COM 0,0
21 05423 104400         NEG 0,1         ;ALL AC'S=0
22 05424 130400         NEG 1,2
23 05425 154400         NEG 2,3
24 05426 014010         DSZ 10          ;-1 TO -2
25 05427 150404         NEG 2,2,SZR
26 05430 063077         HALTE           ;DSZ CHANGED AC2
27 05431 132400         SUB 1,2
28 05432 112400         SUB 0,2
29 05433 172414         SUB# 3,2,SZR
30 05434 063077         HALTE           ;DSZ CHANGED AC0=1 OR 3
31
32                      ;AGAIN TEST DSZ TO NOT ALTER AC'S
33 05435 176520 DSZ03:  SUBZL 3,3       ;.+1
34 05436 054010         STA 3,10                ;TO LOC 10
35 05437 164400         NEG 3,1
36 05440 170240         COMOR 3,2       ;AC'S=-1
37 05441 176000         ADC 3,3
38 05442 161240         MOVOR 3,0
39 05443 014010         DSZ 10
40 05444 063077         HALTE           ;DSZ DID NOT SKP
41 05445 166400         SUB 3,1
42 05446 146000         ADC 2,1
43 05447 106014         ADC# 0,1,SZR
44 05450 063077         HALTE           ;AC0 1 2 OR 3 ALTERED BY DSZ
45 05451 020010         LDA 0,10
46 05452 101004         MOV 0,0,SZR     ;(10) CHANGED TO = 0?
47 05453 063077         HALTE           ;DSZ DID NOT CHNG (0)
```

```
10103 N3LGC
01
02
03                      ;AUTO INCREMENT SHD NOT ALTER AC'S
04 05454 030063 STA13:  LDA 2,K7
05 05455 050023         STA 2,23
06 05456 126400         SUB 1,1
07 05457 044010         STA 1,10
08 05460 020115         LDA 0,KCBE      ;125252 (EVEN BITS)
09 05461 104000         COM 0,1
10 05462 111000         MOV 0,2
11 05463 154000         COM 2,3
12 05464 042023         STA 0,@23       ;125252 GOES TO LOC 0
13 05465 117000         ADD 0,3
14 05466 133000         ADD 1,2
15 05467 156414         SUB# 2,3,SZR
16 05470 063077         HALTE           ;AUTO INC ALTERED AN AC
17
18                      ;AUTO DEC SHD NOT ALTER ANY AC
19 05471 034064 STA14:  LDA 3,K10       ;
20 05472 054037         STA 3,37        ;TO AN AUTO DEC
21 05473 030116         LDA 2,KCB0      ;052525
22 05474 140000         COM 2,0
23 05475 105000         MOV 0,1
24 05476 134000         COM 1,3
25 05477 052037         STA 2,@37       ;AUTO DEC TO LOC 7
26 05500 106414         SUB# 0,1,SZR
27 05501 063077         HALTE           ;AC0 OR 1 ALTERED
28 05502 156414         SUB# 2,3,SZR
29 05503 063077         HALTE           ;AC2 OR 3 ALTERED
30
31                      ;AN LDA WITH IR12=1 SHD NOT "NO LOAD"
32                      ;CALC=0
33
34 05504 102000 LDA38:  ADC 0,0
35 05505 040030         STA 0,30
36 05506 100000         COM 0,0
37 05507 020030         LDA 0,30        ;IR12=1 SHD STILL LOAD
38 05510 100014         COM# 0,0,SZR
39 05511 063077         HALTE           ;IR12=1 STOPPED 2WEN
```

```
10104 N3LGC
01                      ;TEST ISZ AND DSZ TO NOT SKIP
02                      ;DEFINE MACRO FOR TESTING
03                              ,MACRO ISDST
04                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND .+2
05                    ;IDS.+1:
06                              LDA 0,K.+2      ;GET .+2
07                              STA 0,300
08                              ISZ 300 ;+1
09                              DSZ 300 ;-1
10                              DSZ 300 ;-1
11                              ISZ 300 ;+1
12                              LDA 1,300       ;SHD=.+2 AGAIN
13                              SUB# 0,1,SZR
14                              HALTE           ;ISZ/DSZ SEQ FAILED .+2
15                    %
16
17                              ISDST 00,2
18                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 2
19                    ;IDS00:
20 05512 020056                 LDA 0,K2        ;GET 2
21 05513 040300                 STA 0,300
22 05514 010300                 ISZ 300 ;+1
23 05515 014300                 DSZ 300 ;-1
24 05516 014300                 DSZ 300 ;-1
25 05517 010300                 ISZ 300 ;+1
26 05520 024300                 LDA 1,300       ;SHD=2 AGAIN
27 05521 106414                 SUB# 0,1,SZR
28 05522 063077                 HALTE           ;ISZ/DSZ SEQ FAILED 2
29                              ISDST 01,4
30                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 4
31                    ;IDS01:
32 05523 020060                 LDA 0,K4        ;GET 4
33 05524 040300                 STA 0,300
34 05525 010300                 ISZ 300 ;+1
35 05526 014300                 DSZ 300 ;-1
36 05527 014300                 DSZ 300 ;-1
37 05530 010300                 ISZ 300 ;+1
38 05531 024300                 LDA 1,300       ;SHD=4 AGAIN
39 05532 106414                 SUB# 0,1,SZR
40 05533 063077                 HALTE           ;ISZ/DSZ SEQ FAILED 4
41                              ISDST 02,10
42                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 10
43                    ;IDS02:
44 05534 020064                 LDA 0,K10       ;GET 10
45 05535 040300                 STA 0,300
46 05536 010300                 ISZ 300 ;+1
47 05537 014300                 DSZ 300 ;-1
48 05540 014300                 DSZ 300 ;-1
49 05541 010300                 ISZ 300 ;+1
50 05542 024300                 LDA 1,300       ;SHD=10 AGAIN
51 05543 106414                 SUB# 0,1,SZR
52 05544 063077                 HALTE           ;ISZ/DSZ SEQ FAILED 10
53                              ISDST 03,20
54                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 20
55                    ;IDS03:
56 05545 020065                 LDA 0,K20       ;GET 20
57 05546 040300                 STA 0,300
58 05547 010300                 ISZ 300 ;+1
59 05550 014300                 DSZ 300 ;-1
60 05551 014300                 DSZ 300 ;-1
```

```
 0105 N3LGC
01 05552 010300          ISZ 300 ;+1
02 05553 024300          LDA 1,300        ;SHD=20 AGAIN
03 05554 106414          SUB# 0,1,SZR
04 05555 063077          HALTE            ;ISZ/DSZ SEQ FAILED 20
05                       ISDST 04,40
06                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 40
07                 ;IDS04:
08 05556 020066          LDA 0,K40        ;GET 40
09 05557 040300          STA 0,300
10 05560 010300          ISZ 300 ;+1
11 05561 014300          DSZ 300 ;-1
12 05562 014300          DSZ 300 ;-1
13 05563 010300          ISZ 300 ;+1
14 05564 024300          LDA 1,300        ;SHD=40 AGAIN
15 05565 106414          SUB# 0,1,SZR
16 05566 063077          HALTE            ;ISZ/DSZ SEQ FAILED 40
17                       ISDST 05,100
18                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 100
19                 ;IDS05:
20 05567 020067          LDA 0,K100       ;GET 100
21 05570 040300          STA 0,300
22 05571 010300          ISZ 300 ;+1
23 05572 014300          DSZ 300 ;-1
24 05573 014300          DSZ 300 ;-1
25 05574 010300          ISZ 300 ;+1
26 05575 024300          LDA 1,300        ;SHD=100 AGAIN
27 05576 106414          SUB# 0,1,SZR
28 05577 063077          HALTE            ;ISZ/DSZ SEQ FAILED 100
29                       ISDST 06,200
30                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 200
31                 ;IDS06:
32 05600 020070          LDA 0,K200       ;GET 200
33 05601 040300          STA 0,300
34 05602 010300          ISZ 300 ;+1
35 05603 014300          DSZ 300 ;-1
36 05604 014300          DSZ 300 ;-1
37 05605 010300          ISZ 300 ;+1
38 05606 024300          LDA 1,300        ;SHD=200 AGAIN
39 05607 106414          SUB# 0,1,SZR
40 05610 063077          HALTE            ;ISZ/DSZ SEQ FAILED 200
41                       ISDST 07,400
42                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 400
43                 ;IDS07:
44 05611 020072          LDA 0,K400       ;GET 400
45 05612 040300          STA 0,300
46 05613 010300          ISZ 300 ;+1
47 05614 014300          DSZ 300 ;-1
48 05615 014300          DSZ 300 ;-1
49 05616 010300          ISZ 300 ;+1
50 05617 024300          LDA 1,300        ;SHD=400 AGAIN
51 05620 106414          SUB# 0,1,SZR
52 05621 063077          HALTE            ;ISZ/DSZ SEQ FAILED 400
53                       ISDST 08,1000
54                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 1000
55                 ;IDS08:
56 05622 020073          LDA 0,K1000      ;GET 1000
57 05623 040300          STA 0,300
58 05624 010300          ISZ 300 ;+1
59 05625 014300          DSZ 300 ;-1
60 05626 014300          DSZ 300 ;-1
```

```
 0106 N3LGC
01 05627 010300          ISZ 300 ;+1
02 05630 024300          LDA 1,300        ;SHD=1000 AGAIN
03 05631 106414          SUB# 0,1,SZR
04 05632 063077          HALTE            ;ISZ/DSZ SEQ FAILED 1000
05                       ISDST 09,2000
06                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 2000
07                 ;IDS09:
08 05633 020074          LDA 0,K2000      ;GET 2000
09 05634 040300          STA 0,300
10 05635 010300          ISZ 300 ;+1
11 05636 014300          DSZ 300 ;-1
12 05637 014300          DSZ 300 ;-1
13 05640 010300          ISZ 300 ;+1
14 05641 024300          LDA 1,300        ;SHD=2000 AGAIN
15 05642 106414          SUB# 0,1,SZR
16 05643 063077          HALTE            ;ISZ/DSZ SEQ FAILED 2000
17                       ISDST 10,4000
18                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 4000
19                 ;IDS10:
20 05644 020075          LDA 0,K4000      ;GET 4000
21 05645 040300          STA 0,300
22 05646 010300          ISZ 300 ;+1
23 05647 014300          DSZ 300 ;-1
24 05650 014300          DSZ 300 ;-1
25 05651 010300          ISZ 300 ;+1
26 05652 024300          LDA 1,300        ;SHD=4000 AGAIN
27 05653 106414          SUB# 0,1,SZR
28 05654 063077          HALTE            ;ISZ/DSZ SEQ FAILED 4000
29                       ISDST 11,10K
30                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 10K
31                 ;IDS11:
32 05655 020077          LDA 0,K10K       ;GET 10K
33 05656 040300          STA 0,300
34 05657 010300          ISZ 300 ;+1
35 05660 014300          DSZ 300 ;-1
36 05661 014300          DSZ 300 ;-1
37 05662 010300          ISZ 300 ;+1
38 05663 024300          LDA 1,300        ;SHD=10K AGAIN
39 05664 106414          SUB# 0,1,SZR
40 05665 063077          HALTE            ;ISZ/DSZ SEQ FAILED 10K
41                       ISDST 12,20K
42                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 20K
43                 ;IDS12:
44 05666 020100          LDA 0,K20K       ;GET 20K
45 05667 040300          STA 0,300
46 05670 010300          ISZ 300 ;+1
47 05671 014300          DSZ 300 ;-1
48 05672 014300          DSZ 300 ;-1
49 05673 010300          ISZ 300 ;+1
50 05674 024300          LDA 1,300        ;SHD=20K AGAIN
51 05675 106414          SUB# 0,1,SZR
52 05676 063077          HALTE            ;ISZ/DSZ SEQ FAILED 20K
53                       ISDST 13,40K
54                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 40K
55                 ;IDS13:
56 05677 020101          LDA 0,K40K       ;GET 40K
57 05700 040300          STA 0,300
58 05701 010300          ISZ 300 ;+1
59 05702 014300          DSZ 300 ;-1
60 05703 014300          DSZ 300 ;-1
```

```
 0107 N3LGC
01 05704 010300          ISZ 300 /+1
02 05705 024300          LDA 1,300        /SHD=40K AGAIN
03 05706 106414          SUB# 0,1,SZR
04 05707 063077          HALTE            /ISZ/DSZ SEQ FAILED 40K
05                       ISDST 14,100K
06                  /TEST OF ISZ DSZ TO  NOT SKIP AROUND 100K
07                 /IDS14:
08 05710 020102          LDA 0,K100K      /GET 100K
09 05711 040300          STA 0,300
10 05712 010300          ISZ 300 /+1
11 05713 014300          DSZ 300 /-1
12 05714 014300          DSZ 300 /-1
13 05715 010300          ISZ 300 /+1
14 05716 024300          LDA 1,300        /SHD=100K AGAIN
15 05717 106414          SUB# 0,1,SZR
16 05720 063077          HALTE            /ISZ/DSZ SEQ FAILED 100K
```

```
 0108 N3LGC
01
02
03
04                  /******TRAP INSTRUCTION TEST ********
05
06 05721 020406 TP.00:  LDA 0,.+6                /PREPARE
07 05722 040047         STA 0,TPADR              /RETURN ADDR
08 05723 100010         TRAP                     /TRAP INSTRUCTION
09 05724 063077         HALTE            /ERROR....SHD HAVE TRAPPED
10 05725 000403         JMP .+3
11 05726 005723         .-3              /POINT TO TRAP INSTR.
12 05727 005730         .+1              /POINT TO NEXT INSTRUCTION
13 05730 024046         LDA 1,TPLOC      /GET PC AT TRAP TIME
14 05731 020775         LDA 0,.-3        /GET TRAP INSTR. ADDR.
15 05732 122414         SUB# 1,0,SZR     /SKP=TRAP STORED PC OK
16 05733 063077         HALTE            /ERROR= TRAP DIDN'T SAVE PC
17
18
19                  /DEFINE MACRO FOR TESTING TRAP NOT TO DISTURB AC'S
20                      .MACRO TPACT
21                  TP.^1:  LDA 0,.+6                /RTN ADDR
22                          STA 0,TPADR              /SETUP RETURN
23                          ADC ^2,^2        /SET AC^2 TO -1
24                          TRAP             /TRAP INSTR
25                          HALTE            /TRAP DIDN'T JMP @5
26                          JMP .+2
27                          .+1              /RETURN ADDR POINTER
28                          COM ^2,^2,SZR    /SHD COM TO 0 IF STILL OK
29                          HALTE            /TRAP DISTURBED AC^2
30
31                  %
32                          TPACT 01,0
33 05734 020406 TP.01:  LDA 0,.+6                /RTN ADDR
34 05735 040047         STA 0,TPADR              /SETUP RETURN
35 05736 102000         ADC 0,0 /SET AC0 TO -1
36 05737 100010         TRAP             /TRAP INSTR
37 05740 063077         HALTE            /TRAP DIDN'T JMP @5
38 05741 000402         JMP .+2
39 05742 005743         .+1              /RETURN ADDR POINTER
40 05743 100004         COM 0,0,SZR      /SHD COM TO 0 IF STILL OK
41 05744 063077         HALTE            /TRAP DISTURBED AC0
42
43                          TPACT 02,1
44 05745 020406 TP.02:  LDA 0,.+6                /RTN ADDR
45 05746 040047         STA 0,TPADR              /SETUP RETURN
46 05747 126000         ADC 1,1 /SET AC1 TO -1
47 05750 100010         TRAP             /TRAP INSTR
48 05751 063077         HALTE            /TRAP DIDN'T JMP @5
49 05752 000402         JMP .+2
50 05753 005754         .+1              /RETURN ADDR POINTER
51 05754 124004         COM 1,1,SZR      /SHD COM TO 0 IF STILL OK
52 05755 063077         HALTE            /TRAP DISTURBED AC1
53
54                          TPACT 03,2
55 05756 020406 TP.03:  LDA 0,.+6                /RTN ADDR
56 05757 040047         STA 0,TPADR              /SETUP RETURN
57 05760 152000         ADC 2,2 /SET AC2 TO -1
58 05761 100010         TRAP             /TRAP INSTR
59 05762 063077         HALTE            /TRAP DIDN'T JMP @5
60 05763 000402         JMP .+2
```

```
 0109 N3LGC
01 05764 005765          .+1                ;RETURN ADDR POINTER
02 05765 150004          COM 2,2,SZR        ;SHD COM TO 0 IF STILL OK
03 05766 063077          HALTE              ;TRAP DISTURBED AC2
04
05                       TPACT 04,3
06 05767 020406 TP.04:   LDA 0,.+6                  ;RTN ADDR
07 05770 040047          STA 0,TPADR                ;SETUP RETURN
08 05771 176000          ADC 3,3 ;SET AC3 TO =1
09 05772 100010          TRAP               ;TRAP INSTR
10 05773 063077          HALTE              ;TRAP DIDN'T JMP #5
11 05774 000402          JMP .+2
12 05775 005776          .+1                ;RETURN ADDR POINTER
13 05776 174004          COM 3,3,SZR        ;SHD COM TO 0 IF STILL OK
14 05777 063077          HALTE              ;TRAP DISTURBED AC3
15
16
17
18               ;TRY DEFERRING IN TRAP HANDLER ADDRESS
19
20 06000 020106 TP.05:   LDA 0,KD300        ;GET INDIRECT ADDR 300
21 06001 040047          STA 0,TPADR        ;SETUP TRAP ADDRESS
22 06002 020407          LDA 0,TP.5R        ;GET RETURN ADDRESS
23 06003 040300          STA 0,300          ;PLACE IN LOC 300
24 06004 020072          LDA 0,K400
25 06005 040301          STA 0,301          ;PUT HALT IN LOC 301
26 06006 100010          TRAP               ;TRAP INSTR.
27 06007 063077          HALTE              ;ERROR HALT,.DEFER TEST DIDN'T WORK
28 06010 000402          JMP .+2
29 06011 006012 TP.5R:   .+1                ;RETURN ADDRESS
30
31
32
33
```

```
10110 N3LGC
01                ;********STACK TEST ********
02
03                ;FIRST USE OF STACK INSTRUCTIONS(DEV01)
04                ;TEST FOR EXISTANCE OF STACK
05 06012 102000 STK.0:   ADC 0,0            ;A MOVE FROM SP SHD
06 06013 061001          MTSP 0
07 06014 102400          SUB 0,0
08 06015 061201          MFSP 0             ;DISTURB THE DESTINATION REG
09 06016 101005          MOV 0,0,SNR        ;SHD = 77777 IF MFSP WORKED OK
10 06017 063077          HALTE              ;STACK INSTR DIDN'T LOAD AC0
11 06020 101112          MOVL# 0,0,SZC      ;CHECK FOR BIT 0 OFF
12 06021 063077          HALTE              ;CHECK FIXBIT0
13                ;IF ABOVE FAILS SEE DEV01 DECODE,STACK ROMS,NOT DCH,NOT IR9,DEV0
14                ; AT STACK AND GATE.
15
16                ;TRY THE MOVE TO STACK POINTER/MOVE FROM STACK POINTER
17                ;AND ALSO STACK FRAME
18                ;
19                ;DEFINE MACRO FOR USE IN STACK MOVE TESTS
20
21                       .MACRO STTST
22                ST.^1:  LDA ^4,^3          ;PUT ^3 IN AC^4
23                       ADC ^6,^6          ;SET AC^6 TO =1
24                       MOV ^6,^7
25                       MOV ^6,^5          ;AC^5,AC^7 = =1
26                       MTA^2 ^4           ;MOVE AC^4 TO ^2
27                       MFA^2 ^5           ;READ ^2 INTO AC^5
28                       SUB#^4,^5,SZR      ;CHECK RETURNED VALUE
29                       HALTE              ;STACK ERROR,AC^5 SHD= AC^4
30                       COM# ^6,^6,SZR     ;CHECK DISTURB OF AC^6
31                       HALTE              ;MFSP ^5 DISTURBED AC^6
32                       COM# ^7,^7,SZR     ;CHECK AC^7
33                       HALTE              ;MFA^2 ^5 DISTURBED AC^7
34
35                %
36
37
38
39                       STTST 00,SP,K0,0,1,2,3
40 06022 020122 ST.00:   LDA 0,K0           ;PUT K0 IN AC0
41 06023 152000          ADC 2,2 ;SET AC2 TO =1
42 06024 155000          MOV 2,3
43 06025 145000          MOV 2,1 ;AC1,AC3 = =1
44 06026 061001          MTSP 0             ;MOVE AC0 TO SP
45 06027 065201          MFSP 1             ;READ SP INTO AC1
46 06030 106414          SUB#0,1,SZR        ;CHECK RETURNED VALUE
47 06031 063077          HALTE              ;STACK ERROR,AC1 SHD= AC0
48 06032 150014          COM# 2,2,SZR       ;CHECK DISTURB OF AC2
49 06033 063077          HALTE              ;MFSP 1 DISTURBED AC2
50 06034 174014          COM# 3,3,SZR       ;CHECK AC3
51 06035 063077          HALTE              ;MFSP 1 DISTURBED AC3
52
53                       STTST 01,SP,K2525,1,2,3,0
54 06036 024117 ST.01:   LDA 1,K2525        ;PUT K2525 IN AC1
55 06037 176000          ADC 3,3 ;SET AC3 TO =1
56 06040 161000          MOV 3,0
57 06041 171000          MOV 3,2 ;AC2,AC0 = =1
58 06042 065001          MTSP 1             ;MOVE AC1 TO SP
59 06043 071201          MFSP 2             ;READ SP INTO AC2
60 06044 132414          SUB#1,2,SZR        ;CHECK RETURNED VALUE
```

```
 0111 N3LGC
01 06045 063077          HALTE            ;STACK ERROR,AC2 SHD= AC1
02 06046 174014          COM# 3,3,SZR     ;CHECK DISTURB OF AC3
03 06047 063077          HALTE            ;MFSP 2 DISTURBED AC3
04 06050 100014          COM# 0,0,SZR     ;CHECK AC0
05 06051 063077          HALTE            ;MFSP 2 DISTURBED AC0
06
07                       STTST 02,SP,K5252,2,3,0,1
08 06052 030116 ST.02:   LDA 2,K5252      ;PUT K5252 IN AC2
09 06053 102000          ADC 0,0 ;SET AC0 TO -1
10 06054 105000          MOV 0,1
11 06055 115000          MOV 0,3 ;AC3,AC1 = -1
12 06056 071001          MTSP 2           ;MOVE AC2 TO SP
13 06057 075201          MFSP 3           ;READ SP INTO AC3
14 06060 156414          SUB#2,3,SZR      ;CHECK RETURNED VALUE
15 06061 063077          HALTE            ;STACK ERROR,AC3 SHD= AC2
16 06062 100014          COM# 0,0,SZR     ;CHECK DISTURB OF AC0
17 06063 063077          HALTE            ;MFSP 3 DISTURBED AC0
18 06064 124014          COM# 1,1,SZR     ;CHECK AC1
19 06065 063077          HALTE            ;MFSP 3 DISTURBED AC1
20
21                       STTST 03,SP,K0777,3,0,1,2
22 06066 034103 ST.03:   LDA 3,K0777      ;PUT K0777 IN AC3
23 06067 126000          ADC 1,1 ;SET AC1 TO -1
24 06070 131000          MOV 1,2
25 06071 121000          MOV 1,0 ;AC0,AC2 = -1
26 06072 075001          MTSP 3           ;MOVE AC3 TO SP
27 06073 061201          MFSP 0           ;READ SP INTO AC0
28 06074 162414          SUB#3,0,SZR      ;CHECK RETURNED VALUE
29 06075 063077          HALTE            ;STACK ERROR,AC0 SHD= AC3
30 06076 124014          COM# 1,1,SZR     ;CHECK DISTURB OF AC1
31 06077 063077          HALTE            ;MFSP 0 DISTURBED AC1
32 06100 150014          COM# 2,2,SZR     ;CHECK AC2
33 06101 063077          HALTE            ;MFSP 0 DISTURBED AC2
34
35                       STTST 04,FP,K0,0,1,2,3
36 06102 020122 ST.04:   LDA 0,K0         ;PUT K0 IN AC0
37 06103 152000          ADC 2,2 ;SET AC2 TO -1
38 06104 155000          MOV 2,3
39 06105 145000          MOV 2,1 ;AC1,AC3 = -1
40 06106 060001          MTFP 0           ;MOVE AC0 TO FP
41 06107 064201          MFFP 1           ;READ FP INTO AC1
42 06110 106414          SUB#0,1,SZR      ;CHECK RETURNED VALUE
43 06111 063077          HALTE            ;STACK ERROR,AC1 SHD= AC0
44 06112 150014          COM# 2,2,SZR     ;CHECK DISTURB OF AC2
45 06113 063077          HALTE            ;MFSP 1 DISTURBED AC2
46 06114 174014          COM# 3,3,SZR     ;CHECK AC3
47 06115 063077          HALTE            ;MFFP 1 DISTURBED AC3
48
49                       STTST 05,FP,K2525,1,2,3,0
50 06116 024117 ST.05:   LDA 1,K2525      ;PUT K2525 IN AC1
51 06117 176000          ADC 3,3 ;SET AC3 TO -1
52 06120 161000          MOV 3,0
53 06121 171000          MOV 3,2 ;AC2,AC0 = -1
54 06122 064001          MTFP 1           ;MOVE AC1 TO FP
55 06123 070201          MFFP 2           ;READ FP INTO AC2
56 06124 132414          SUB#1,2,SZR      ;CHECK RETURNED VALUE
57 06125 063077          HALTE            ;STACK ERROR,AC2 SHD= AC1
58 06126 174014          COM# 3,3,SZR     ;CHECK DISTURB OF AC3
59 06127 063077          HALTE            ;MFSP 2 DISTURBED AC3
60 06130 100014          COM# 0,0,SZR     ;CHECK AC0
```

```
 0112 N3LGC
01 06131 063077          HALTE            ;MFFP 2 DISTURBED AC0
02
03                       STTST 06,FP,K5252,2,3,0,1
04 06132 030116 ST.06:   LDA 2,K5252      ;PUT K5252 IN AC2
05 06133 102000          ADC 0,0 ;SET AC0 TO -1
06 06134 105000          MOV 0,1
07 06135 115000          MOV 0,3 ;AC3,AC1 = -1
08 06136 070001          MTFP 2           ;MOVE AC2 TO FP
09 06137 074201          MFFP 3           ;READ FP INTO AC3
10 06140 156414          SUB#2,3,SZR      ;CHECK RETURNED VALUE
11 06141 063077          HALTE            ;STACK ERROR,AC3 SHD= AC2
12 06142 100014          COM# 0,0,SZR     ;CHECK DISTURB OF AC0
13 06143 063077          HALTE            ;MFSP 3 DISTURBED AC0
14 06144 124014          COM# 1,1,SZR     ;CHECK AC1
15 06145 063077          HALTE            ;MFFP 3 DISTURBED AC1
16
17                       STTST 07,FP,K0777,3,0,1,2
18 06146 034103 ST.07:   LDA 3,K0777      ;PUT K0777 IN AC3
19 06147 126000          ADC 1,1 ;SET AC1 TO -1
20 06150 131000          MOV 1,2
21 06151 121000          MOV 1,0 ;AC0,AC2 = -1
22 06152 074001          MTFP 3           ;MOVE AC3 TO FP
23 06153 060201          MFFP 0           ;READ FP INTO AC0
24 06154 162414          SUB#3,0,SZR      ;CHECK RETURNED VALUE
25 06155 063077          HALTE            ;STACK ERROR,AC0 SHD= AC3
26 06156 124014          COM# 1,1,SZR     ;CHECK DISTURB OF AC1
27 06157 063077          HALTE            ;MFSP 0 DISTURBED AC1
28 06160 150014          COM# 2,2,SZR     ;CHECK AC2
29 06161 063077          HALTE            ;MFFP 0 DISTURBED AC2
30
31
```

```
10113 N3LGC
01                ;CHECK INTERREACTION OF SP AND SF MOVE INSTRUCTIONS
02
03 06162 152400 ST.08:  SUB 2,2          ;SET AC2 TO 0
04 06163 070001          MTFP 2          ;PLACE 0'S IN FP
05 06164 152000          ADC 2,2
06 06165 071001          MTSP 2          ;PUT -1 IN SP
07 06166 074201          MFFP 3          ;GET FP
08 06167 175004          MOV 3,3,SZR     ;FP SHD = 0'S
09 06170 063077          HALTE           ;AC3/FP NOT= 0'S
10 06171 176400          SUB 3,3
11 06172 074001          MTFP 3          ;NOW TRY SP
12 06173 071201          MFSP 2          ;GET SP
13 06174 150134          COMZL# 2,2,SZR  ;SHD=-1 BEFORE NOW
14 06175 063077          HALTE           ;WAS NOT =-1 SP/SF INTERFERRANCE
15
```

```
10114 N3LGC
01
02
03                ;SET STACK POINTER TO LOC 400 .
04                ; FOR THE REST OF THE TESTING
05
06 06176 030072          LDA 2,K400      ;GET ADDR OF 400
07 06177 071001          MTSP 2
08 06200 070001          MTFP 2          ;PUT ADDR OF 400 IN SP/SF
09 06201 102000          ADC 0,0         ;-1 FOR MASK
10 06202 062077          MSKO 0          ;MASK OFF TTO/TTI
11 06203 060177          INTEN           ;ENABLE INT FOR STACK OVERFLOW ERRORS
12
13
14                ;TEST FOR EXISTANCE OF POP INSTRUCTION
15 06204 102400 PP.00:   SUB 0,0         ;TRY LOADING A VARIABLE FROM
16 06205 042072          STA 0,@K400             ;MEMORY USING POP INSTR
17 06206 102000          ADC 0,0
18 06207 061601          POP 0           ;SHD GET 0
19 06210 100004          COM 0,0,SZR     ;SHD NOT SKP IF POP WORKED
20 06211 101001          MOV 0,0,SKP     ;SKP OVER HALTE
21 06212 063077          HALTE           ;POP INSTR DIDN'T LOAD AC0
22
23                ;TRY POP OF -1 FROM STACK INTO AC1
24 06213 102000 PP.01:   ADC 0,0
25 06214 042072          STA 0,@K400
26 06215 020072          LDA 0,K400
27 06216 061001          MTSP 0  ;PUT 400 IN SP
28 06217 126400          SUB 1,1 ;
29 06220 065601          POP 1           ;POP -1 INTO AC1
30 06221 124014          COM# 1,1,SZR    ;SHD COM TO 0
31 06222 063077          HALTE           ;POP DIDN'T LOAD AC1 WITH -1
32
33
34                ;PSH 0 ONTO STACK CONTAINING -1
35 06223 024414 PP.02:   LDA 1,.+12.
36 06224 044003          STA 1,3         ;IN CASE OF OVFLO
37 06225 102000          ADC 0,0
38 06226 030072          LDA 2,K400
39 06227 041001          STA 0,1,2       ;PUT -1 INTO LOC 401
40 06230 071001          MTSP 2          ;SET SP TO 400
41 06231 102400          SUB 0,0
42 06232 061401          PSH 0           ;PSH 0 ONTO STACK
43 06233 000405          JMP .+5         ;JMP OVER HALTE
44 06234 063077          HALTE           ;PSH SKIPPED
45 06235 000403          JMP .+3
46 06236 063077          HALTE           ;PSH OVERFLOWED
47 06237 006236          .-1             ;POINT TO HALTE
48 06240 025001          LDA 1,1,2       ;GET PSHD DATA FROM LOC 401
49 06241 125004          MOV 1,1,SZR     ;DID PSH STORE ON STACK?
50 06242 063077          HALTE           ;PSH DIDN'T WORK
```

```
10115 N3LGC
01                ;DEFINE MACRO FOR PSH/POP TESTING
02
03                        .MACRO PSPT
04                PP.^1:  LDA ^2,^3       ;GET ^3
05                        LDA ^4,PP^1E    ;STACK OVFLO ERR ADDR
06                        STA ^4,3        ;PUT IN LOC 3
07                        PSH ^2          ;PUT AC^2 ON STACK
08                        POP ^4          ;LOAD AC^4 WITH FIRST OFF THE STACK
09                        SUB# ^2,^4,SZR  ;CHECK AC^2 AGAINST AC^4
10                        HALTE           ;ERROR,,AC^2 NOT EQUAL TO AC^4
11                                        ;AFTER PSH/POP
12                        JMP .+3
13                PP^1E:  .+1
14                        HALTE           ;STACK OVERFLOW ERROR HALTE
15                %
16                        PSPT 03,0,K0,1
17  06243 020122 PP.03:   LDA 0,K0        ;GET K0
18  06244 024407          LDA 1,PP03E     ;STACK OVFLO ERR ADDR
19  06245 044003          STA 1,3 ;PUT IN LOC 3
20  06246 061401          PSH 0           ;PUT AC0 ON STACK
21  06247 065601          POP 1           ;LOAD AC1 WITH FIRST OFF THE STACK
22  06250 106414          SUB# 0,1,SZR    ;CHECK AC0 AGAINST AC1
23  06251 063077          HALTE           ;ERROR,,AC0 NOT EQUAL TO AC1
24                                        ;AFTER PSH/POP
25  06252 000403          JMP .+3
26  06253 006254 PP03E:   .+1
27  06254 063077          HALTE           ;STACK OVERFLOW ERROR HALTE
28                        PSPT 04,1,K2,2
29  06255 024056 PP.04:   LDA 1,K2        ;GET K2
30  06256 030407          LDA 2,PP04E     ;STACK OVFLO ERR ADDR
31  06257 050003          STA 2,3 ;PUT IN LOC 3
32  06260 065401          PSH 1           ;PUT AC1 ON STACK
33  06261 071601          POP 2           ;LOAD AC2 WITH FIRST OFF THE STACK
34  06262 132414          SUB# 1,2,SZR    ;CHECK AC1 AGAINST AC2
35  06263 063077          HALTE           ;ERROR,,AC1 NOT EQUAL TO AC2
36                                        ;AFTER PSH/POP
37  06264 000403          JMP .+3
38  06265 006266 PP04E:   .+1
39  06266 063077          HALTE           ;STACK OVERFLOW ERROR HALTE
40                        PSPT 05,2,K6,3
41  06267 030062 PP.05:   LDA 2,K6        ;GET K6
42  06270 034407          LDA 3,PP05E     ;STACK OVFLO ERR ADDR
43  06271 054003          STA 3,3 ;PUT IN LOC 3
44  06272 071401          PSH 2           ;PUT AC2 ON STACK
45  06273 075601          POP 3           ;LOAD AC3 WITH FIRST OFF THE STACK
46  06274 156414          SUB# 2,3,SZR    ;CHECK AC2 AGAINST AC3
47  06275 063077          HALTE           ;ERROR,,AC2 NOT EQUAL TO AC3
48                                        ;AFTER PSH/POP
49  06276 000403          JMP .+3
50  06277 006300 PP05E:   .+1
51  06300 063077          HALTE           ;STACK OVERFLOW ERROR HALTE
52                        PSPT,06,3,K40,0
53  06301 034066 PP.06:   LDA 3,K40       ;GET K40
54  06302 020407          LDA 0,PP06E     ;STACK OVFLO ERR ADDR
55  06303 040003          STA 0,3 ;PUT IN LOC 3
56  06304 075401          PSH 3           ;PUT AC3 ON STACK
57  06305 061601          POP 0           ;LOAD AC0 WITH FIRST OFF THE STACK
58  06306 162414          SUB# 3,0,SZR    ;CHECK AC3 AGAINST AC0
59  06307 063077          HALTE           ;ERROR,,AC3 NOT EQUAL TO AC0
60                                        ;AFTER PSH/POP
```

```
 0116 N3LGC
01  06310 000403          JMP .+3
02  06311 006312 PP06E:   .+1
03  06312 063077          HALTE           ;STACK OVERFLOW ERROR HALTE
04
```

```
10117 N3LGC
01
02
03                ;TEST PSH OVER BOUNDARY CAUSES STACK OVERFLOW ERROR
04                ;FIRST LEGAL OVERFLOW ERROR
05
06 06313 030131 PP.07:  LDA 2,K377        ;GET BOUNDARY -1
07 06314 071001         MTSP 2            ;PUT IN SP
08 06315 030405         LDA 2,STER2       ;GET GET RETURN ADDR
09 06316 050003         STA 2,3           ;PUT IN LOC 3
10 06317 071401         PSH 2             ;PSH AC2 ON STACK/FORCE OVERFLOW
11 06320 063077         HALTE             ;NO OVERFLOW , CHECK ION
12 06321 000402         JMP .+2
13 06322 006323 STER2:  .+1
14 06323 073601         POP 3             ;GET STACKED VALUE
15 06324 156414         SUB# 2,3,SZR      ;PSH SHD HAVE COMPLETED
16 06325 063077         HALTE             ;PSH DIDN'T COMPLETE STORE OF AC3
17 06326 063577         SKPBZ CPU         ;ION RESET?
18 06327 063077         HALTE             ;OVFLO DIDN'T RESET ION
19
20                ;TEST TRAP WITH OVFLO SET .
21 06330 030131 TP.08:  LDA 2,K377
22 06331 071001         MTSP 2            ;SETUP SP FOR OVFLO
23 06332 060277         INTDS
24 06333 102400         SUB 0,0
25 06334 042072         STA 0,@K400       ;INIT LOC 400
26 06335 125000         ADC 1,1           ;VALUE FOR PSH IS -1
27 06336 044046         STA 1,TPLOC       ;ALSO STORE IT IN TRAP PC LOC
28 06337 065401         PSH 1             ;FORCE OVERFLOW
29 06340 020406         LDA 0,PP.8R       ;GET RETURN ADDRESS FROM TRAP
30 06341 040047         STA 0,TPADR       ;SETUP TRAP RETN
31 06342 100010         TRAP              ;***TRAP***
32 06343 063077         HALTE             ;SHDN'T GET TO HERE
33 06344 000403         JMP .+3
34 06345 006342         .-3               ;POINT TO TRAP
35 06346 006347 PP.8R:  .+1               ;RETRN ADDRESS
36 06347 020776         LDA 0,.-2         ;GET ADDRESS OF TRAP
37 06350 024046         LDA 1,TPLOC       ;GET SAVED PC
38 06351 156414         SUB# 0,1,SZR      ;PC SAVED OK?
39 06352 063077         EHALT             ;PC SAVE ERROR--TRAP INSTR.
40 06353 020406         LDA 0,.+6         ;GET RETRN ADDRESS
41 06354 040003         STA 0,3 ;SETUP RETRN AFTER OVERFLO INTR.
42 06355 060177         INTEN             ;ALLOW INTR NOW
43 06356 101000         MOV 0,0
44 06357 063077         EHALT             ;INTERRUPT FROM OVERFLO LOST?
45 06360 000402         JMP .+2
46 06361 006362         .+1               ;POINT TO RETRN
47 06362 063577         SKPBZ CPU         ;ION RESET?
48 06363 063077         EHALT             ;OVFLO DIDN'T RESET ION
49 06364 060177         INTEN
50
51                ;TEST INC/DEC OF SP WITH PSH/POP INSTRUCTIONS
52 06365 020072 PP.09:  LDA 0,K400
53 06366 061001         MTSP 0
54 06367 111400         INC 0,2           ;AC2= 401
55 06370 065401         PSH 1             ;PSH INSTR SHD INC SP
56 06371 065201         MFSP 1            ;CHECK IT
57 06372 146414         SUB# 2,1,SZR      ;IS IT = 401?
58 06373 063077         HALTE             ;PSH DIDN'T INC SP
59 06374 065601         POP 1
60 06375 065201         MFSP 1            ;SHD BE 400 NOW
```

```
 0118 N3LGC
01 06376 106414         SUB# 0,1,SZR      ;IS SP = 400?
02 06377 063077         HALTE             ;SP NOT DECREMENTED BY POP
03
04
```

```
10119 N3LGC
01
02                ;SAVE / RETURN INSTRUCTION TESTS
03                ;FIRST TIME FOR SAVE INSTRUCTION
04
05 06400 102400 SV.00:  SUB 0,0           ;SET AC0 TO 0
06 06401 105400         INC 0,1           ;SET AC1 TO 1
07 06402 030072         LDA 2,K400        ;GET VALUE OF 400
08 06403 071001         MTSP 2            ;GET STACK POINTER
09 06404 070001         MTFP 2            ;SET FP TO 400
10 06405 131400         INC 1,2
11 06406 155400         INC 2,3           ;AC2=2, AC3=3
12 06407 101040         MOVO 0,0          ;SET CARRY TO 1
13 06410 062401         SAVE              ;SAVE AC'S
14 06411 175003         MOV 3,3,SNC       ;CHECK THAT CARRY STILL A 1
15 06412 063077         HALTE             ;SAVE CHANGED THE CARRY BIT...
16                                        ;OR SAVE INSTR, SKIPPED..
17                                        ;CHECK NOT RETURNCARRY AT STOP2/D ROM
18 06413 165000         MOV 3,1           ;PUT AC3 IN AC1
19 06414 075201         MFSP 3
20 06415 166414         SUB# 3,1,SZR      ;SP SHD = AC3
21 06416 063077         HALTE             ;STACK POINTER NOT = AC3 AFTER SAVE
22 06417 074201         MFFP 3            ;GET FRAME POINTER
23 06420 166414         SUB# 3,1,SZR      ;FP SHD=AC3
24 06421 063077         HALTE             ;FP NOT=AC3
25 06422 030071         LDA 2,K405        ;GET 405 INTO AC2
26 06423 146404         SUB 2,1,SZR       ;CHECK AC1 FOR PROPER VALUE OF SP
27 06424 063077         HALTE             ;AC1 NOT = ORIG, SP + 5 ....ERROR HALT
28 06425 021000         LDA 0,0,2         ;DIRECTLY GET SAVED AC3 & CRY
29 06426 101103         MOVL 0,0,SNC      ;IS CRY A 1
30 06427 063077         HALTE             ;SAVE INSTR DIDN'T SAVE THE CRY
31                                        ;CHECK NOT SAVECARRY, NOT WRITE AT STOP2
32 06430 101220         MOVZR 0,0         ;REPOSITION CONTENTS
33 06431 024057         LDA 1,K3          ;AND DROP CARRY BIT
34 06432 106404         SUB 0,1,SZR       ;IS IT = 3?
35 06433 063077         HALTE             ;SAVE DIDN'T STORE AC3 CORRECTLY
36 06434 021377         LDA 0,-1,2        ;GET SAVED FP
37 06435 024072         LDA 1,K400
38 06436 106414         SUB#0,1,SZR       ;FP=400 ?
39 06437 063077         HALTE             ;SAVE DIDN'T STORE FP CORRECTLY
40 06440 021374         LDA 0,-4,2        ;GET SAVED AC0
41 06441 101004         MOV 0,0,SZR       ;SHD BE = 0
42 06442 063077         HALTE             ;AC0 NOT = 0
43 06443 105400         INC 0,1
44 06444 021375         LDA 0,-3,2        ;GET SAVED AC1
45 06445 106414         SUB#0,1,SZR       ;AC1=1?
46 06446 063077         HALTE             ;AC1 NOT SAVED CORRECTLY
47 06447 021376         LDA 0,-2,2        ;GET SAVED AC2
48 06450 125400         INC 1,1
49 06451 106414         SUB#0,1,SZR
50 06452 063077         HALTE             ;AC2 NOT = 2
51
```

```
10120 N3LGC
01 06453 034420 RT.01:  LDA 3,RTTTA       ;PUT RETURN ADDRESS IN AC3
02 06454 030072         LDA 2,K400        ;400
03 06455 071001         MTSP 2            ;INIT SP
04 06456 070001         MTFP 2            ;INIT FP
05 06457 101020         MOVZ 0,0          ;SET CARRY TO 0
06 06460 030055         LDA 2,K1          ;INIT AC2
07 06461 024054         LDA 1,K10         ;INIT AC1
08 06462 020067         LDA 0,K100        ;INIT AC0
09 06463 062401         SAVE              ;SAVE INSTRUCTION********
10 06464 102040         ADCO 0,0          ;SET CARRY TO 1,AC0 TO -1
11 06465 105000         MOV 0,1
12 06466 111000         MOV 0,2
13 06467 115000         MOV 0,3           ;SET ALL AC'S TO -1
14 06470 062601         RTRN              ;RETURN INSTUEM   N*********
15 06471 063077         HALTE             ;ERROR HALT,SHDN'T GET HERE
16 06472 063077         HALTE             ;IF RTN INSTR, WORKED
17 06473 006474 RTTTA:  .+1               ;RTN ADDR POINTER
18 06474 054137         STA 3,TSTLC       ;SAVE AC3
19 06475 175002         MOV 3,3,SZC       ;CHECK CARRY FOR 0
20 06476 063077         HALTE             ;RETURN INSTR CHANGED CARRY OF 0
21                                        ;CHECK NOT RETURNCARRY AT STOP2/D ROM
22 06477 034055         LDA 3,K1          ;K1=1
23 06500 156414         SUB# 2,3,SZR      ;AC2 =1?
24 06501 063077         HALTE             ;AC2 NOT CORRECT AFTER RETURN
25 06502 034054         LDA 3,K10
26 06503 136414         SUB# 1,3,SZR      ;AC1 = 10?
27 06504 063077         HALTE             ;AC1 NOT = 10 AFTER RETURN
28 06505 034067         LDA 3,K100
29 06506 116414         SUB# 0,3,SZR      ;AC0 = 100?
30 06507 063077         HALTE             ;AC0 NOT=100 AFTER RETURN
31 06510 024072         LDA 1,K400
32 06511 071201         MFSP 2            ;GET SP
33 06512 132404         SUB 1,2,SZR       ;CHECK SP FOR 400
34 06513 063077         HALTE             ;SP NOT =400
35 06514 070201         MFFP 2
36 06515 132414         SUB# 1,2,SZR      ;FP = 400?
37 06516 063077         HALTE             ;FP NOT = 400 AFTER RETURN
38 06517 024137         LDA 1,TSTLC       ;GET SAVED AC3=FP
39 06520 132404         SUB 1,2,SZR       ;CHECK SAVED FP
40 06521 063077         HALTE             ;SAVED FP NOT = CURRENT FP
```

```
10121 N3LGC
01
02
03                ;STACK OVERFLOW TESTS - SAVE INSTRUCTION
04
05 06522 020405 STOV1:  LDA 0,.+5         ;GET RETURN ADDRESS
06 06523 040003          STA 0,3           ;PLACE IT IN LOC 3
07 06524 024072          LDA 1,K400        ;
08 06525 020056          LDA 0,K2          ;
09 06526 106405          SUB 0,1,SNR       ;FORM ADDR OF 376,ALWAS SKIP NEXT
10 06527 006536          STOV2
11 06530 131000          MOV 1,2           ;PUT AC1 IN AC2
12 06531 071001          MTSP 2            ;PUT ADDR OF 376 IN SP
13 06532 060177          INTEN             ;ENABLE INTERRUPTS
14 06533 062401          SAVE              ;FORCE OVER FLOW/INTERRUPT
15 06534 063077          HALTE             ;IF INT. WORKS SHOULD'T GET HERE
16 06535 063077          HALTE             ;IN CASE SAVE SKIPS
17
18                ;TRY DISABLE INT./THEN ENABLE???
19
20 06536 071001 STOV2:  MTSP 2            ;PUT 376 IN SP AGAIN
21 06537 020405          LDA 0,.+5         ;GET ILLEGAL RETURN ADDR
22 06540 040003          STA 0,3           ;PLACE IN LOC 3
23 06541 060277          INTDS             ;DISABLE INT.
24 06542 062401          SAVE              ;FORCE OVERFLOW/INT. DISABLED
25 06543 000403          JMP .+3           ;JMP OVER HALT
26 06544 006545          .+1               ;POINT TO RETURN ADDRESS
27 06545 063077          HALTE             ;ILLEGAL RETURN ADDRESS..HALT
28 06546 020406          LDA 0,.+6         ;GET GOOD RETURN ADDRESS
29 06547 040003          STA 0,3           ;PLACE RETURN ADRESS IN LOC 3
30 06550 060177          INTEN             ;ENABLE INTERRUPTS
31 06551 101000          MOV 0,0
32 06552 063077          HALTE             ;SHOULD'T GET HERE IF INT. OCCURRED
33 06553 000402          JMP .+2
34 06554 006555          .+1               ;POINT TO RETURN ADDRESS
35 06555 063577          SKPBZ CPU         ;ION SET?
36 06556 063077          EHALT             ;ION NOT RESET AFTER OVFLO
37                ;RE-ENABLE TTY INTR.
38 06557 102400          SUB 0,0
39 06560 062077          MSKO 0
40 06561 060177          INTEN
41
42                ;SETUP ILLEGAL STACK OVERFLOW ADDRESS FOR REST OF TEST
43 06562 020403          LDA 0,ILOVF
44 06563 040003          STA 0,3           ;SET LOC 3 TO ILLEGAL HALT
45 06564 000403          JMP .+3
46 06565 006566 ILOVF:   .+1
47 06566 063077          HALTE             ;ILLEGAL OVERFLOW -STACK
```

```
10122 N3LGC
01
02                ;CHECK IF TEST IS RUNNING WITH CAT/KITTEN
03 06567 020140          LDA 0,KATSW
04 06570 101005          MOV 0,0,SNR       ;SKP IS CAT/KITTEN RUN
05 06571 000416          JMP PRCSS         ;NOT CAT/KITTEN RUN
06 06572 014134          DSZ PKR00
07 06573 000201          JMP A1A
08 06574 020135          LDA 0,PKR01
09 06575 040134          STA 0,PKR00
10 06576 014124          DSZ TESTK
11 06577 000201          JMP A1A
12 06600 020076          LDA 0,K3.3K
13 06601 040124          STA 0,TESTK       ;SET UP LOOP CONSTANTS
14 06602 020064          LDA 0,K10
15 06603 040135          STA 0,PKR01
16 06604 040134          STA 0,PKR00
17 06605 002401          JMP @.+1
18 06606 007441          PASSC
19
```

```
                        .TITL PRCST
02
03                  ;PROCESSOR I/O INSTR TESTS
04
05 06607 102620 PRCSS:  SUBZR 0,0
06 06610 060277         INTDS
07 06611 040001         STA 0,1             ;INTA'S WILL BE 0
08                  ;ION SHD=0 NO SKIP ON BUSY NON ZERO
09 06612 063477 IO.00:  SKPBN CPU           ;ION=0 SHD NOT SKP
10 06613 101001         MOV 0,0,SKP
11 06614 063077         HALTE               ;IR8 IR9=00 NO SKIP BN
12                  ;POWER LOW SHD=0 NO SKIP ON DONE NON ZERO
13 06615 063677 IO.01:  SKPDN CPU           ;SHD NOT SKP
14 06616 101001         MOV 0,0,SKP         ;DION'T IR8 IR9=10
15 06617 063077         HALTE               ;SEE PWR LOW=1(SHDN'T)
16
17                  ;SKPBZ TO SKP ION=0 FIRST IO SKP TRUE
18 06620 063577 IO.02:  SKPBZ CPU           ;IR8 IR9=01
19 06621 063077         HALTE               ;BUSY=0 DID NOT SKP
20                  ;TEST SKPDZ POWER LOW SHD=0
21 06622 063777 IO.03:  SKPDZ CPU           ;IR8 IR9=11
22 06623 063077         HALTE               ;DONE=0 NO SKP(PWR LOW)
23                  ;NIO SHD NEITHER SKP NOR ALTER ANY AC'S
24 06624 102000 IO.04:  ADC 0,0
25 06625 105000         MOV 0,1             ;ALL AC'S=-1
26 06626 131000         MOV 1,2
27 06627 155000         MOV 2,3
28 06630 060077         NIO CPU             ;MAKE SURE IO SKP=0
29 06631 122001         ADC 1,0,SKP
30 06632 063077         HALTE               ;NIO CPU SKIPPED
31 06633 156000         ADC 2,3
32 06634 162414         SUB# 3,0,SZR
33 06635 063077         HALTE               ;NIO CHANGED AN AC
34
35                      .MACRO IOTS1
36                  ;DIA6 A2, CPU SHOULD ONLY ALTER AC<A>2
37                ;IO.A1:
38                      LDA A2,K5252
39                      MOV A2,A3                   ;ALL AC'S=52525
40                      MOV A3,A4
41                      MOV A4,A5
42                      DIA6 A2,CPU         ;A7 A2
43                      SUB# A3,A4,SZR      ;AC<A>3  SHD = AC<A>4
44                      HALTE               ;DIA6 SKPD OR AC<A>3 NOT = AC<A>4
45                      SUB# A5,A4,SZR
46                      HALTE               ;AC<A>3,A4OR<A>5 ALTERED
47                      SUB# A2,A5,SNR      ;DID AC<A>2 CHANGE?
48                      HALTE               ;AC<A>2 NOT LOADED
49                %
50
51                      IOTS1 05,0,1,2,3,A,READS
52                  ;DIA 0, CPU SHOULD ONLY ALTER AC0
53                ;IO.05:
54 06636 020116         LDA 0,K5252
55 06637 105000         MOV 0,1             ;ALL AC'S=52525
56 06640 131000         MOV 1,2
57 06641 155000         MOV 2,3
58 06642 060477         DIA 0,CPU           ;READS 0
59 06643 132414         SUB# 1,2,SZR        ;AC1  SHD = AC2
60 06644 063077         HALTE               ;DIA SKPD OR AC1 NOT = AC2
```



```
01 06645 172414         SUB# 3,2,SZR
02 06646 063077         HALTE               ;AC1,2OR3 ALTERED
03 06647 116415         SUB# 0,3,SNR        ;DID AC0 CHANGE?
04 06650 063077         HALTE               ;AC0 NOT LOADED
05                      IOTS1 06,1,0,2,3,A,READS
06                  ;DIA 1, CPU SHOULD ONLY ALTER AC1
07                ;IO.06:
08 06651 024116         LDA 1,K5252
09 06652 121000         MOV 1,0             ;ALL AC'S=52525
10 06653 111000         MOV 0,2
11 06654 155000         MOV 2,3
12 06655 064477         DIA 1,CPU           ;READS 1
13 06656 112414         SUB# 0,2,SZR        ;AC0  SHD = AC2
14 06657 063077         HALTE               ;DIA SKPD OR AC0 NOT = AC2
15 06660 172414         SUB# 3,2,SZR
16 06661 063077         HALTE               ;AC0,2OR3 ALTERED
17 06662 136415         SUB# 1,3,SNR        ;DID AC1 CHANGE?
18 06663 063077         HALTE               ;AC1 NOT LOADED
19                      IOTS1 07,2,3,0,1,A,READS
20                  ;DIA 2, CPU SHOULD ONLY ALTER AC2
21                ;IO.07:
22 06664 030116         LDA 2,K5252
23 06665 155000         MOV 2,3             ;ALL AC'S=52525
24 06666 161000         MOV 3,0
25 06667 105000         MOV 0,1
26 06670 070477         DIA 2,CPU           ;READS 2
27 06671 162414         SUB# 3,0,SZR        ;AC3  SHD = AC0
28 06672 063077         HALTE               ;DIA SKPD OR AC3 NOT = AC0
29 06673 122414         SUB# 1,0,SZR
30 06674 063077         HALTE               ;AC3,0OR1 ALTERED
31 06675 146415         SUB# 2,1,SNR        ;DID AC2 CHANGE?
32 06676 063077         HALTE               ;AC2 NOT LOADED
33                      IOTS1 08,3,0,1,2,A,READS
34                  ;DIA 3, CPU SHOULD ONLY ALTER AC3
35                ;IO.08:
36 06677 034116         LDA 3,K5252
37 06700 161000         MOV 3,0             ;ALL AC'S=52525
38 06701 105000         MOV 0,1
39 06702 131000         MOV 1,2
40 06703 074477         DIA 3,CPU           ;READS 3
41 06704 106414         SUB# 0,1,SZR        ;AC0  SHD = AC1
42 06705 063077         HALTE               ;DIA SKPD OR AC0 NOT = AC1
43 06706 146414         SUB# 2,1,SZR
44 06707 063077         HALTE               ;AC0,1OR2 ALTERED
45 06710 172415         SUB# 3,2,SNR        ;DID AC3 CHANGE?
46 06711 063077         HALTE               ;AC3 NOT LOADED
47                      IOTS1 09,0,1,2,3,B,INTA
48                  ;DIB 0, CPU SHOULD ONLY ALTER AC0
49                ;IO.09:
50 06712 020116         LDA 0,K5252
51 06713 105000         MOV 0,1             ;ALL AC'S=52525
52 06714 131000         MOV 1,2
53 06715 155000         MOV 2,3
54 06716 061477         DIB 0,CPU           ;INTA 0
55 06717 132414         SUB# 1,2,SZR        ;AC1  SHD = AC2
56 06720 063077         HALTE               ;DIB SKPD OR AC1 NOT = AC2
57 06721 172414         SUB# 3,2,SZR
58 06722 063077         HALTE               ;AC1,2OR3 ALTERED
59 06723 116415         SUB# 0,3,SNR        ;DID AC0 CHANGE?
60 06724 063077         HALTE               ;AC0 NOT LOADED
```

```
 0125 N3LGC
01                      IOTS1 10,1,0,3,2,8,INTA
02                  ;DIB 1, CPU SHOULD ONLY ALTER AC1
03                ;IO.10:
04 06725 024116         LDA 1,K5252
05 06726 121000         MOV 1,0             ;ALL AC'S=52525
06 06727 115000         MOV 0,3
07 06730 171000         MOV 3,2
08 06731 065477         DIB 1,CPU           ;INTA 1
09 06732 116414         SUB# 0,3,SZR        ;AC0  SHD = AC3
10 06733 063077         HALTE               ;DIB SKPD OR AC0 NOT = AC3
11 06734 156414         SUB# 2,3,SZR
12 06735 063077         HALTE               ;AC0,3OR2 ALTERED
13 06736 132415         SUB# 1,2,SNR        ;DID AC1 CHANGE?
14 06737 063077         HALTE               ;AC1 NOT LOADED
15                      IOTS1 11,2,3,1,0,8,INTA
16                  ;DIB 2, CPU SHOULD ONLY ALTER AC2
17                ;IO.11:
18 06740 030116         LDA 2,K5252
19 06741 155000         MOV 2,3             ;ALL AC'S=52525
20 06742 165000         MOV 3,1
21 06743 121000         MOV 1,0
22 06744 071477         DIB 2,CPU           ;INTA 2
23 06745 166414         SUB# 3,1,SZR        ;AC3  SHD = AC1
24 06746 063077         HALTE               ;DIB SKPD OR AC3 NOT = AC1
25 06747 106414         SUB# 0,1,SZR
26 06750 063077         HALTE               ;AC3,1OR0 ALTERED
27 06751 142415         SUB# 2,0,SNR        ;DID AC2 CHANGE?
28 06752 063077         HALTE               ;AC2 NOT LOADED
29                      IOTS1 12,3,2,0,1,8,INTA
30                  ;DIB 3, CPU SHOULD ONLY ALTER AC3
31                ;IO.12:
32 06753 034116         LDA 3,K5252
33 06754 171000         MOV 3,2             ;ALL AC'S=52525
34 06755 141000         MOV 2,0
35 06756 105000         MOV 0,1
36 06757 075477         DIB 3,CPU           ;INTA 3
37 06760 142414         SUB# 2,0,SZR        ;AC2  SHD = AC0
38 06761 063077         HALTE               ;DIB SKPD OR AC2 NOT = AC0
39 06762 122414         SUB# 1,0,SZR
40 06763 063077         HALTE               ;AC2,0OR1 ALTERED
41 06764 166415         SUB# 3,1,SNR        ;DID AC3 CHANGE?
42 06765 063077         HALTE               ;AC3 NOT LOADED
43
```

```
↓0126 N3LGC
01
02
03                  ;FIRST TIME FOR ANY DOA =8 OR C
04 06766 176000 IO.13:  ADC 3,3
05 06767 102400         SUB 0,0
06 06770 062077         DOB 0,CPU           ;SHD NOT SKP HALTE OR ALTER AC'S
07 06771 101004         MOV 0,0,SZR
08 06772 063077         HALTE               ;DOB SKPD OR ALTERED AC0
09 06773 174004         COM 3,3,SZR
10 06774 063077         HALTE               ;DOB ALTERED AC3
11
12                  ;IN TESTING FROM THIS POINT ON
13                  ;TTO "DONE" IS USED FOR "TRUE" INTERRUPT TESTING
14                  ;TTO DONE=0 AND BUSY=0 "FALSE" INTERRUPT TESTS
15                  ;TTO DONE=0 AND BUSY=1 LOOP BACK TO A1A
16 06775 176000 IOX00:  ADC 3,3             ;SET PASS SWITCH
17 06776 063611         SKPDN TTO           ;DONE=?
18 06777 000413         JMP IOX01           ;=0
19 07000 063511         SKPBZ TTO           ;DONE=1  BUSY MUST=0
20 07001 063077         HALTE               ;BUSY=0 OR DONE=1 FAILED
21 07002 063711         SKPDZ TTO           ;DONE=2 Z SHD NOT SKP
22 07003 101001         MOV 0,0,SKP
23 07004 063077         HALTE               ;"DZ" ERR OR MAYBE "DN"
24 07005 063411         SKPBN TTO           ;DONE=1  BUSY CAN'T=1
25 07006 002403         JMP @IOX01-1        ;OK TO DO INTR TSTS
26 07007 063077         HALTE               ;TTO IS BUSY NOT
27 07010 000765         JMP IOX00
28 07011 007216         INT00
29 07012 063511 IOX01:  SKPBZ TTO           ;NO SKP IS WAITING
30 07013 000201         JMP A1A             ;DON'T WAIT FOR TTO DONE
31 07014 175404         INC 3,3,SZR
32 07015 063077         HALTE               ;2ND TRY
33 07016 063711         SKPDZ TTO           ;FINITE TIME TWXT "DN" AND "BZ"
34 07017 000757         JMP IOX00+1         ;MAYBE DONE=1 (TIME LAPSE)
35                  ;TTO DONE AND BUSY=0
36                  ;PERFORM TESTS THAT REQUIRE  INTERRUPT TO BE FALSE
37
38 07020 102620 NIN00:  SUBZR 0,0
39 07021 040001         STA 0,1             ;1=00
40 07022 060177         NIOS CPU            ;1 TO ION "SHD NOT SKP"
41 07023 063477         SKPBN CPU           ;BUSY SHD=1 FOR CPU
42 07024 063077         HALTE               ;ION DID NOT SET (NIOS SKPD)
43 07025 063477         SKPBN CPU           ;ION=0 HERE IS INTR
44 07026 063077         HALTE               ;SEE PI AND NOT INTR
45                  ;THERE SHD BE NO INTR REQUESTS PENDING
46                  ;NIOC SHD CLR ION SKPBZ SHD NOT SKP
47 07027 060177 NIN01:  NIOS CPU            ;1 TO ION
48 07030 063577         SKPBZ CPU           ;BUSY=1
49 07031 063477         SKPBN CPU           ;SHD NOT CLR ION
50 07032 063077         HALTE               ;BZ SKPD OR BN DIDN'T
51 07033 060277 NIN02:  NIOC CPU            ;SHD CLR ION
52 07034 063477         SKPBN CPU           ;BUSY=0
53 07035 063577         SKPBZ CPU
54 07036 063077         HALTE               ;"C" DID NOT CLR ION
55
```

```
↓0127 N3LGC
01
02                      ;DOAC 0,CPU SHD CLR ION
03
04 07037 060177 NIN03:  NIOS CPU
05 07040 061277         DOAC 0,CPU              ;
06 07041 063577         SKPBZ CPU
07 07042 063077         HALTE                   ;DOAC 0,CPU FAILED CLR ION
08
09                      ;DOA SHD ONLY CLR IO BUS NOT ION
10 07043 060177 NIN04:  NIOS CPU
11 07044 061077         DOA 0,CPU               ;NO "C" ION SHD STILL=1
12 07045 063477         SKPBN CPU               ;IR8,9=00 DID ION CLR
13 07046 063077         HALTE                   ;DIS CLRD ION IR8,9=00
14                      ;SAME TEST WITH "P" SHD NOT CLR ION IR8,9=11
15 07047 060177 NIN05:  NIOS CPU
16 07050 061377         DOAP 0,CPU              ;IR8,9=11 "P" NOT "C"
17 07051 063477         SKPBN CPU
18 07052 063077         HALTE                   ;"P" CLRD ION
19                      ;"P" PULSE SHD NOT SET ION
20 07053 060277 NIN06:  NIOC CPU
21 07054 060377         NIOP CPU                ;IR8,9=11 "P" NOT "S"
22 07055 063577         SKPBZ CPU
23 07056 063077         HALTE                   ;"P" SET ION
24                      ;"S" WITH ION=1 SHD LEAVE IT=1
25 07057 060177 NIN07:  NIOS CPU                ;1 TO ION
26 07060 061177         DOAS 0,CPU              ;AGAIN WITH DOAC 0,CPU
27 07061 063477         SKPBN CPU
28 07062 063077         HALTE                   ;2ND "S" CLRD ION
29                      ;ION=1 AND SKPDN ON DEV 0 SHD NOT SKIP
30 07063 061277 NIN08:  DOAC 0,CPU
31 07064 060177         NIOS CPU                ;SET ION
32 07065 063600         SKPDN 0                 ;DEV #0 SHD NOT SKP
33 07066 101001         MOV 0,0,SKP             ;OK
34 07067 063077         HALTE                   ;CPUINST IN IO SKIP
35
36                      ;TEST "AND'S" DECODING CPU INST FOR "FALSE"
37                      .MACRO IOTS2
38                  ;NIN^A1:
39                      DOAC 0,CPU
40                      NIOS CPU                ;SET ION FOR DEV^A2
41                      SKPBN ^A2               ;TEST NOT BIT ^A3
42                      MOV 0,0,SKP
43                      HALTE                   ;ONLY DEV 77 SHD SKP
44                    ;IF ABOVE HALTE SEE BIT^A3 INTO "CPU INST" AND'S
45                  %
46                      IOTS2 09,76,15
47                  ;NIN09:
48 07070 061277         DOAC 0,CPU
49 07071 060177         NIOS CPU                ;SET ION FOR DEV76
50 07072 063476         SKPBN 76                ;TEST NOT BIT 15
51 07073 101001         MOV 0,0,SKP
52 07074 063077         HALTE                   ;ONLY DEV 77 SHD SKP
53                    ;IF ABOVE HALTE SEE BIT15 INTO "CPU INST" AND'S
54                      IOTS2 10,75,14
55                  ;NIN10:
56 07075 061277         DOAC 0,CPU
57 07076 060177         NIOS CPU                ;SET ION FOR DEV75
58 07077 063475         SKPBN 75                ;TEST NOT BIT 14
59 07100 101001         MOV 0,0,SKP
60 07101 063077         HALTE                   ;ONLY DEV 77 SHD SKP
```

```
 0128 N3LGC
01                    ;IF ABOVE HALTE SEE BIT14 INTO "CPU INST" AND'S
02                        IOTS2 11,73,13
03                  ;NIN11:
04 07102 061277         DOAC 0,CPU
05 07103 060177         NIOS CPU                ;SET ION FOR DEV73
06 07104 063473         SKPBN 73                ;TEST NOT BIT 13
07 07105 101001         MOV 0,0,SKP
08 07106 063077         HALTE                   ;ONLY DEV 77 SHD SKP
09                    ;IF ABOVE HALTE SEE BIT13 INTO "CPU INST" AND'S
10                        IOTS2 12,67,12
11                  ;NIN12:
12 07107 061277         DOAC 0,CPU
13 07110 060177         NIOS CPU                ;SET ION FOR DEV67
14 07111 063467         SKPBN 67                ;TEST NOT BIT 12
15 07112 101001         MOV 0,0,SKP
16 07113 063077         HALTE                   ;ONLY DEV 77 SHD SKP
17                    ;IF ABOVE HALTE SEE BIT12 INTO "CPU INST" AND'S
18                        IOTS2 13,57,11
19                  ;NIN13:
20 07114 061277         DOAC 0,CPU
21 07115 060177         NIOS CPU                ;SET ION FOR DEV57
22 07116 063457         SKPBN 57                ;TEST NOT BIT 11
23 07117 101001         MOV 0,0,SKP
24 07120 063077         HALTE                   ;ONLY DEV 77 SHD SKP
25                    ;IF ABOVE HALTE SEE BIT11 INTO "CPU INST" AND'S
26                        IOTS2 14,37,10
27                  ;NIN14:
28 07121 061277         DOAC 0,CPU
29 07122 060177         NIOS CPU                ;SET ION FOR DEV37
30 07123 063437         SKPBN 37                ;TEST NOT BIT 10
31 07124 101001         MOV 0,0,SKP
32 07125 063077         HALTE                   ;ONLY DEV 77 SHD SKP
33                    ;IF ABOVE HALTE SEE BIT10 INTO "CPU INST" AND'S
34
```

```
;0129 N3LGC
01
02                  ;AN "S" PULSE WITH DEV 0 (NOT CPU INST)
03                  ;SHD NOT SET ION
04 07126 061277 NIN15:  DOAC 0,CPU
05 07127 060100         NIOS 0              ;"NOT" CPU BUT "S"
06 07130 063577         SKPBZ CPU           ;SEE 9301 GENERATING SETION
07 07131 063077         HALTE               ;ION=1 ILLEGAL (CPU INST NOT)
08
09                  ;A "C" PULSE WITH DEV 0 (NOT CPU INST) SHD NOT CLR ION
10 07132 061277 NIN16:  DOAC 0,CPU
11 07133 060177         NICS CPU
12 07134 060200         NICC 0              ;NOT CPU BUT "C"
13 07135 063477         SKPBN CPU           ;ION SHD STILL=1
14 07136 063077         HALTE               ;"C" CLRD ION (NOT CPU=DEV 0)
15
16                  ;IO SKIPS SHD NOT GET TO  PTS1 "S" SHD NOT BE GEN
17 07137 061277 NIN17:  DOAC 0,CPU
18 07140 063577         SKPBZ CPU           ;IR8,9=01 BUT IS NOT "S"
19 07141 063077         HALTE
20 07142 063577         SKPBZ CPU           ;ION SHD STILL=0
21 07143 063077         HALTE               ;FIRST BZ GEN'D "S"
22
23                  ;IO SKIP "ON" SHD NOT="C" NO PTS1
24 07144 060177 NIN18:  NIOS CPU
25 07145 063677         SKPDN CPU           ;IR8,9=10 BUT IS NOT "C"
26 07146 101001         MOV 0,0,SKP         ;POWER LOW=0 SHD NOT SKP
27 07147 063077         HALTE               ;ON SKP'D WITH ION=1
28 07150 063477         SKPBN CPU           ;ABOVE HALTE SEE NOT IR8
29 07151 063077         HALTE               ;"ON" CLRD ION
30                  ;SET UP ALL CONDITIONS FOR IO SKP EXCEPT IN/OUT TIME
31 07152 061277 NIN19:  DOAC 0,CPU
32 07153 102420         SUBZ 0,0
33 07154 103577         ANDCL# 0,0,SBN      ;EVERYTHING=0 NO SKP
34 07155 101001         MOV 0,0,SKP
35 07156 063077         HALTE               ;AND=SKPBZ CPU
36                  ;SET UP ALL CONDITIONS FOR NIOS CPU EXCEPT PTS1
37 07157 061277 NIN20:  DOAC 0,CPU
38 07160 102040         ADCO 0,0
39 07161 100177         COMCL# 0,0,SBN      ;ALL=0 NO SKP
40 07162 063577         SKPBZ CPU           ;ION SHD STILL=0
41 07163 063077         HALTE               ;COMCL#=NIOS CPU
42
43                  ;SET UP ALL CONDITIONS FOR NIOS CPU
44                  ;EXCEPT IO ALCEN=0
45 07164 061277 NIN21:  DOAC 0,CPU
46 07165 020177         LDA 0,177           ;NO IOALCEN
47 07166 063577         SKPBZ CPU           ;SEE IOALCEN (NOT),PTS1
48 07167 063077         HALTE               ;LDA=NIOS CPU
```

```
;0130 N3LGC
01                  ;SET UP ALL CONDITIONS FOR IO SKPBZ CPU EX(IN/OUT)
02 07170 176400 NIN22:  SUB 3,3             ;USING AN LDA
03 07171 054177         STA 3,177           ;MAKE SURE SKP DOESN'T SET
04 07172 054000         STA 3,0
05 07173 023577         LDA 0,@177,3        ;ALMOST AN SKPBZ CPU
06 07174 101004         MOV 0,0,SZR
07 07175 063077         HALTE               ;LDA=SKPBZ CPU
08 07176 014134         DSZ PKR00
09 07177 000201         JMP A1A
10 07200 020135         LDA 0,PKR01
11 07201 040134         STA 0,PKR00
```

```
10131 N3LGC
01
02
03                ;START DEL CODE TO TTO
04                ;FOR INTERRUPT TESTING WHEN DONE=1
05
06 07202 102000 TTO00:  ADC 0,0           ;=1
07 07203 061111         DOAS 0,TTO        ;OUT TO TTO
08 07204 063411         SKPBN TTO         ;BUSY SHD=1
09 07205 063077         HALTE             ;NO SKP TTO "BN"
10 07206 063511         SKPBZ TTO         ;
11 07207 100004         COM 0,0,SZR
12 07210 063077         HALTE             ;TTO "BZ" ERR
13 07211 063711         SKPDZ TTO         ;DONE SHD=0 TTO
14 07212 063077         HALTE             ;TTO "DZ" ERR
15 07213 063611         SKPDN TTO         ;TTO DONE SHD=0
16 07214 000201         JMP A1A           ;OK LOOP THROUGH TEST
17 07215 063077         HALTE             ;TTO DONE=1 IN ERR
18
19                ;TTO DONE=1 USE TO TEST INTERRUPTS
20 07216 020416 INT00:  LDA 0,INT0K
21 07217 024133         LDA 1,JMP3K
22 07220 030056         LDA 2,K2          ;SET UP FOR
23 07221 050001         STA 2,1           ;TEST FIRST
24 07222 044002         STA 1,2           ;REAL INTERRUPT
25 07223 040300         STA 0,300
26 07224 176400         SUB 3,3
27 07225 076077         DOB 3,CPU         ;0 MSKO
28 07226 054000         STA 3,0           ;0 ADRS 0
29 07227 060177         NIOS CPU          ;ION
30 07230 000401         JMP .+1           ;WAIT
31 07231 063077         HALTE             ;INTERRUPT DID NOT OCCUR
32 07232 063077         HALTE
33 07233 007231         .=2
34 07234 007235 INT0K:  .+1
35 07235 034000         LDA 3,0
36 07236 020775         LDA 0,INT0K-1
37 07237 116414         SUB# 0,3,SZR
38 07240 063077         HALTE             ;(0) NOT=NIOS+2
```

```
10132 N3LGC
01
02                ;TEST TO MAKE SURE #IN LOC 1 WILL DEFER
03 07241 020056 INT01:  LDA 0,K2          ;AND KEEP DEFERING
04 07242 103240         ADDOR 0,0
05 07243 040001         STA 0,1           ;#2 ALSO=COM 0,0,SZC
06 07244 024133         LDA 1,JMP3K       ;JMP @300
07 07245 044003         STA 1,3           ;WILL EXECUTE IN ERR
08 07246 030414         LDA 2,INT1K       ;IF FETCH IS DIRECTLY TO 1
09 07247 050300         STA 2,300         ;OR 2ND DEFER FAILS
10 07250 151400         INC 2,2           ;LEGAL RET
11 07251 050004         STA 2,4           ;WILL BE IN 4
12 07252 103000         ADD 0,0           ;@4=COM 0,0,SZR (WON'T SKIP)
13 07253 103240         ADDOR 0,0
14 07254 040002         STA 0,2           ;@4 TO LOC 2
15 07255 101020         MOVZ 0,0          ;0 CRY JMP @300 IN0
16 07256 060177         NIOS CPU
17 07257 000401         JMP .+1           ;FIRST INTR @@
18 07260 063077         HALTE
19 07261 063077         HALTE
20 07262 007263 INT1K:  .+1
21 07263 063077         HALTE             ;LOC 1 OR 2 EXECUTED
22                ;ABOVE HALTE INTERRUPT IS NOT DOING #1
23                ;OR DEFER BIT IN LOC 1 WAS NOT RECOGNIZED
24
25                ;ION/IOF SHOULD NOT INTR
26 07264 102400 INT02:  SUB 0,0
27 07265 040000         STA 0,0
28 07266 101240         MOVOR 0,0
29 07267 040001         STA 0,1
30 07270 060177         NIOS CPU          ;ION
31 07271 060277         NIOC CPU          ;IOF
32 07272 000401         JMP .+1           ;STALL
33 07273 024000         LDA 1,0
34 07274 125004         MOV 1,1,SZR
35 07275 063077         HALTE             ;INTR AFTER IOF
36
```

```
10133 N3LGC
01
02                ;MSKO=-1 SHD NOT ALLOW TTO INTR
03 07276 102000 INT03:  ADC 0,0
04 07277 062177         DOBS 0,CPU        ;MSKO=-1
05 07300 000401         JMP .+1           ;STALL
06 07301 024000         LDA 1,0           ;AWHILE
07 07302 063477         SKPBN CPU
08 07303 063077         HALTE             ;MASK0=1 ALLOWED TTO INTR
09 07304 125004         MOV 1,1,SZR
10 07305 063077         HALTE             ;LOC 0 ALTERED
11 07306 102400         SUB 0,0
12 07307 062077         DOB 0,CPU         ;0'S TO MASK 0
13 07310 000401         JMP .+1           ;STALL WAIT FOR INTR
14 07311 024000         LDA 1,0           ;INTR DID NOT OCCUR
15 07312 063577         SKPBZ CPU         ;IF BZ NO SKP
16 07313 063077         HALTE
17 07314 125005         MOV 1,1,SNR       ;OR LOC0
18 07315 063077         HALTE             ;WAS STILL=0
19                ;INTERRUPT OVER A SKIP INSTRUCTION
20                ;SHD STORE THE CORRECT ADDRESS IN LOC 0
21 07316 024407 INT04:  LDA 1,INT4K       ;RET ADRS
22 07317 044001         STA 1,1           ;TO LOC 1
23 07320 060177         NIOS CPU          ;ION
24 07321 125005         MOV 1,1,SNR       ;SET SKIP
25 07322 063077         HALTE
26 07323 063077         HALTE
27 07324 007323         .-1
28 07325 007326 INT4K:  .+1
29 07326 101001         MOV 0,0,SKP
30 07327 063077         HALTE             ;INTR SKIPD
31 07330 020000         LDA 0,0
32 07331 030773         LDA 2,INT4K-1     ;ADRS (LOC 0) SHD=
33 07332 142414         SUB# 2,0,SZR
34 07333 063077         HALTE             ;(LOC 0) INCOR
35                ;INTERRUPT OVER SKIP INST FAILED
36                ;INTERRUPT AFTER AN I/O SKIP
37                ;SHD STORE CORRECT RESULT IN LOC 0
38 07334 024407 INT05:  LDA 1,INT5K
39 07335 044001         STA 1,1           ;RET ADRS
40 07336 060177         NIOS CPU          ;ION
41 07337 063477         SKPBN CPU         ;IO SKIP SET SKIP
42 07340 063077         HALTE
43 07341 063077         HALTE
44 07342 007341         .-1
45 07343 007344 INT5K:  .+1
46 07344 020000         LDA 0,0           ;INTR SKP WILL MISS THIS
47 07345 030775         LDA 2,INT5K-1     ;VALID INTR ADRS
48 07346 142414         SUB# 2,0,SZR
49 07347 063077         HALTE             ;INC PC IN LOC 0
50
```

```
10134 N3LGC
01
02                ;INTERRUPT AFTER A JSR SHD STORE
03                ;THE CORRECT ADDRESS IN LOC 0
04 07350 030410 INT06:  LDA 2,INT6K
05 07351 050001         STA 2,1
06 07352 153240         ADCOR 2,2         ;BIT 0 OF AC2=1
07 07353 060177         NIOS CPU          ;ION JSR GOES .+2
08 07354 005375         JSR -3,2          ;JSR ADRS CALC BIT 0=1
09 07355 063077         HALTE
10 07356 063077         HALTE             ;JSR/INT PREVENTS
11 07357 063077         HALTE             ;EITHER HALT
12 07360 007361 INT6K:  .+1
13 07361 105401         INC 3,1,SKP       ;JSR+1 SHD=INTR ADRS
14 07362 063077         HALTE
15 07363 020000         LDA 0,0           ;GET (LOC 0)
16 07364 101112         MOVL# 0,0,SZC     ;BIT 0 MUST=0
17 07365 063077         HALTE             ;BIT 0 LOC 0=1
18 07366 106414         SUB# 0,1,SZR      ;
19 07367 063077         HALTE             ;LOC 0 OR AC3 INCORRECT
20                ;LOC 0 SHD=PC AFTER JSR  (JSR+2)
21                ;AC3 SHD=PC BEFORE JSR  (JSR+1)
22                ;NEITHER SHOULD HAVE BIT 0=1 =SEE CPB0=
23                ;NOT JSR OR FIXBIT0 FORCES NOT CPB0
24 07370 102620         SUBZR 0,0
25 07371 040001         STA 0,1           ;LOC 1 = 00
26 07372 014134         DSZ PKR00
27 07373 000201         JMP A1A
28 07374 020135         LDA 0,PKR01
29 07375 040134         STA 0,PKR00
30 07376 014124         DSZ TESTK
31 07377 000410         JMP INT07
32
33 07400 024123         LDA 1,K60
34 07401 044124         STA 1,TESTK
35 07402 020064         LDA 0,K10
36 07403 040134         STA 0,PKR00
37 07404 040135         STA 0,PKR01               ;RESTORE LOOP CNT
38 07405 002401         JMP @.+1
39 07406 007441         PASSC
40
41                ;FIRST LEVEL INTERRUPT TESTS COMPLETE
42                ;CLR TTO DONE AND ION
43                ;REDO NON INT TESTS
44 07407 102620 INT07:  SUBZR 0,0
45 07410 040001         STA 0,1
46 07411 101120         MOVZL 0,0
47 07412 040000         STA 0,0
48 07413 060177         NIOS CPU
49 07414 060211         NIOC TTO
50 07415 060210         NIOC TTI
51 07416 000401         JMP .+1
52 07417 024000         LDA 1,0
53 07420 101004         MOV 0,0,SZR
54 07421 063077         HALTE             ;NIOC FAILED TO STOP INTERRUPT
55 07422 063511         SKPBZ TTO
56 07423 063077         HALTE             ;NIOC DID NOT MAKE TTY BUSY=0
57 07424 063411         SKPBN TTO
58 07425 101001         MOV 0,0,SKP
59 07426 063077         HALTE    ;TTO BUSY SHD =0
60 07427 063711         SKPDZ TTO
```

```
 0135 N3LGC
01 07430 063077          HALTE   ;TTO DONE SHD =0
02 07431 063611          SKPDN TTO
03 07432 101001          MOV 0,0,SKP
04 07433 063077          HALTE
05 07434 060277          NIOC CPU          ;RESET ION
06 07435 063577          SKPBZ CPU
07 07436 063077          HALTE
08 07437 002401          JMP .+1
09 07440 006612          ID.00
```

```
10136 N3LGC
01                  ;60 PASSES THROUGH INTERRUPT TESTS = PASS COMPLETE
02 07441 020125 PASSC:  LDA 0,K215        ;TRY VARIOUS WAIT LOOPS
03 07442 061111         DOAS 0,TTO        ;OUT CAR RET
04 07443 063411         SKPBN TTO         ;BUSY SHD=1
05 07444 063077         HALTE
06 07445 063711         SKPDZ TTO         ;DONE SHD=0
07 07446 063077         HALTE
08 07447 063511         SKPBZ TTO         ;WAIT LOOP
09 07450 000777         JMP .-1           ;FIRST TIME THIS WAY
10 07451 063611         SKPDN TTO         ;DONE=1 IF REAL "BZ"
11 07452 063077         HALTE
12                  ;NOW OUTPUT LINE FEED
13 07453 024126         LDA 1,K212
14 07454 065111         DOAS 1,TTO
15 07455 063711         SKPDZ TTO
16 07456 063077         HALTE
17 07457 063411         SKPBN TTO
18 07460 063077         HALTE
19 07461 063611         SKPDN TTO         ;FIRST SKPDN
20 07462 000777         JMP .-1           ;WAIT LOOP
21 07463 063511         SKPBZ TTO         ;BUSY=0 IF REAL DONE
22 07464 063077         HALTE
23                  ;OUTPUT P
24 07465 030132         LDA 2,K320
25 07466 071111         DOAS 2,TTO
26 07467 063511         SKPBZ TTO         ;ION STILL=1
27 07470 000777         JMP .-1           ;WHEN IT=0 TTO DONE
28 07471 063611         SKPDN TTO         ;TTO DONE=0
29 07472 063077         HALTE             ;BZ BEFORE INTR
30
```

```
0137 N3LGC
01
02                      ;OUTPUT "A"
03 07473 034105                 LDA 3,K300
04 07474 175400                 INC 3,3
05 07475 024140                 LDA 1,KATSW
06 07476 060177                 NIOS CPU
07 07477 075111                 DOAS 3,TTO
08 07500 125004                 MOV 1,1,SZR     ;DON'T CHECK ION IF RUNNING CAT
09 07501 000403                 JMP .+3
10 07502 063477                 SKPBN CPU       ;ION SHD STILL=1
11 07503 063077                 HALTE
12 07504 020116 PASL1:  LDA 0,KCBO
13 07505 126000                 ADC 1,1         ;DO XOR'S
14 07506 131000                 MOV 1,2         ;WHILE WAITING
15 07507 113520                 ANDZL 0,2       ;ODD BITS XOR'D TO
16 07510 107000                 ADD 0,1         ;-1=ENEN BITS
17 07511 146400                 SUB 2,1         ;XOR'D TO =1
18 07512 152000                 ADC 2,2         ;AGAIN SHOULD=
19 07513 155000                 MOV 2,3         ;THE ODD BITS
20 07514 137520                 ANDZL 1,3
21 07515 133000                 ADD 1,2
22 07516 172400                 SUB 3,2
23 07517 142414                 SUB# 2,0,SZR
24 07520 063077                 HALTE           ;PROCESSOR ARITH ERR
25 07521 063577                 SKPBZ CPU       ;INTR OCCUR YET
26 07522 000762                 JMP PASL1       ;NO
27 07523 063611                 SKPDN TTO       ;TTO YES DONE=1
28 07524 063077                 HALTE           ;NO ERROR AT "BZ"
29 07525 030127                 LDA 2,K323
30 07526 071111                 DOAS 2,TTO      ;OUTPUT FIRST S
31 07527 063511                 SKPBZ TTO               ;WAIT FOR TTO
32 07530 000777                 JMP .-1
33 07531 063611                 SKPDN TTO               ;DONE SHD =1
34 07532 063077                 HALTE
35 07533 071111                 DOAS 2,TTO              ;OUTPUT SECOND S
36 07534 063511                 SKPBZ TTO
37 07535 000777                 JMP .-1
38 07536 060211                 NIOC TTO
39
40                      ;DTOS MONITOR STUFF
41 07537 034045                 LDA 3,45
42 07540 021404                 LDA 0,4,3
43 07541 101005                 MOV 0,0,SNR     ;SKP IS DTOS RUN
44 07542 000417                 JMP NXTPAS
45 07543 020140                 LDA 0,KATSW
46 07544 101005                 MOV 0,0,SNR     ;SKP IS CAT ALREADY STARTED
47 07545 000415                 JMP CKCAT
48 07546 034045 ATOCK:  LDA 3,45
49 07547 021400                 LDA 0,0,3       ;GET AUTO SWITCH
50 07550 101005                 MOV 0,0,SNR     ;SKP IS AUTO-RUN
51 07551 000410                 JMP NXTPAS      ;NOT AUTO,CONTINUE
52 07552 015403                 DSZ 3,3
53 07553 000406                 JMP NXTPAS
54 07554 062677                 IORST
55 07555 021403                 LDA 0,3,3
56 07556 035404                 LDA 3,4,3
57 07557 041776                 STA 0,-2,3
58 07560 001400                 JMP 0,3         ;RETURN TO DTOS
59 07561 000201 NXTPAS: JMP A1A
60
```

```
0138 N3LGC
01
02                      ;CKCAT= CHECK IF DTOS RUN WITH CAT
03 07562 021402 CKCAT:  LDA 0,2,3       ;GET DTOS CAT SWITCH
04 07563 101005                 MOV 0,0,SNR     ;SKP IS WITH CAT/KITTEN
05 07564 000752                 JMP ATOCK       ;NO CAT/KITTEN
06 07565 040140                 STA 0,KATSW     ;SET SWITCH
07 07566 020076                 LDA 0,K3.3K
08 07567 040124                 STA 0,TESTK     ;SET UP FOR LONG LOOP COUNT
09 07570 025404                 LDA 1,4,3       ;GET DTOS START ADDR
10 07571 030136                 LDA 2,K1377
11 07572 146400                 SUB 2,1         ;FORM CAT/KITTEN ADDR
12 07573 135000                 MOV 1,3
13 07574 005400                 JSR 0,3         ;START CAT/KITTEN
14 07575 000751                 JMP ATOCK
15
                        .TITL N3LGC
17                      .END
```

```
JSR00 005056      95/05   95/07
JSR01 005070      95/16   95/18
JSR02 005340     101/21
K0    000122       4/09  110/40  111/36  115/17
K0777 000103       3/53  111/22  112/18
K1    000055       3/31   79/04   79/30   79/36   79/42   79/48   79/54
                  79/60   80/06   80/12   80/18   80/24   80/30   80/36
                  81/19   84/46   87/03  120/06  120/22
K10   000064       3/38   81/40   85/37   87/54   95/31  101/22  103/19
                 104/44  120/07  120/25  122/14  134/35
K100  000067       3/41   82/01   86/28   88/45   96/36  105/20  120/08
                 120/28
K1000 000073       3/45   82/22   85/04   87/19  105/56
K100K 000102       3/52   83/04   86/46   89/01  107/08
K10K  000077       3/49   82/43   85/55   88/10  106/32
K1377 000136       4/21  138/10
K2    000056       3/32   81/26   85/03   87/20  104/20  115/29  121/08
                 131/22  132/03
K20   000065       3/39   81/47   85/54   88/11   97/05   99/24  101/06
                 104/56
K200  000070       3/42   82/08   86/45   89/02   96/35   96/48  105/32
K2000 000074       3/46   82/29   85/21   87/36  106/08
K20K  000100       3/50   82/50   86/12   88/27  106/44
K210  000111       3/59   96/06   96/15   96/23   97/18   98/26
K212  000126       4/13  136/13
K215  000125       4/12  136/02
K2525 000117       4/05  110/54  111/50
K3    000057       3/33  119/33
K300  000105       3/55   96/47   98/06   99/07   99/36  100/25  101/07
                 101/27  137/03
K320  000132       4/17  136/24
K323  000127       4/14  137/29
K377  000131       4/16  117/06  117/21
K3.3K 000076       3/48  122/12  138/07
K4    000060       3/34   81/33   85/20   87/37  104/32
K40   000066       3/40   81/54   86/11   88/28  105/08  115/53
K400  000072       3/44   82/15   84/47   87/02   97/06  105/44  109/24
                 114/06  114/16  114/25  114/26  114/38  117/25  117/52
                 119/07  119/37  120/02  120/31  121/07
K4000 000075       3/47   82/36   85/38   87/53  106/20
K405  000071       3/43  115/25
K40K  000101       3/51   82/57   86/29   88/44  106/56
K420  000120       4/07
K5    000061       3/35   95/11
K5252 000116       4/06  111/08  112/04  123/54  124/08  124/22  124/36
                 124/50  125/04  125/18  125/32
K6    000062       3/36  115/41
K60   000123       4/10  134/33
K7    000063       3/37   95/24  103/04
KATSW 000140       4/23    6/05  122/03  137/05  137/45  138/06
KCBE  000115       4/03  103/08
KCBC  000116       4/04    4/06  103/21  137/12
KD11  000107       3/57   99/05
KD17  000110       3/58   99/25
KD21  000113       4/01   99/34
KD300 000106       3/56  109/20
KD37  000114       4/02   99/47
KJRET 000121       4/08  101/31
```



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KLDA, 000104       3/54   92/08
KMB   000112       3/60   99/27
KTTC  000130       4/15
LDA00 004127      79/02
LDA29 004712      92/06
LDA30 004717      92/14
LDA31 004725      92/22
LDA32 004733      92/29
LDA33 004745      92/41
LDA34 005104      95/31
LDA36 005314     100/25
LDA37 005326     101/06
LDA38 005504     103/34
LDAT1 001016  MC   79/19   79/27   79/33   79/39   79/45   79/51   79/57
                  80/03   80/09   80/15   80/21   80/27   80/33
LDAT2 001035  MC   81/05   81/17   81/24   81/31   81/38   81/45   81/52
                  81/59   82/06   82/13   82/20   82/27   82/34   82/41
                  82/48   82/55   83/02
NEG00 003216      64/05
NEG01 003223      64/14
NEG19 003533      71/03
NEG20 003545      71/18
NEG21 003551      71/25
NEGTS 000602  MC   64/23   65/09   65/31   65/53   66/15   66/37   66/59
                  67/21   67/43   68/05   68/27   68/49   69/11   69/33
                  69/55   70/17   70/39
NG19A 003541      71/10
NIN00 007000     126/38
NIN01 007027     126/47
NIN02 007033     126/51
NIN03 007037     127/04
NIN04 007043     127/10
NIN05 007047     127/15
NIN06 007053     127/20
NIN07 007057     127/25
NIN08 007063     127/30
NIN15 007126     129/04
NIN16 007132     129/10
NIN17 007137     129/17
NIN18 007144     129/24
NIN19 007152     129/31
NIN20 007157     129/37
NIN21 007164     129/45
NIN22 007170     130/02
NLD1  004634      90/15
NLD2  004643      90/23
NLD3  004652      90/31
NLD4  004661      90/39
NOLOD 001140  MC   90/05   90/14   90/22   90/30   90/38
NXTPA 007561     137/44  137/51  137/53  137/59
PASL1 007504     137/12  137/26
PASSC 007441     122/18  134/39  136/02
PKR00 000134       4/19    6/07  122/06  122/09  122/16  130/08  130/11
                 134/26  134/29  134/36
PKR01 000135       4/20    6/08  122/08  122/15  130/10  134/28  134/37
PP03E 006253     115/18  115/26
PP04E 006265     115/30  115/38
PP05E 006277     115/42  115/50
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PP06E 006311      115/54  116/02
PP.00 006204      114/15
PP.01 006213      114/24
PP.02 006223      114/35
PP.03 006243      115/17
PP.04 006255      115/29
PP.05 006267      115/41
PP.06 006301      115/53
PP.07 006313      117/06
PP.09 006365      117/52
PP.8R 006346      117/29  117/35
PWCSS 006607      122/05  123/05
PSPT  001332  MC  115/03  115/16  115/28  115/40  115/52
RESTR 000170       6/03
RTTTA 006473      120/01  120/17
RT.01 006453      120/01
SHIFT 000065  MC   17/04   17/21   17/31   17/41   17/51   18/01   18/11
                   18/21   18/31   18/41   18/51   19/01   19/11   19/21
                   19/31   19/41   20/10   20/20   20/30   20/40   20/50
                   20/60   21/10   21/20   21/30   21/40   21/50   21/60
                   22/10   22/20   22/30
SHIFZ 000141  MC   23/03   24/02   24/16   24/30   24/44   24/58   25/12
                   25/26   25/40   25/54   26/08   26/22   26/36   26/50
                   27/04   27/18   28/02   28/16   28/30   28/44   28/58
                   29/12   29/26   29/40   29/54   30/08   30/22   30/36
                   30/50   31/04   31/18
STA00 004700       91/22
STA01 004705       91/28
STA02 005116       96/06
STA03 005123       96/15
STA04 005131       96/23
STA05 005137       96/35
STA06 005147       96/47
STA07 005156       97/05
STA08 005166       97/18
STA09 005202       98/06
STA10 005217       98/26
STA11 005234       99/05
STA12 005247       99/24   99/31   99/35
STA13 005454      103/04
STA14 005471      103/19
START 000200        6/09    6/11
STEK2 006322      117/08  117/13
STK.0 006012      110/05
STOV1 006522      121/05
STOV2 006536      121/10  121/20
STTST 001261  MC  110/21  110/39  110/53  111/07  111/21  111/35  111/49
                  112/03  112/17
ST.00 006022      110/40
ST.01 006036      110/54
ST.02 006052      111/08
ST.03 006066      111/22
ST.04 006102      111/36
ST.05 006116      111/50
ST.06 006132      112/04
ST.07 006146      112/18
ST.08 006162      113/03
SUB00 003555       72/05
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SUB01 003560       72/09
SUBTS 000726  MC   72/17   73/02   73/21   73/40   73/59   74/18   74/37
                   74/56   75/15   75/34   75/53   76/12   76/31   76/50
                   77/09   77/28   77/47
SV.00 006400      119/05
SWP00 004340       84/06
SWP01 004343       84/09
SWP02 004346       84/12
SWP03 004351       84/15
SWPTS 001054  MC   84/21   84/42   84/59   85/16   85/33   85/50   86/07
                   86/24   86/41   86/58   87/15   87/32   87/49   88/06
                   88/23   88/40   88/57
SWREG 000146       4/29
TESTK 000124       4/11  122/10  122/13  134/30  134/34  138/08
TPACT 001224  MC  108/20  108/32  108/43  108/54  109/05
TPADR 000047       5/18  108/07  108/34  108/45  108/56  109/07  109/21
                  117/30
TPLOC 000046       5/17  108/13  117/27  117/37
TP.00 005721      108/06
TP.01 005734      108/33
TP.02 005745      108/44
TP.03 005756      108/55
TP.04 005767      109/06
TP.05 006000      109/20
TP.08 006330      117/21
TP.5R 006011      109/22  109/29
TSTLC 000137       4/22  120/18  120/38
TT000 007202      131/06
XXYZ  000441       12/29   12/31
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