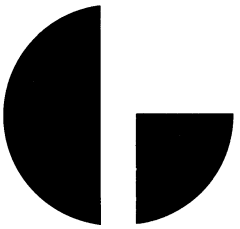

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PROGRAM

Nova 1200 Logic Test

TAPES

Binary 095-000036-01

ABSTRACT

Nova 1200 Logic Test is a maintenance program designed to test the Nova 1200 central processing unit. It is a gate by gate test of the logic used to implement the Nova 1200 instruction set. The test does not include any input or output equipment.

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096-000150-01

```
0001   .MAIN
01
02   .
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: 12LGCTST.SR                          PART NUMBER: 094-000092
10              ;
11              ;
12              ; DESCRIPTION: NOVA 1200 LOGIC TEST
13              ;
14              ;
15              ; REVISION HISTORY:
16              ;
17              ;       REV.            DATE
18              ;
19              ;       00              12/04/70
20              ;       01              02/01/74
21              ;
22              ;
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25              ;*****************************************************************
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```
A 0002  .MAIN
01
02                  ;                   NOVA 1200 LOGIC TEST
03
04
05                  ;1.     ABSTRACT
06                  ;           NOVA 1200 LOGIC TEST IS A MAINTENANCE PROGRAM
07                  ;           DESIGNED TO TEST THE NOVA 1200 CENTRAL PROCESS-
08                  ;           ING UNIT. IT IS A GATE BY GATE TEST OF THE
09                  ;           LOGIC USED TO IMPLEMENT THE NOVA 1200 INSTRUCT-
10                  ;           ION SET. THE TEST DOES NOT INCLUDE ANY INPUT
11                  ;           OR OUTPUT EQUIPMENT.
12
13                  ;2.     MACHINE REQUIREMENTS
14                  ;2.1        NOVA 1200 PROCESSOR
15                  ;2.2        4K READ/WRITE MEMORY
16
17                  ;3.     SWITCH SETTINGS
18                  ;3.1        STARTING ADDRESS=400
19
20                  ;4.     OPERATING PROCEEDURE
21                  ;4.1        LOAD THE PROGRAM VIA THE BINARY LOADER
22                  ;4.2        SET THE SWITCHES TO 000400
23                  ;4.3        PRESS START
24                  ;4.4        PROCESSOR SHOULD HALT
25                  ;4.5        PRESS CONTINUE
26
27                  ;5.     ERROR DESCRIPTION
28                  ;5.1        THE HALT INSTRUCTION IS USED TO INDICATE ERRORS.
29                  ;5.2        WHEN A ERROR IS DETECTED RECORD THE STATE OF THE
30                  ;           MACHINE. CONSULT THE LISTING FOR POSSIABLE
31                  ;           CAUSES OF FAILURE. CONSTRUCT A PROGRAM LOOP
32                  ;           WHICH WILL REPRODUCE THE ERROR. SCOPE THE LOGIC.
33
34                  ;6.     PROGRAM DESCRIPTION
35                  ;           THIS PROGRAM IS A COLLECTION OF SMALL ROUTINES
36                  ;           EACH DESIGNED TO TEST A PORTION OF THE PROCESSOR
37                  ;           LOGIC. EACH ROUTINE IS DESIGNED TO TEST AS
38                  ;           SMALL A PART OF THE LOGIC AS POSSIABLE. EACH TEST
39                  ;           IN THE SEQUENCE IS BASED ON PREVIOUS TEST WORKING.
40
41                  ;7.     MISC
42                  ;           THE TIME FOR ONE COMPLETE PASS IS MEASURED IN
43                  ;           MILLISECONDS.
```

```
▲ 0003   .MAIN
01
02 ..      000000 .LOC 0
03 00000 063077          HALT
04 00001 100000          @0
05 00002 063077          HALT                ;START AT 400, NOT HERE.
06
07         000043        .LOC 43
08 00043 002044 START:   JMP @.+1
09 00044 000400          A00
10 00045 000046          EGGS
11 00046 000000 EGGS:    0                   ;HEN FLAG
12 00047 000000          0                   ;NOT USED
13 00050 000000          0                   ;DATA BLOCK ADDR
14 00051 000000          0                   ;# OF PASSES
15 00052 000000          0                   ;RETURN ADDR
16
17         000121 .LOC 121
18 00121 000000 PASS:    0                   ;ITERATION COUNTER
19
20 00122 000000 K0:      0
21 00123 177777 M1:      -1
22 00124 177776 M2:      -2
23 00125 177775 M3:      -3
24 00126 177773 M5:      -5
25 00127 177767 M9:      177767
26 00130 100000 K100K:   100000
27 00131 040000 K40K:    40000
28 00132 020000 K20K:    20000
29 00133 010000 K10K:    10000
30 00134 000377 K377:    377
31 00135 000001 K1:      1
32 00136 000003 K3:      3
33 00137 000007 K7:      7
34 00140 000017 K17:     17
35 00141 000004 K4:      4
36 00142 000010 K10:     10
37 00143 000002 K2:      2
38 00144 000020 K20:     20
39 00145 000200 K200:    200
40
41 00146 167356 K1673:   167356
42 00147 156735 K1567:   156735
43 00150 135673 K1356:   135673
44 00151 073567 K0735:   073567
45 00152 010421 K0104:   010421
46 00153 021042 K0210:   021042
47 00154 042104 K0421:   042104
48 00155 104210 K1042:   104210
49 00156 001234 K1234:   1234
50 00157 000420 K420:    420
51 00160 010020 K1002:   10020
52 00161 000123 K123:    123
53 00162 002707 ER:      ERR
54         006162 EHALT=JSR @ER
55
```

```
A 0004   .MAIN
01
02          000400 .LOC 400                 ;THE PROGRAM STARTS HERE
03
04  00400 063700 A00:   SKPDZ 0             ;THE COMPUTER SHOULD STOP.
05  00401 000401        JMP .+1             ;THIS TEST FOR PROPER OPERATION
06  00402 024046        LDA 1,EGGS          ;OF THE HALT INSTRUCTION.
07  00403 125005        MOV 1,1,SNR         ;PRESS CONTINUE TO RESUME TEST.
08  00404 063077        HALT
09
10  00405 063700 A01:   SKPDZ 0             ;INSTRUCTION SHOULD SKIP THE
11  00406 006162        EHALT               ;EHALT. PERHAPS SKIP FLOP FAIL
12                                          ;TO SET. ALSO CHECK ADD ONE
13                                          ;LOGIC AT PTG=0,TS3 OF THE
14                                          ;SKIP.
15
16  00407 063777 A02:   SKPDZ CPU           ;THIS SKIP INSTRUCTION WILL EHALT
17  00410 000401        JMP .+1             ;THE PROCESSOR IF IR7 FAILS TO
18                                          ;SET. CHECK AND GATE FORMING
19                                          ;EHALT, THE IR7 INPUT.
20
21  00411 063777 A03:   SKPDZ CPU           ;CHECK TO INSURE (PWR LOW)
22  00412 006162        EHALT               ;FROM THE POWER SUPPLY IS O.K.
23                                          ;CHECK O.C. GATE OF (CPU INST,
24                                          ;PWR LOW) TO THE SKIP FLOP LOGIC.
25
26  00413 063677 A03A:  SKPDN CPU           ;THE "SKPDN" INSTRUCTION SHOULD
27  00414 063700        SKPDZ 0             ;NOT SKIP BUT IT DID. CHECK
28  00415 006162        EHALT               ;THE EXCLUSIVE OR GATE (MBC 9,
29                                          ;WITH THE SKIP CONDITION).
30
31  00416 063500 A04:   SKPBZ 0             ;THE SELB LINE SHOULD BE
32  00417 006162        EHALT               ;POSITIVE AND THE EHALT SKIPPED.
33                                          ;CHECK THE OR/AND GATE FEEDING
34                                          ;THE XOR WITH (MBC 9) TO SKIP FLOP.
35
36  00420 060700 A05:   DIAP 0,0            ;THE DIA INSTRUCTION SHOULD
37  00421 063500        SKPBZ 0             ;NOT SKIP BECAUSE I/O SKIP
38  00422 006162        EHALT               ;SHOULD NOT BE ASSERTED. CHECK
39                                          ;AND/OR GATE WITH (IO SKIP) FEEDING
40                                          ;THE SKIP FLOP.
41
42  00423 061700 A06:   DIBP 0,0            ;THE DIB INSTRUCTION SKIPPED.
43  00424 063500        SKPBZ 0             ;CHECK FOR FALSE DECODE OF
44  00425 006162        EHALT               ;DATIB. IO SKIP SHOULD NOT ASSERT.
45
46  00426 062700 A07:   DICP 0,0            ;THE DIC INSTRUCTION SKIPPED.
47  00427 063500        SKPBZ 0             ;CHECK FOR FALSE DECODE OF
48  00430 006162        EHALT               ;DATIC. IO SKIP SHOULD NOT ASSERT.
49
```

```
A 00005  .MAIN
01
02 00431 102400 A08:    SUB 0,0          ;THESE "DOC" INSTRUCTIONS SHOULD
03 00432 063076         DOC 0,76         ;NOT ASSERT THE CPU INST LEVEL.
04 00433 063075         DOC 0,75         ;IF THAY DO THE COMPUTER WILL
05 00434 063073         DOC 0,73         ;ASSUME A EHALT INSTRUCTION AND
06 00435 063067         DOC 0,67         ;STOP. CHECK THE AND GATES FORMING
07 00436 063057         DOC 0,57         ;CPU INST AND THE MBC10-MBC15
08 00437 063037         DOC 0,37         ;FLOPS.
09
10 00440 062677 A09:    IORST            ;THE ION FLOP SHOULD BE OFF
11 00441 063577         SKPBZ CPU        ;(SEE CONSOLE LIGHT). THE EHALT
12 00442 006162         EHALT            ;SHOULD BE SKIPPED. CHECK D.C.
13                                       ;GATE (CPU INST,ION) TO THE
14                                       ;SKIP LOGIC.
15
16 00443 060100 A10:    NIOS 0           ;A STRT PULSE TO DEVICE 0
17 00444 063577         SKPBZ CPU        ;SHOULD NOT SET THE ION FLOP.
18 00445 006162         EHALT            ;CHECK DECODER FOR PULSES,
19                                       ;CPU INST SHOULD PREVENT
20                                       ;THE (SET ION) LEVEL.
21
22 00446 060377 A11:    NIOP CPU         ;A "P" PULSE TO THE PROCESSOR
23 00447 063577         SKPBZ CPU        ;SHOULD NOT SET THE ION FLOP.
24 00450 006162         EHALT            ;CHECK THE DECODER FOR PULSES.
25
26 00451 060277 A12:    NIOC CPU         ;A "C" PULSE SHOULD NOT SET
27 00452 063577         SKPBZ CPU        ;THE ION FLOP. CHECK PULSE
28 00453 006162         EHALT            ;DECODER.
29
30 00454 102040 A13:    ADCO 0,0         ;THE "ADC" INSTRUCTION SKIPPED.
31 00455 063500         SKPBZ 0          ;CHECK EXCLUSIVE OR GATE
32 00456 006162         EHALT            ;AND THE AND/OR GATE FEEDING
33                                       ;THE SKIP FLOP. MBC15 SHOULD
34                                       ;NOT BE TRUE.
35
36 00457 102041 A14:    ADCO 0,0,SKP     ;THE"ADC" INSTRUCTION SHOULD SKIP.
37 00460 006162         EHALT            ;CHECK EXCLUSIVE OR GATE AND
38                                       ;THE AND/OR GATE FEEDING THE
39                                       ;SKIP FLOP , ETC.
40
41 00461 102021 A15:    ADCZ 0,0,SKP     ;THE "ADC" INSTRUCTION SHOULD SKIP.
42 00462 006162         EHALT            ;CHECK AND/OR GATE (MBC14,
43                                       ;CRY SET SAVE) THE MBC14 INPUT
44                                       ;SHOULD NOT BE TRUE. SEE SKIP
45                                       ;FLOP LOGIC.
46
47 00463 102401 A16:    SUB 0,0,SKP      ;THE "SUB" INSTRUCTION SHOULD SKIP.
48 00464 006162         EHALT            ;CHECK AND/OR GATE (MBC13,
49                                       ;ZEROS) THE MBC13 INPUT SHOULD
50                                       ;NOT BE TRUE. SEE SKIP FLOP LOGIC.
```

```
▲ 00006  .MAIN
01
02 00465 102177 A17:    ADCCL# 0,0,SBN   ;THE "ADC" INSTRUCTION SET
03 00466 000401          JMP .+1          ;THE ION FLOP. CHECK AND
04 00467 063577          SKPBZ CPU        ;GATE (IO.E,AND ENAB,PULSE ENAB).
05 00470 006162          EHALT            ;THE IO.E LEVEL SHOULD NOT
06 00471 102400          SUB 0,0          ;BE TRUE DURING ADC INSTRUCTION.
07
08 00472 103420 A18:     ANDZ 0,0         ;TEST FOR ZERO CARRY. IF
09 00473 103422          ANDZ 0,0,SZC     ;CARRY LIGHT IS OUT, CHECK AND
10 00474 006162          EHALT            ;GATE (CRY SET SAVE,MBC14) INPUT
11                                        ;TO SKIP LOGIC. IF THE CARRY
12                                        ;LIGHT IS ON , CHECK THE
13                                        ;INPUTS TO THE CARRY FLOP.
14
15 00475 103423 A19:     ANDZ 0,0,SNC     ;CARRY IS ZERO. THIS INSTRUCTION
16 00476 101001          MOV 0,0,SKP      ;SHOULD NOT SKIP. CHECK THE
17 00477 006162          EHALT            ;EXCLUSIVE OR GATE WITH MBC15
18                                        ;IN THE SKIP LOGIC.
19
20 00500 103440 A20:     ANDO 0,0         ;CARRY CHOULD BE CLEARED FROM
21 00501 103422          ANDZ 0,0,SZC     ;A ONE TO A ZERO. CHECK CARRY
22 00502 006162          EHALT            ;LIGHT. CHECK OR/AND GATE (CARRY,
23                                        ;MBC11,CARRY,MBC10) TO EXCLUSIVE
24                                        ;OR GATE PRODUCING CRY ENAB.
25
26 00503 103420 A21:     ANDZ 0,0         ;CARRY SHOULD BE SET. SEE
27 00504 103443          ANDO 0,0,SNC     ;CONSOLE LIGHT. IF LIGHT IS
28 00505 006162          EHALT            ;ON, CHECK AND/OR GATE
29                                        ;(CRY SET SAVE,MBC14) IN THE
30                                        ;SKIP LOGIC. IF CARRY LIGHT IS
31                                        ;OUT CHECK AND/OR GATE
32                                        ;(CARRY,MBC11,CARRY,MBC10) TO
33                                        ;XOR GATE PRODUCING CRY ENAB.
34
35 00506 103440 A22:     ANDO 0,0         ;CARRY SHOULD BE SET. SEE
36 00507 103443          ANDO 0,0,SNC     ;PREVIOUS TEST FOR POSSIABLE
37 00510 006162          EHALT            ;CAUSE OF FAILURE.
38
39 00511 103420 A23:     ANDZ 0,0         ;THE FACT THAT CARRY WAS
40 00512 103402          AND 0,0,SZC      ;CLEARED SHOULD BE REMEMBERED
41 00513 006162          EHALT            ;BY THE CARRY FLOP. CHECK THE
42                                        ;CARRY FLOP INPUTS, ALSO THE
43                                        ;OR/AND GATE (CARRY,MBC11,CARRY
44                                        ;MBC10).
45
46 00514 103440 A24:     ANDO 0,0         ;THE FACT THAT CARRY WAS
47 00515 103403          AND 0,0,SNC      ;SET SHOULD BE REMEMBERED
48 00516 006162          EHALT            ;BY THE CARRY FLOP. SEE THE
49                                        ;PREVIOUS TEST.
```

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▲ 0007   .MAIN
01
02 00517 103440 A25:    ANDO 0,0          ;CARRY SHOULD BE SET TO (1).
03 00520 103462          ANDC 0,0,SZC      ;CARRY SHOULD COMPLIMENT
04 00521 006162          EHALT             ;TO ZERO. CHECK OR/AND GATE
05                                         ;(CARRY,MBC11,CARRY,MBC10).
06
07 00522 103420 A26:     ANDZ 0,0          ;CARRY SHOULD BE SET TO (0).
08 00523 103463          ANDC 0,0,SNC      ;CARRY SHOULD COMPLIMENT
09 00524 006162          EHALT             ;TO ONE. SEE PREVIOUS TEST.
10
11 00525 102620 A27:     SUBZR 0,0         ;SET AC0 TO 100000.
12 00526 103422          ANDZ 0,0,SZC      ;CLEAR AND TEST CARRY. CHECK
13 00527 006162          EHALT             ;AND GATE INPUTS (SHL,ADDER 0)
14                                         ;TO AND/OR GATE PRODUCION
15                                         ;CRY SET.
16
17 00530 102520 A28:     SUBZL 0,0         ;SET AC0 TO 000001.
18 00531 103422          ANDZ 0,0,SZC      ;CLEAR AND TEST CARRY. CHECK
19 00532 006162          EHALT             ;AND GATE INPUTS (SHR,ACB11)
20                                         ;TO AND/OR GATE PRODUCING
21                                         ;CRY SET.
22
23 00533 103420 A29:     ANDZ 0,0          ;CARRY IS SET TO ZERO VIA AND.
24 00534 101002          MOV 0,0,SZC       ;CARRY SHOULD STILL TEST ZERO
25 00535 006162          EHALT             ;ON THE MOV INSTRUCTION. CHECK
26                                         ;AND GATE (CRY OUT,AND) FEEDING
27                                         ;EXCLUSIVE OR GATE IN CARRY LOGIC.
28
29 00536 103421 A30:     ANDZ 0,0,SKP      ;CARRY IS CLEARED VIA THE AND
30 00537 101040          MOVO 0,0          ;INSTRUCTION AND SHOULD NOT BE
31 00540 103412          AND# 0,0,SZC      ;SET VIA THE SKIPPED "MOV".
32 00541 006162          EHALT             ;CHECK 4 INPUT AND GATE
33                                         ;PRODUCING LOAD CRY, THE
34                                         ;(ALC.SKIP) INPUT.
35
36 00542 103440 A31:     ANDO 0,0          ;CARRY IS SET VIA THE AND
37 00543 000401          JMP .+1           ;INSTRUCTION. MBC12 ON THE
38 00544 101003          MOV 0,0,SNC       ;"MOVZ" INSTRUCTION SHOULD
39 00545 006162          EHALT             ;PREVENT CARRY FROM CLEARING.
40                                         ;CHECK 4 INPUT AND GATE TO "C"
41                                         ;INPUT OF CARRY FLOP. LOAD CRY
42                                         ;SHOULD NOT BE TRUE DURING "MOVZ".
43
44 00546 102000 A32:     ADC 0,0           ;SET AC TO (-1). CLEAR CARRY
45 00547 103722          ANDZS 0,0,SZC     ;AND SWAP RESULTS. THE CARRY
46 00550 006162          EHALT             ;WAS SET HOWEVER. CHECK FOR
47                                         ;A FALSE DECODE OF SHL, OR
48                                         ;SHR LEVEL.
49
50 00551 034402 A32A:    LDA 3,.+2         ;A LDA INSTRUCTION CHANGED THE
51 00552 101001          MOV 0,0,SKP       ;PC. CHECK FOR FALSE DECODE
52 00553 006162          EHALT             ;OF JSR. AND GATE (EFA,JMP+JSR,IR4).
53
54 00554 034122 A32B:    LDA 3,K0
55 00555 030122          LDA 2,K0
56 00556 024122          LDA 1,K0
```

```
A 0008   .MAIN
01
02 00557 020122 A33:    LDA 0,K0          ;CLEAR AC0 AND CARRY.
03 00560 103420         ANDZ 0,0          ;THE ADC INSTRUCTION SET
04 00561 102002         ADC 0,0,SZC       ;THE CARRY. PERHAPS ADD ONE
05 00562 006162         EHALT             ;ASSERTED FALSELY AT (PTG=0,TS3)
06                                        ;TIME OF THE ADC INSTRUCTION.
07                                        ;CHECK OR/AND GATE (ALC,IR7,
08                                        ;IR7,KEY) IN THE ADD ONE LOGIC.
09
10 00563 020123 A34:    LDA 0,M1          ;"ADC" SHOULD NOT PRODUCE A
11 00564 024123         LDA 1,M1          ;CARRY FROM THE ADDER. IF THE
12 00565 030123         LDA 2,M1          ;RESULT IN AC0 IS 177776 THE
13 00566 034123         LDA 3,M1          ;ADC INSTRUCTION DID NOT ADD THE
14 00567 102022         ADCZ 0,0,SZC      ;COMPLIMENT BUT DID A STRAIGHT
15 00570 006162         EHALT             ;ADD. CHECK AND GATE (ALC,IR6)
16                                        ;TO PRODUCE (S2) LEVEL TO THE
17                                        ;ADDER.
18
19 00571 062677 A35:    IORST             ;A "P" PULSE SHOULD NOT SET
20 00572 060377         NIOP CPU          ;THE ION FLOP. CHECK
21 00573 063577         SKPBZ CPU         ;THE DECODING OF SET ION
22 00574 006162         EHALT             ;LEVEL.
23
24 00575 060277 A36:    NIOC CPU          ;A "C" PULSE SHOULD NOT
25 00576 063577         SKPBZ CPU         ;SET THE ION FLOP. CHECK
26 00577 006162         EHALT             ;THE DECODE OF SET ION LEVEL.
27
28 00600 060077 A37:    NIO CPU           ;A NIO INSTRUCTION WITHOUT
29 00601 063577         SKPBZ CPU         ;A STRT PULSE SHOULD NOT
30 00602 006162         EHALT             ;SET THE ION FLOP.
31
32 00603 060177 A38:    NIOS CPU          ;A CLEAR PULSE TO THE
33 00604 060277         NIOC CPU          ;CPU FAILED TO CLEAR THE
34 00605 063577         SKPBZ CPU         ;ION FLOP. CHECK THE
35 00606 006162         EHALT             ;DECODE OF THE (CLR ION) LEVEL
36                                        ;AND THE CLR ION INPUT TO
37                                        ;THE ION FLOP.
38
39 00607 060177 A39:    NIOS CPU          ;SET AND TEST THE ION FLOP.
40 00610 063477         SKPBN CPU         ;IF THE CONSOLE ION LIGHT IS
41 00611 006162         EHALT             ;OUT CHECK FOR PROPER DECODE
42 00612 060277         NIOC CPU          ;OF (SET ION) LEVEL, THE SET AND
43                                        ;RESET INPUTS TO THE OR GATES
44                                        ;WHICH COMPRISE THE ION FLOP.
45                                        ;IF THE LIGHT IS ON CHECK THE
46                                        ;O.C. GATE (CPU INST,ION) TO THE
47                                        ;SKIP LOGIC. ALSO EXCLUSIVE OR GATE
48                                        ;WITH MBC9 IN THE SKIP LOGIC.
```

```
A 00009   .MAIN
01
02 00613 060177 A40:    NIOS CPU        ;THE "SKPBZ" INSTRUCTION
03 00614 063577         SKPBZ CPU       ;SKIPPED WHEN ION WAS SET.
04 00615 103401         AND 0,0,SKP     ;CHECK THE EXCLUSIVE OR GATE
05 00616 006162         EHALT           ;WITH MBC9 IN THE SKIP LOGIC.
06 00617 060277         NIOC CPU
07
08 00620 060177 A41:    NIOS CPU        ;THE SKIP INSTRUCTION IS TESTED
09 00621 063500         SKPBZ 0         ;THE SELB LINE NOT THE ION FLOP.
10 00622 006162         EHALT           ;THE O.C. GATE (CPU INST,ION)
11 00623 060277         NIOC CPU        ;GROUNDS THE SELB LINE WHEN
12                                      ;CPU INST IS NOT PRESENT.
13
14 00624 060177 A42:    NIOS CPU        ;THE FACT THAT ION IS SET
15 00625 063777         SKPDZ CPU       ;SHOULD NOT EFFECT THE
16 00626 006162         EHALT           ;TESTING OF THE SELD LINE.
17 00627 060277         NIOC CPU        ;CHECK THE OR/AND GATE
18                                      ;(SELB,MBC8,MBC8,SELD).
19
20 00630 024122 A43:    LDA 1,K0        ;ACS SHOULD CONTAIN (-1)
21 00631 102022         ADCZ 0,0,SZC    ;EXCEPT AC1 WHICH CONTAINS
22 00632 006162         EHALT           ;ZEROS. IF THE "ADC" INSTRUCTION
23                                      ;SELECTED SOURCE AC1 NOT ZERO
24                                      ;A CARRY WOULD RESULD. CHECK
25                                      ;ACS2 SELECT LEVEL, SOURCE
26                                      ;AC SELECTION ETC.
27
28 00633 030122 A44:    LDA 2,K0        ;ACS SHOULD CONTAIN (-1)
29 00634 102022         ADCZ 0,0,SZC    ;EXCEPT AC 1 AND 2. IF THE
30 00635 006162         EHALT           ;ALC INSTRUCTION SELECTED SOURCE
31                                      ;AC2 NOT ZERO A CARRY WOULD
32                                      ;RESULT. CHECK ACS1 SEL LEVEL,
33                                      ;SOURCE AC SELECTION ETC.
34
35 00636 020122 A45:    LDA 0,K0        ;AC0=0 ALL OTHERS (-1).
36 00637 024123         LDA 1,M1        ;IF THE ADC INSTRUCTION SELECTS
37 00640 030124         LDA 2,M2        ;SOURCE AC0 INSTEAD OF AC1
38 00641 034125         LDA 3,M3        ;A CARRY WILL RESULT.
39 00642 126022         ADCZ 1,1,SZC    ;CHECK ACS 1 SEL LEVEL DURING
40 00643 006162         EHALT           ;THE ALC, ALSO CHECK SOURCE
41                                      ;AC MEMORY.
42
43 00644 152022 A46:    ADCZ 2,2,SZC    ;ACS 2 SEL LEVEL FAILED,
44 00645 006162         EHALT           ;SEE PREVIOUS TEST.
45
```

```
▲ 0010   .MAIN
01
02 00646 176005 A47:    ADC 3,3,SNR      ;ADD COMPLIMENT ANY NUMBER
03 00647 006162          EHALT            ;TO ITSELF SHOULD PRODUCE
04                                        ;MINUS ONE. CHECK INPUT
05                                        ;TO SKIP LOGIC AND/OR GATE
06                                        ;WITH MBC13.
07
08 00650 176400 A48:    SUB 3,3          ;ZERO RESULT SHOULD NOT
09 00651 175043          MOVO 3,3,SNC     ;AFFECT STATE OF CARRY SKIP.
10 00652 006162          EHALT            ;CHECK AND/OR GATE TO SKIP LOGIC.
11
12 00653 176000 A49:    ADC 3,3          ;ADC INSTRUCTION PRODUCES 177777
13 00654 175005          MOV 3,3,SNR      ;IN AC3. IF IR6 OF THT "MOV"
14 00655 006162          EHALT            ;FAILS THE RESULT IN AC3 WILL
15                                        ;BE ZERO AND NO SKIP.
16
17 00656 020122 A50:    LDA 0,K0         ;AC0 SHOULD BE LOADED WITH
18 00657 024123          LDA 1,M1         ;ZERO AND INCREMENTED TO
19 00660 101422          INCZ 0,0,SZC     ;+1. IF THE LOAD AC1 INSTRUCTION
20 00661 006162          EHALT            ;LOADED ZERO ALSO THE
21                                        ;INC WOULD SET THE CARRY.
22                                        ;CHECK ACS 2 SEL LEVEL.
23                                        ;SYNC SCOPE ON LDA AND PACK.
24
25 00662 020122 A51:    LDA 0,K0         ;IF LOAD AC2 INSTRUCTION LOADED
26 00663 030123          LDA 2,M1         ;AC ZERO INSTEAD, THEN INC
27 00664 101422          INCZ 0,0,SZC     ;INSTRUCTION WOULD SET THE CARRRY.
28 00665 006162          EHALT            ;CHECK ACS 1 SELECT LEVEL
29                                        ;DURING THE SECOND "LDA" INSTRUCTION.
30                                        ;SYNC SCOPE ON LDA AND PACK.
31
32 00666 024122 A52:    LDA 1,K0         ;IF LOAD AC0 REALLY LOADED AC1
33 00667 020123          LDA 0,M1         ;THE INC INSTRUCTION WOULD
34 00670 125422          INCZ 1,1,SZC     ;SET THE CARRY. CHECK AC
35 00671 006162          EHALT            ;SOURCE SELECTION FOR LDA.
36
37 00672 030122 A53:    LDA 2,K0         ;IF LOAD AC0 REALLY LOADED AC2
38 00673 020123          LDA 0,M1         ;THE INC INSTRUCTION WOULD
39 00674 151422          INCZ 2,2,SZC     ;SET THE CARRY. CHECK AC
40 00675 006162          EHALT            ;SOURCE SELECTION FOR LDA.
41
42 00676 020130 A54:    LDA 0,K100K      ;AC0 SHOULD CONTAIN 1000000
43 00677 101005          MOV 0,0,SNR      ;AND THE MOVE INSTRUCTION SHOULD
44 00700 006162          EHALT            ;SKIP. CHECK THE SHIFT 0 INPUT
45                                        ;TO THE 4 INPUT OR GATE IN
46                                        ;THE ZERO SKIP LOGIC.
```

```
A 0011   .MAIN
01
02 00701 020131 A55:     LDA 0,K40K        ;CHECK THE SHIFT 1 INPUT TO
03 00702 101005           MOV 0,0,SNR       ;THE 4 INPUT OR GATE IN THE
04 00703 006162           EHALT             ;SKIP ZERO LOGIC.
05
06 00704 020132 A56:     LDA 0,K20K        ;CHECK THE SHIFT 2 INPUT TO
07 00705 101005           MOV 0,0,SNR       ;THE 4 INPUT OR GATE IN
08 00706 006162           EHALT             ;THE SKIP ZERO LOGIC.
09
10 00707 020133 A57:     LDA 0,K10K        ;CHECK THE SHIFT 3 INPUT TO
11 00710 101005           MOV 0,0,SNR       ;THE 4 INPUT OR GATE IN
12 00711 006162           EHALT             ;THE SKIP ZERO LOGIC.
13
14 00712 020134 A58:     LDA 0,K377        ;THE ZERO SAVE FLOP SHOULD
15 00713 101005           MOV 0,0,SNR       ;REMEMBER THAT THE AC WAS
16 00714 006162           EHALT             ;NOT ALL ZEROS AND THUS
17                                          ;THE MOVE SHOULD SKIP. CHECK
18                                          ;ZERO SAVE SETTING, AND GATE
19                                          ;ON THE ONE  IP LOGIC, ETC.
20
21 00715 020122 A59:     LDA 0,K0          ;AC0 SHOULD BE LOADED WITH
22 00716 101405           INC 0,0,SNR       ;ZEROS AND INCREMENTED TO +1.
23 00717 006162           EHALT             ;CHECK TO INSURE ADD ONE
24                                          ;ASSERTS AT PTG=0,TS3 OF
25                                          ;THE INC INSTRUCTION.
26
27 00720 020135 A60:     LDA 0,K1          ;INCREMENT FROM +1 TO +2
28 00721 101405           INC 0,0,SNR
29 00722 006162           EHALT
30
31 00723 020136 A61:     LDA 0,K3          ;INCREMENT FROM +3 TO +4
32 00724 101405           INC 0,0,SNR
33 00725 006162           EHALT
34
35 00726 020137 A62:     LDA 0,K7          ;INCREMENT FROM +7 TO +10
36 00727 101405           INC 0,0,SNR
37 00730 006162           EHALT
38
39 00731 020140 A63:     LDA 0,K17         ;INCREMENT FROM +17 TO +20.
40 00732 101405           INC 0,0,SNR       ;THE INCREMENT RESULTED IN
41 00733 006162           EHALT             ;+0 NOT +20. CHECK AND GATE
42                                          ;(PTG=0,TS0,PTG=0,TS3,SERIAL CRY)
43                                          ;TO THE ADD ONE LOGIC. ALSO
44                                          ;CHECK SERIAL CRY FLOP.
```

```
A 0012  .MAIN
01
02 00734 020123 A64:    LDA 0,M1          ;ADDITION OF (-1) TO (-1)
03 00735 024123         LDA 1,M1          ;SHOULD PRODUCE (-2) AND A
04 00736 030123         LDA 2,M1          ;CARRY. CHECK AND GATE
05 00737 034123         LDA 3,M1          ;(AND,CRY OUT) TO THE
06 00740 103033         ADDZ# 0,0,SNC     ;EXCLUSIVE OF GATE PRODUCING
07 00741 006162         EHALT             ;CRY ENAB.
08
09 00742 103052 A65:    ADDO# 0,0,SZC     ;CHECK EXCLUSIVE OR GATE
10 00743 006162         EHALT             ;PRODUCING CRY-ENABLE. SEE
11                                        ;PREVIOUS TEST.
12
13 00744 103432 A66:    ANDZ# 0,0,SZC     ;CHECK AND GATE (AND,CRY OUT).
14 00745 006162         EHALT             ;CARRY SHOULD BE ZERO.
15
16
17 00746 024122 A67:    LDA 1,K0          ;AC0=-1, OTHER ACS=0.
18 00747 030122         LDA 2,K0          ;CHECK TO INSURE DESTINATION
19 00750 034122         LDA 3,K0          ;AC1 IS SELECTED ON THE MOV.
20 00751 020123         LDA 0,M1
21 00752 105000         MOV 0,1
22 00753 125015         MOV# 1,1,SNR
23 00754 006162         EHALT
24
25 00755 111000 A68:    MOV 0,2           ;CHECK TO INSURE DESTINATION
26 00756 151015         MOV# 2,2,SNR      ;AC2 IS SELECTED ON THE FIRST
27 00757 006162         EHALT             ;MOVE.
28
29 00760 020122 A69:    LDA 0,K0          ;TEST TO INSURE "ADD" USES
30 00761 024123         LDA 1,M1          ;THE DESTINATION AC.
31 00762 107005         ADD 0,1,SNR       ;CHECK AND/OR GATE (ALC,IR5)
32 00763 006162         EHALT             ;IN THE DISABLE D MULT LOGIC.
33
34 00764 020122 A70:    LDA 0,K0          ;0+1=1
35 00765 024135         LDA 1,K1          ;CHECK DESTINATION AC
36 00766 107005         ADD 0,1,SNR       ;BUFFER+MULTIPLEXOR.
37 00767 006162         EHALT
38
39 00770 020122 A71:    LDA 0,K0          ;SEE ABOVE
40 00771 024143         LDA 1,K2          ;0+2=2
41 00772 107005         ADD 0,1,SNR
42 00773 006162         EHALT
43
44 00774 020122 A72:    LDA 0,K0          ;SEE ABOVE
45 00775 024141         LDA 1,K4          ;0+4=4
46 00776 107005         ADD 0,1,SNR
47 00777 006162         EHALT
48
49 01000 020122 A73:    LDA 0,K0          ;SEE ABOVE
50 01001 024142         LDA 1,K10         ;0+10=10
51 01002 107005         ADD 0,1,SNR
52 01003 006162         EHALT
```

```
▲ 0013  .MAIN
01
02 01004 020123 A74:    LDA 0,M1          ;ADDITION OF (-1) TO (+0)
03 01005 024122          LDA 1,K0          ;SHOULD NOT PRODUCE A CARRY OUT.
04 01006 107022          ADD7 0,1,SZC      ;PERHAPS ADC OUT FAILED TO
05 01007 006162          EHALT             ;ASSERT AT TS3 TIME AND
06                                         ;MAC NOT DESTINATION AC WAS
07                                         ;ADDED.
08
09 01010 102001 A75:     ADC 0,0,SKP       ;ADC SETS AC0 TO (-1). THE
10 01011 102400          SUB 0,0           ;"SUB" BECAUSE IT IS SKIPPED SHOULD
11 01012 101005          MOV 0,0,SNR       ;NOT CHANGE C(AC0). LOAD CRY
12 01013 006162          EHALT             ;SHOULD PREVENT PACK AND LOAD AC.
13                                         ;CHECK INPUTS TO PACK FLOP.
14
15 01014 020122 A76:     LDA 0,K0          ;CHECK FOR LOADING OF AC0
16 01015 102000          ADC 0,0           ;VIA THE ADC INSTRUCTION.
17 01016 101005          MOV 0,0,SNR
18 01017 006162          EHALT
19
20 01020 102400 A77:     SUB 0,0           ;CHECK THAT AC0 IS LOADED
21 01021 020123          LDA 0,M1          ;VIA THE LDA INSTRUCTION. CHECK
22 01022 101005          MOV 0,0,SNR       ;OR GATES INPUTS TO PACK FLOP.
23 01023 006162          EHALT
24
25 01024 020122 A78:     LDA 0,K0          ;ANY NUMBER SUBTRACTED FROM
26 01025 102404          SUB 0,0,SZR       ;ITSELF SHOULD PRODUCE 0.
27 01026 006162          EHALT             ;IF C(AC0)=0 CHECK AND/OR
28                                         ;GATE (MBC13,ZEROS) TO
29                                         ;SKIP LOGIC. IF C(AC0) IS NOT
30                                         ;ZERO, SCOPE ACB REGISTER,
31                                         ;ADDER ETC.
32
33 01027 020123 A79:     LDA 0,M1          ;SEE PREVIOUS TEST
34 01030 102404          SUB 0,0,SZR
35 01031 006162          EHALT
36
37 01032 020123 A80:     LDA 0,M1          ;FIRST "SUB" SHOULD NOT
38 01033 102405          SUB 0,0,SNR       ;SKIP, SECOND SHOULD.
39 01034 102404          SUB 0,0,SZR
40 01035 006162          EHALT
41
42 01036 102000 A81:     ADC 0,0           ;ADC SETS ALL BITS.
43 01037 100004          COM 0,0,SZR       ;COM SHOULD COMPLIMENT
44 01040 006162          EHALT             ;THEM TO ALL ZEROS.
45
46 01041 102400 A82:     SUB 0,0           ;CHECK THAT MOV WILL
47 01042 105000          MOV 0,1           ;PICK UP ANY BITS.
48 01043 125014          MOV# 1,1,SZR
49 01044 006162          EHALT
```

```
A 0014   .MAIN
01
02 01045 102400 A83:     SUB 0,0          ;CHECK MOVE OF AC0 TO AC2
03 01046 024123          LDA 1,M1         ;WITH ALL ZEROS.
04 01047 030123          LDA 2,M1
05 01050 034123          LDA 3,M1
06 01051 111000          MOV 0,2
07 01052 153004          ADD 2,2,SZR
08 01053 006162          EHALT
09
10 01054 102400 A84:     SUB 0,0          ;CHECK MOVE OF AC0 TO AC3
11 01055 115000          MOV 0,3          ;WITH ALL ZEROS, CAN THE
12 01056 177004          ADD 3,3,SZR      ;DESTINATION AC HOLD ZEROS?
13 01057 006162          EHALT
14
15 01060 102400 A85:     SUB 0,0          ;CHECK MOVE OF AC0 TO AC0
16 01061 101000          MOV 0,0          ;WITH ALL ZEROS, CAN THE
17 01062 103004          ADD 0,0,SZR      ;DESTINATION AC HOLD ZEROS.
18 01063 006162          EHALT
19
20 01064 102400 A86:     SUB 0,0
21 01065 105000          MOV 0,1
22 01066 127004          ADD 1,1,SZR
23 01067 006162          EHALT
24
25 01070 020122 A87:     LDA 0,K0         ;TEST MOVING (MOV) OF ONES
26 01071 024122          LDA 1,K0         ;FROM AC3 TO AC0
27 01072 030122          LDA 2,K0         ;CHECK IF DESTINATION
28 01073 176000          ADC 3,3          ;AC CAN HOLD ONES.
29 01074 161000          MOV 3,0
30 01075 116404          SUB 0,3,SZR
31 01076 006162          EHALT
32
33 01077 176000 A88:     ADC 3,3          ;SEE PREVIOUS TEST.
34 01100 165000          MOV 3,1
35 01101 136404          SUB 1,3,SZR
36 01102 006162          EHALT
37
38 01103 176000 A89:     ADC 3,3          ;SEE PREVIOUS TEST.
39 01104 171000          MOV 3,2
40 01105 156404          SUB 2,3,SZR
41 01106 006162          EHALT
42
43 01107 102000 A90:     ADC 0,0          ;SEE PREVIOUS TEST.
44 01110 115000          MOV 0,3
45 01111 162404          SUB 3,0,SZR
46 01112 006162          EHALT
```

```
A 0015  .MAIN
01
02 01113 102000 A91:    ADC 0,0          ;ADD COMPLIMENT ANY NUMBER
03 01114 100004         COM 0,0,SZR      ;TO ITSELF CHOULD PRODUCE (-1).
04 01115 006162         EHALT            ;(-1) COMPLIMENTED = (+0).
05
06 01116 126000 A92:    ADC 1,1          ;SEE PREVIOUS TEST.
07 01117 124004         COM 1,1,SZR
08 01120 006162         EHALT
09
10 01121 152000 A93:    ADC 2,2          ;SEE PREVIOUS TEST.
11 01122 150004         COM 2,2,SZR
12 01123 006162         EHALT
13
14 01124 176000 A94:    ADC 3,3          ;SEE PREVIOUS TEST.
15 01125 174004         COM 3,3,SZR
16 01126 006162         EHALT
17
18 01127 176000 A95:    ADC 3,3          ;SET AC3 TO (-1) , THEN
19 01130 161404         INC 3,0,SZR      ;INCREMENT IT TO (+0).
20 01131 006162         EHALT            ;CHECK ADDER ETC.
21
22 01132 176000 A96:    ADC 3,3          ;(-1) INCREMENTED SHOULD
23 01133 161423         INCZ 3,0,SNC     ;PRODUCE (+0) AND A CARRY.
24 01134 006162         EHALT
25
26 01135 176000 A97:    ADC 3,3          ;SET C(AC3)=177777
27 01136 102400         SUB 0,0          ;SET C(AC0)=000000
28 01137 105400         INC 0,1          ;0+1=000001
29 01140 137014         ADD# 1,3,SZR     ;(-1)+(+1)=000000
30 01141 006162         EHALT
31
32 01142 102020 A98:    ADCZ 0,0         ;MISC TEST OF CARRY.
33 01143 101462         INCC 0,0,SZC
34 01144 006162         EHALT
35
36 01145 102740 A99:    SUBOS 0,0        ;SUBTRACT SHOULD PRODUCE
37 01146 101004         MOV 0,0,SZR      ;ALL ZEROS. THE SWAP HAVES
38 01147 006162         EHALT            ;WILL CAUSE THE LOADING
39                                       ;OF AC BUFFER REGISTER INTO
40                                       ;ITSELF. FOR ANY BIT SET
41                                       ;IN AC0, CHECK THE AC BUFFER
42                                       ;INPUT AT LOAD ACB TIME
43                                       ;OF THE SUBTRACT INSTRUCTION.
44
45 01150 102340 A100:   ADCOS 0,0        ;ADC SHOULD PRODUCE ALL
46 01151 104004         COM 0,1,SZR      ;ONES. THE SWAP HAVES WILL
47 01152 006162         EHALT            ;CAUSE THE LOADING OF AC BUFFER
48                                       ;REGISTER FROM ITSELF. CHECK
49                                       ;THE AC BUFFER INPUT AT LOAD
50                                       ;ACB TIME FOR ANY BIT NOT
51                                       ;SET IN AC0.
52
53 01153 102001 A101:   ADC 0,0,SKP      ;THE "ADC" AND "MOV" SHOULD BE
54 01154 102401         SUB 0,0,SKP      ;EXECUTED. THE "SUB" INSTRUCTION
55 01155 101001         MOV 0,0,SKP      ;SHOULD NOT BE PERMITTED TO SKIP.
56 01156 006162         EHALT            ;CHECK INPUTS TO TEST SKIP FLOP.
```

```
A 0016   .MAIN
01
02 01157 102322 B00:     ADCZS 0,0,SZC     ;THE SWAP COMMAND WAS
03 01160 006162          EHALT             ;DECODED FALSELY INTO A
04                                         ;SHIFT LEFT OR RIGHT
05                                         ;THUS SETTING THE CARRY.
06
07 01161 102340 B01:     ADCOS 0,0         ;MISC TEST OF CARRY.
08 01162 102763          SUBCS 0,0,SNC
09 01163 006162          EHALT
10
11 01164 102400 B02:     SUB 0,0           ;ADDITION OF 0 TO 0 SHOULD
12 01165 103404          AND 0,0,SZR
13 01166 006162          EHALT
14
15 01167 102000 B03:     ADC 0,0           ;AND (-1) TO (-1) SHOULD
16 01170 103400          AND 0,0           ;PRODUCE (-1).
17 01171 104004          COM 0,1,SZR
18 01172 006162          EHALT
19
20 01173 102000 B04:     ADC 0,0           ;AND (-1) TO (0) SHOULD
21 01174 126400          SUB 1,1           ;PRODUCE 0.
22 01175 107404          AND 0,1,SZR
23 01176 006162          EHALT
24
25 01177 102000 B05:     ADC 0,0           ;AND (0) TO (-1) SHOULD
26 01200 126400          SUB 1,1           ;PRODUCE 0.
27 01201 123404          AND 1,0,SZR
28 01202 006162          EHALT
29
30 01203 102400 B06:     SUB 0,0           ;0 AND 0 SHOULD
31 01204 103704          ANDS 0,0,SZR      ;PRODUCE A ZERO.
32 01205 006162          EHALT
33
34 01206 102400 B07:     SUB 0,0           ; 0 NEGATED IS STILL
35 01207 100404          NEG 0,0,SZR       ; 0. CHECK NEG INSTRUCTION
36 01210 006162          EHALT
37
38 01211 102000 B08:     ADC 0,0           ;(-1) NEGATED SHOULD RESULT
39 01212 104400          NEG 0,1           ;IN +1, IN AC1.
40 01213 107414          ADD# 0,1,SZR
41 01214 006162          EHALT
42
43 01215 030135 B09:     LDA 2,K1          ;TEST SHIFT2 INPUT FROM
44 01216 151125          MOVZL 2,2,SNR     ;ACB15 ON LEFT SHIFT.
45 01217 006162          EHALT             ;CORRECT RESULT=2
46
47 01220 030143 B10:     LDA 2,K2          ;TEST SHIFT1 INPUT FROM
48 01221 151125          MOVZL 2,2,SNR     ;ACB14 ON FEFT SHIFT.
49 01222 006162          EHALT             ;CORRECT RESULT=4
50
51 01223 030141 B11:     LDA 2,K4          ;TEST SHIFT0 INPUT FROM
52 01224 151125          MOVZL 2,2,SNR     ;ACB13 ON LEFT SHIFT.
53 01225 006162          EHALT
```

```
A 0417   .MAIN
01
02 01226 030143 B12:    LDA 2,K2          ;TEST INPUT TO SHIFT3
03 01227 151225         MOVZR 2,2,SNR     ;FROM ACB14 ON SHIFT RIGHT.
04 01230 006162         EHALT             ;CORRECT RESULT=1
05
06 01231 030141 B13:    LDA 2,K4          ;TEST INPUT TO SHIFT2
07 01232 151225         MOVZR 2,2,SNR     ;FROM ACB13 ON RIGHT SHIFT.
08 01233 006162         EHALT             ;CORRECT RESULT=2
09
10 01234 030142 B14:    LDA 2,K10         ;TEST INPUT TO SHIFT1
11 01235 151225         MOVZR 2,2,SNR     ;FROM ACB12 ON RIGHT SHIFT.
12 01236 006162         EHALT             ;CORRECT RESULT=2
13
14 01237 102400 B15:    SUB 0,0           ;SHIFT LEFT SHOULD PLACE
15 01240 101122         MOVZL 0,0,SZC     ;A ZERO IN THE CARRY FLOP.
16 01241 006162         EHALT             ;CHECK AND/OR GATE PRODUCING
17                                        ;CRY SET LEVEL. CHECK THE
18                                        ;(SHL,ADDER 0) INPUTS.
19
20 01242 102400 B16:    SUB 0,0           ;SHIFT RIGHT SHOULD PLACE
21 01243 101222         MOVZR 0,0,SZC     ;A ZERO IN THE CARRY FLOP.
22 01244 006162         EHALT             ;CHECK AND/OR GATE PRODUCING
23                                        ;CRY SET LEVFL. CHECK THF
24                                        ;(SHR,ACB11) INPUTS.
25
26 01245 102400 B17:    SUB 0,0           ;SHIFT LEFT SHOULD PLACE A
27 01246 101142         MOVOL 0,0,SZC     ;ZERO IN THE CARRY. CHECK
28 01247 006162         EHALT             ;AND/OR GATE PRODUCING CRY SET
29                                        ;LEVEL. THE TOP AND (CRY ENAB,
30                                        ;SHR,SHL) WAS NOT INHIBITED VIA SHL.
31
32 01250 102400 B18:    SUB 0,0           ;SHIFT RIGHT SHOULD PLACE A
33 01251 101242         MOVOR 0,0,SZC     ;ZERO IN CARRY FLOP. CHECK
34 01252 006162         EHALT             ;AND/OR GATE PRODUCING CRY SET
35                                        ;LEVEL. THE TOP GATE(CRY ENAB,
36                                        ;SHL,SHR) IS NOT INHIBITED VIA
37                                        ;THE SHR LEVEL.
38
39 01253 102000 B19:    ADC 0,0           ;SHIFT LEFT SHOULD PLACE A
40 01254 101123         MOVZL 0,0,SNC     ;ONE IN THE CARRY FLOP.
41 01255 006162         EHALT             ;CHECK AND/OR GATE PRODUCING
42                                        ;CRY SET. CHECK THE (SHL,ADDER0)
43                                        ;INPUTS.
44
45 01256 102000 B20:    ADC 0,0           ;SHIFT RIGHT SHOULD PLACE A
46 01257 101223         MOVZR 0,0,SNC     ;ONE IN THE CARRY FLOP.
47 01260 006162         EHALT             ;CHECK AND/OR GATE PRODUCING
48                                        ;CRY SET. CHECK THE (SHR,ACB11)
49                                        ;INPUTS.
50
51 01261 102525 B21:    SUBZL 0,0,SNR     ;THIS INSTRUCTION SHOULD LEAVE
52 01262 006162         EHALT             ;THE NUMBER (+1) IN AC0. CHECK
53                                        ;THE LEFT INPUT TO SHIFT3,
54                                        ;THE AND/OR GATE, CRY ENAB
55                                        ;SAVE, ETC.
```

```
A 0018   .MAIN
01
02 01263 126540 B22:     SUBOL 1,1          ;SUBOL SHOULD PRODUCE A
03 01264 131202          MOVR 1,2,SZC       ;ZERO RESULT IN AC1. IF BIT
04 01265 006162          FHALT              ;15 IS SET CHECK AND/OR GATE
05                                          ;(CRY ENAB SAVE,PTG=0,TS0) TO
06                                          ;LEFT INPUT OF SHIFT 3.
07
08 01266 020124 B23:     LDA 0,M2           ;(SHIFT2) LEFT INPUT FROM
09 01267 101140          MOVOL 0,0          ;ACB15 PICKED UP A BIT DURING
10 01270 104005          COM 0,1,SNR        ;THE MOV INSTRUCTION.
11 01271 006162          FHALT
12
13 01272 024125 B24:     LDA 1,M3           ;(SHIFT1) LEFT INPUT FROM
14 01273 125140          MOVOL 1,1          ;ACB14 PICKED UP A BIT DURING
15 01274 130005          COM 1,2,SNR        ;THE MOV INSTRUCTION.
16 01275 006162          FHALT
17
18 01276 030126 B25:     LDA 2,M5           ;(SHIFT0) LEFT INPUT FROM
19 01277 151140          MOVOL 2,2          ;ACB13 PICKED UP A BIT
20 01300 154005          COM 2,3,SNR        ;DURING THE MOV INSTRUCTION.
21 01301 006162          FHALT
22
23 01302 034142 B26:     LDA 3,K10          ;10 SHIFTED LEFT SHOULD BE
24 01303 175125          MOVZL 3,3,SNR      ;20 NOT ZERO. CHECK INPUT
25 01304 006162          FHALT              ;TO SHIFT3 LEFT INPUT GATE.
26
27 01305 102544 B27:     SUBOL 0,0,SZR      ;AC0 SHOULD BE ZERO. CHECK
28 01306 006162          FHALT              ;THE LEFT INPUTS TO THE SHIFT
29                                          ;LEVELS.
30
31 01307 176000 B28:     ADC 3,3            ;THE SUBZL INSTRUCTION SHOULD
32 01310 102520          SUBZL 0,0          ;PRODUCE THE NUMBER +1 IN
33 01311 117014          ADD# 0,3,SZR       ;AC0. PLUS ONE ADDED TO
34 01312 006162          FHALT              ;MINUS ONE SHOULD EQUAL ZERO.
35
36 01313 020135 B29:     LDA 0,K1           ;ADD EFFECTIVELY PERFORMS A
37 01314 024135          LDA 1,K1           ;SHIFT LEFT.
38 01315 127000          ADD 1,1            ;CHECK WITH SHIFT LEFT ON MOV
39 01316 101120          MOVZL 0,0          ;INSTRUCTION.
40 01317 106414          SUB# 0,1,SZR
41 01320 006162          FHALT
42
43 01321 020143 B30:     LDA 0,K2           ;SEE PREVIOUS TEST
44 01322 105120          MOVZL 0,1
45 01323 103000          ADD 0,0
46 01324 106414          SUB# 0,1,SZR
47 01325 006162          FHALT
48
49 01326 020141 B31:     LDA 0,K4           ;SEE PREVIOUS TEST
50 01327 105120          MOVZL 0,1
51 01330 103000          ADD 0,0
52 01331 106414          SUB# 0,1,SZR
53 01332 006162          FHALT
54
55 01333 020142 B32:     LDA 0,K10          ;SEE PREVIOUS TEST
56 01334 105120          MOVZL 0,1
57 01335 103000          ADD 0,0
58 01336 106414          SUB# 0,1,SZR
59 01337 006162          FHALT
```

0010 .MAIN

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A 0020   .MAIN
01
02 01340 102400 B33:    SUB 0,0          ;MISC SWAP TEST TO
03 01341 100704         NEGS 0,0,SZR     ;SEE IF CARRY IS FAST
04 01342 006162         EHALT            ;ENOUGH.
05
06 01343 152520 B34:    SUBZL 2,2        ;TEST TO INSURE MOVE SWAP
07 01344 155300         MOVS 2,3         ;REALLY CAUSES A SWAP.
08 01345 156415         SUB# 2,3,SNR     ;C(AC2) SHOULD EQUAL +1.
09 01346 006162         EHALT            ;C(AC3) SHOULD EQUAL 400
10
11 01347 102625 B35:    SUBZR 0,0,SNR    ;CORRECT C(AC0)=100000
12 01350 006162         EHALT            ;CHECK SHIFT0 RIGHT INPUT
13                                       ;AND THE AND/OR GATE
14                                       ;FEEDING IT.
15
16 01351 102640 B36:    SUBOR 0,0        ;CORRECT C(AC0)=0, IF AC0
17 01352 103032         ADDZ# 0,0,SZC    ;CONTAINS 100000 CHECK AND/OR
18 01353 006162         EHALT            ;GATE (CRY ENAB,END CYCLE) AND
19                                       ;THE (SHIFT0) RIGHT INPUT GATE.
20
21 01354 102644 B37:    SUBOR 0,0,SZR    ;CORRECT C(AC0)=0 . CHECK AND/OR
22 01355 006162         EHALT            ;GATE (ACB11,END CYCLE) FEEDING
23                                       ;SHIFT 0 RIGHT INPUT.
24
25 01356 034144 B38:    LDA 3,K20        ;20 SHIFTED RIGHT SHOULD EQUAL
26 01357 175225         MOVZR 3,3,SNR    ;10. CHECK AND/OR GATE
27 01360 006162         EHALT            ;(ACB11,END CYCLE) FEEDING
28                                       ;SHIFT0 RIGHT INPUT.
29
30 01361 152620 B39:    SUBZR 2,2        ;SET C(AC2)=100000
31 01362 153014         ADD# 2,2,SZR     ;ADDITION SHOULD RESULT
32 01363 006162         EHALT            ;IN ZERO AND A CARRY.
33
34 01364 020130 B40:    LDA 0,K100K      ;TEST ADD RIGHT. THE ACTION
35 01365 105000         MOV 0,1          ;OF ADDITION IS EFFECTIVELY
36 01366 127220         ADDZR 1,1        ;A SHIFT LEFT, THE RIGHT
37 01367 106414         SUB# 0,1,SZR     ;COMMAND RESTORES THE
38 01370 006162         EHALT            ;ORIGIONAL NUMBER.
39
40 01371 024131 B41:    LDA 1,K40K       ;SEE PREVIOUS TEST.
41 01372 131000         MOV 1,2
42 01373 153220         ADDZR 2,2
43 01374 132414         SUB# 1,2,SZR
44 01375 006162         EHALT
45
46 01376 030132 B42:    LDA 2,K20K       ;SEE PREVIOUS TEST.
47 01377 155000         MOV 2,3
48 01400 177220         ADDZR 3,3
49 01401 156414         SUB# 2,3,SZR
50 01402 006162         EHALT
51
52 01403 034133 B43:    LDA 3,K10K       ;SEE PREVIOUS TEST.
53 01404 161000         MOV 3,0
54 01405 103220         ADDZR 0,0
55 01406 116414         SUB# 0,3,SZR
56 01407 006162         EHALT
```

```
A 0021   .MAIN
01
02 01410 034403 B44:     LDA 3,.+3          ;MISC SHIFTING TEST.
03 01411 171120          MOVZL 3,2
04 01412 145200          MOVR 2,1           ;AC3=CORRECT
05 01413 136414          SUB# 1,3,SZR       ;AC1=ERROR
06 01414 006162          EHALT
07
08 01415 102520 B45:     SUBZL 0,0          ;SET AC0 TO +1, AC3 TO -1.
09 01416 176000          ADC 3,3            ;THE I/O SKIP INSTRUCTION SHOULD
10 01417 063600          SKPDN 0            ;NOT CHANGE AC BECAUSE
11 01420 117014          ADD# 0,3,SZR       ;AND ENAB SHOULD PREVENT PACK
12 01421 006162          EHALT              ;FLOP FROM SETTING. SEE 4 INPUT
13                                          ;AND GATE IN PACK FLOP LOGIC.
14
15
16 01422 102000 B46:     ADC 0,0            ;THE IORST (DICC 0,CPU) INSTRUCTION
17 01423 062677          IORST              ;SHOULD NOT CHANGE THE STATE OF
18 01424 100014          COM# 0,0,SZR       ;AC0. CHECK AND GATE (IR5,CPU INST),
19 01425 006162          EHALT              ;ITS OUTPUT TO AND GATE WITH
20                                          ;(IO.E,AND ENAB,IR7) IN THE PACK
21                                          ;FLOP LOGIC.
22
23 01426 102000 B47:     ADC 0,0            ;THE "DIB" INSTRUCTION SHOULD
24 01427 061400          DIB 0,0            ;ALTER THE CONTENTS OF AC0.
25 01430 100015          COM# 0,0,SNR       ;PACK FAILED TO SET VIA AND GATE
26 01431 006162          EHALT              ;((IO.E,AND ENAB,IR7,(IR5,CPU)).
27
28 01432 102000 B48:     ADC 0,0            ;INTA (DIB-,CPU) FAILED TO
29 01433 061477          DIB 0,CPU          ;ALTER C(AC0). CHECK AND GATE
30 01434 100015          COM# 0,0,SNR       ;((IR5,CPU INST) IN THE PACK
31 01435 006162          EHALT              ;FLOP LOGIC. IF THE AND ASSERTED
32                                          ;IT WOULD PREVENT PACK FROM SETTING.
33
34 01436 102000 B49:     ADC 0,0            ;THE DIC INSTRUCTION SHOULD SET
35 01437 062400          DIC 0,0            ;THE PACK FLOP AND STORE IN
36 01440 100015          COM# 0,0,SNR       ;AC0. AND GATE (IR5,CPU INST)
37 01441 006162          EHALT              ;ASSERTED WITHOUT THE (CPU INST)
38                                          ;LEVEL THUS INHIBITING PACK.
39
40 01442 102000 B50:     ADC 0,0            ;THE NIO INSTRUCTION SHOULD
41 01443 060000          NIO 0              ;NOT ALTER C(AC0) BECAUSE
42 01444 100014          COM# 0,0,SZR       ;IR7 IS NOT TRUE. CHECK 4 INPUT
43 01445 006162          EHALT              ;AND GATE (IO.E,AND ENAB,IR7,ETC)
44                                          ;FEEDING THE PACK FLOP.
45
46 01446 102000 B51:     ADC 0,0            ;THE "NEG" INSTRUCTION SHOULD
47 01447 000401          JMP .+1            ;NOT ALTER C(AC0). CHECK INPUTS
48 01450 100014          COM# 0,0,SZR       ;TO PACK FLOP, 4 INPUT AND
49 01451 006162          EHALT              ;GATE (IO.E,AND ENAB,IR7,ETC).
50                                          ;THE IO.E BEING ABSENT SHOULD
51                                          ;PREVENT ASSERTION OF THE AND.
```

```
▲ 0022  .MAIN
01
02 01452 102520 B52:    SUBZL 0,0          ;MISC TEST
03 01453 101000          MOV 0,0            ;AC0=+1
04 01454 105000          MOV 0,1            ;AC1 SHOULD EQUAL +1
05 01455 122414          SUB# 1,0,SZR       ;RESULT OF SUB SHOULD BE ZERO.
06 01456 006162          EHALT
07
08 01457 020000 B53:     LDA 0,0            ;THE LDA INSTRUCTIONS
09 01460 105000          MOV 0,1            ;DID NOT LOAD THE SAME DATA?
10 01461 020000          LDA 0,0
11 01462 106414          SUB# 0,1,SZR
12 01463 006162          EHALT
13
14 01464 020000 B54:     LDA 0,0            ;BOTH LDA INSTRUCTIONS SHOULD LOAD
15 01465 024000          LDA 1,0            ;THE SAME DATA. IF THE EFA FLOP
16 01466 106414          SUB# 0,1,SZR       ;FAILED TO SET OR (DISABLE D MULT)
17 01467 006162          EHALT              ;IS GROUND DURING EFA TIME THE
18                                          ;DATA LOADED WILL BE THE LDA
19                                          ;INSTRUCTION ITSELF. CHECK AND GATE
20                                          ;(EFA,IR6,IR7) TO (DISABLE D MULT).
21
22 01470 176400 B55:     SUB 3,3            ;TEST EFFECTIVE ADDRESS OF LDA
23 01471 152400          SUB 2,2            ;INSTRUCTION. IF (DISABLE D MULT)
24 01472 024001          LDA 1,1            ;WERE + DURING THE EFA TIME
25 01473 020401          LDA 0,.+1          ;OF THE SECOND LDA INSTRUCTION, IT
26 01474 106415          SUB# 0,1,SNR       ;WOULD LOAD FROM LOCATION 1 , NOT
27 01475 006162          EHALT              ;FROM CURRENT ADDRESS +1.
28                                          ;CHECK AND/OR GATE (EFA,IR6,IR7),
29                                          ;THE IR7 INPUT DID NOT INHIBIT
30                                          ;THE AND.
31
32 01476 176000 B56:     ADC 3,3            ;SECOND LDA INSTRUCTION LOADED
33 01477 152000          ADC 2,2            ;FROM LOCATION 1,NOT FROM C(AC2)
34 01500 024001          LDA 1,1            ;DISPLACED BY +1. SEE PREVIOUS TEST.
35 01501 021001          LDA 0,1,2
36 01502 106415          SUB# 0,1,SNR
37 01503 006162          EHALT
38
39 01504 102400 B57:     SUB 0,0            ;THE FIRST LDA INSTRUCTION INDEX
40 01505 126400          SUB 1,1            ;IS ON MA (PROGRAM COUNTER) THE
41 01506 152400          SUB 2,2            ;SECOND IS ON AC2. ALL ACS ARE
42 01507 176400          SUB 3,3            ;ZERO. IF BOTH USE THE ACS OR
43 01510 020402          LDA 0,.+2          ;BOTH USE THE MA THIS TEST WILL
44 01511 025001          LDA 1,1,2          ;EHALT. CHECK THE GENERATION OF
45 01512 106415          SUB# 0,1,SNR       ;(ACD OUT) VIA AND/OR GATE
46 01513 006162          EHALT              ;(EFA,IR6). SYNC SCOPE ON EFA.
```

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A 0023  .MAIN
01
02 01514 102400 B58:    SUB 0,0          ;THE FIRST "LDA" INSTRUCTION
03 01515 126400         SUB 1,1          ;USES AC3 AS A INDEX. SECOND
04 01516 152520         SUBZL 2,2        ;LDA IS NOT INDEXED. IF THE
05 01517 176520         SUBZL 3,3        ;INDEX USED WERE AC1 NOT AC3
06 01520 025400         LDA 1,0,3        ;THIS TEST WOULD EHALT. CHECK
07 01521 020000         LDA 0,0          ;(ACD 3 SEL) LEVEL AT EFA TIME
08 01522 106415         SUB# 0,1,SNR     ;OF THE FIRST LDA INSTRUCTION
09 01523 006162         EHALT
10
11 01524 102400 B59:    SUB 0,0          ;THE FIRST "LDA" INSTRUCTION USES
12 01525 126400         SUB 1,1          ;AC3 AS A INDEX. SECOND LDA IS
13 01526 152400         SUB 2,2          ;NOT INDEXED. IF THE INDEX USED
14 01527 176520         SUBZL 3,3        ;WERE AC2 NOT AC3 THIS TEST WOULD
15 01530 021400         LDA 0,0,3        ;EHALT. CHECK THE AND/OR GATE
16 01531 024000         LDA 1,0          ;PRODUCING (ACD 4 SEL), AT EFA
17 01532 106415         SUB# 0,1,SNR     ;TIME OF THE FIRST LDA INSTRUCTION.
18 01533 006162         EHALT
19
20 01534 102400 B60:    SUB 0,0          ;THE FIRST "LDA" INSTRUCTION USES
21 01535 126400         SUB 1,1          ;AC2 AS A INDEX. SECOND LDA IS
22 01536 152520         SUBZL 2,2        ;NOT INDEXED. IF THE INDEX USED
23 01537 176400         SUB 3,3          ;WERE AC3 NOT AC2 THIS TEST
24 01540 021000         LDA 0,0,2        ;WOULD EHALT. CHECK THE AND/OR
25 01541 024000         LDA 1,0          ;GATE PRODUCING (ACD 4 SEL),
26 01542 106415         SUB# 0,1,SNR     ;AT EFA TIME OF THE FIRST
27 01543 006162         EHALT            ;LDA INSTRUCTION.
28
29 01544 152400 B61:    SUB 2,2          ;AC2 AND AC3 ARE BOTH SET TO
30 01545 176400         SUB 3,3          ;ZEROS. A LDA INSTRUCTION INDEXED
31 01546 021000         LDA 0,0,2        ;ON AC2 SHOULD PRODUCE THE
32 01547 025400         LDA 1,0,3        ;SAME RESULT AS A INDEX ON
33 01550 106414         SUB# 0,1,SZR     ;AC3. CHECK FOR A FALSE
34 01551 006162         EHALT            ;ADD ONE AT TS3 TIME VIA
35                                       ;OR/AND GATE WITH IR7.
36
37 01552 020122 B62:    LDA 0,K0         ;TEST TO INSURE THE LDA
38 01553 105004         MOV 0,1,SZR      ;INSTRUCTION CAN ADDRESS
39 01554 006162         EHALT            ;A LOCATION IN PAGE ZERO.
40
41 01555 020123 B63:    LDA 0,M1         ;SEE PREVIOUS TEST
42 01556 104004         COM 0,1,SZR
43 01557 006162         EHALT
44
45 01560 020135 B64:    LDA 0,K1         ;SEE PREVIOUS TEST.
46 01561 024123         LDA 1,M1
47 01562 107014         ADD# 0,1,SZR
48 01563 006162         EHALT
49
50 01564 020402 B65:    LDA 0,.+2        ;LOADING AC0 AND AC1
51 01565 024401         LDA 1,.+1        ;RELATIVE TO PC SHOULD
52 01566 106414         SUB# 0,1,SZR     ;LOAD THE SAME DATA
53 01567 006162         EHALT            ;IN THIS TEST.
```

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▲ 0024  .MAIN
01
02 01570 020402 B66:    LDA 0,.+2          ;TRY TO LOAD THE
03 01571 101001         MOV 0,0,SKP        ;ZEROS VIA INDEX ON
04 01572 000000         0                  ;PROGRAM COUNTER.
05 01573 101004         MOV 0,0,SZR        ;EFFECTIVE ADDRESS
06 01574 006162         EHALT              ;CALCULATION FAILED.
07
08 01575 020402 B67:    LDA 0,.+2          ;SEE ABOVE.
09 01576 101001         MOV 0,0,SKP
10 01577 177777         -1
11 01600 100014         COM# 0,0,SZR
12 01601 006162         EHALT
13
14 01602 020402 B68:    LDA 0,.+2          ;LOAD AC0 AND AC1
15 01603 101001         MOV 0,0,SKP        ;RELATIVE TO PROGRAM COUNTER.
16 01604 123456         123456             ;THE SECOND LDA INSTRUCTION
17 01605 024777         LDA 1,.-1          ;MUST ADD (-1) FOR 16
18 01606 106414         SUB# 0,1,SZR       ;BITS. CHECK TO INSURE S0
19 01607 006162         EHALT              ;IS ACTIVATED VIA AND GATE
20                                         ;(EFA,MBCB,ETC).
21
22 01610 020200 B69:    LDA 0,200          ;LOAD LOCATION 200 DIRECT.
23 01611 030145         LDA 2,K200         ;LOAD VIA INDEX LOCATION 200.
24 01612 025000         LDA 1,0,2          ;CHECK SM LEVEL AT EFA TIME
25 01613 106414         SUB# 0,1,SZR       ;OF FIRST LDA INSTRUCTION.
26 01614 006162         EHALT
27
28 01615 020177 B70:    LDA 0,177          ;SEE PREVIOUS TEST.
29 01616 034145         LDA 3,K200
30 01617 025377         LDA 1,-1,2
31 01620 106414         SUB# 0,1,SZR
32 01621 006162         EHALT
33
34 01622 102300 B71:    ADCS 0,0           ;MISC TEST OF ALC.
35 01623 104004         COM 0,1,SZR
36 01624 006162         EHALT
37
38 01625 152000 B72:    ADC 2,2            ;TEST INDEX ON AC2.
39 01626 020000         LDA 0,0            ;LOAD LOCATION 0.
40 01627 025001         LDA 1,1,2          ;LOAD LOCATION 0, (-1+1=0).
41 01630 106414         SUB# 0,1,SZR
42 01631 006162         EHALT
43
44
45 01632 176000 B73:    ADC 3,3            ;SEE PREVIOUS TEST.
46 01633 020000         LDA 0,0
47 01634 025401         LDA 1,1,3
48 01635 106414         SUB# 0,1,SZR
49 01636 006162         EHALT
50
51 01637 176401 B74:    SUB 3,3,SKP        ;THE JSR INSTRUCTION SHOULD
52 01640 004401         JSR .+1            ;NOT BE EXECUTED BECAUSE
53 01641 175004         MOV 3,3,SZR        ;(IR0+SKIP) SHOULD PREVENT
54 01642 006162         EHALT              ;THE DECODE OF (JMP+JSR)(F+D).
```

```
A 0025  .MAIN
01
02 01643 020000 B75:    LDA 0,0          ;THE ISZ INSTRUCTION SHOULD
03 01644 101001         MOV 0,0,SKP      ;NOT BE EXECUTED. CHECK
04 01645 010000         ISZ 0            ;IR DECODING.
05 01646 024000         LDA 1,0
06 01647 106414         SUB# 0,1,SZR
07 01650 006162         EHALT
08
09 01651 020000 B76:    LDA 0,0          ;THE STA INSTRUCTION SHOULD
10 01652 126001         ADC 1,1,SKP      ;NOT BE ASSERTED. CHECK IR
11 01653 044000         STA 1,0          ;DECODING.
12 01654 024000         LDA 1,0
13 01655 106414         SUB# 0,1,SZR
14 01656 006162         EHALT
15
16 01657 102001 B77:    ADC 0,0,SKP      ;THE DIA INSTRUCTION SHOULD
17 01660 060477         DIA 0,CPU        ;NOT BE EXECUTED. CHECK IR
18 01661 100014         COM# 0,0,SZR     ;DECODE.
19 01662 006162         EHALT
20
21 01663 102001 B78:    ADC 0,0,SKP      ;THE LDA INSTRUCTION SHOULD
22 01664 020000         LDA 0,0          ;NOT BE EXECUTED.
23 01665 100014         COM# 0,0,SZR
24 01666 006162         EHALT
25
26 01667 102000 B79:    ADC 0,0          ;TEST STORE INSTRUCTION.
27 01670 040000         STA 0,0
28 01671 024000         LDA 1,0
29 01672 125015         MOV# 1,1,SNR
30 01673 006162         EHALT
31
32 01674 020124 B80:    LDA 0,M2         ;STA FAILED . CHECK INPUT
33 01675 040000         STA 0,0          ;TO MULT3 FROM ACD3.
34 01676 024000         LDA 1,0          ;BIT PICKED UP.
35 01677 124015         COM# 1,1,SNR
36 01700 006162         EHALT
37
38 01701 020125 B81:    LDA 0,M3         ;STA FAILED. CHECK INPUT
39 01702 040000         STA 0,0          ;TO MULT2 FROM ACD2.
40 01703 024000         LDA 1,0          ;BIT PICKED UP.
41 01704 124015         COM# 1,1,SNR
42 01705 006162         EHALT
43
44 01706 020126 B82:    LDA 0,M5         ;STA FAILED. CHECK INPUT
45 01707 040000         STA 0,0          ;TO MULT1 FROM ACD1.
46 01710 024000         LDA 1,0
47 01711 124015         COM# 1,1,SNR
48 01712 006162         EHALT
49
50 01713 020127 B83:    LDA 0,M9         ;STA FAILED. CHECK INPUT
51 01714 040000         STA 0,0          ;TO MULT0 FROM ACD0.
52 01715 024000         LDA 1,0          ;BIT PICKED UP.
53 01716 124015         COM# 1,1,SNR
54 01717 006162         EHALT
```

```
▲ 0026  .MAIN
01
02 01720 020135 B84:    LDA 0,K1          ;STA FAILED, CHECK INPUT
03 01721 040000         STA 0,0           ;TO MULT3 FROM ACD3.
04 01722 024000         LDA 1,0
05 01723 125005         MOV 1,1,SNR       ;BIT DROPED.
06 01724 006162         EHALT
07
08 01725 020143 B85:    LDA 0,K2          ;STA FAILED . CHECK INPUT
09 01726 040000         STA 0,0           ;TO MULT2 FROM ACD2.
10 01727 024000         LDA 1,0           ;BIT DROPPED.
11 01730 125005         MOV 1,1,SNR
12 01731 006162         EHALT
13
14 01732 020141 B86:    LDA 0,K4          ;STA FAILED, CHECK INPUT
15 01733 040000         STA 0,0           ;TO MULT1 FROM ACD1.
16 01734 024000         LDA 1,0           ;BIT DROPED.
17 01735 125005         MOV 1,1,SNR
18 01736 006162         EHALT
19
20 01737 020142 B87:    LDA 0,K10         ;STA FAILED, CHECK INPUT
21 01740 040000         STA 0,0           ;TO MULT0 FROM ACD0.
22 01741 024000         LDA 1,0
23 01742 125005         MOV 1,1,SNR
24 01743 006162         EHALT
25
26 01744 020145 B88:    LDA 0,K167356     ;TEST STA.
27 01745 040000         STA 0,0
28 01746 024000         LDA 1,0
29 01747 106414         SUB# 0,1,SZR
30 01750 006162         EHALT
31
32 01751 020147 B89:    LDA 0,K156735     ;TEST STA.
33 01752 040000         STA 0,0
34 01753 024000         LDA 1,0
35 01754 106414         SUB# 0,1,SZR
36 01755 006162         EHALT
37
38 01756 020150 B90:    LDA 0,K135673     ;TEST STA.
39 01757 040000         STA 0,0
40 01760 024000         LDA 1,0
41 01761 106414         SUB# 0,1,SZR
42 01762 006162         EHALT
43
44 01763 020151 B91:    LDA 0,K073567     ;TEST STA.
45 01764 040000         STA 0,0
46 01765 024000         LDA 1,0
47 01766 106414         SUB# 0,1,SZR
48 01767 006162         EHALT
```

```
A 0027   .MAIN
01
02 01770 020152 B92:     LDA 0,K010421    ;TEST STA RELATIVE TO PC.
03 01771 101001          MOV 0,0,SKP
04 01772 000000          0
05 01773 040777          STA 0,.-1
06 01774 024776          LDA 1,.-2
07 01775 106414          SUB# 0,1,SZR
08 01776 006162          EHALT
09
10 01777 024153 B93:     LDA 1,K021042
11 02000 101001          MOV 0,0,SKP
12 02001 000000          0
13 02002 044777          STA 1,.-1
14 02003 030776          LDA 2,.-2
15 02004 146414          SUB# 2,1,SZR
16 02005 006162          EHALT
17
18 02006 030154 B94:     LDA 2,K042104    ;TEST STA RELATIVE TO PC.
19 02007 101001          MOV 0,0,SKP
20 02010 000000          0
21 02011 050777          STA 2,.-1
22 02012 034776          LDA 3,.-2
23 02013 156414          SUB# 2,3,SZR
24 02014 006162          EHALT
25
26 02015 102400 B94A:    SUB 0,0          ;STA SHOULD NOT CHANGE
27 02016 040000          STA 0,0          ;CONTENTS OF AC0.
28 02017 103014          ADD# 0,0,SZR
29 02020 006162          EHALT
30
31 02021 034155 B95:     LDA 3,K104210    ;TEST STA INSTRUCTION.
32 02022 175001          MOV 3,3,SKP
33 02023 000000          0
34 02024 054777          STA 3,.-1
35 02025 030776          LDA 2,.-2
36 02026 156414          SUB# 2,3,SZR
37 02027 006162          EHALT
38
39 02030 020155 B96:     LDA 0,K104210    ;TEST STA INSTRUCTION
40 02031 176000          ADC 3,3          ;INDEXED ON AC3.
41 02032 041401          STA 0,1,3
42 02033 024000          LDA 1,0
43 02034 106414          SUB# 0,1,SZR
44 02035 006162          EHALT
45
46 02036 102401 B97:     SUB 0,0,SKP      ;MISC STA TEST OF
47 02037 177777          -1               ;ALL ZEROS.
48 02040 040777          STA 0,.-1
49 02041 024776          LDA 1,.-2
50 02042 125004          MOV 1,1,SZR
51 02043 006162          EHALT
52
53 02044 102301 B98:     ADCS 0,0,SKP     ;MISC STA TEST OF
54 02045 000000          0                ;ALL ONES.
55 02046 040777          STA 0,.-1
56 02047 024776          LDA 1,.-2
57 02050 124014          COM# 1,1,SZR
58 02051 006162          EHALT
```

```
A 0028  .MAIN
01
02 02052 102400 C00:    SUB 0,0          ;STORE ZEROS IN LOCATION
03 02053 040000          STA 0,0          ;ZERO. AFTER A ISZ INSTRUCTION
04 02054 010000          ISZ 0            ;C(0) SHOULD EQUAL (+1) NOT (+0).
05 02055 000401          JMP .+1          ;CHECK ADD ONE LOGIC AT
06 02056 020000          LDA 0,0          ;ISZ EXECUTE TIME.
07 02057 101035          MOV 0,0,SNR
08 02060 006162          EHALT
09
10 02061 102400 C01:    SUB 0,0          ;LOCATION ZERO IS SET TO
11 02062 040000          STA 0,0          ;+0, THEN INCREMENTED. AC1
12 02063 010000          ISZ 0            ;IS MADE (+1) AND COMPARED
13 02064 000401          JMP .+1          ;WITH LOC 0 AFTER THE
14 02065 126520          SUBZL 1,1        ;INCREMENT. CHECK ISZ
15 02066 020000          LDA 0,0          ;INSTRUCTION.
16 02067 106414          SUB# 0,1,SZR
17 02070 006162          EHALT
18
19 02071 102000 C02:    ADC 0,0          ;LOCATION ZERO IS SET TO (-1),
20 02072 040000          STA 0,0          ;THEN INCREMENTED TO ZERO.
21 02073 010000          ISZ 0            ;CHECK THE ISZ INSTRUCTION
22 02074 000401          JMP .+1          ;ABILITY TO INCREMENT.
23 02075 020000          LDA 0,0
24 02076 101004          MOV 0,0,SZR
25 02077 006162          EHALT
26
27 02100 152020 C03:    ADC# 2,2         ;ISZ SHOULD NOT CHANGE
28 02101 050000          STA 2,0          ;THE ACS! OR STAET OF
29 02102 010000          ISZ 0            ;THE CARRY FLOP.
30 02103 000401          JMP .+1
31 02104 150015          COM# 2,2,SNR
32 02105 101002          MOV 0,0,SZC
33 02106 006162          EHALT
34
35 02107 020156 C04:    LDA 0,K1234      ;INCREMENT OF THE NUMBER
36 02110 040000          STA 0,0          ;(1234) CAUSED ISZ TO SKIP.
37 02111 010000          ISZ 0            ;CHECK FOR PROPER SHIFT OF
38 02112 101001          MOV 0,0,SKP      ;MBC REGISTER VIA EFA,ETC.
39 02113 006162          EHALT
40
41 02114 020156 C05:    LDA 0,K1234      ;SEE PREVIOUS TEST.
42 02115 040000          STA 0,0
43 02116 152520          SUBZL 2,2
44 02117 011377          ISZ -1,2
45 02120 101001          MOV 0,0,SKP
46 02121 006162          EHALT
47
48 02122 020156 C06:    LDA 0,K1234      ;SEE PREVIOUS TEST.
49 02123 040000          STA 0,0
50 02124 152040          ADCO 2,2
51 02125 011001          ISZ 1,2
52 02126 101001          MOV 0,0,SKP
53 02127 006162          EHALT
```

```
▲ 0129   .MAIN
01
02 02130 020156 C07:     LDA 0,K1234      ;SEE PREVIOUS TEST.
03 02131 040000          STA 0,0
04 02132 152520          SUBZL 2,2
05 02133 151040          MOVO 2,2
06 02134 011377          ISZ -1,2
07 02135 101011          MOV#  0,0,SKP
08 02136 006162          EHALT
09
10 02137 102220 C08:     ADCZR 0,0        ;INCREMENT OF THE NUMBER
11 02140 040000          STA 0,0          ;77777 SHOULD PRODUCE THE
12 02141 010000          ISZ 0            ;NUMBER 100000 AND THE
13 02142 101001          MOV 0,0,SKP      ;ISZ INSTRUCTION SHOULD NOT
14 02143 006162          EHALT            ;SKIP.
15
16 02144 102000 C09:     ADC 0,0          ;INCREMENT OF THE NUMBER (-1)
17 02145 040000          STA 0,0          ;SHOULD PRODUCE (+0) AND A SKIP.
18 02146 010000          ISZ 0            ;TEST THE OR GATE TO THE SET
19 02147 006162          EHALT            ;SIDE OF (TEST SKIP) FLOP.
20
21 02150 102001 C10:     ADC 0,0,SKP      ;CHECK ABILITY TO INCREMENT
22 02151 000000          0                ;(ISZ) RELATIVE TO PC.
23 02152 040777          STA 0,.-1
24 02153 010776          ISZ .-2
25 02154 006162          EHALT            ;ISZ SHOULD SKIP...
26
27 02155 102620 C11:     SUBZR 0,0        ;IF THE LDA INSTRUCTION
28 02156 040000          STA 0,0          ;HANGS, THE SKIP FLOP FAILED
29 02157 101001          MOV 0,0,SKP      ;TO INHIBIT DEFER. CHECK
30 02160 022000          LDA 0,@0         ;AND GATE (EFA,IR5,SKIP)
31                                        ;TO THE DEFER LOGIC.
32
33 02161 020020 C12:     LDA 0,20         ;DEFER SHOULD NOT SET
34 02162 101001          MOV 0,0,SKP      ;IN THIS TEST, BECAUSE
35 02163 036020          LDA 3,@20        ;SKIP IS SET. SEE PREVIOUS
36 02164 024020          LDA 1,20         ;TEST.
37 02165 106414          SUB# 0,1,SZR
38 02166 006162          EHALT
39
40 02167 102400 C13:     SUB 0,0          ;DECREMENT (VIA DSZ) LOCATION
41 02170 040000          STA 0,0          ;ZERO FROM +0 TO -1.  NO
42 02171 014000          DSZ 0            ;DECREMENT OCCURED. CHECK
43 02172 000401          JMP .+1          ;OR GATE GENERATING S0, THE
44 02173 020000          LDA 0,0          ;(DSZ.E.TS0) INPUT.
45 02174 101005          MOV 0,0,SNR
46 02175 006162          EHALT
47
48 02176 102400 C14:     SUB 0,0          ;SEE PREVIOUS TEST.
49 02177 040000          STA 0,0
50 02200 014000          DSZ 0
51 02201 000401          JMP .+1
52 02202 020000          LDA 0,0
53 02203 100014          COM# 0,0,SZR
54 02204 006162          EHALT
```

```
A 00330   .MAIN
31
32  02205 102001  C15:    ADC 0,0,SKP       ;TEST "DSZ" DECREMENT
33  02206 000000          0                 ;177777 TO 177776.
34  02207 034777          STA 0,.-1
35  02210 014776          DSZ .-2
36  02211 024775          LDA 1,.-3
37  02212 122014          ADC# 1,0,SZR
38  02213 006162          FHALT
39
40  02214 102521  C16:    SUBZL 0,0,SKP     ;DECREMENT +1 TO +0.
41  02215 000000          0                 ;CHECK TO INSURE SKIP
42  02216 034777          STA 0,.-1         ;OCCURES ON DSZ.
43  02217 014776          DSZ .-2
44  02220 006162          FHALT
45
46  02221 126400  C17:    SUB 1,1           ;WAS JSR FLOP FAILED
47  02222 004401          JSR .+1           ;TO SET VIA JSR.
48  02223 125004          MOV 1,1,SZR
49  02224 006162          FHALT
50
51  02225 004402  C20:    JSR .+2           ;JSR FAIL TO CHANGE PC.
52  02226 006162          FHALT             ;CHECK AND/OR GATE (JMP+JSR)
53                                          ;AT TS3 TO PRODUCE (PC ENAB)
54                                          ;LEVEL.
55
56  02227 176400  C21:    SUB 3,3           ;JSR FAILED TO STORE IN AC3.
57  02230 004401          JSR .+1           ;PACK FLOP FAILED TO SET VIA
58  02231 175005          MOV 3,3,SNR       ;(JSR.EFA) LEVEL.
59  02232 006162          FHALT
60
61  02233 004402  C22:    JSR .+2           ;THE JSR INSTRUCTION STORED
62  02234 002235          .+1               ;THE EFFECTIVE ADDRESS NOT
63  02235 020777          LDA 0,.-1         ;THE OLD PROGRAM COUNTER.
64  02236 116415          SUB# 0,3,SNR      ;CHECK JSR.EFA INPUT
65  02237 006162          FHALT             ;TO SHIFT ACB LEVEL. THE
66                                          ;SHIFT WAS NOT INHIBITED.
67
68  02240 004401  C23:    JSR .+1           ;BIT 0 OF THE PROGRAM
69  02241 175112          MOVL# 3,3,SZC     ;COUNTER SHOULD NEVER BE
70  02242 006162          FHALT             ;SET...
71
72  02243 004402  C24:    JSR .+2           ;CHECK TO INSURE PC IS
73  02244 002244          .                 ;STORED PROPERLY (VIA JSR)
74  02245 020777          LDA 0,.-1         ;IN AC3.
75  02246 116414          SUB# 0,3,SZR
76  02247 006162          FHALT
77
78  02250 004401  C25:    JSR .+1           ;LOAD AC3 WITH PROGRAM
79  02251 177240          ADDOR 3,3         ;COUNTER, THEN SET THE SIGN BIT.
80  02252 005402          JSR 2,3           ;LOAD PC FROM AC3 BUT
81  02253 175112          MOVL# 3,3,SZC     ;CHECK TO INSURE SIGN BIT IS
82  02254 006162          FHALT             ;NOT LOADED.
```

```
A 00031   .MAIN
01 002255 152400 C26:     SUB 2,2          ;THE JMP INSTRUCTION STORED
02 002256 176400          SUB 3,3          ;THE PROGRAM COUNTER IN THE
03 002257 000401          JMP .+1          ;ACS. PERHAPS THE (JSR.EFA) LEVEL
04 002260 157014          ADD# 2,3,SZR     ;WAS ASSERTED. CHECK AND
05 002261 006162          EHALT            ;GATE (EFA,(JMP+JSR),IR4)
06                                         ;THE IR4 INPUT.
07
08 002262 000402 C27:     JMP .+2          ;JMP FAILED?
09 002263 006162          EHALT
10
11 002264 102000 C28:     ADC 0,0          ;SET LOC 377 TO ZEROS
12 002265 040000          STA 0,0          ;INDIRECT SHOULD NOT DECREMENT
13 002266 102400          SUB 0,0          ;THIS REGISTER. SYNC SCOPE ON
14 002267 040377          STA 0,377        ;DEFER, LOOP FLOP SHOULD NOT
15 002270 022377          LDA 0,@377       ;SET. CHECK AND GATE (DEFER,
16 002271 020377          LDA 0,377        ;ADDER TEST,PTG2.LOOP).
17 002272 101004          MOV 0,0,SZR      ;FALSE AUTO DECREMENT OCCURED.
18 002273 006162          EHALT
19
20 002274 102400 C29:     SUB 0,0          ;LOCATION 0 IS NOT A AUTO
21 002275 040000          STA 0,0          ;INDEX REGISTER AND THUS
22 002276 022000          LDA 0,@0         ;SHOULD NOT INCREMENT DURING
23 002277 020000          LDA 0,0          ;THE DEFER CYCLE. EXCLUSIVE OR
24 002300 101004          MOV 0,0,SZR      ;GATE (PTG=1.TS0,MAC15) IN THE
25 002301 006162          EHALT            ;ADDER TEST LOGIC FAILED.
26                                         ;SYNC SCOPE ON DEFER, THE
27                                         ;ZERO SAVE FLOP SHOULD SET
28                                         ;ON CLOCK PULSE AFTER (PTG=1.TS0).
29
30 002302 030157 C30:     LDA 2,K420       ;LOCATION 420 IS NOT A AUTO
31 002303 025000          LDA 1,0,2        ;INCREMENT REGISTER, YET A
32 002304 023000          LDA 0,@0,2       ;INDIRECT REFFERANCE CHANGED IT.
33 002305 021000          LDA 0,0,2        ;EXCLUSIVE OR GATE (PTG=1.TS0,MAC15)
34 002306 106414          SUB# 0,1,SZR     ;IN THE ADDER TEST LOGIC FAILED.
35 002307 006162          EHALT            ;SYNC SCOPE ON DEFER, THE ZERO
36                                         ;SAVE FLOP SHOULD SET.
37
38 002310 102400 C31:     SUB 0,0          ;LOCATION 220 IS NOT A
39 002311 040220          STA 0,220        ;AUTO INDEX REGISTER.
40 002312 022220          LDA 0,@220       ;CHECK OR GATE (MAC12,PTG2),
41 002313 020220          LDA 0,220        ;INPUT TO ZERO SAVE FLOP
42 002314 101004          MOV 0,0,SZR      ;IN ADDER TEST LOGIC.
43 002315 006162          EHALT
44
45 002316 102400 C31A:    SUB 0,0          ;LOCATION 120 IS NOT A
46 002317 040120          STA 0,120        ;AUTO INDEX REGISTER. CHECK
47 002320 022120          LDA 0,@120       ;OR GATE (MAC13,MAC14,ETC,ETC)
48 002321 020120          LDA 0,120        ;IN THE ADDER TEST LOGIC.
49 002322 101004          MOV 0,0,SZR      ;THE MAC13 INPUT SHOULD SET
50 002323 006162          EHALT            ; THE ZERO SAVE FLOP. SYNC
51                                         ;ON DEFER.
52
53 002324 102400 C32:     SUB 0,0          ;LOCATION 60 IS NOT A
54 002325 040060          STA 0,60         ;AUTO INCREMENT REGISTER. CHECK
55 002326 022060          LDA 0,@60        ;OR GATE (MAC13,MAC14,ETC,ETC)
56 002327 020060          LDA 0,60         ;IN THE ADDER TEST LOGIC.
57 002330 101004          MOV 0,0,SZR      ;THE MAC14 INPUT SHOULD SET
58 002331 006162          EHALT            ;THE ZERO SAVE FLOP.
```

```
A 1032  .MAIN
01
02 02332 022402 C33:    LDA 0,@.+2          ;A LDA INSTRUCTION WITH
03 02333 101011          MOV# 0,0,SKP        ;A INDIRECT BIT LOADED
04 02334 002334          .                   ;THE WRONG DATA. CHECK THE
05 02335 024777          LDA 1,.-1           ;INPUT TO THE MA REGISTER
06 02336 106414          SUB# 0,1,SZR        ;DURING DEFER CYCLE
07 02337 006162          EHALT
08
09 02340 022402 C34:    LDA 0,@.+2          ;THE INDIRECT CYCLE OF THIS
10 02341 101011          MOV# 0,0,SKP        ;INSTRUCTION WAS NOT EXECUTED.
11 02342 002343          .+1                 ;CHECK AND GATE (EFA,IR5,SKIP)
12 02343 024777          LDA 1,.-1           ;TO THE D SET LOGIC.
13 02344 106415          SUB# 0,1,SNR
14 02345 006162          EHALT
15
16 02346 020134 C35:    LDA 0,K377          ;LOCATION 0 AND AC0 ARE
17 02347 040000          STA 0,0             ;LOADED WITH (377). AC3
18 02350 115300          MOVS 0,3            ;IS LOADED WITH (177400).
19 02351 014000          DSZ 0               ;THE DSZ INSTRUCTION CHANGED
20 02352 170000          COM 3,2             ;THE CONTENTS OF AC3.
21 02353 112414          SUB# 0,2,SZR
22 02354 006162          EHALT
23
24 02355 102400 C36:    SUB 0,0             ;A REFFERANCE TO AUTO
25 02356 040030          STA 0,30            ;DECREMENT LOCATION 30
26 02357 020030          LDA 0,30            ;WITHOUT THE INDIRECT BIT
27 02360 101004          MOV ?,0,SZR         ;DECREMENTED THE REGISTER.
28 02361 006162          EHALT
29
30 02362 102000 C37:    ADC 0,0             ;A REFFERANCE TO AUTO INC
31 02363 040020          STA 0,20            ;REGISTER 20 WITH OUT DEFER
32 02364 020020          LDA 0,20            ;BIT SHOULD NOT CAUSE IT
33 02365 100014          COM# 0,0,SZR        ;TO INCREMENT.
34 02366 006162          EHALT
35
36 02367 102400 C38:    SUB 0,0             ;A INDIRECT REFFERANCE TO
37 02370 040020          STA 0,20            ;LOCATION 20 SHOULD CAUSE IT
38 02371 022020          LDA 0,@20           ;TO INCREMENT FROM +0 TO +1.
39 02372 020020          LDA 0,20            ;SYNC ON DEFER. CHECK LOOP SET
40 02373 101005          MOV 0,0,SNR         ;LEVEL VIA AND GATE (DEFER,
41 02374 006162          EHALT               ;ADDER TEST,PTG2.LOOP). ALSO
42                                           ;CHECK ADD ONE LOGIC VIA
43                                           ;(DEFER,MAC12,SAVE).
44
45 02375 102400 C39:    SUB 0,0             ;LOCATION 20 PERFORMED A
46 02376 040020          STA 0,20            ;AUTO DECREMENT NOT A AUTO
47 02377 022020          LDA 0,@20           ;INCREMENT. CHECK THE
48 02400 020020          LDA 0,20            ;MAC12 SAVE FLOP.
49 02401 100015          COM# 0,0,SNR
50 02402 006162          EHALT
```

```
A 0033   .MAIN
01
02 02403 102400 C40:     SUB 0,0          ;AUTO DECREMENT LOCATION
03 02404 040030          STA 0,30         ;30 PERFORMED A AUTO INCREMENT.
04 02405 026030          LDA 1,@30        ;THE MAC12 SAVE FLOP
05 02406 024030          LDA 1,30         ;FAILED TO SET.
06 02407 106015          ADC# 0,1,SNR
07 02410 006162          EHALT
08
09 02411 102400 C40A:    SUB 0,0          ;LOCATION 20 SHOULD INCREMENT
10 02412 040020          STA 0,20         ;IN THE DEFER CYCLE FROM (+0)
11 02413 026020          LDA 1,@20        ;TO (+1). CHECK AND/OR GATE
12 02414 024020          LDA 1,20         ;(DEFER,MAC12 SAVE) IN THE
13 02415 106014          ADC# 0,1,SZR     ;ADD ONE LOGIC.
14 02416 006162          EHALT
15
16 02417 102520 C41:     SUBZL 0,0        ;LOCATION 30 SHOULD DECREMENT
17 02420 040030          STA 0,30         ;FROM +1 TO +0. CHECK FOR
18 02421 026030          LDA 1,@30        ;A FAILURE TO ASSERT S0 VIA
19 02422 024030          LDA 1,30         ;(DEFER,MAC12 SAVE) OR ADD ONE
20 02423 125004          MOV 1,1,SZR      ;WAS ASSERTED FALSELY.
21 02424 006162          EHALT
22
23 02425 102400 C42:     SUB 0,0          ;AUTO INDEX LOCATION 20
24 02426 040000          STA 0,0          ;WAS NOT INDEXED WHEN SIGN
25 02427 102620          SUBZR 0,0        ;BIT WAS SET.
26 02430 040020          STA 0,20         ;CHECK OR GATE (PTG2,MAC12)
27 02431 026020          LDA 1,@20        ;IN THE ADDER TEST LOGIC.
28 02432 024020          LDA 1,20         ;SYNC ON FIRST DEFER CYCLE.
29 02433 106014          ADC# 0,1,SZR
30 02434 006162          EHALT
31
32 02435 102400 C43:     SUB 0,0          ;AUTO INDEX LOCATION 22
33 02436 040022          STA 0,22         ;WAS NOT INDEXED VIA INDIRECT
34 02437 026022          LDA 1,@22        ;REFFERANCE. CHECK AND GATE
35 02440 024022          LDA 1,22         ;(DEFER,PTG=0,TS0) IN THE
36 02441 106014          ADC# 0,1,SZR     ;ZERO SAVE,ADDER TEST LOGIC.
37 02442 006162          EHALT            ;SYNC ON DEFER,ZERO SAVE
38                                        ;FLOP SHOULD NOT SET.
39
40 02443 034160 C44:     LDA 3,K10020     ;PERFORM A INDIRECT REFFERANCE
41 02444 031400          LDA 2,0,3        ;TO LOCATION 10020. CHECK
42 02445 102400          SUB 0,0          ;TO INSURE THAT IT DOES NOT
43 02446 041400          STA 0,0,3        ;ACT AS A AUTO INCREMENT REGISTER.
44 02447 021400          LDA 0,0,3
45 02450 101004          MOV 0,0,SZR      ;IF NO MEMORY DONT
46 02451 000407          JMP C45          ;PERFORM THE TEST.
47 02452 023400          LDA 0,@0,3       ;CHECK THE AND GATE PRODUCING
48 02453 021400          LDA 0,0,3        ;ADDER TEST LEVEL.
49 02454 051400          STA 2,0,3        ;THE BOTTEM INPUT SHOULD NOT
50 02455 126520          SUBZL 1,1        ;BE TRUE.
51 02456 106415          SUB# 0,1,SNR
52 02457 006162          EHALT
```

```
A 0434   .MAIN
01
02 02460 102400 C45:     SUB 0,0          ;MISC ISZ TEST.
03 02461 040030          STA 0,30
04 02462 010030          ISZ 30
05 02463 000401          JMP .+1
06 02464 024030          LDA 1,30
07 02465 106014          ADC# 0,1,SZR
08 02466 006162          EHALT
09
10 02467 102400 C46:     SUB 0,0          ;MISC DEFER/AUTO DECREMENT
11 02470 040010          STA 0,10         ;TEST.
12 02471 026010          LDA 1,@10
13 02472 024010          LDA 1,10
14 02473 125004          MOV 1,1,SZR
15 02474 006162          EHALT
16
17 02475 102400 C47:     SUB 0,0          ;MISC JMP TEST.
18 02476 000402          JMP .+2
19 02477 102000          ADC 0,0
20 02500 101001          MOV 0,0,SKP
21 02501 006162          EHALT
22
23 02502 102400 C50:     SUB 0,0          ;MISC ISZ TEST
24 02503 040010          STA 0,10
25 02504 012010          ISZ @10
26 02505 024010          LDA 0,10
27 02506 101004          MOV 0,0,SZR
28 02507 006162          EHALT
29
30 02510 102400 C51:     SUB 0,0          ;LOCATION 10 SHOULD POINT
31 02511 040010          STA 0,10         ;TO LOCATION ZERO WHICH
32 02512 102000          ADC 0,0          ;CONTAINS ALL ONES. ISZ
33 02513 040000          STA 0,0          ;OF ALL ONES SHOULD CAUSE
34 02514 012010          ISZ @10          ;A SKIP.
35 02515 006162          EHALT
36
37 02516 102520 C52:     SUBZL 0,0        ;LOCATION 10 POINTS TO
38 02517 040000          STA 0,0          ;LOCATION 0 WHICH CONTAINS
39 02520 102400          SUB 0,0          ;(+1). DSZ SHOULD DECREMENT
40 02521 040010          STA 0,10         ;LOCATION ZERO TO +0 AND
41 02522 016010          DSZ @10          ;SKIP.
42 02523 006162          EHALT
43
44 02524 102400 C53:     SUB 0,0          ;NO INTERRUPT SHOULD
45 02525 040000          STA 0,0          ;OCCURE WHEN ION IS SET.
46 02526 060177          INTEN            ;CHECK OR GATE (INTR,PWR LOW)
47 02527 000401          JMP .+1          ;IN THE PI SET LOGIC.
48 02530 020000          LDA 0,0          ;IS THERE ANY TELETYPE
49 02531 060277          INTDS            ;RUNNING OPEN OR KEY STRUCK?
50 02532 101004          MOV 0,0,SZR
51 02533 006162          EHALT
```

```
▲ 00035  .MAIN
01
02 002534 102400 C54:    SUB 0,0          ;MISC MULTI DEFER TEST
03 002535 040000         STA 0,0          ;LOC 1=100000
04 002536 022001         LDA 0,@1
05 002537 101004         MOV 0,0,SZR
06 002540 006162         EHALT
07
08 002541 102000 C55:    ADC 0,0          ;CORRECT PROCEEDURE IS TO
09 002542 040000         STA 0,0          ;MULTI DEFER AND LOAD
10 002543 022402         LDA 0,@.+2       ;LOCATION 0. THE DEFER
11 002544 000403         JMP .+3          ;AGAIN FLOP FAILED TO
12 002545 102546         @.+1             ;SET. CHECK "C","D", AND RESET
13 002546 000000         0                ;INPUTS. CHECK 3 INPUT OR
14 002547 101005         MOV 0,0,SNR      ;GATE TO (D SET) LEVEL.
15 002550 006162         EHALT
16
17 002551 102000 C56:    ADC 0,0          ;CORRECT PROCEEDURE IS TO
18 002552 040000         STA 0,0          ;MULTI DEFER AND LOAD
19 002553 022402         LDA 0,@.+2       ;LOCATION 0.
20 002554 000403         JMP .+3
21 002555 102556         @.+1
22 002556 000000         0
23 002557 100014         COM# 0,0,SZR
24 002560 006162         EHALT
25
26 002561 102000 C57:    ADC 0,0          ;AC3=100000
27 002562 040000         STA 0,0          ;LOAD ACO INDEXED ON
28 002563 176620         SUBZR 3,3        ;AC3 SHOULD LOAD LOCATION
29 002564 021400         LDA 0,0,3        ;ZERO.
30 002565 100014         COM# 0,0,SZR
31 002566 006162         EHALT
32
33 002567 022402 C58:    LDA 0,@.+2       ;TEST MULTI DEFER.
34 002570 000405         JMP .+5
35 002571 102572         @.+1
36 002572 102573         @.+1
37 002573 002574         .+1
38 002574 012345         12345
39 002575 024777         LDA 1,.-1
40 002576 106414         SUB# 0,1,SZR
41 002577 006162         EHALT
42
43 002600 006401 C59:    JSR @.+1         ;MULTI LEVEL INDIRECT
44 002601 102602         @.+1             ;ON JSR SHOULD STORE
45 002602 102603         @.+1             ;ADDRESS C59+1 IN AC3.
46 002603 002604         .+1              ;CHECK AND GATE PRODUCING
47 002604 020775         LDA 0,C59+1
48 002605 152154         ADCOL# 3,0,SZR
49 002606 006162         EHALT
```

```
▲ 0036   .MAIN
01
02 02607 102400 C60:    SUB 0,0          ;MISC AC SELECT TEST.
03 02610 176400          SUB 3,3
04 02611 126000          ADC 1,1
05 02612 152000          ADC 2,2
06 02613 117014          ADD# 0,3,SZR
07 02614 006162          EHALT
08
09 02615 102400 C61:     SUB 0,0          ;MISC AC SELECT TEST.
10 02616 126400          SUB 1,1
11 02617 152000          ADC 2,2
12 02620 176000          ADC 3,3
13 02621 162015          ADC# 3,0,SNR
14 02622 146004          ADC 2,1,SZR
15 02623 006162          EHALT
16
17 02624 063700 C62:     SKPDZ 0          ;SUB INSTRUCTION SHOULD
18 02625 102401          SUB 0,0,SKP      ;SHOULD NOT BE EXECUTED.
19 02626 101001          MOV 0,0,SKP
20 02627 006162          EHALT
21
22 02630 102000 C63:     ADC 0,0          ;SUB INSTRUCTION SHOULD
23 02631 040000          STA 0,0
24 02632 010000          ISZ 0
25 02633 102401          SUB 0,0,SKP
26 02634 100004          COM 0,0,SZR
27 02635 006162          EHALT
28
29 02636 102444 C64:     SUBO 0,0,SZR     ;TEST SBN
30 02637 000401          JMP .+1
31 02640 100067          COMC 0,0,SBN
32 02641 006162          EHALT
33
34 02642 102625 C65:     SUBZR 0,0,SNR    ;MISC ALC TEST.
35 02643 006162          EHALT
36
37 02644 102626 C66:     SUBZR 0,0,SEZ
38 02645 006162          EHALT
39
40 02646 102426 C67:     SUBZ 0,0,SEZ
41 02647 006162          EHALT
42
43 02650 102046 C68:     ADCO 0,0,SEZ
44 02651 101001          MOV 0,0,SKP
45 02652 006162          EHALT
46
47 02653 034144 C69:     LDA 3,K20        ;THE INDIRECT LOAD SHOULD
48 02654 054020          STA 3,20         ;LOAD THE CONTENTS OF
49 02655 020161          LDA 0,K123       ;LOCATION 21.
50 02656 040021          STA 0,21
51 02657 026020          LDA 1,@20
52 02660 106414          SUB# 0,1,SZR
53 02661 006162          EHALT
```

```
A 0037   .MAIN
01
02 002662 102520 C70:     SUBZL 0,0          ;AFTER DECREMENT C(37)
03 002663 040037          STA 0,37           ;POINTS TO LOC 0 WHICH
04 002664 040000          STA 0,0            ;SHOULD DECREMENT TO 0 AND
05 002665 016037          DSZ @37            ;SKIP ON THE DSZ.
06 002666 006162          EHALT
07 002667 020001 C71:     LDA 0,1            ;LOC 1 IS LOADED TO
08 002670 152620          SUBZR 2,2          ;100000 WHEN THE PROGRAM
09 002671 112414          SUB# 0,2,SZR       ;WAS READ IN. NOTHING SHOULD
10 002672 006162          EHALT              ;CHANGE IT...
11 002673 010121 C72:     ISZ PASS           ;END OF THE TEST!
12 002674 000401          JMP .+1            ;INCREMENT THE PASS COUNTER
13 002675 024046          LDA 1,EGGS         ;AND ITERATE THE PROGRAM.
14 002676 125005          MOV 1,1,SNR
15 002677 002407          JMP @.+7
16 002700 014051          DSZ EGGS+3
17 002701 002405          JMP @.+5
18 002702 034052          LDA 3,EGGS+4
19 002703 020051          LDA 0,EGGS+3
20 002704 041776          STA 0,-2,3
21 002705 001400          JMP 0,3
22 002706 000405          A01
23
24 002707 054433 ERR:     STA 3,RETURN
25 002710 044412          STA 1,.AA01
26 002711 024046          LDA 1,EGGS
27 002712 125004          MOV 1,1,SZR
28 002713 000404          JMP .+4
29 002714 024406          LDA 1,.AA01
30 002715 063077          HALT
31 002716 001400          JMP 0,3
32 002717 004404          JSR EPRINT
33 002720 034052          LDA 3,EGGS+4
34 002721 001400          JMP 0,3
35 002722 000000 .AA01:   0
36
37 002723 054422 EPRINT:  STA 3,ESWIT
38 002724 006413          JSR @ICRLF
39 002725 006407          JSR @IMESS
40 002726 002744          HEADER
41 002727 020413          LDA 0,RETURN
42 002730 125000          ADC 1,1
43 002731 107000          ADD 0,1
44 002732 006406          JSR @IPOCT
45 002733 002410          JMP @ESWIT
46
47 002734 002746 IMESS:   MESS
48 002735 003042 ICHAR:   CHAR
49 002736 003115 ITYPE:   TYPE
50 002737 003071 ICRLF:   CRLF
51 002740 002765 IPOCT:   POCT
52 002741 002770 IPDEC:   PDEC
53 002742 000000 RETURN:  0
54 002743 000000 ESWIT:   0
55               HEADER:  .TXT  !
56 002744 041520 PC       !
   002745 000011
```

```
A 0038  .MAIN
01
02                ;TTO NON INTERRUPT PACKAGE
03                ;"MESS" PRINTS ASCII MESSAGES AS SPECIFIED BY ASSEMBLR
04                ;"CHAR" PRINTS ASCII CHARACTOR, C(0)R,C(0)L MUST BE 0
05                ;WILL RETURN +2 IF C(0)R=0,CORRECTS THE PARITY,33 SIMULATE
06                ;"TYPE" PRINTS C(0)R. MUST HAVE PROPER PARITY. RETURN IS
07                ;TO CALL+1.REPLACE THIS ROUTINE WITH INTERRUPT TYPE IF DESIRED.
08                ;"CRLF" PRINTS A CARRIAGE RETURN
09                ;"POCT" PRINTS C(1) IN OCTAL FOLLEOOWED BY A TAB
10                ;"PDEC" PRINTS C(1) IN DECIMAL,LEADONG ZEROS SUPPRESSED,
11                ;FOLLOWED BY A TAB.
12
13 02746 054546 MESS:   STA 3,MESSR       ;PRINT A TEXT MESSAGE
14 02747 010545          ISZ MESSR
15 02750 031400          LDA 2,0,3        ;C(2) POINTS TO MESSAGE
16 02751 024542          LDA 1,C377       ;A 8 BIT MASK
17 02752 021000          LDA 0,0,2        ;C(2)=DATA WORD
18 02753 125112          MOVL# 1,1,SZC
19 02754 123701          ANDS 1,0,SKP
20 02755 123401          AND 1,0,SKP      ;C(0)=DATA CHARACTOR RIGHT
21 02756 151400          INC 2,2          ;INC TO NEXT WORD
22 02757 124000          COM 1,1          ;FLIP MASK
23 02760 004462          JSR CHAR         ;PRINT
24 02761 000771          JMP MESS+4       ;ANOTHER
25 02762 002532          JMP @MESSR       ;LAST
26
27 02763 020525 ZOCT:   LDA 0,CH240
28 02764 101001          MOV 0,0,SKP
29
30 02765 020525 POCT:   LDA 0,K60
31 02766 030433          LDA 2,OCTAB      ;PRINT C(1) IN OCTAL
32 02767 000403          JMP .+3
33 02770 030441 PDEC:   LDA 2,DECTB      ;PRINT C(1) IN DECIMAL
34 02771 020517          LDA 0,CH240      ;SUPPRESS LEADING  ZEROS
35 02772 054447          STA 3,RADRET     ;BOTH ENTRYS PRINT NUMBER
36 02773 040445          STA 0,ZSUPP      ;THEN TAB TO NEXT POSITION
37 02774 050401          STA 2,.+1
38 02775 000000 DECOCT: 0                ;A"LDA 2,TABLE" INSTRUCTION
39 02776 010777          ISZ .-1
40 02777 034442          LDA 3,RADRET     ;SETUP "TAB" AT END
41 03000 020503          LDA 0,CHTAB
42 03001 151005          MOV 2,2,SNR      ;IF TABLE ENTRY=0
43 03002 000440          JMP CHAR         ;EXIT WITH TAB
44 03003 034435          LDA 3,ZSUPP      ;ZEROS SUPPRESS STUF
45 03004 102400          SUB 0,0
46 03005 146512 DECOT:  SUBL# 2,1,SZC
47 03006 000405          JMP DECP
48 03007 146400          SUB 2,1          ;FORM THE DIGIT
49 03010 034502          LDA 3,K60
50 03011 101400          INC 0,0
51 03012 000773          JMP DECOT
52 03013 151235 DECP:   MOVZR# 2,2,SNR
53 03014 034476          LDA 3,K60
54 03015 054423          STA 3,ZSUPP      ;C(0)=DIGIT
55 03016 163000          ADD 3,0          ;MAKE ASCII
56 03017 004423          JSR CHAR         ;PRINT
57 03020 000755          JMP DECOCT       ;GET NEXT DIGIT
58
```

```
▲ 00030  .MAIN
01
02
03 03021 030425 OCTAB:  LDA 2,.+1+.-DECOCT
04 03022 100000         100000
05 03023 010000         10000
06 03024 001000         1000
07 03025 000100         100
08 03026 000010         10
09 03027 000001         1
10 03030 000000         0
11
12 03031 030435 DECTB:  LDA 2,.+1+.-DECOCT
13       000012 .RDX 10
14 03032 023420         10000
15 03033 001750         1000
16 03034 000144         100
17 03035 000012         10
18 03036 000001         1
19 03037 000000         0
20       000010 .RDX 8
21
22 03040 000000 ZSUPP:  0
23 03041 000000 RADRET: 0
24
25 03042 054442 CHAR:   STA 3,CHRET      ;PRINT C(0) RIGHT
26 03043 101325         MOVZS 0,0,SNR    ;RETURN +2 IF NULL
27 03044 001401         JMP 1,3
28 03045 040440         STA 0,CHSAV
29 03046 176000         ADC 3,3          ;COMPUTE THE PARITY
30 03047 117000         ADD 0,3
31 03050 163404         AND 3,0,SZR
32 03051 000775         JMP .-3
33 03052 176660         SUBCR 3,3        ;COMBIND PARITY WITH CHAR
34 03053 020432         LDA 0,CHSAV
35 03054 163300         ADDS 3,0
36
37 03055 034426 CHAR1:  LDA 3,CHTAB      ;IS THIS A TAB
38 03056 116405         SUB 0,3,SNR
39 03057 000403         JMP .+3          ;YES
40 03060 004435         JSR TYPE         ;NO PRINT IT
41 03061 002423         JMP @CHRET       ;EXIT
42
43 03062 020424         LDA 0,CHORZ      ;SIMULATE A TAB
44 03063 034424         LDA 3,CHAR7      ;VIA 1 TO 8 SPACES
45 03064 117405         AND 0,3,SNR
46 03065 002417         JMP @CHRET
47 03066 020422         LDA 0,CH240
48 03067 004426         JSR TYPE
49 03070 000772         JMP .-6
50
```

```
A 0040  .MAIN
01
02
03
04 03071 054420 CRLF:   STA 3,CRLFR      ;SAVE RETURN
05 03072 020410         LDA 0,C215
06 03073 004747         JSR CHAR         ;PRINT CARRIAGE AND LF
07 03074 020405         LDA 0,C212
08 03075 004745         JSR CHAR
09 03076 102400         SUB 0,0
10 03077 040407         STA 0,CHORZ      ;CLEAR HORZ POSISTION
11 03100 002411         JMP @CRLFR       ;EXIT
12
13 03101 000212 C212:   212
14 03102 000215 C215:   215
15 03103 000011 CHTAB:  11
16 03104 000000 CHRET:  0
17 03105 000000 CHSAV:  0
18 03106 000000 CHORZ:  0
19 03107 000007 CHAR7:  7
20 03110 000240 CH240:  240
21 03111 000000 CRLFR:  0
22 03112 000060 K60:    60
23
24 03113 000377 C377:   377
25 03114 000000 MESSR:  0
26 03115 054412 TYPE:   STA 3,TYPRET     ;TYPE THE C(0)R TF
27 03116 010770         ISZ CHOR7
28 03117 074477         READS 3          ;SWITCH 1(0).
29 03120 175100         MOVL 3,3
30 03121 175102         MOVL 3,3,SZC
31 03122 002405         JMP @TYPRET      ;INHIBIT TYPE EXIT.
32 03123 063511         SKPBZ TTO
33 03124 000777         JMP .-1
34 03125 061111         DOAS 0,TTO
35 03126 002401         JMP @TYPRET
36 03127 000000 TYPRET: 0
37
38       003130         .LOC 3130
39                      .TXT    /COPYRIGHT (C) DGC,1970,74
   03130 047503
   03131 054520
   03132 044522
   03133 044107
   03134 020124
   03135 041450
   03136 020051
   03137 043504
   03140 026103
   03141 034461
   03142 030067
   03143 033454
40 03144 040464 ALL RIGHTS RESERVED/
   03145 046114
   03146 051040
   03147 043511
   03150 052110
   03151 020123
   03152 042522
   03153 042523
```

```
 0001   .MAIN
  03154 053122
  03155 042105
  03156 000000
01
02        003170          .LOC 3170
03                        .TXTE  !LOGIC TST1!
  03170 147714
  03171 144507
  03172 120303
  03173 051724
  03174 130724
  03175 000000
04 03176 000010           000010
05 03177 000043           START
06 03200 000144           000144
07 03201 000000           000000
08 03202 000000           000000
09 03203 000000           000000
10 03204 000000           000000
11 03205 000000           000000
12
13                .END
```

A00	000400	3/09	4/04
A01	000405	4/10	37/22
A02	000407	4/16	
A03	000411	4/21	
A03A	000413	4/26	
A04	000416	4/31	
A05	000420	4/36	
A06	000423	4/42	
A07	000426	4/46	
A08	000431	5/02	
A09	000440	5/10	
A10	000443	5/16	
A100	001150	15/45	
A101	001153	15/53	
A11	000446	5/22	
A12	000451	5/26	
A13	000454	5/30	
A14	000457	5/36	
A15	000461	5/41	
A16	000463	5/47	
A17	000465	6/02	
A18	000472	6/08	
A19	000475	6/15	
A20	000500	6/20	
A21	000503	6/26	
A22	000506	6/35	
A23	000511	6/39	
A24	000514	6/46	
A25	000517	7/02	
A26	000522	7/07	
A27	000525	7/11	
A28	000530	7/17	
A29	000533	7/23	
A30	000536	7/29	
A31	000542	7/36	
A32	000546	7/44	
A32A	000551	7/50	
A32B	000554	7/54	
A33	000557	8/02	
A34	000563	8/10	
A35	000571	8/19	
A36	000575	8/24	
A37	000600	8/28	
A38	000603	8/32	
A39	000607	8/39	
A40	000613	9/02	
A41	000620	9/08	
A42	000624	9/14	
A43	000630	9/20	
A44	000633	9/28	
A45	000636	9/35	
A46	000644	9/43	
A47	000646	10/02	
A48	000650	10/08	
A49	000653	10/12	
A50	000656	10/17	
A51	000662	10/25	
A52	000666	10/32	
A53	000672	10/37	

A54	000676	10/42
A55	000701	11/02
A56	000704	11/06
A57	000707	11/10
A58	000712	11/14
A59	000715	11/21
A60	000720	11/27
A61	000723	11/31
A62	000726	11/35
A63	000731	11/39
A64	000734	12/02
A65	000742	12/09
A66	000744	12/13
A67	000746	12/17
A68	000755	12/25
A69	000760	12/29
A70	000764	12/34
A71	000770	12/39
A72	000774	12/44
A73	001000	12/49
A74	001004	13/02
A75	001010	13/09
A76	001014	13/15
A77	001020	13/20
A78	001024	13/25
A79	001027	13/33
A80	001032	13/37
A81	001036	13/42
A82	001041	13/46
A83	001045	14/02
A84	001054	14/10
A85	001060	14/15
A86	001064	14/20
A87	001070	14/25
A88	001077	14/33
A89	001103	14/38
A90	001107	14/43
A91	001113	15/02
A92	001116	15/06
A93	001121	15/10
A94	001124	15/14
A95	001127	15/18
A96	001132	15/22
A97	001135	15/26
A98	001142	15/32
A99	001145	15/36
B00	001157	16/02
B01	001161	16/07
B02	001164	16/11
B03	001167	16/15
B04	001173	16/20
B05	001177	16/25
B06	001203	16/30
B07	001206	16/34
B08	001211	16/38
B09	001215	16/43
B10	001220	16/47
B11	001223	16/51
B12	001226	17/02

B13	001231	17/06
B14	001234	17/10
B15	001237	17/14
B16	001242	17/20
B17	001245	17/26
B18	001250	17/32
B19	001253	17/39
B20	001256	17/45
B21	001261	17/51
B22	001263	18/02
B23	001266	18/08
B24	001272	18/13
B25	001276	18/18
B26	001302	18/23
B27	001305	18/27
B28	001307	18/31
B29	001313	18/36
B30	001321	18/43
B31	001326	18/49
B32	001333	18/55
B33	001340	20/02
B34	001343	20/06
B35	001347	20/11
B36	001351	20/16
B37	001354	20/21
B38	001356	20/25
B39	001361	20/30
B40	001364	20/34
B41	001371	20/40
B42	001376	20/46
B43	001403	20/52
B44	001410	21/02
B45	001415	21/08
B46	001422	21/16
B47	001426	21/23
B48	001432	21/28
B49	001436	21/34
B50	001442	21/40
B51	001446	21/46
B52	001452	22/02
B53	001457	22/08
B54	001464	22/14
B55	001470	22/22
B56	001476	22/32
B57	001504	22/39
B58	001514	23/02
B59	001524	23/11
B60	001534	23/20
B61	001544	23/29
B62	001552	23/37
B63	001555	23/41
B64	001560	23/45
B65	001564	23/50
B66	001570	24/02
B67	001575	24/08
B68	001602	24/14
B69	001610	24/22
B70	001615	24/28
B71	001622	24/34

B72	001625	24/38	
B73	001632	24/45	
B74	001637	24/51	
B75	001643	25/02	
B76	001651	25/09	
B77	001657	25/16	
B78	001663	25/21	
B79	001667	25/26	
B80	001674	25/32	
B81	001701	25/38	
B82	001706	25/44	
B83	001713	25/50	
B84	001720	26/02	
B85	001725	26/08	
B86	001732	26/14	
B87	001737	26/20	
B88	001744	26/26	
B89	001751	26/32	
B90	001756	26/38	
B91	001763	26/44	
B92	001770	27/02	
B93	001777	27/10	
B94	002006	27/18	
B94A	002015	27/26	
B95	002021	27/31	
B96	002030	27/39	
B97	002036	27/46	
B98	002044	27/53	
C00	002052	28/02	
C01	002061	28/10	
C02	002071	28/19	
C03	002100	28/27	
C04	002107	28/35	
C05	002114	28/41	
C06	002122	28/48	
C07	002130	29/02	
C08	002137	29/10	
C09	002144	29/16	
C10	002150	29/21	
C11	002155	29/27	
C12	002161	29/33	
C13	002167	29/40	
C14	002176	29/48	
C15	002205	30/02	
C16	002214	30/10	
C17	002221	30/16	
C20	002225	30/21	
C21	002227	30/26	
C212	003101	40/07	40/13
C215	003102	40/05	40/14
C22	002233	30/31	
C23	002240	30/38	
C24	002243	30/42	
C25	002250	30/48	
C26	002255	31/01	
C27	002262	31/08	
C28	002264	31/11	
C29	002274	31/20	
C30	002302	31/30	

C31	002310	31/38						
C31A	002316	31/45						
C32	002324	31/53						
C33	002332	32/02						
C34	002340	32/09						
C35	002346	32/16						
C36	002355	32/24						
C37	002362	32/30						
C377	003113	38/16	40/24					
C38	002367	32/36						
C39	002375	32/45						
C40	002403	33/02						
C40A	002411	33/09						
C41	002417	33/16						
C42	002425	33/23						
C43	002435	33/32						
C44	002443	33/40						
C45	002460	33/46	34/02					
C46	002467	34/10						
C47	002475	34/17						
C50	002502	34/23						
C51	002510	34/30						
C52	002516	34/37						
C53	002524	34/44						
C54	002534	35/02						
C55	002541	35/08						
C56	002551	35/17						
C57	002561	35/26						
C58	002567	35/33						
C59	002600	35/43	35/47					
C60	002607	36/02						
C61	002615	36/09						
C62	002624	36/17						
C63	002630	36/22						
C64	002636	36/29						
C65	002642	36/34						
C66	002644	36/37						
C67	002646	36/40						
C68	002650	36/43						
C69	002653	36/47						
C70	002662	37/02						
C71	002667	37/07						
C72	002673	37/11						
CH240	003110	38/27	38/34	39/47	40/20			
CHAR	003042	37/48	38/23	38/43	38/56	39/25	40/06	40/08
CHAR1	003055	39/37						
CHAR7	003107	39/44	40/19					
CHOR7	003106	39/43	40/10	40/18	40/27			
CHRET	003104	39/25	39/41	39/46	40/16			
CHSAV	003105	39/28	39/34	40/17				
CHTAB	003103	38/41	39/37	40/15				
CRLF	003071	37/50	40/04					
CRLFR	003111	40/04	40/11	40/21				
DECOC	002775	38/38	38/57	39/03	39/12			
DECOT	003005	38/46	38/51					
DECP	003013	38/47	38/52					
DECTB	003031	38/33	39/12					
EGGS	000046	3/10	3/11	4/06	37/13	37/16	37/18	37/19
		37/33						37/26