DataGeneral

PRELIMINARY

NOVA 4/C
FIELD REPLACEABLE
UNIT MANUAL

015-000097-00

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Printed in the United States of America
Rev. 00, June 1979

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PREFACE

This manual is a guide to troubleshooting and repairing NOVA 4/C computers at the field replaceable unit level, commonly referred to as "board swapping".

It is organized around four major sections.

Part I is a product description, which

- Introduces the major assemblies and explains how they interconnect
- Defines the field replaceable units
- Lists the related documentation
- Explains how to use the consoles.

Part II is devoted to troubleshooting. It explains both how to perform an initial checkout and how to repair a system that failed after normal operation. It describe procedures for finding a failing field replaceable unit using:

- Visual checks
- The CPU's self-test feature
- Reliability and diagnostic test programs
- Simple manual tests

These procedures, written in a "cookbook" manner, should allow the field engineer to repair most failures in a minimum period of time.

Part III contains reference information about the power supplies and the the major printed circuit boards. This information is useful when you troubleshoot with an oscilloscope.

Part IV provides detailed mechanical replacement procedures for each field replaceable unit.

WARNING: The power supplies in these units have hazardous voltages on their printed circuit boards. They should be repaired only by trained service personnel.

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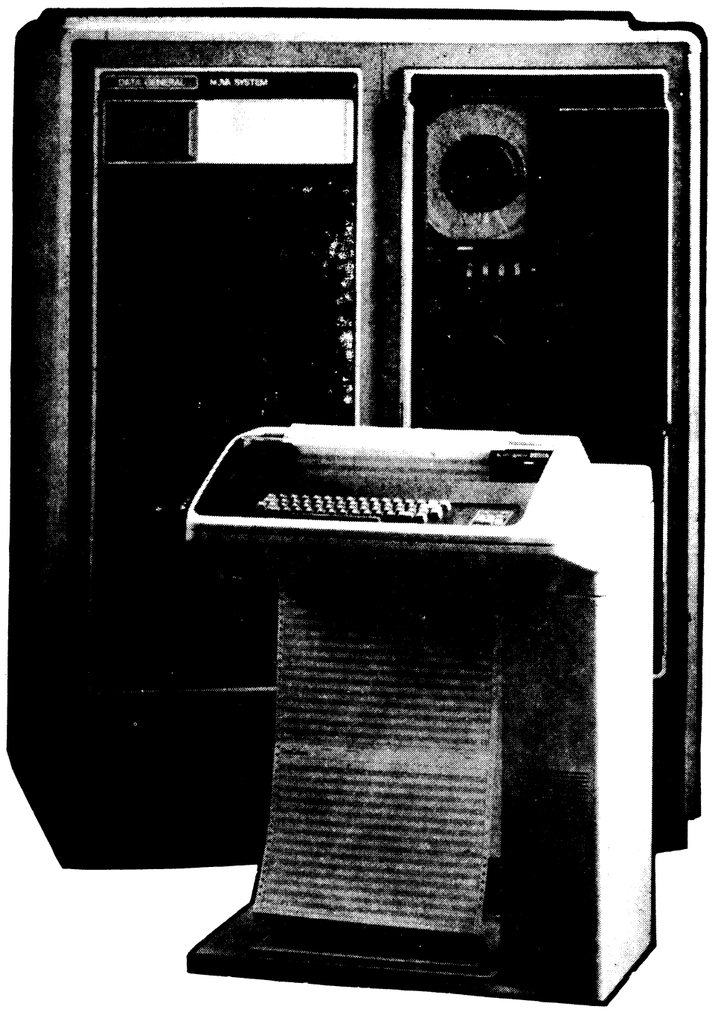


Figure 1.1 NOVA 4/C Computer System

CHAPTER 1
INTRODUCTION TO NOVA 4/C COMPUTERS

NOVA 4/C computers incorporate a modular design plus self-diagnostic capabilities that facilitate maintenance and provide high reliability. In most cases, the user can identify the failing field replaceable unit by running simple tests, thus minimizing repair time.

The NOVA 4/C computer supports up to 64K bytes of dynamic RAM (random access memory).

NOVA 4 computers are rack-mounted in NEMA-standard equipment cabinets. These cabinets also provide housing for NOVA line peripheral equipment, such as magnetic tape drives and rack-mounted disc drives.

The computer consist of the following basic modules, which are tailored to the user's selected configuration:

- Computer chassis
- Power supply
- Fan module
- Front console
- Printed circuit CPU board

CHASSIS

Two computer chassis are available to NOVA 4 users: 5- and 16-slot. Each has its own backpanel printed circuit board with connectors for the system printed circuit boards. These boards, including a slide-in power supply board (5 or 16-slot version), are inserted from the front of the chassis, which is easily accessed by removing the NOVA 4 front panel attached to the equipment cabinet. Access to the backpanel is via the rear door of the equipment cabinet.

16-Slot Chassis

This chassis holds up to sixteen 15-inch by 15-inch printed circuit boards plus the 16-slot power supply and fan module.

Bus termination for the backpanel is provided by a resistor fence (soldered into the backpanel below slot 1) and two bus terminator cards, one for the A side and one for the B side. The bus terminator cards push onto the backpanel pins of slot 2.

The 16-slot chassis supports up to twenty I/O paddleboards, which are vertically mounted at the rear of the unit.

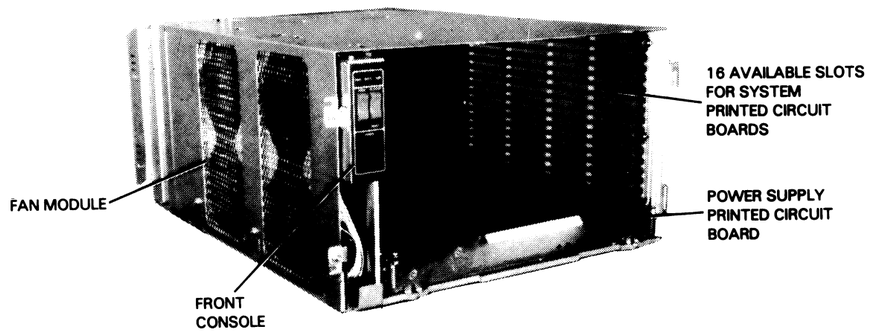


Figure 1.2 16-Slot Chassis (Front View)

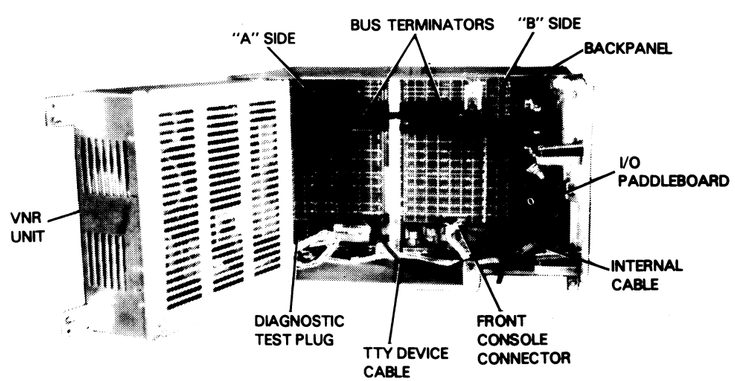


Figure 1.3 16-Slot Chassis (Rear View)

5-Slot Chassis

This chassis holds up to five 15-inch by 15-inch printed circuit boards plus the 5-slot power supply and fan modules.

Bus termination for the backpanel is provided by a resistor fence, which is soldered into the backpanel above slot 5.

The 5-slot chassis supports up to ten I/O paddleboards. Like the 16-slot chassis, the paddleboards are vertically mounted at the rear of the unit.

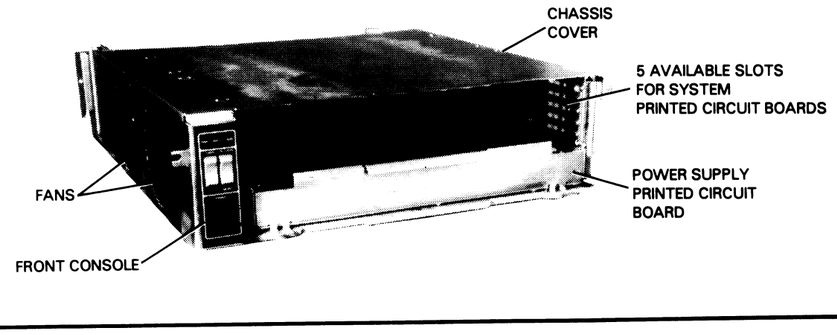


Figure 1.4 5-Slot Chassis (Front View)

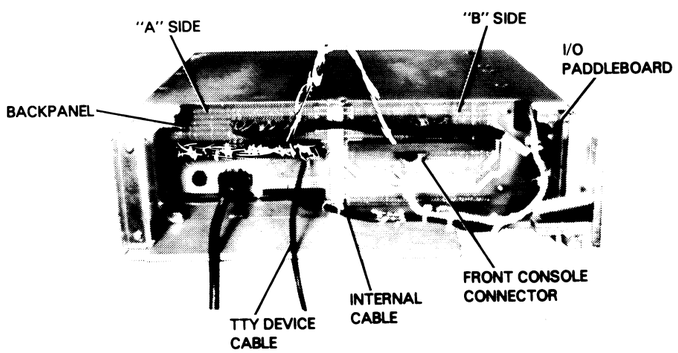


Figure 1.5 5-Slot Chassis (Rear View)

POWER SUPPLY

Each chassis has its own power supply, which is available with or without battery backup.

16-Slot Power Supply

The 16-slot power supply and distribution system consists of a VNR (voltage non-regulated) unit that is vertically mounted to the rear of the chassis and a slide-in power supply printed circuit board which plugs into the chassis backpanel.

The VNR unit converts power from the ac supply line to non-regulated dc power, which it supplies to the power supply board via an internal cable. The internal cable also:

- Carries ac power from the VNR unit to the fan module
- Connects the front console switches and indicators to the backpanel
- Connects the power switch to the VNR unit.

When the battery backup option is present, the VNR unit contains a a battery that supplies power to the battery backup circuits in the power supply board.

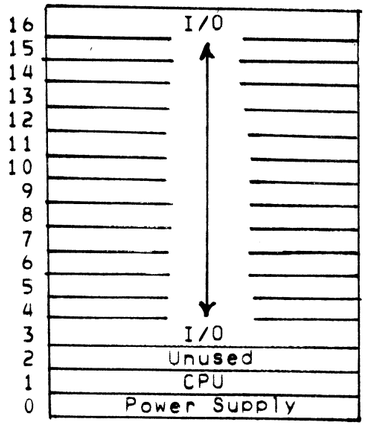


Figure 1.6
Slot assignment Diagram
16-slot chassis

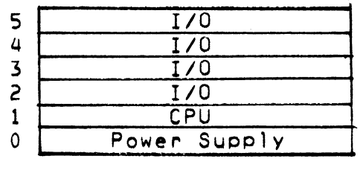


Figure 1.7
Slot assignment diagram
5-slot chassis

The power supply board regulates the dc voltages from the VNR unit and supplies the required voltages to the remainder of the system via the etch on the backpanel. It also generates the system clocks and supplies them to the system printed circuit boards via the backpanel.

For more information about the operation of the 16-slot power supply, see Part II, Chapter 6, and Part III, Chapter 9.

5-Slot Power Supply

The 5-slot distribution system and power supply resides on a single slide-in power supply printed circuit board. It converts power from the ac supply line to regulated dc voltages. When the battery backup option is present, the battery also resides on the power supply board.

The 5-slot power supply supplies the required dc voltages to the system printed circuit boards via the etch on the backpanel while it supplies ac power to the fan modules via the internal cable. The internal cable also:

- Connects the front console switches and indicators to the backpanel
- Connects the power switch to the power supply.

The 5-slot power supply also generates the system clocks and supplies them to the system printed circuit boards via the backpanel.

For more information about the operation of the 5-slot power supply, see Part II, Chapter 6, and Part III, Chapter 10.

FAN MODULES

Both the 16 and 5-slot fan modules reside on the left side of their respective chassis. They draw air from outside the cabinet and force it through the chassis. On the 16-slot chassis, the fan module, containing four fans, slides into the chassis from the front of the unit. On the 5-slot chassis, two fans mount on the inside of the chassis cover.

FRONT CONSOLE

The front console assembly mounts on the fan module in the 16-slot chassis and on the cover in the 5-slot chassis. It consists of three switches and three indicator lights. The switches allow the user to control basic functions such as power up/down, program load and reset while the indicator lights provide information concerning power status and the CPU's operating mode. The remaining operator control functions are implemented by a virtual console (see below under "CPU Board"). Operator information for both consoles appears in Part I, Chapter 2.

CPU BOARD

The CPU board occupies slot 1 of the chassis. This board contains:

- Central processing unit (CPU)
- Main memory (dynamic RAM array)
- Full-duplex, asynchronous communications interface
- Virtual console, residing in 512 words of ROM (read only memory) with 16 words of scratchpad RAM
- Programmable real-time clock (optional)

CPU

The CPU is a 16-bit microprogrammed processor, which means its data paths are controlled by microinstructions stored in internal ROM. It incorporates the full NOVA 16-bit architecture, including four 16-bit accumulators and hardware stack and frame pointers. NOVA 4 CPUs execute an extended NOVA 3 instruction set, augmented with load and store byte instructions and, optionally, signed multiply and divide instructions.

The CPU operates in two modes: run and console. In run mode, the CPU executes instructions stored in main memory (dynamic RAM). In console mode, the CPU executes instructions stored in the resident virtual console ROM.

On power up or after a power fail when battery backup is not present, the CPU runs a self-test. This test:

- Exercises basic CPU functions
- Checks main memory
- Checks the operation of the device connected to the resident asynchronous interface.

On completion of the self-test, the CPU enters console mode and is ready to accept user commands. For more information about the self-test, see Part II, Chapter 5.

As shown in figure 1.8, the CPU communicates with the main memory and the virtual console via the two internal buses, ALUOUT<0-15> and MBUS<0-15>. The ALUOUT bus carries 15-bit addresses and 16-bit data words from the CPU to main memory and 9-bit addresses from the CPU to the virtual console. The MBUS bus carries 16-bit data words from main memory and the virtual console to the CPU.

The CPU communicates with the resident asynchronous interface via the two internal buses, ALUOUT<0-15> and ALUIN<0-15>. It communicates with any other I/O controller using the standard 48-line NOVA I/O bus.

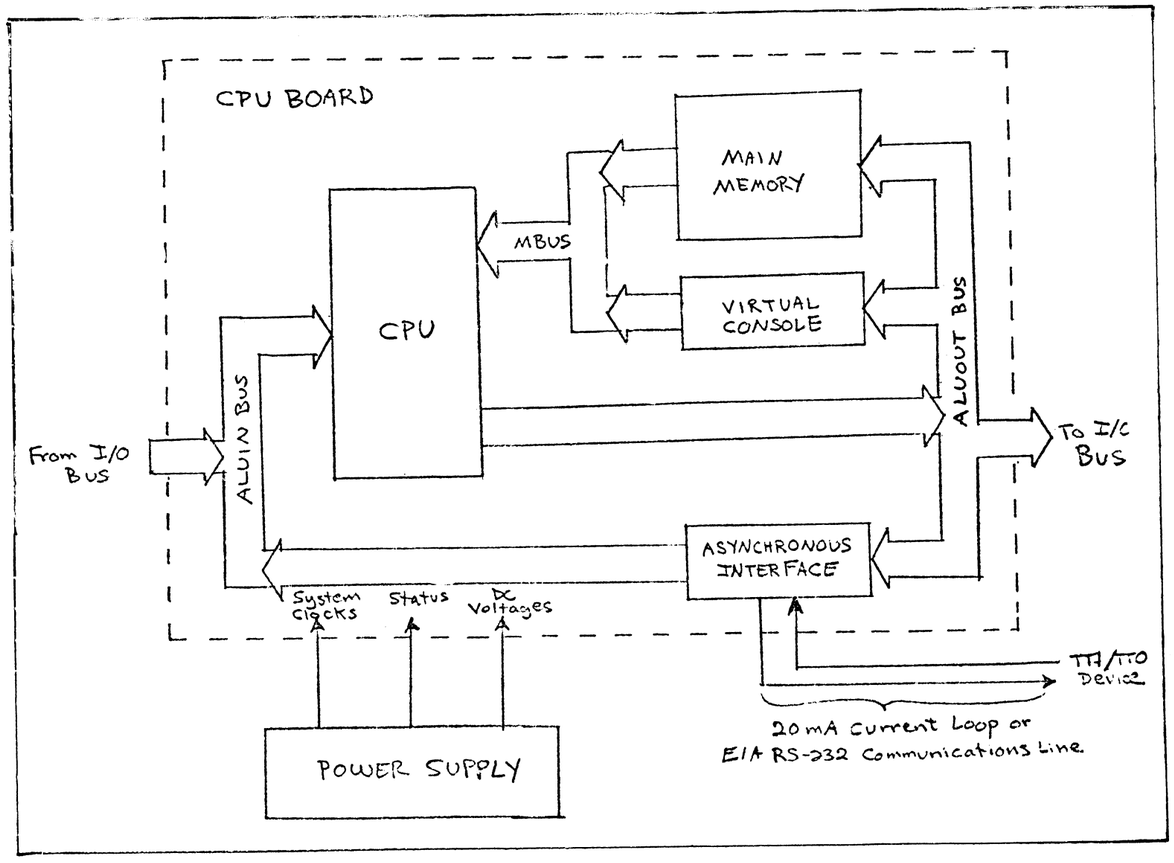


Figure 1.8 Simplified Printed Circuit Board Interconnection Diagram

Main Memory

Main memory contains a dynamic RAM array and refresh logic. Two different sizes of RAM arrays are available:

- 32K bytes (16K words)
- 64K bytes (32K words)

Each array use N-channel MOS memory elements which have a 16,384 by 1 bit organization. Memory read/write cycle time is 400 ns.

Asynchronous Interface

This interface is a programmed I/O controller containing both a transmitter and receiver. It allows full-duplex communications between a serial, asynchronous terminal via either a 20mA current loop or an EIA RS-232C communications line connected to the CPU board's A connector via the backpanel. In addition to standard send/receive terminals, it supports both an automatic send/receive terminal (i.e., a terminal equipped with a paper tape reader) as well as a 60cps DASHER terminal printer.

When the CPU is in run mode and unlocked (as indicated by the position of the front console Lock switch), a BREAK character received by the interface interrupts the executing program and places the CPU in console mode.

Virtual Console

The virtual console allows a user whose terminal is connected to the resident asynchronous interface to inspect and modify the system's state and aid program debugging.

It provides the user with the ability to:

- Stop, start and continue program execution
- Examine and/or alter CPU registers and memory locations
- Initiate program load sequences.

Real-Time Clock

This optional interface can supply program interrupt requests at one of four program-selectable frequencies: 10Hz, 100Hz, 1000Hz or power line frequency.

For more information concerning the CPU board, see Part III, Chapter 11.

FIELD REPLACEABLE UNITS

Figures 1.9 and 1.10 show the field replaceable units and their interconection. Tables 1.1 and 1.2 list their Data General assembly numbers.

NOVA 4/C with 32K byte Memory

NOVA 4/C with 32K byte Memory & Real-Time Clock option

NOVA 4/C with 32K byte Memory & Multiply/Divide option

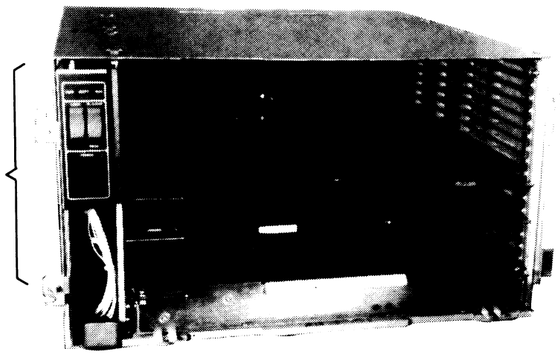
NOVA 4/C with 32K byte Memory & Real-Time Clock & Multiply/Divide options

NOVA 4/C with 64K byte Memory

NOVA 4/C with 64K byte Memory & Real-Time Clock option

NOVA 4/C with 64K byte Memory & Multiply/Divide option

NOVA 4/C with 64K byte Memory & Real-Time Clock & Multiply/Divide options



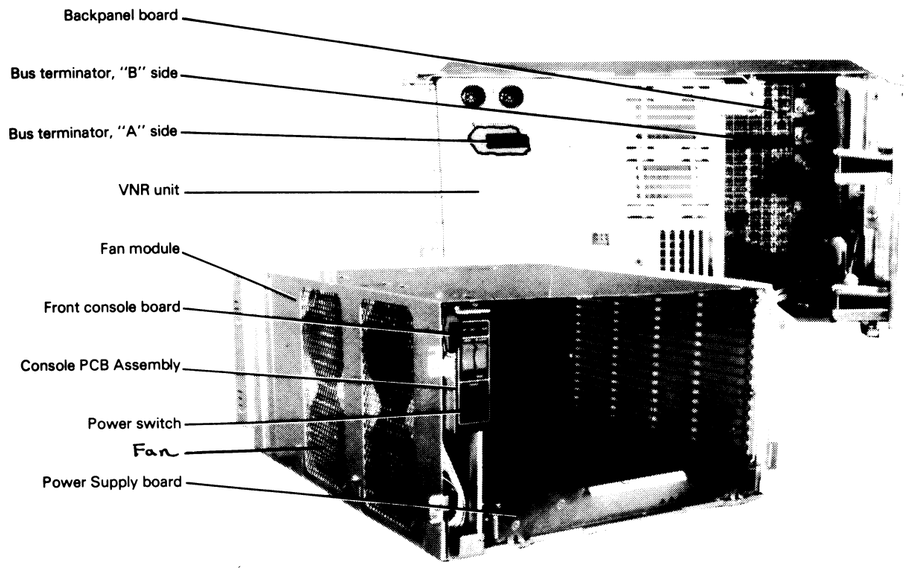
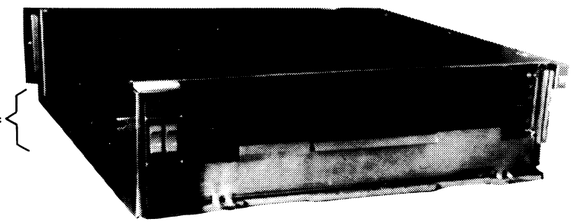


Figure 1.9 Exploded View of 16-Slot FRUs

NOVA 4/C with 32K byte Memory
NOVA 4/C with 32K byte Memory & Real-Time Clock option
NOVA 4/C with 32K byte Memory & Multiply/Divide option
NOVA 4/C with 32K byte Memory & Real-Time Clock & Multiply/Divide options
NOVA 4/C with 64K byte Memory
NOVA 4/C with 64K byte Memory & Real-Time Clock option
NOVA 4/C with 64K byte Memory & Multiply/Divide option
NOVA 4/C with 64K byte Memory & Real-Time Clock & Multiply/Divide options



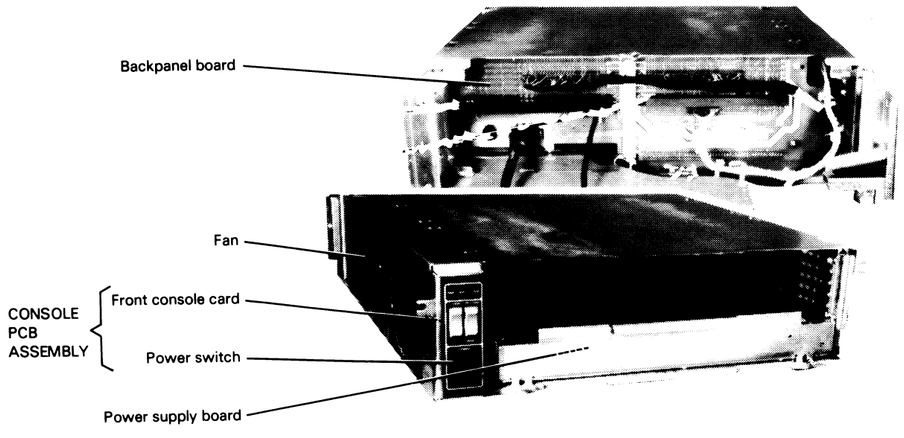


Figure 1.10 Exploded View of 5-Slot FRUs

Table 1.1 16-slot field replaceable units

Assembly No.	ROM Part No. Loc 29N	ROM Part No. Loc 33N	Description
005-12413	100-1831	100-1832	NOVA 4/C CPU with 32K byte (16K word) memory
005-12413	100-1833	100-1834	NOVA 4/C CPU with 32K byte (16K word) memory and real-time clock
005-12413	100-1835	100-1836	NOVA 4/C CPU with 32K byte (16K word) memory and multipy/divide option
005-12413	100-1837	100-1838	NOVA 4/C CPU with 32K byte (16K word) memory, real-time clock, and multipy/divide option
005-12415	100-1831	100-1832	NOVA 4/C CPU with 64K byte (32K word) memory
005-12415	100-1833	100-1834	NOVA 4/C CPU with 64K byte (32K word) memory and real-time clock
005-12415	100-1835	100-1836	NOVA 4/C CPU with 64K byte (32K word) memory and multiply/divide option
005-12415	100-1837	100-1838	NOVA 4/C CPU with 64K byte (32K word) memory, real-time clock, and multiply divide option
005-12073			Backpanel board
005-14135			Console PCB assembly
005-12429			VNR unit
005-12064			Power supply board with batttery backup
005-12061			Power supply board without battery backup
115-163			Fan
005-12076			Fan module
005-12438			Bus terminator, "A" side
005-12439			Bus terminator, "B" side
005-12489			Internal cable
005-07093			12V battery

Table 1.2 5-slot field replaceable units

Assembly No.	ROM Part No. Loc 29N	ROM Part No. Loc 33N	Description
005-12413	100-1831	100-1832	NOVA 4/C CPU with 32K byte (16K word) memory
005-12413	100-1833	100-1834	NOVA 4/C CPU with 32K byte (16K word) memory and real-time clock
005-12413	100-1835	100-1836	NOVA 4/C CPU with 32K byte (16K word) memory and multipy/divide option
005-12413	100-1837	100-1838	NOVA 4/C CPU with 32K byte (16K word) memory, real-time clock, and multipy/divide option
005-12415	100-1831	100-1832	NOVA 4/C CPU with 64K byte (32K word) memory
005-12415	100-1833	100-1834	NOVA 4/C CPU with 64K byte (32K word) memory and real-time clock
005-12415	100-1835	100-1836	NOVA 4/C CPU with 64K byte (32K word) memory and multiply/divide option
005-12415	100-1837	100-1838	NOVA 4/C CPU with 64K byte (32K word) memory, real-time clock, and multiply divide option
005-12402			Backpanel board
005-14135			Console PCB assembly
005-12406			Power supply board with battery backup
005-12404			Power supply board without battery backup
115-121			Fan
005-13470			Internal Cable
005-12873			6V battery

Power Supply Board

The power supply board provides several regulated dc voltages for the computer chassis. It also generates several clock and status signals for the CPU. Figure 9.3 shows the component parts of the power supply board. It does not show the battery backup circuits; we will cover those later.

Before we examine the off-line switching regulator, we should look at some of the support circuits:

- The auxiliary supply regulators power all supply circuits except the main voltage regulators. They also provide an adjustable voltage reference. This reference sets the levels of all the output voltages (which eliminates the need for individual adjustments).
- The master clocks generate several clock signals for the CPU. They also provide a ramp signal for the pulse width modulator along with switch signals for the H-bridge chopper.
- The sequencing logic turns the off-line switching regulator on or off in several steps. The power-up sequence begins after the power switch is turned on (ONSW), the clocks start up (RAMP) and the high voltage bulk supply stabilizes (HVS). First the relay closes. Then the +11 SW signal starts the H-bridge chopper. Finally the power-on (PON) signal starts the buck regulator. If the power switch is turned off, or a power or clock fault occurs, the sequencer opens the relay, stops the buck regulator and disables the H-bridge chopper.

We can now look at the main supply regulators. You will recognize all the main components of the off-line switching regulator at the top of the diagram.

Unfortunately, the off-line switcher can produce only one regulated output. So additional circuits are needed to regulate the remaining outputs. Because the power demands on these outputs are relatively low, linear series pass regulators are a practical choice. The 10 volt transformer winding powers the -5V regulator. The 14 volt transformer winding powers the +12V regulator. This component regulates ac power from the transformer before it rectifies it. The 3V regulator is powered by the 4 volt transformer winding. It rides on top of the 12V regulator to provide a +15V output.

The remaining circuits detect various kinds of power faults. They protect the supply from excessive loads, protect the computer from excessive voltages, and flag power failures.

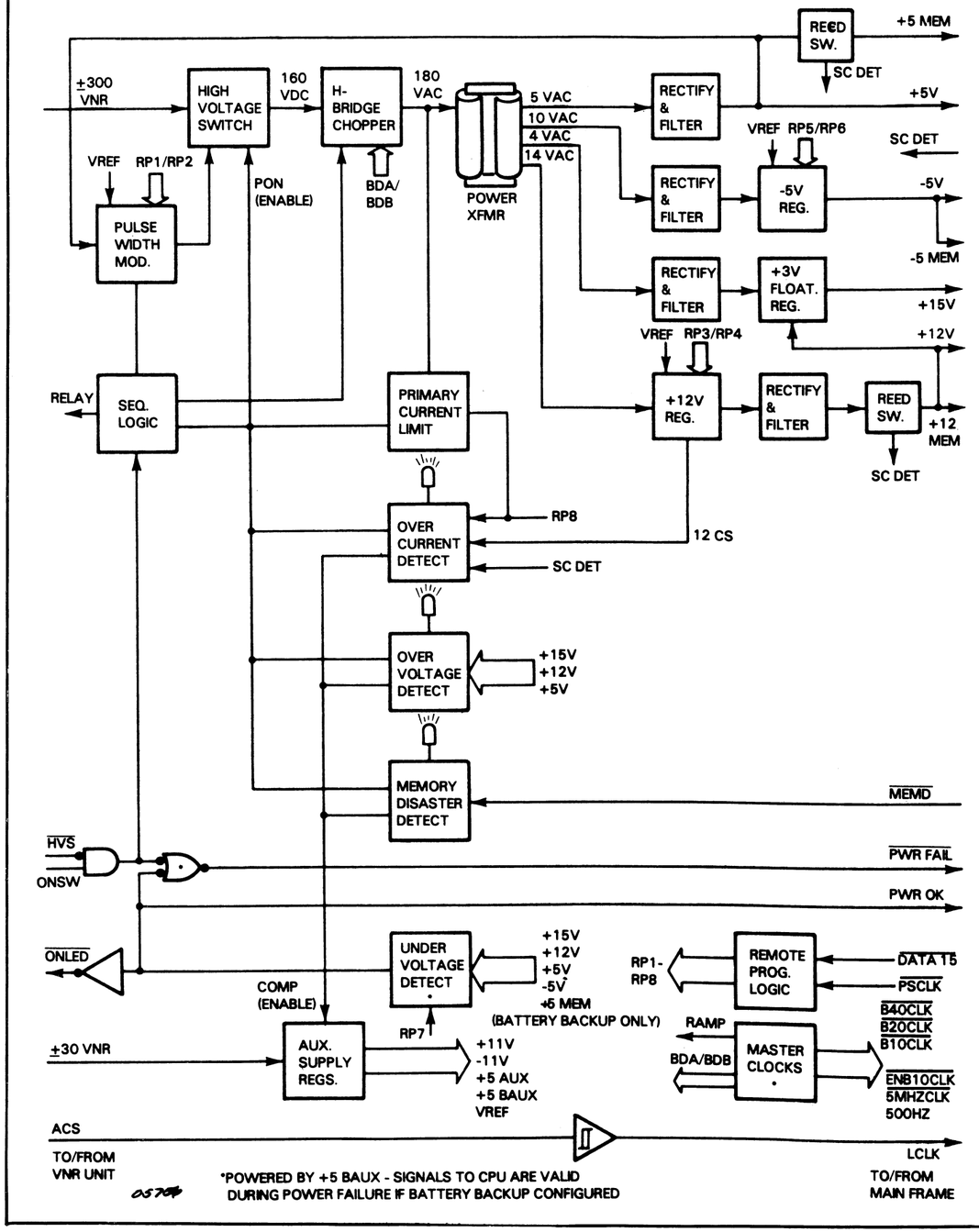


Figure 9.3 Power Supply Block Diagram

The over-current detector monitors signals from several sources:

- The 12CS signal indicates that the +12V regulator is overloaded.
- The SC DET signal indicates that there is a short circuit on one of the supply outputs (except -5V or -5 MEM-P). (Short circuits on +5V are detected on the backpanel.)
- The primary current limiter monitors the total current flow into all the loads. If an over-current condition occurs, the limiter immediately drives the PON signal to the low state and disables the buck regulator for the remainder of the 40 KHz clock cycle (the regulator turns on again at the start of the next cycle). This effectively reduces the duty cycle of the pulse width modulator, and so limits the amount of power delivered. (The supply actually goes into full current limiting when you first turn it on in order to charge the output filter capacitors). If the supply stays in current limiting too long, the limiter circuits drive the RP8 signal to the high state.

Table 9.1 16-slot chassis power supply specifications without battery backup

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+5.10V	+5.20V	7.5A	100A
+12V	+11.8V	+12.2V	0	12.5A *
+15V	+14.5V	+15.5V	0	1.5A *
-5V	-4.9V	-5.1V	0	3A
-11V	-11.0V	-12.5V	0	0.02A
+5 MEM	+5.10V	+5.20V	0	4.5A *
+12 MEM	+11.8V	+12.2V	0	6A *
-5 MEM	-4.9	-5.1 V	0	0.3A *

* The sum of the currents on +12V, +15, and +12 MEM must NOT exceed 12.5 Amps.

When an over-current fault occurs, the over-current light turns on and the detector drives the PON and COMP signals to the low state. This shuts down the entire supply. The detector re-enables the supply two seconds later. If the overload is still present, the detector shuts the supply down again. This process can continue for five more cycles. If the overload is still present, the supply shuts down for good.

The over-voltage detectors monitor the +15V, +12V and +5V outputs. If any of these outputs exceed a preset voltage level, the over-voltage light turns on and the detector shuts down the supply. (The -5V regulator has a built-in over-voltage protector. If a fault occurs, the protector clamps the -5V bus to less than -8 volts.)

The memory disaster detector monitors the MEMD signal from the main memory on the CPU board. If main memory loses -5 MEM, a critical memory voltage, the memory disaster light comes on and the detector shuts down the supply.

The under-voltage detector monitors all of the output voltages. If any output falls below a preset level, the detector drives the Power OK signal to the low state, turns off the power-on light and flags a power failure. A power failure is also flagged when the power switch is turned off or if the 300 VNR supply fails.

Battery Backup

The battery backup option supports the memory voltages when a power failure occurs. It also powers the system clocks and the power status indicators and provides a Memory OK status flag to indicate that the memory voltages are okay. Figure 9.4 shows the parts of the battery backup option that are added to the power supply board.

The battery backup option generates three voltages: +12 MEM, +5 MEM-P, and -5 MEM-P (note that the main supply regulators support these voltages when battery backup is not configured). It draws power from one of two sources. During normal operation, power comes from the +12V main supply output. If a failure occurs, power then comes from the battery. The backup option includes three voltage regulators along with some control circuits. To see how these circuits work, let us examine each voltage regulator and then follow a power failure sequence.

The +12V regulator draws power directly from the battery. It is a simple linear series pass design and has no built-in protection circuits.

The +5V regulator draws power from either the +12V main supply or from the battery. It is a buck switching regulator and is very similar to the one in the main supply. When the low voltage switch turns on, current flows from the source, through the primary winding of the flyback transformer and on to the output. The pulse width modulator controls the duty cycle of the switch to regulate the output voltage. If too much current flows in the primary winding, the current limiter reduces the modulator's duty cycle.

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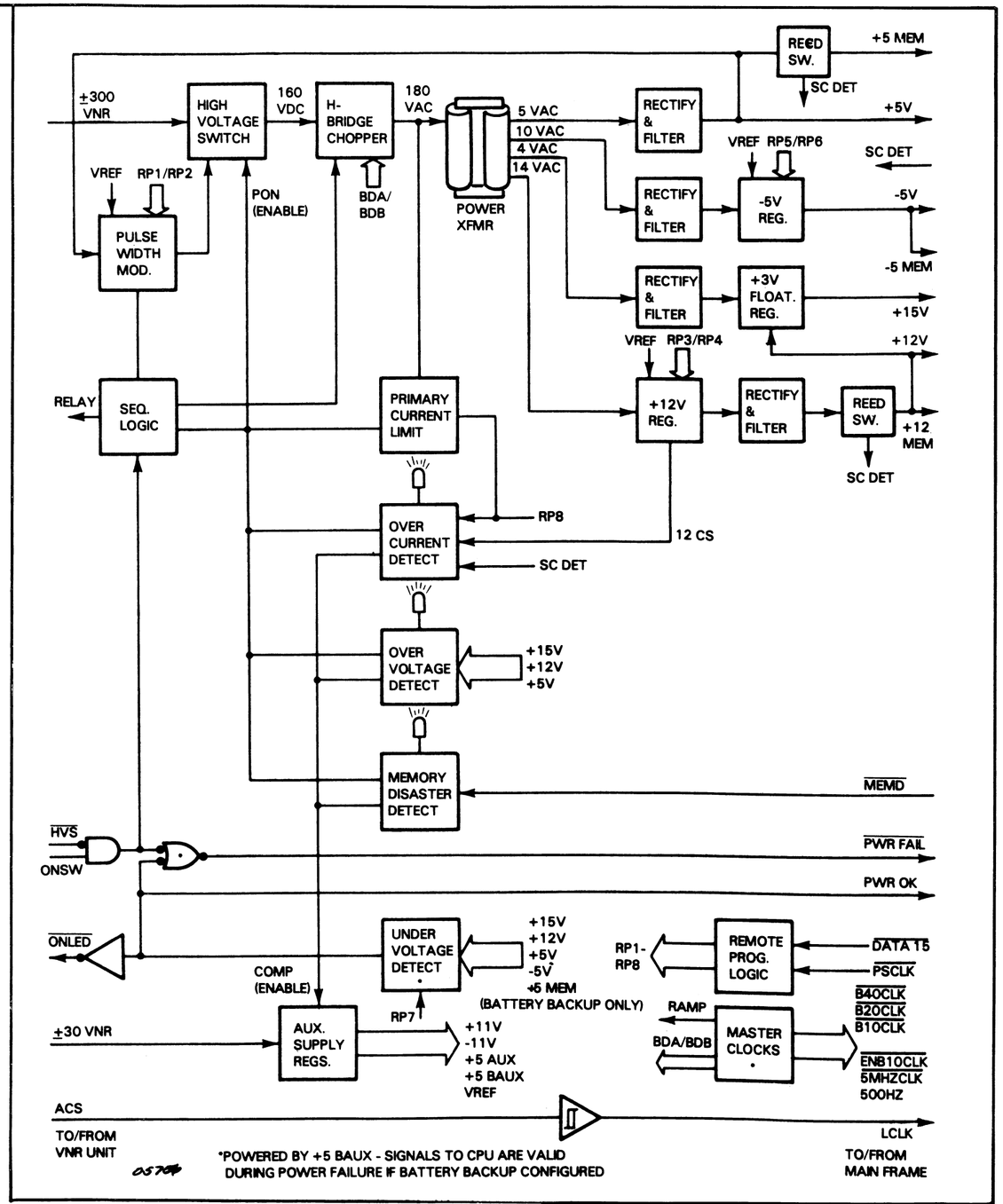

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- The 12CS signal indicates that the +12V regulator is overloaded.
- The SC DET signal indicates that there is a short circuit on one of the supply outputs (except -5V or -5 MEM-P). (Short circuits on +5V are detected on the backpanel.)
- The primary current limiter monitors the total current flow into all the loads. If an over-current condition occurs, the limiter immediately drives the PON signal to the low state and disables the buck regulator for the remainder of the 40 KHz clock cycle (the regulator turns on again at the start of the next cycle). This effectively reduces the duty cycle of the pulse width modulator, and so limits the amount of power delivered. (The supply actually goes into full current limiting when you first turn it on in order to charge the output filter capacitors). If the supply stays in current limiting too long, the limiter circuits drive the RP8 signal to the high state.

Table 9.1 16-slot chassis power supply specifications without battery backup

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+5.10V	+5.20V	7.5A	100A
+12V	+11.8V	+12.2V	0	12.5A *
+15V	+14.5V	+15.5V	0	1.5A *
-5V	-4.9V	-5.1V	0	3A
-11V	-11.0V	-12.5V	0	0.02A
+5 MEM	+5.10V	+5.20V	0	4.5A *
+12 MEM	+11.8V	+12.2V	0	6A *
-5 MEM	-4.9	-5.1 V	0	0.3A *

* The sum of the currents on +12V, +15, and +12 MEM must NOT exceed 12.5 Amps.

When an over-current fault occurs, the over-current light turns on and the detector drives the PON and COMP signals to the low state. This shuts down the entire supply. The detector re-enables the supply two seconds later. If the overload is still present, the detector shuts the supply down again. This process can continue for five more cycles. If the overload is still present, the supply shuts down for good.

The over-voltage detectors monitor the +15V, +12V and +5V outputs. If any of these outputs exceed a preset voltage level, the over-voltage light turns on and the detector shuts down the supply. (The -5V regulator has a built-in over-voltage protector. If a fault occurs, the protector clamps the -5V bus to less than -8 volts.)

The memory disaster detector monitors the MEMD signal from the main memory on the CPU board. If main memory loses -5 MEM, a critical memory voltage, the memory disaster light comes on and the detector shuts down the supply.

The under-voltage detector monitors all of the output voltages. If any output falls below a preset level, the detector drives the Power OK signal to the low state, turns off the power-on light and flags a power failure. A power failure is also flagged when the power switch is turned off or if the 300 VNR supply fails.

Battery Backup

The battery backup option supports the memory voltages when a power failure occurs. It also powers the system clocks and the power status indicators and provides a Memory OK status flag to indicate that the memory voltages are okay. Figure 9.4 shows the parts of the battery backup option that are added to the power supply board.

The battery backup option generates three voltages: +12 MEM, +5 MEM-P, and -5 MEM-P (note that the main supply regulators support these voltages when battery backup is not configured). It draws power from one of two sources. During normal operation, power comes from the +12V main supply output. If a failure occurs, power then comes from the battery. The backup option includes three voltage regulators along with some control circuits. To see how these circuits work, let us examine each voltage regulator and then follow a power failure sequence.

The +12V regulator draws power directly from the battery. It is a simple linear series pass design and has no built-in protection circuits.

The +5V regulator draws power from either the +12V main supply or from the battery. It is a buck switching regulator and is very similar to the one in the main supply. When the low voltage switch turns on, current flows from the source, through the primary winding of the flyback transformer and on to the output. The pulse width modulator controls the duty cycle of the switch to regulate the output voltage. If too much current flows in the primary winding, the current limiter reduces the modulator's duty cycle.

RELATED DOCUMENTATION

A list of documentation for NOVA 4/C computers appears in Table 1.3.

Table 1.3 Documentation summary

Affected Assemblies	DGC No.	Description
NOVA 4/C	014-000617	NOVA 4 Programmer's Reference Manual
	015-000031	Interface Designer's Reference, NOVA and ECLIPSE Line Computers
	015-000056	Diagnostic Operating System Technical Manual
	015-000082	DTOS Summary
16-Slot NOVA 4/C	010-000213	Installation Data Sheets, NOVA 4 16-Slot
5-Slot NOVA 4/C	010-000212	Installation Data Sheets, NOVA 4 5-Slot
CPU Board	001-001600	CPU schematic
	016-000857	CPU with 32K byte memory illustrated parts
	016-000864	CPU with 16K byte or 64K byte memory illustrated parts
Power Supply PCB 16-slot	001-001524	Power Supply schematic
	016-000688	Power Supply illustrated parts (including battery backup)
VNR Unit 16-slot	001-001523	Power Supply VNR Card schematic
	016-000670	Power Supply VNR Card illustrated parts
Power Supply PCB 5-slot	001-001616	Power Supply schematic
	016-000861	Power Supply illustrated parts
Backpanel 16-slot	001-001563	Backpanel schematic
	016-000675	Backpanel illustrated parts
Backpanel 5-slot	001-001619	Backpanel schematic
	016-000696	Backpanel illustrated parts
Front Console PCB	001-001585	Front Panel schematic
	016-000661	Front Panel illustrated parts
Internal Cable 16-slot	001-001607	16-slot system wiring diagram
Internal Cable 5-slot	001-001637	5-slot system wiring diagram
I/O Paddleboards		
005-012472	008-003294	Wire list (General Purpose I/O)
005-012751	008-002599	Wire list (External I/O bus)
005-012765	008-002570	Wire list (for ULM models 4241, 4241A, 4242, 4243)
005-012476	008-003287	Wire list (Model 8315 Bus Repeater)
005-012590	008-003301	Wire list (DCU 50, models 4250, 4254)
005-012473	008-003288	Wire list (asynchronous interfaces, models 4007, 4010, 4023, 4075, 4077, 4078)
005-012585	008-003300	Wire list (MCA, model 4206)

DG-03380

CHAPTER 2
HOW TO USE THE CONSOLES

The NOVA 4 conputers contain two consoles: a front console and a virtual console. These are described below.

FRONT CONSOLE

The front console is located on the upper-left corner of the front panel. It consists of the following three switches and three lights:

Switches

POWER - Powers up and powers down the system.

PL/LOAD-RESET - When pressed to the PL/LOAD position, the CPU performs a program load from the device whose device code is jumpered on the CPU board. (See installation data sheets or "CPU Board Replacement," Part IV, for jumpering information.)

When pushed to the RESET position, the CPU performs a system reset and enters virtual console mode, described below.

LOCK - When in the LOCK position, the other two switches, described above, are disabled. Additionally, auto restart is enabled after a power failure when the battery backup is present, while access to the virtual console by a BREAK character from the system terminal is disabled.

In a 16-slot system, if this switch is in the LOCK position, the system cannot be powered down (i.e., the power switch is disabled). In a 5-slot system, if this switch is in the LOCK position and the power switch is placed in the OFF position, the system will go into battery backup mode if that option is present. If the 5-slot system does not contain the batery backup option, the system will be powered down.

Lights

PWR - When lit, indicates that the system is powered up and the voltages are within operation specifications. When the PL/LOAD-RESET switch is in the RESET position, this light goes out.

BATT - When lit, indicates that the system is running on battery backup power. This is usually a result of a power failure.

RUN - When lit, indicates that the system is in run mode and or the PL/LOAD-RESET switch is in the RESET position. This light goes out when the system is in virtual console mode.

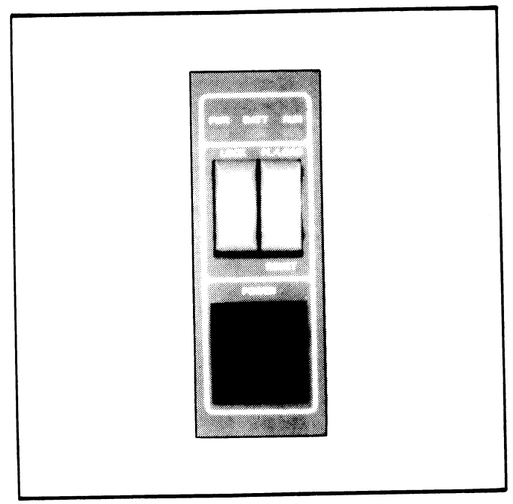


Figure 2.1 Front Console

VIRTUAL CONSOLE

The virtual console (VC) allows you to interact with the computer through the system terminal which is connected to the CPU's on-board asychronous interface. Simple commands which you enter on the terminal's keyboard allow you to: examine and/or modify processor registers or memory locations; start, stop, and continue program execution; and, initiate a program load from a selected device.

On power up, the computer performs a self-test. After a sucessful completion of the self-test, the following information is typed on the terminal:

```
OK
!000000
!
```

"OK" followed by "!" indicates that the self-test ran sucessfully. This, in turn is followed by the contents of the program counter, which are all zeroes on power-up. The next "!" is the VC prompt; it tells you that VC is ready and at your service.

In addition to power-up, VC is entered when:

- A HALT instruction is executed,
- The RESET switch on the front console is pressed and the front console is unlocked, or
- The BREAK key on the system terminal is pressed and the front console is unlocked.

Under any of these conditions, a "!" and the incremented contents of the program counter are typed when the VC is entered. These are followed by the "!" VC prompt. For example, if the program is about to execute an instruction at location 2077 when the VC is entered, the following is typed:

```
002077
!
```

Cells

The VC operates on 'cells'. A cell is either a memory location (memory cell) or an internal register (internal cell) such as an accummulator. Each internal register that is accessible by the VC is assigned an internal cell number. The cell numbers are listed in Table 2.1.

In order to examine or modify any cell, you must 'open' it. Opening a cell causes its contents to be printed, in octal, on the terminal. To open a cell, use one of the commands listed in Table 2.2. The VC will respond only to octal numbers and upper case letters. In the table, 'current cell' means the last cell that you opened.

When you open a memory cell, VC interprets the address as a 15-bit physical address. You do not have to type leading zeroes. All you have to type is the physical address in octal representation. For example, if you want to open location 5, type 5/. If you want to examine the top location of a system which contains 64K bytes of memory, type 77777/.

Once you have opened a cell, you may change its contents by simply typing the octal number whose value is to be placed in the cell. Terminate the expression with a Carriage Return, Line Feed, or New Line. Note that if you type Carriage Return, the next cell will also be opened. This is convenient when you need to enter data into several consecutive locations.

Table 2.1 Internal Cells

Internal Cell No.	Internal Register
0-3	The contents of the accumulators AC0 through AC3, respectively.
4	Return address (the contents of the program counter when the VC was entered).
5	Stack pointer
6	Frame pointer
7	Interrupt enable flag status bit: 0 = interrupts off 1 = interrupts on
11	Data switch register: Replaces the conventional console data switches. When the system is in RUN mode (i.e., not in VC mode), and a READS instruction is executed, the 16-bit contents of this register are read by the CPU.
12	value of the carry bit

Table 2.2 Cell commands

Command	Function
nA	Open the internal cell whose internal cell number is equal to "n." (See Table 2.1.)
n/	Open the memory location whose address is equal to the octal number "n."
(carriage return)	Close the current cell and open the next consecutive cell.
(line feed or new line)	Close the current cell but do not open another.
/	Close the current cell and open the memory cell whose address is equal to the contents of the current memory or internal cell.

Table 2.3 Function commands

Command	Function
P	Starts program execution at the memory location specified by the contents of internal cell number 4. (See Table 2.1.)
nR	Issues an I/O Reset and starts program execution at the memory location specified by the octal number "n."
I	Issues an I/O Reset.
nL	Performs a program load from the device whose device code is equal to "n." Bit 0 of "n" is a 0 for a low-speed device and a 1 for a high-speed device.
F	Performs a DG field service cassette bootstrap load. (For DGC use only.)
K	Cancels the entire line just typed, and prints a question mark (?).

Function Commands

Table 2.3 lists the VC function commands. All commands must be typed in octal numbers and upper case letters.

The VC has two commands to start program execution. Typing "P" starts program execution at the location specified by internal cell number 4 (the return address). You can also start program execution by typing "nR." In this case, the CPU issues an I/O Reset command and starts program execution at the location specified by the octal number "n."

Typing "I" causes the CPU to issue an I/O Reset command.

You can program load from an I/O device by typing "nL" where "n" is the device code, in octal, of the I/O device to be used. Bit 0 of "n" should be 1 if the I/O device is high-speed, and 0 if the I/O device is low-speed. For example, if the program load device is a high-speed 6060 disc drive whose device code is 27, you would type the following:

```
100027L
```

You can perform a Data General field service cassette bootstrap by typing "F."

Virtual Console Errors

If you type a character that the VC does not recognize, it will print a "?" followed by a New Line. If you wish to cancel an entire line you just entered, type a "K." In this case, VC will respond with a "?" followed by a New Line.

If you attempt to open a non-existent memory cell, the 16-bit contents of the cell printed on the terminal are meaningless. If you attempt to open an internal cell with a cell number greater than 13, VC will respond with a "?."

CHAPTER 3
INTRODUCTION TO TROUBLESHOOTING

Part II of this manual contains troubleshooting procedures intended for use during:

- Initial checkout of a new installation or addition to an existing system
- Repair of an existing system

While these situations are different, many of the procedures required to perform both initial checkout and repair are the same, as shown in the troubleshooting flowchart, Figure 3.1. This flowchart leads you through a logical sequence of fault isolation, referencing Chapters 4 through 8. These chapters contain step-by-step procedures for detecting faulty assemblies and checking the reliability of the system. (Actual replacement procedures are outlined in Part IV.)

PRE-SITE INFORMATION

Before going to the customer's site, check the list below and learn the customer's configuration, if possible. This will help to ensure that you have the appropriate field replaceable units (FRUs) with you on arrival.

- Chassis: 16 or 5-slot
- Main memory size
- CPU options
- Battery backup option
- Terminal used as system console
- Other peripherals

Also if you are going to repair a failing unit, try to get information from the customer that may give you a clue to the failing FRU.

CONFIGURATION CHART

Each system is shipped with a configuration chart which should reflect its configuration. Attach the chart to the rear door (outside) of the cabinet. Whenever you or anyone else reconfigures or retailors the system, update the chart to reflect the changes.

INITIAL CHECKOUT

If you are performing an initial checkout of a new installation, start with Chapter 4 and follow the steps outlined in the troubleshooting flowchart.

REPAIR

If you are servicing a failing system, the type of failure determines the procedures you will use to troubleshoot it. Thus, it is important to ask the customer the following questions:

1. Was the computer operating properly before the failure?
2. Is the failure a hard or intermittent one?
3. Did the operating system generate any panic codes?
4. Can the computer successfully complete the self-test?
5. Was the failure detected by reliability and/or diagnostic testing?
6. Was the failure detected while running user programs?

With the answers to these questions, you are now ready to follow the steps indicated in the troubleshooting flowchart.

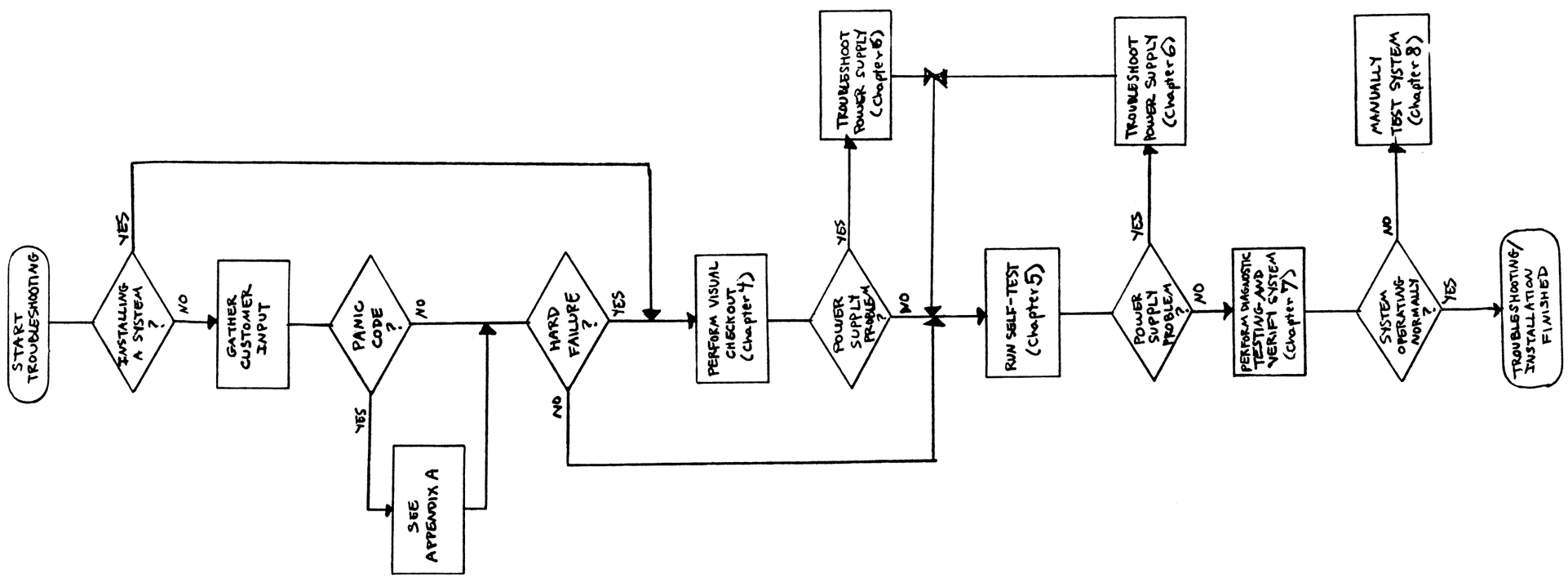


Figure 3.1 Troubleshooting Flowchart

CHAPTER 4
VISUAL CHECKOUT

You should perform the visual checkout whenever you initially check out a system (or addition to a system) or repair an existing system.

WARNING: The VNR unit (16-slot only) and the slide-in power supply board (both chassis) carry dangerously high voltages. Turn the power off before removing any unit.

Visually checkout the system using the following procedure. Try to correct any simple problems you find.

1. Turn power off.

2. Check the configuration chart on the rear door (outside) of the cabinet to find out what the system contains and how it is tailored.

3. Open the rear cabinet door and unplug the ac line cord from the cabinet.

4. If you are repairing a system, check the ac line fuses and replace them if they are blown. The 16-slot power supply has two 15 Amp line fuses which screw into the rear of the VNR unit (see Figure 4.1). The 5-slot power supply has one 7 AMP line fuse which screws into the rear of the power supply board and extends through a cutout in the backpanel (see Figure 4.2).

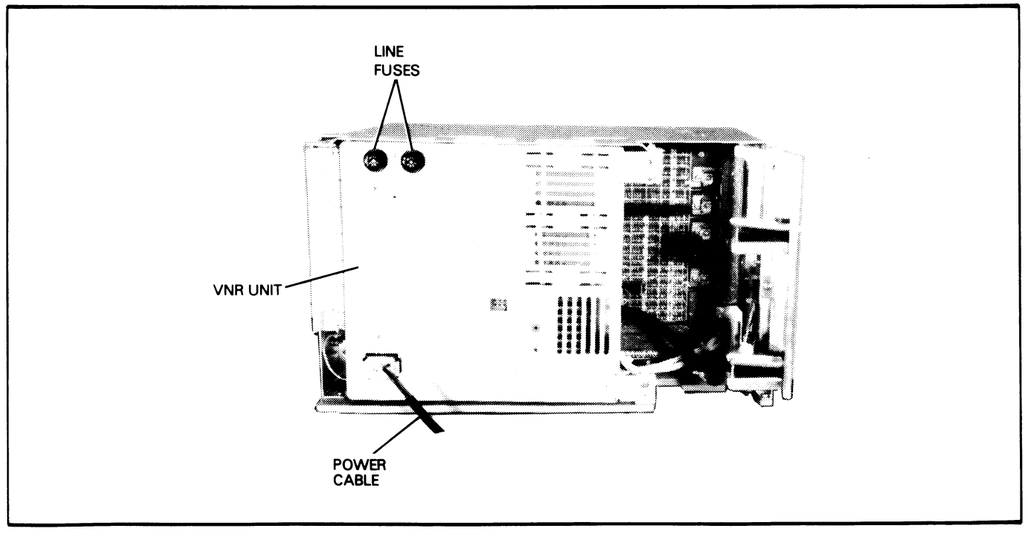


Figure 4.1 Line Fuses

5. On a 16-slot chassis:

   a. Swing the VNR unit away from the backpanel (see "VNR Unit Replacement," Part IV).

   b. Check for bent pins which cause shorts. Straighten any bent pins.

   c. Make sure the diagnostic test plug is inserted with the "RUN" label up (see Figure 4.3). If it is not, remove the plug, turn it over, and reinsert it with the "RUN" side up.

   d. Make sure none of the connectors to the backpanel or to the paddleboards are hanging loose.

   e. If you are repairing a system which you suspect has had an I/O problem since installation:

      - Make sure the priority jumpers are inserted as described in the installation data sheets.

      - Make sure the correct paddleboards are used and connected to the proper backpanel slots (see installation data sheets).

   f. Reposition the VNR unit (see "VNR Unit Replacement," Part IV).

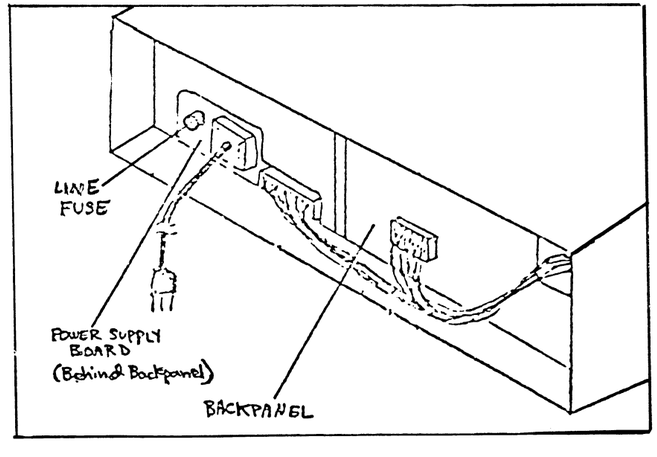


Figure 4.2 Line Fuses

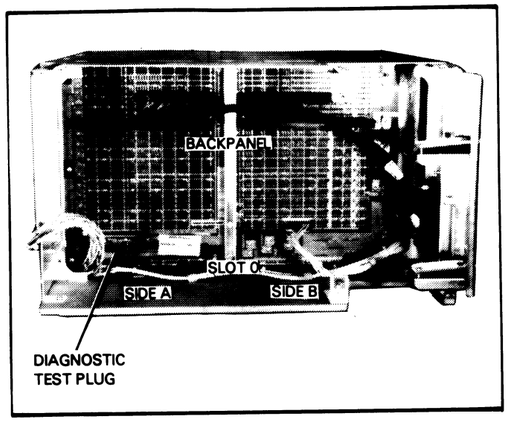


Figure 4.3 Diagnostic Test Plug

6. On a 5-slot chassis:

   a. Check for bent pins which cause shorts. Straighten any bent pins.

   b. Make sure none of the connectors to the backpanel or to the paddleboards are hanging loose.

   c. If you are repairing a system which you suspect has had an I/O problem since installation:

      - Make sure the priority jumpers are inserted as described in the installation data sheets.
      - Make sure the correct paddleboards are used and connected to the proper backpanel slots (see installation data sheets).

7. Plug the ac line cord back into cabinet and close the rear cabinet door.

8. Remove the front panel (see "Front Panel Replacement," Part IV).

9. If you are installing a system or repairing a system which has never operated normally:

   a. Remove each printed circuit board, except the power supply board, and make sure it is tailored properly (see "CPU Board Replacement," Part IV, or the appropriate I/O device documentation).

   b. If necessary, update the configuration chart on the rear (outside) of the cabinet door to reflect the proper tailoring.

10. Check the fans as follows:

    a. If you are servicing a 16-slot chassis with boards in slots 6 and 15, remove them. If you are servicing a 5-slot chassis with a board in slot 4, remove it.

    b. Turn the power on.

    c. Look through the open slots on the left side of the chassis and see if all the fans are running. You may need to use a flashlight. If all the fans are running, continue the visual checkout; otherwise, proceed as follows:

       - If some, but not all, of the fans are running, replace the faulty fans and make sure the cable connectors to the fans and the console PCB assembly are seated securely.
       - If none of the fans are running, go to Chapter 6, "Troubleshooting the Power Supplies."
       - After correcting the problem, continue the visual checkout.

    d. Turn the power off and reinsert any boards you removed.

11. Replace the front panel (see "Front Panel Replacement," Part IV).

12. Turn the power on and check the Power-On light on the front console. If the power light is on, you can assume that the voltages are within operating margins. In this case, go to Chapter 5, "Computer Self-Test"; otherwise, go to Chapter 6, "Troubleshooting the Power Supplies." After correcting the power supply problem, go to Chapter 5.

CHAPTER 5
COMPUTER SELF-TEST

Whenever the computer is powered up with the Lock switch off, the CPU automatically runs a 4-second self-test to ensure that the computer can load and run diagnostic programs. (The CPU also runs this test after a power failure when battery backup is not present.) The self-test consists of several ROM-resident diagnostic tests which check the operation of the power supply, the system terminal, the basic CPU functions, and main memory. As the CPU completes portions of the self-test it prints (displays) part of the following message on the system terminal:

```
OK
!000000
!
```

The last exclamation point (!) is the VC prompt.

If the entire message is printed, all the diagnostic tests have run and the self-test is successfully completed. If only part of the message is printed, the self-test found a bad unit. The indicator lights on the front console together with the printed part of the message indicates the probable faulty unit as shown in the Table 5.1.

Table 5.1 Fault indicators

Power light	Run light	Message printed on system console	Fault indicated
Off	On or Off		Power supply
On	Off		CPU/System terminal
On	Off	0	Main memory (first 32KB) *
On	Off	OK	Main memory (second 32KB) *

* In a 32K byte (16K word) system, this fault indicates a fault somewhere in the entire 32K byte memory.

TROUBLESHOOTING WITH THE SELF-TEST

Check out the computer with the self-test as follows:

1. Switch the power on.

2. If the self-test is completed (the entire message is printed out) and any problems found during the visual check are corrected, go to Chapter 7, "Diagnostic Testing."

3. If the self-test is not successfully completed, follow the procedure given below for the fault indicated. Turn off the power before removing or installing any board. If you replace a board and the self-test still indicates the same fault, replace the original board before continuing, unless otherwise indicated. Procedures for replacing FRUs are given in Part IV.

   NOTE: Each time you replace an FRU, repeat steps 1 through 3 until the self-test is successfully completed.

Power Supply Fault

Go to Chapter 6, "Troubleshooting the Power Supplies."

CPU/System Terminal Fault

1. Visually check out the terminal as follows:

   a. Make sure the connectors on the device cable for the system terminal are securely plugged into the backpanel and the terminal.

   b. Make sure that the terminal is connected to the ac line source, turned on, on-line, and in upper case mode. Also make sure that the correct interface type and baud rate are selected (see CPU tailoring of the appropriate installation data sheets.)

2. If you have any reason to think that the terminal is faulty, go to step 4a; otherwise, continue to step 3.

3. Check for a faulty CPU as follows:

   a. Replace the CPU board.

   b. If the self-test still indicates a CPU/system terminal fault, do the following:

      - Enter the virtual console (VC) by pressing the RESET switch on the front console.
      - Read the contents of accumulators AC0, AC1, and AC2 using the VC (see Chapter 2).
      - Replace the new CPU board with the original CPU board and repeat two previous steps.
      - If the contents of the accumulators are NOT identical in both cases, both CPU boards are probably faulty. Try another CPU board, if you have one.
      - If the contents of the accumulators are identical in both cases, remove all the printed circuit boards from the chassis except the power supply board and the CPU board. If the self-test still indicates a CPU/system terminal fault, replace the power supply board.

4. If the self-test still indicates a CPU/system terminal fault, check out the system terminal as follows:

   a. If you have NOT already replaced the CPU board, replace the CPU board. If the self-test still indicates a CPU/system terminal fault with the new CPU board, check the contents of the accumulators as described in step 3b, using both the new and original CPU boards. If the contents of the accumulators are identical for both boards, continue to step b below; otherwise, try another CPU board, if you have one.

   b. See if the system terminal works in local mode. If it does, replace the device cable; otherwise, troubleshoot the system terminal (see the documentation for the appropriate terminal).

   c. If the terminal uses an EIA interface and you have NOT already replaced the power supply board, replace the power supply board.

5. If you have already replaced the CPU and power supply boards in a 16-slot chassis, replace the bus terminators.

Main Memory Fault (First or Second 32KB)

1. Replace the CPU board.

2. If the self-test still indicates a memory fault with the new CPU board, check the contents of the accumulators as described in "CPU Fault," step 2, using both the new and original CPU boards. If the contents of the accumulators are identical for both boards, replace the power supply board; otherwise, try another CPU board, if you have one.

CHAPTER 6
TROUBLESHOOTING THE POWER SUPPLIES

This chapter will help you find the failing field replaceable units in the power supply and power distribution system. When you find a failing unit, replace it following the replacement procedure given in Part IV. For a detailed description of how the power supply operates, see Chapter 9 or 10.

OVERVIEW

Before you try to troubleshoot the power supply, it is helpful to know what the power supply does and how its indicator lights function.

Major Functions

The power supplies for both the 16-slot and the 5-slot chassis perform the following functions:

- Supply regulated dc operating voltages for the chassis
- Supply ac voltages for the fans
- Generate a time bases for the CPU and real-time clock
- Detect and respond to emergency conditions (power loss, excessive voltage or current, etc.)
- Provide power status indicators for the CPU (power fail, power ok, etc.)
- Provide emergency battery backup for the memory voltages (optional).

Indicator Lights

Two indicator lights on the front console of both chassis display the status of the power supply (see Figure 6.1).

Power-on Light - Indicates that the dc voltages are stable. If the power switch is on and the light is out, one of the following may have occurred:

- Ac power brownout or blackout
- Power supply failure
- Excessive load or short circuit on backpanel
- Diagnostic test plug not in "RUN" position (16-slot chassis only).

Battery Backup Light - Indicates that the battery is supplying the dc operating votages for the memories because either a power line failure, a power supply failure, or a shutdown (due to external shorts) occurred.

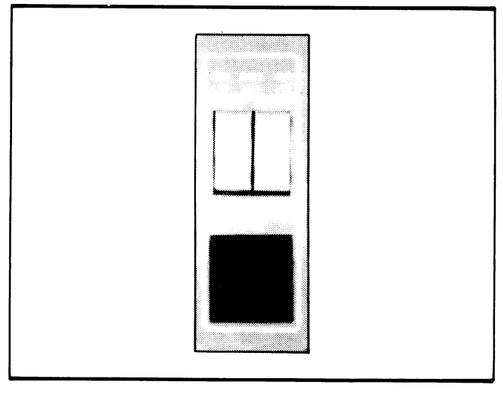


Figure 6.1 Front Console Indicator Lights

The 16-slot chassis has three additional indicator lights which give further status information. These lights are located on the front of the power supply board as shown in Figure 6.2.

Over-Current Light - Indicates that an over-current condition appeared in the supply or on the backpanel. The supply automatically tries to recover from an over-current condition. As a result, you may see this light blink up to 6 times before it finally stays on. Once it stays on you must power the supply down to clear the fault light (this probably will not correct the fault).

Over-Voltage Light - Indicates that an over-voltage condition appeared in the supply. You must power the supply down to clear the fault light (this probably will not correct the fault).

Memory Disaster Light - Indicates that the main memory detected a dc power failure on -5 MEM. You must power the supply down to clear the fault light (this probably will not correct the fault).

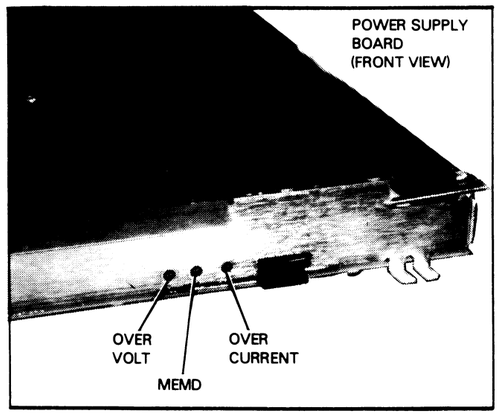


Figure 6.2 Power Supply Board Indicator Lights

Functional Description

16-Slot Power Supply

The power supply and distribution system for the 16-slot chassis consists of a VNR unit, a power supply printed circuit board, a fan module, and a backpanel circuit board. These four modules are interconnected by an internal cable (wiring harness) and by etch on the backpanel, as shown in Figure 6.3.

The VNR unit converts power from the ac line to unregulated dc voltages for the power supply board. It also routes ac power to the fans in the fan module. In a system with battery backup, the VNR unit contains a battery charger along with a small battery that supplies power for the battery backup circuits on the power supply board. A plug on the back of the unit lets you connect an external battery when longer backup times are required.

The power supply board is a printed circuit board which regulates the dc voltages from the VNR unit and in turn powers the chassis. It also provides clock and status signals for the CPU board. Fault detection circuits automatically shut down the power supply if an emergency condition occurs.

The backpanel routes power, control, and status signals between the power supply board and the printed circuit boards. It includes several reed switches that detect excessive current flow in the printed circuit boards. (These switches replace the fuses commonly found on other backpanels.)

5-Slot Power Supply

The power supply and distribution system for the 5-slot chassis consist of a power supply board, a fan module, a console PCB assembly, and a backpanel circuit board. These modules are interconnected by an internal cable (wiring harness) and by etch on the backpanel, as shown in Figure 6.4.

The power supply board converts the power from the ac line to regulated dc voltages and in turn powers the chassis. It also provides clock and status signals for the CPU and main memory. Fault detection circuits automatically shut down the supply if an emergency condition occurs. In a system with battery backup, the power supply board contains a battery charger along with a small battery that supplies power for the battery backup circuits.

The backpanel routes power, control, and status signals between the power supply circuit board and the printed circuit boards.

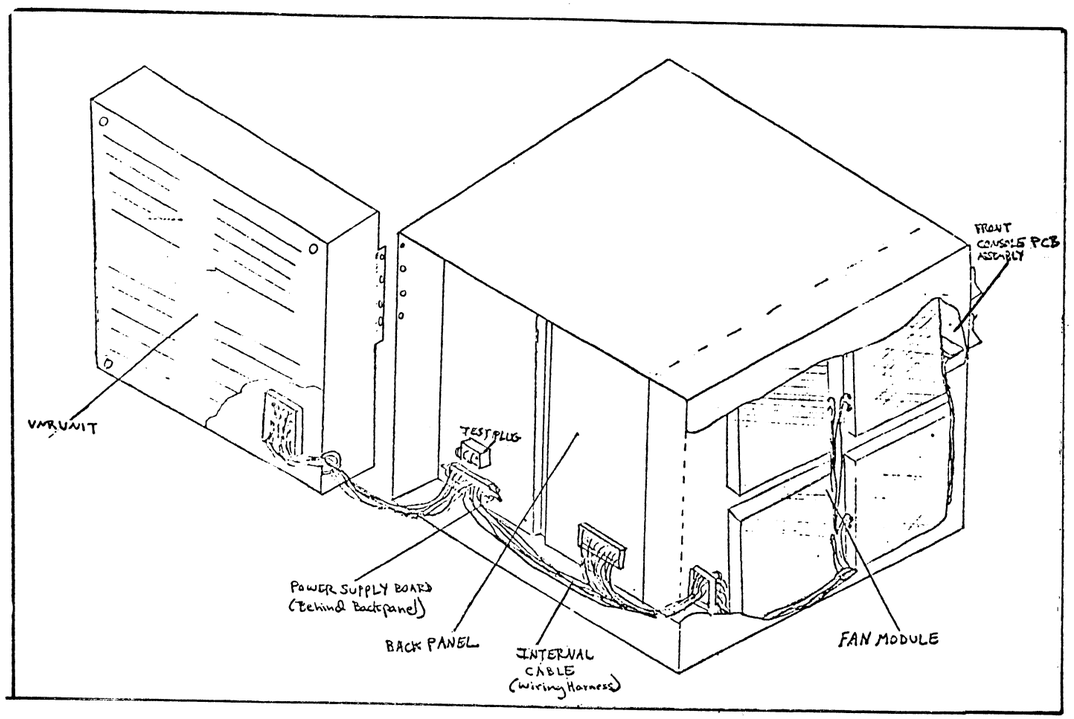


Figure 6.3 16-Slot Power Supply

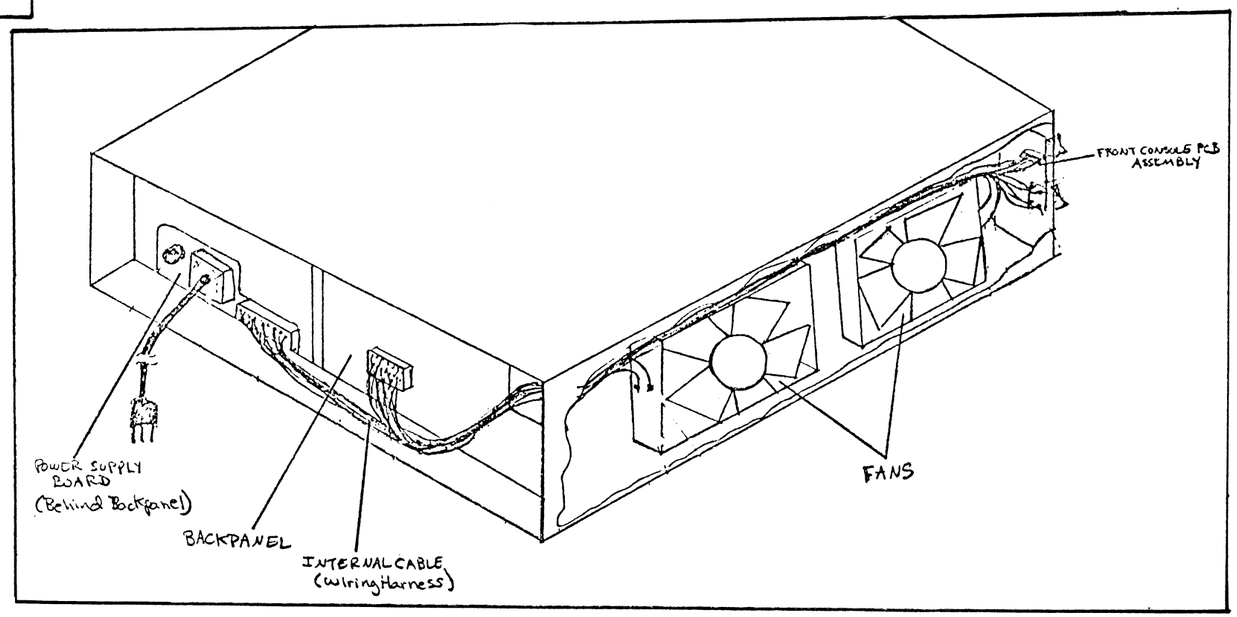


Figure 6.4 5-Slot Power Supply

TROUBLESHOOTING 16-SLOT POWER SUPPLY

WARNING: The VNR unit and power supply board generate dangerously high voltages. DO NOT ATTEMPT TO MEASURE VOLTAGES INSIDE THEM. Before you remove the cover on the VNR unit or the power supply board, WAIT AT LEAST 5 MINUTES AFTER POWERING DOWN THE SYSTEM to allow the high voltages to dissipate.

Turn off the power before removing or inserting any boards.

To troubleshoot the 16-slot power supply, carry out the following steps:

1. Initial checkout
2. Indicator light checkout
3. Voltage checkout
4. Final checkout
5. Battery backup checkout

Complete all steps in the order in which they are presented. (Step 5 is only for systems with battery backup.) Failure to do so may result in longer system down time and unnecessary assistance from DGC Field Service. Whenever you replace a unit, repeat the check that indicated a unit was faulty. If the check still indicates the unit is faulty, replace the original unit before continuing. Procedures for replacing FRUs are given in Part IV.

NOTE: The steps for troubleshooting the power supply assume the following conditions:

- The CPU board is in the chassis. (An unloaded power supply will not produce regulated outputs so do not troubleshoot the the power supply without at least the CPU board in the chassis.)
- The load on the power supply is balanced. (You may upset this balance if you remove or add boards while troubleshooting. See the installation data sheets, DGC No. 010-000213, for the load balancing rules.)
- All the electrical connections between units are good.
- The lock switch on the front console is in the UNLOCK position.

If you have any reason to think that these conditions are not met, check them before proceeding.

Initial Checkout

1. Turn power off and unplug the chassis ac line cord from the cabinet.
2. Make sure the cabinet is supplying the proper ac line voltage.
3. Plug the line cord back into the cabinet.
4. Swing the VNR unit away from backpanel (see "VNR Unit Replacement," Part IV).
5. Make sure the diagnostic test plug is inserted in the correct location with the "RUN" label up (see Figure 6.5).

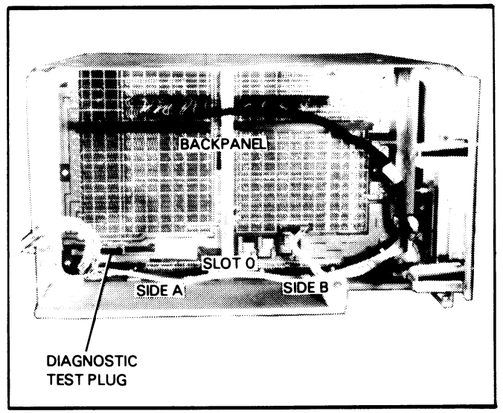


Figure 6.5 Diagnostic Test Plug

6. Swing the VNR unit back into position (see "VNR Unit Replacement," Part IV).
7. Remove the front panel (see "Front Panel Replacement," Part IV).
8. Turn the power on.
9. Look through any open slots on the left side of the chassis and see if all the fans are running. You may need to remove boards from slots 6 and 15 and use a flashlight to see the fans.
   a. If all four fans are running, reinsert any boards you removed, and go to "Indicator Light Checkout."
   b. If some, but not all, of the fans are running, replace the faulty fans and make sure the cable connectors to the fans and the console PCB assembly are seated securely. (See "Fan and Fan Module Replacement for 16-Slot Chassis," Part IV.)
   c. If none of the fans are running, continue checkout.

10. If you have not replaced a fan:

    a. Remove the fan module and make sure the cable connectors to the console PCB boards are seated securely (see "Fan Module Replacement for 16-Slot Chassis," Part IV).

    b. Reinstall the fan module.

11. Make sure the internal cable (wiring harness) connectors to the backpanel, the power supply board, and the VNR unit are seated securely (see "VNR Unit Replacement," Part IV).

12. Turn the power off.

13. Check the two 15 Amp ac line fuses which screw into the upper left rear corner of the VNR unit (see Figure 6.6).

    a. If the fuses are all right, replace the fan module.

    b. If the fuses are blown:

    - Replace them if you have NOT already replaced them; otherwise,
    - If the fans still do not run, replace the VNR unit.

14. If you cannot get the fans to run after carrying out steps 9 through 13, replace the internal cable (see "16-Slot Wiring Harness Replacement," Part IV).

15. If the fans still do not run after carrying out step 14, replace the fan module (see "Fan and Fan Module Replacement for 16-Slot Chassis," Part IV).

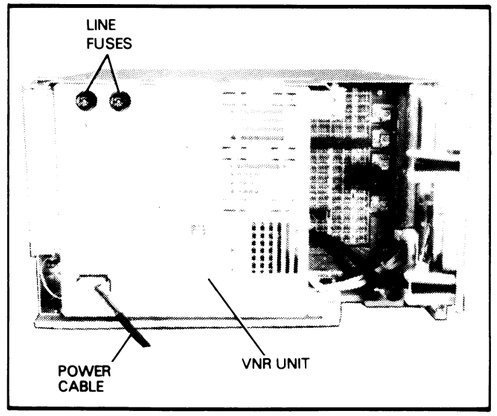


Figure 6.6 Line Fuses

Indicator Light Checkout

1. Turn the power on.

2. Check the indicator lights on the front end of the power supply board (see Figure 6.2). If they are all out, go to "Voltage Checkout"; otherwise, turn the power off and then on again. If any of the lights turn on again, follow the procedure below for the lights which are on. Whenever you replace a unit, repeat this step.

Memory Disaster Light

1. Turn the power off.

2. Check that the diagnostic test plug is in the correct location with the "RUN" label up (see Figure 6.5). If it is, continue to step 3; otherwise:

    a. Reposition the plug.

    b. Turn the power on.

    c. Check the memory disaster light. If it is on, continue to step 3.

3. Replace the power supply board. If the memory disaster light is still on, replace the CPU board.
4. If you have already done steps 1 through 3 and the memory disaster light is still on, replace the wiring harness.

Over-Current Light

1. Turn the power off.

2. Replace the power supply board.

3. Turn the power on.

4. Check the over-current light. If the light is on, turn the power off and remove any printed circuit board, other than the power supply board.

5. Turn the power on.

6. Check the over-current light.

   a. If the light is NOT on, replace the board being sure to insert the correct jumpers (see the appropriate I/O device documentation).

   b. If the light is on, reinsert the removed board, and repeat steps 4 through 6 with any other printed circuit board you have not already tried removing.

   c. If you have already done steps a and b and the over-current light is still on, check that the load on the power supply is balanced (see the installation data sheets, DGC No. 010-000213, for the load balancing rules).

7. If you have already done steps 1 through 6 and the over-current light is still on, replace the internal cable (wiring harness).

Over-Voltage Light

1. Turn the power off.
2. Replace the power supply board.
3. If the light is still on, replace the CPU board.
4. If you have already done steps 1 through 3 and the over voltage light is still on, replace the internal cable (wiring harness).

Voltage Checkout

1. Turn the power on.
2. Check the +5V voltage at test plug J1-15 (see Figure 6.8). If +5V is between 5.10V and 5.20V, go to "Final Checkout"; otherwise, continue the checkout.
3. Turn the power off.
4. Short MEMD at J35-21 to GND at J35-1 (see Figure 6.7). Before continuing the checkout, make sure you have shorted the correct pins.
5. Turn the power on and check the memory disaster light.

   a. If the light is NOT on, turn the power off, remove the short, and replace the VNR unit.

   b. If the light is on, turn the power off, remove the short, and then turn the power on.

      - Check the -11V voltage at J35-25 (see Figure 6.7).
      - If -11V is NOT between -11.0V and -12.5V (-30VNR not ok), check the VREF at test plug J1-14 (see figure 6.8). If VREF is 5.8V, replace the VNR unit; otherwise, replace the power supply board.
      - If -11V is between -11.0V and -12.5V (-30VNR ok), check the HVS voltage at test plug J1-4 (see Figure 6.8). If HVS is greater then 2.9V, replace the power supply board; otherwise, replace the VNR unit.

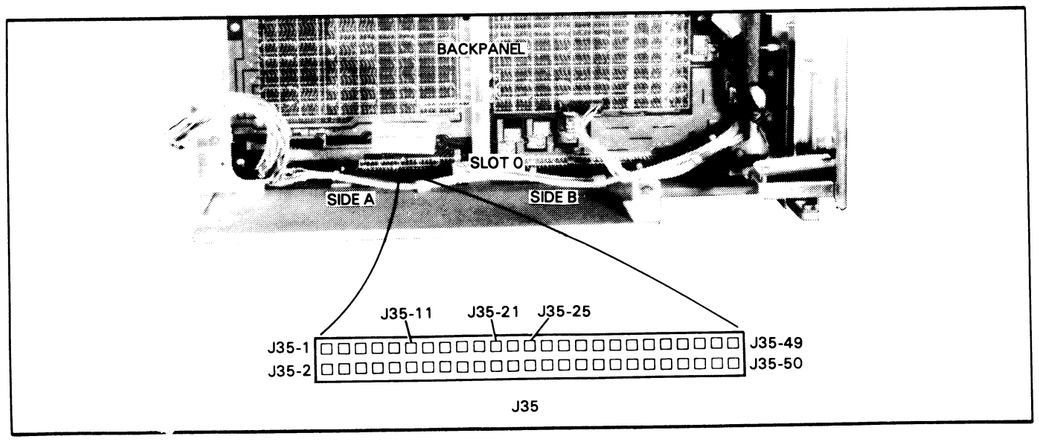


Figure 6.7 Jack 35

6. Recheck the +5V voltage at test plug J1-15 (see Figure 6.8). If it is between 5.10V and 5.20V, go to "Final Checkout"; otherwise, try replacing the internal cable (wiring harness). If this does not work, get help from DGC Field Service.

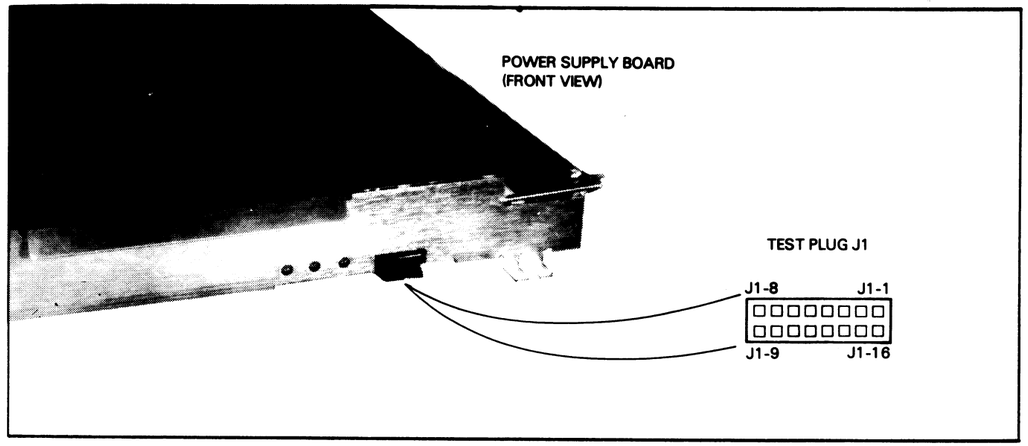


Figure 6.8 Test Plug

Final Checkout

1. Turn power on.
2. Check the power on light on the front console.
   a. If the light is on, continue to step 3 of this checkout.
   b. If the light is NOT on, check the $\overline{\text{ONLED-P}}$' voltage at J35-11 (see Figure 6.7).
      - If $\overline{\text{ONLED-P}}$' is 3V or GREATER, replace the power supply board; otherwise, replace the console PCB assembly.
      - If the light still is not on, replace the fan module, and if this does not correct the problem, replace the internal cable (wiring harness).
3. Turn the power off and see if the fans stop.
   a. If the fans stop:
      - Go to "Battery Backup Checkout" if the system has battery backup.
      - Go to Chapter 5, "Computer Self-Test," if the system does not have battery backup.
   b. If the fans do NOT stop:
      - Make sure the LOCK switch is in the UNLOCK position. If the fans still do not stop, check the $\overline{\text{PWR FAIL}}$' voltage at test plug J1-3 (see Figure 6.8).
      - If $\overline{\text{PWR FAIL}}$' is NOT less than 0.4V, replace the fan module.
      - If $\overline{\text{PWR FAIL}}$ is less than 0.4V, check PON at test plug J1-11 (see Figure 6.8). If PON is less than 0.4V, replace the VNR unit; otherwise, replace the power supply board.

Battery Backup Checkout

Only carry out this checkout if the system has battery backup. This procedure will not discharge the battery a significant amount. Note that it takes 16 hours for the battery to fully recharge.

1. Turn the power on and unplug the chassis ac line cord from the cabinet.

2. Check the +12 MEM voltage at location J35-3 (see Figure 6.7).

   a. If this voltage is GREATER THAN 11.0 volts and remains CONSTANT for MORE THAN 1 MINUTE, continue to step 3; otherwise,

   b. Check the BAT+ voltage at jack J3-1 (see Figure 6.9).

      - If BAT+ is greater than 12V, replace the power supply board.
      - If BAT+ is NOT greater than 12V, then measure the voltage DIFFERENCE between J3-5 and J3-6 (see Figure 6.9). If it is greater than one volt, replace the battery; otherwise, replace the VNR unit.

3. Check the battery backup light on the front console,

   a. If this light is on, plug the power cord into the ac source and then go to Chapter 5, "Computer Self-Test."

   b. If the light is NOT on, replace the power supply board, and if the light still does not turn on, replace the console PCB assembly.

4. Plug the ac line cord back into the cabinet.

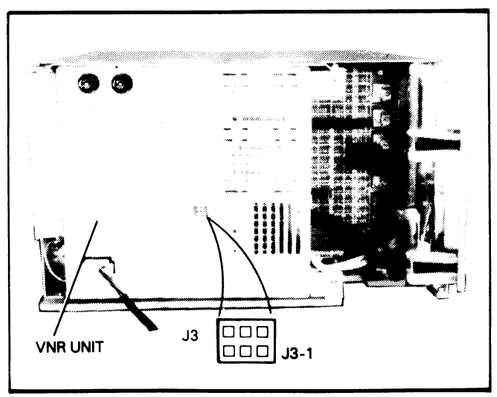


Figure 6.9 Jack 3

TROUBLESHOOTING 5-SLOT POWER SUPPLY

WARNING: The power supply board generates dangerously high voltages. DO NOT ATTEMPT TO MEASURE VOLTAGES INSIDE THEM. Before you remove the cover on the power supply board WAIT AT LEAST 5 MINUTES AFTER POWERING DOWN THE SYSTEM to allow the high voltages to dissipate.

Turn off the power before removing or installing any boards.

To troubleshoot the 5-slot power supply, carry out the following steps:

1. Initial checkout
2. Final checkout
3. Battery backup checkout

Complete all steps in the order in which they are presented. (Step 3 is only for systems with battery backup.) Failure to do so may result in a longer system down time and unnecessary assistance from DGC Field Service.

Whenever you replace a unit, repeat the check which indicated that unit was faulty. If the check still indicates the unit is faulty, replace the orginal unit before continuing. Procedures for replacing field replaceable units are given in Part IV.

IMPORTANT: The steps for troubleshooting the power supply assume the following conditions:

- The CPU board is in the chassis. (An unloaded power supply will not produce regulated outputs so do not troubleshoot the system without at least the CPU board in the chassis.)
- All the electrical connections between units are good.
- The lock switch on the front console is in the UNLOCK position.

If you have any reason to think that these conditions are not met, check them before proceeding.

Initial Checkout

1. Turn the power off and unplug the chassis ac line cord from cabinet.

2. Make sure the ac line source in the cabinet is supplying the proper ac line voltage.

3. Plug the line cord back into the cabinet.

4. Turn the power on.

5. Look through any open slot and see on the left side of the chassis if both fans are running. You may need to remove the board from slot 4 and use a flashlight to see the fans.

    a. If both fans are running, reinsert the board you removed, and go to "Final Checkout."

    b. If only one fan is running, replace the faulty fan and make sure the internal cable connectors to the fans and the console PCB assembly are seated securely.

    c. If neither fan is running, continue with this checkout.

6. If you have not replaced a fan, make sure the internal cable (wiring harness) connectors to the console PCB assembly are seated securely (see "16-Slot Internal Cable Replacement," Part IV).

7. Make sure the internal cable (wiring harness) connectors to the backpanel and the power supply board are seated securely.

8. Switch the power off.

9. Check the 7 Amp ac line fuse which screws into the left rear corner of the power supply board and extends through a cutout in the backpanel (see Figure 6.10).

    a. If the fuse is all right, replace the power supply board.

    b. If the fuse is blown:

        - Replace it if you have NOT already replaced it; otherwise,
        - Replace the power supply board.

10. If you cannot get the fans to run after carrying out steps 1 through 9, replace the internal cable (see "5-Slot Wiring Harness Replacement," Part IV).

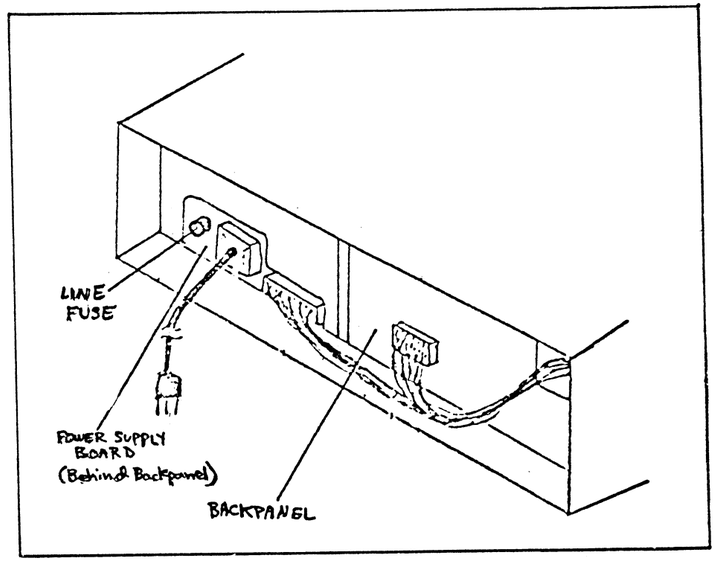


Figure 6.10 Line Fuse

Final Checkout

1. Turn power on.
2. Check the power on light on the front console.
   a. If the light is on, continue to step 3 of this checkout.
   b. If light is NOT on:
      - Replace the power supply board.
      - If the light still does not go on, reseat the internal cable (wiring harness) connectors to the the console PCB assembly. If this does not correct the problem, first replace the console PCB assembly, and then the internal cable.
3. Turn the power off and see if the fans stop.
   a. If the fans stop:
      - Go to "Battery Backup Checkout" if the system has battery backup.
      - Go to Chapter 5, "Computer Self-Test," if the system does not have battery backup.
   b. If the fans do NOT stop, replace the power supply board. If this does not correct the problem, first try reseating the internal cable (wiring harness) connectors, and then replace the internal cable.

Battery Backup Checkout

Only carry out this checkout if the system has battery backup. This procedure will not discharge the battery a significant amount. Note that it takes 24 hours to fully recharge the battery.

1. Turn the power on and unplug the chassis ac line cord from the cabinet.
2. Check the +12 MEM voltage at backpanel pin B47.
   a. If this voltage is GREATER than 11.3 volts and REMAINS CONSTANT FOR MORE THAN 5 MINUTES, go to step 3 of this checkout; otherwise, continue with step b.
   b. Most likely the battery is bad or the battery charger on the power supply board is not operating properly. If you have reason to suspect the battery is bad, replace it; otherwise, replace the power supply board. Note that an unused battery lasts about 3 1/2 years at 23 deg.C and its life expectancy decreases greatly with increases in operating temperature. A battery can be used for about 200 cycles.
3. Check the battery backup light on the front console,
   a. If this light is on, plug the line cord back into the cabinet and go to Chapter 5, "Computer Self-Test."
   b. If the light is NOT on, replace the power supply board, and if the light still does not turn on, replace the console PCB assembly.
4. Plug the ac line cord back into the cabinet.

CHAPTER 7
DIAGNOSTIC TESTING

Successful completion of the self-test indicates that the main portion of the NOVA 4/C computer is operating properly. This means that the reliability and diagnostic test programs described in the program summary table below can be loaded into main memory and used to:

- Detect faulty field replaceable units during troubleshooting
- Verify that the computer is operating properly during initial checkout or after repair.

The programs listed in Table 7.1 are available on either:

Magnetic tape or diskette (NOVA 4 DTOS)

Data General Field Service cassette

Loading procedures for DTOS (Diagnostic Operating System) appear in Appendix B. Procedures for using the field service cassette appear in Appendix C.

TROUBLESHOOTING FLOWCHART

The troubleshooting flowchart, Figure 7.1, leads you through sequences of reliability and diagnostic tests that will both isolate faulty field replaceable units and verify the proper operation of the NOVA 4/C computer. It assumes that the programs are loaded and run under the control of DTOS and specifies the DTOS commands to be used. If a DTOS loading device (i.e., magnetic tape unit or disc drive) is not present in the system or is inoperable, the flowchart can still be used by running the programs in the sequences indicated, using the field service cassette.

NOTE: Detailed information concerning DTOS and DTOS commands appears in Diagnostic Operating System Technical Manual, DG No. 015-000056, and DTOS Summary, DG No. 015-000082.

Throughout the flowchart, action recommendations following each program test are made solely on a pass/fail basis. To determine if a test passed, refer to the sample program run summary for that test at the end of this chapter. Each summary describes both the operator input and the program output, i.e., the information that will be printed (displayed) by the system terminal when the specified test passes.

Table 7.1 Reliability and diagnostic test program summary

Program Name	DTOS Mnemonic	Program Description
NOVA 3 Reliability Test Short	N3MORT S	This reliability program consists of a series of individual programs that test the interactive capabilities of the CPU; the CPU-resident real-time clock, asynchronous interface, and memory; and the I/O tester board.
NOVA 4 Logic Test	N4LGCTST	This program tests the logic used by the CPU to implement the instruction set. It also performs minimum level testing of the CPU I/O instructions, system terminal I/O, and the program interrupt facility.
NOVA 4 EXERCISER	N4EXER	This program exercises the CPU instruction set and tests the CPU's reliability.
NOVA 4/C Memory Diagnostic	N4CMD	This program consists of a series of tests that check main memory for faulty address decoding, memory accessibility, sense amplifier recovery, refresh sensitivity, interaction between memory elements, memory access time and memory cell reliability.
Basic Input/Output Test	BASICIOT	This program requires the presence of the multi-mode I/O tester board No. 005-004283. It tests the I/O instructions, the operation of the data channel and the real-time clock.
Real-Time Clock Test	RTC TST	This program tests the operation of the real-time clock.

When the flowchart specifies the replacement of a field replaceable unit (FRU), proceed as follows:

- Power down the system
- Replace the specified FRU (see Part IV for replacement procedures)
- Power up the system
- Reload DTOS
- Begin with the failing test and continue through the testing sequence.

Memory Diagnostic

The diagnostic testing sequences outlined in the first part of the troubleshooting flowchart are run in DTOS auto mode. If this testing fails to detect suspected, intermittent memory errors, more vigorous testing of memory can be accomplished by running the memory diagnostic test in DTOS manual mode. Operating procedures for running the memory diagnostic in both modes are outlined in the appropriate sample program run summaries.

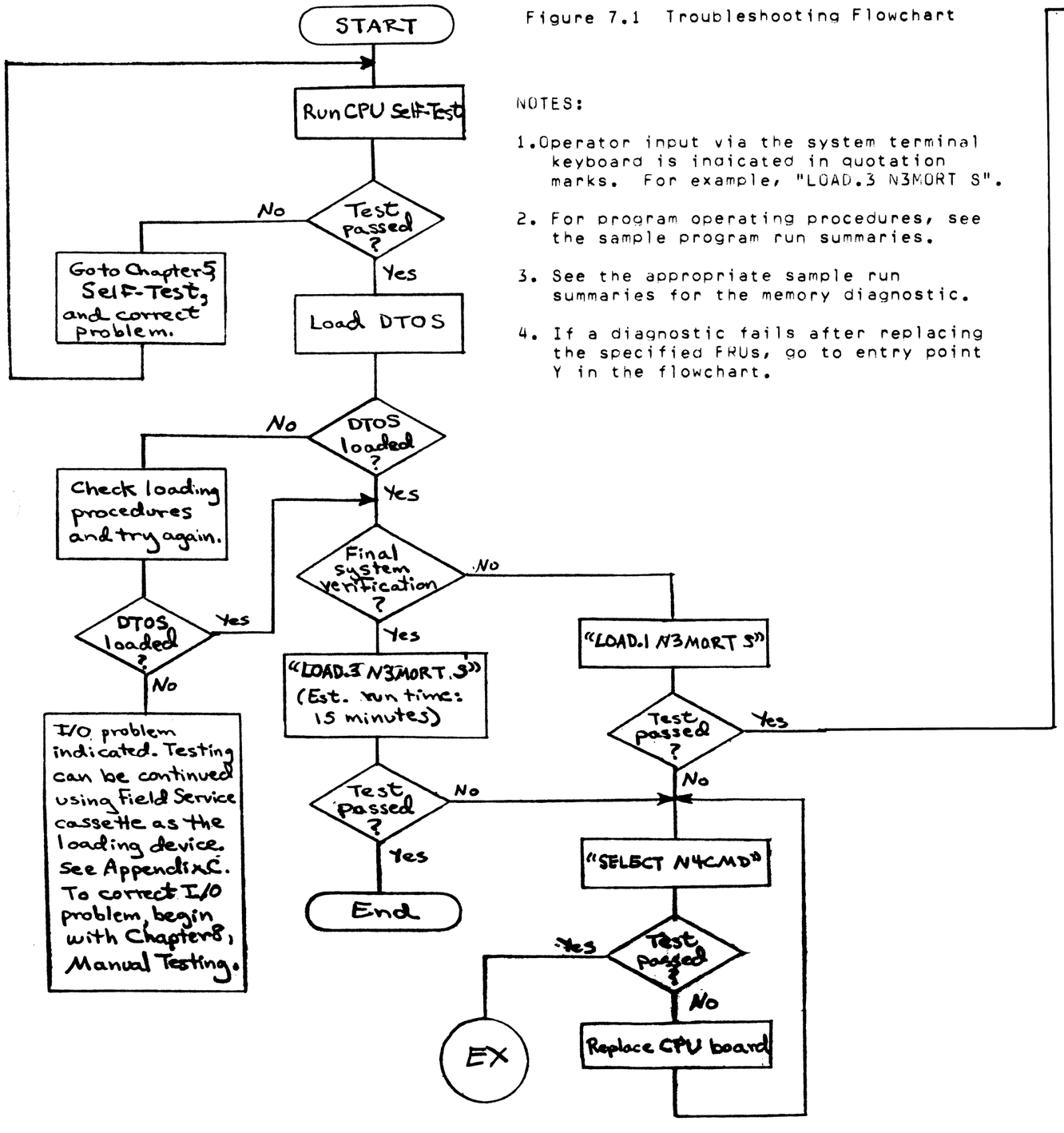


Figure 7.1 Troubleshooting Flowchart

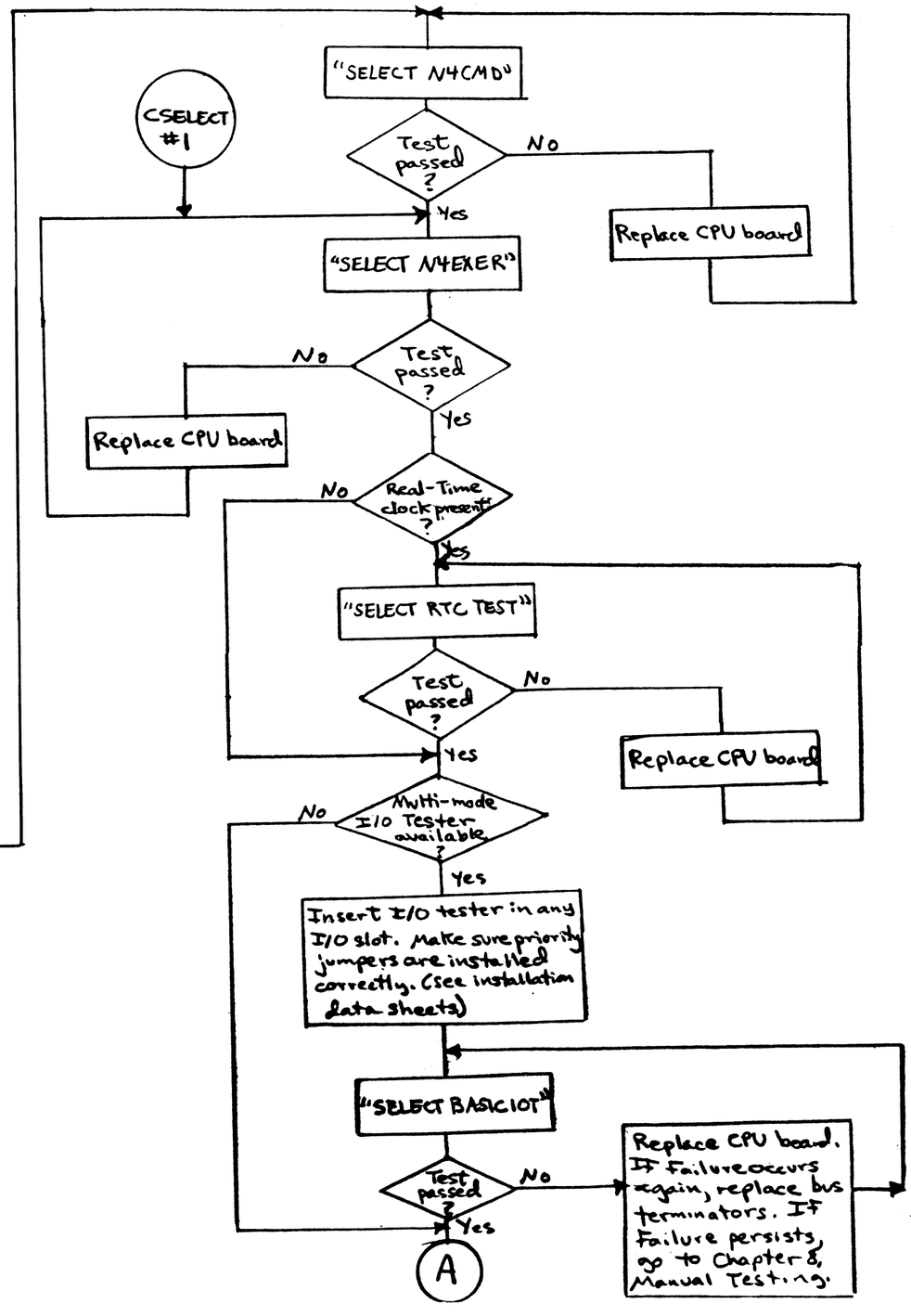
NOTES:

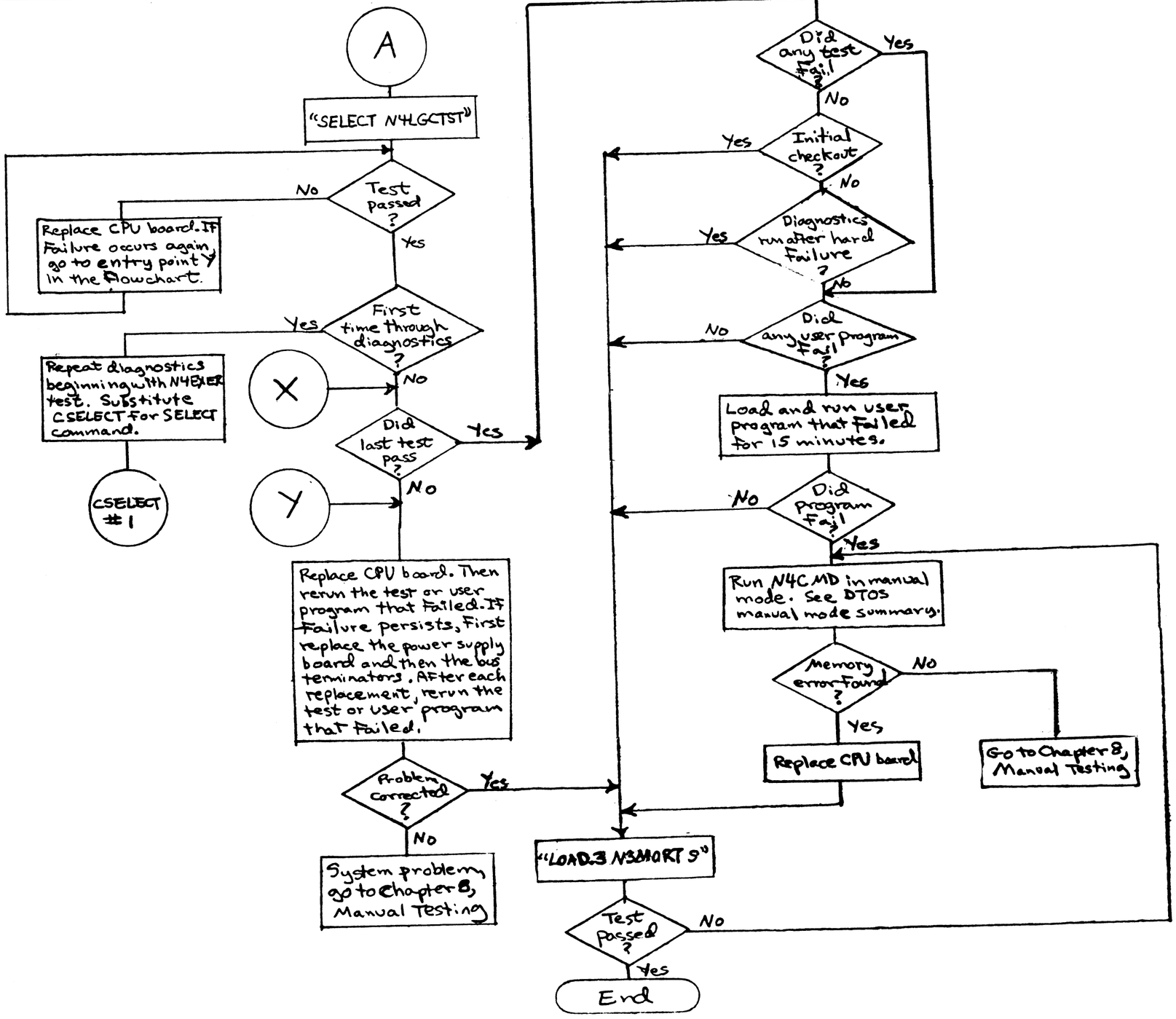
1. Operator input via the system terminal keyboard is indicated in quotation marks. For example, "LOAD.3 N3MORT S".

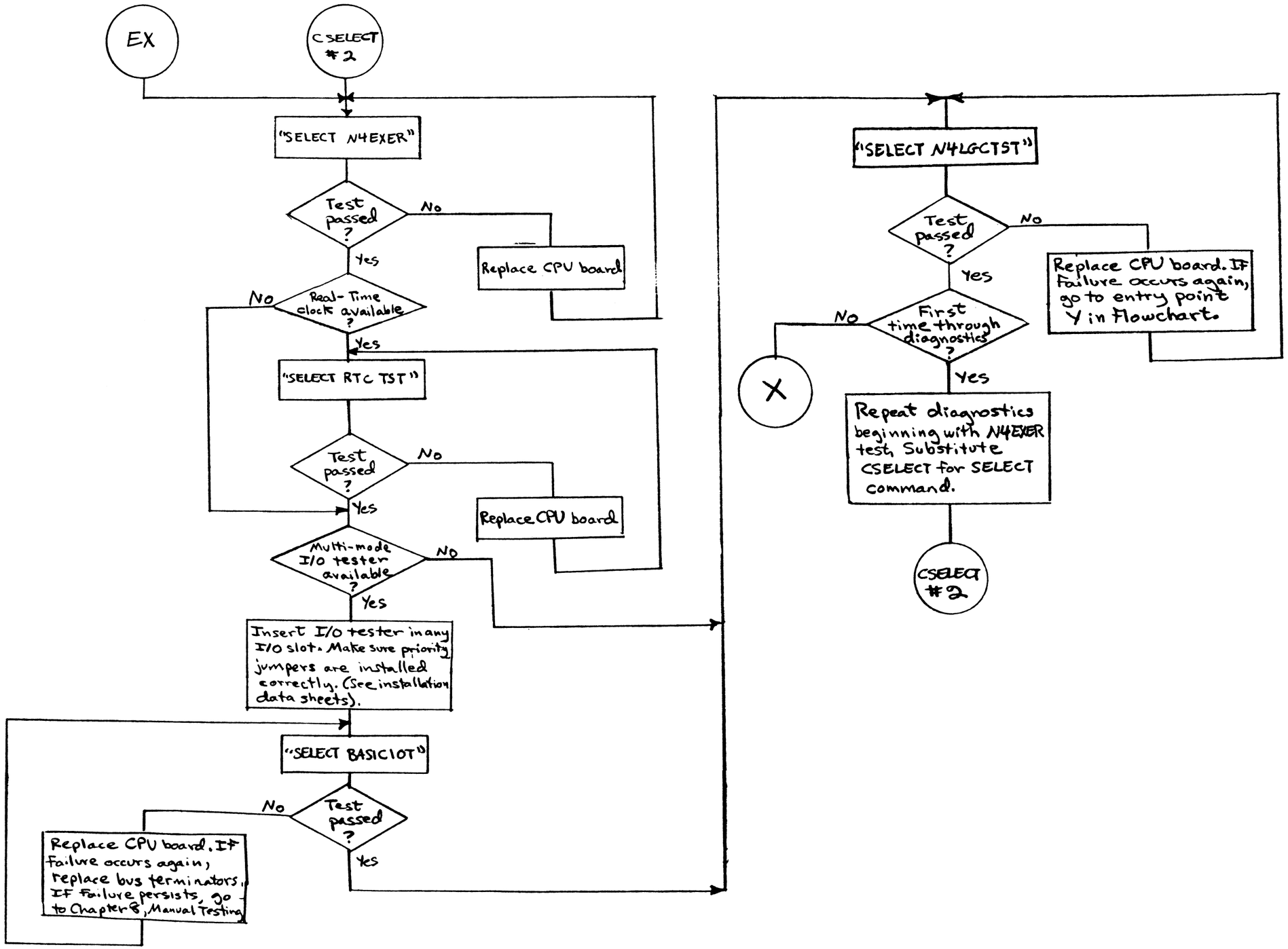
2. For program operating procedures, see the sample program run summaries.

3. See the appropriate sample run summaries for the memory diagnostic.

4. If a diagnostic fails after replacing the specified FRUs, go to entry point Y in the flowchart.







SAMPLE PROGRAM RUN SUMMARY
NOVA 3 MULTIPROGRAM TEST - SHORT
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: N3MORT S
DTOS Directory: HOST
DTOS Command: LOAD.1
Special Machine Requirements: None
Reference: Listing No. 096-000347
Estimated Program Run Time: 5 minutes

Operator Input:

*HOST
*SELECT N3MORT S

Comments

Program Output:

```
LOAD:
N3MORT S REV.  04
N3MORT SHORT - REV 04
TOTAL # 1K'S = 32   NO MAP
TEST RUN LIST                                          Note 1
TST# DESCRIPTION
0 CHKRBRD RAN
1 SC MEMORY TEST
2 ARITHMETIC TEST
4 MUL/DIV TEST
5 REAL TIME CLOCK
6 TTY TEST

!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ      Note 2

R/T (HRS,MIN,ERTOT)= 0   5                                 Note 3

*
```

NOTES:

1. The contents of the test run list will vary depending upon the program revision level and equipment configuration.

2. Teletypewriter test. This information may not be printed due to the running time of the program.

3. This information may not be printed due to the running time of the program. The two digits following the (HRS,MIN,ERTOT)= mean that the test ran 0 hours, 5 minutes. If a third digit is appended, it refers to the error total, indicating at least one test failed.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4/C MEMORY DIAGNOSTIC
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: N4CMD
Directory: HOST DTOS
Command: SELECT
Special Machine Requirements: None
Reference: Listing No. 096-001677
Estimated Program Run Time: 10 seconds

Operator Input:

*SELECT N4CMD

Comments

Program Output:

```
ACTIVE DIRECTORY =     HOST
PROCESSOR UNDER TEST = HOST

LOAD: N4CMD
N4MCMD  REV. 00  <Date>

** PROGRAM EXEC **                                      Note 1
TOP OF MEMORY = 37777
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: STUCK ADDRESS BIT
TEST NAME: MARCHING 1-0
TEST NAME: RELOCATING ISZ-DSZ TEST
          .
          .
          .
          .
          .
          .
TEST NAME: RELOCATING ISZ-DSZ TEST

TESTING COMPLETED ...

***END PROGRAM***
PASS= 1

*
```

NOTES:

1. In a 64K byte system, "TOP OF MEMORY = 77777" is printed.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4/C MEMORY DIAGNOSTIC
(DTOS Auto Mode; Errors Found)

DTOS Mnemonic: N4CMD
Directory: HOST DTOS Command: SELECT
Special Machine Requirements: None
Reference: Listing No. 096-001677
Estimated Program Run Time: 10 seconds

Operator Input:

*SELECT N4CMD

Program Output:

ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST

LOAD: N4CMD
N4MCMD REV. 00 <Date>

** PROGRAM EXEC **
TOP OF MEMORY = 37777
TEST NAME: MODIFIED DATA=ADDRESS
TEST NAME: STUCK ADDRESS BIT
TEST NAME: MARCHING 1-0

*** ERROR ENCOUNTERED

ADDRESS =
EXPECTED DATA =
ACTUAL DATA =

TEST NAME:
BIT NUMBER(S) =
<UPPER (OR) LOWER BANK>

Comments

Note 1

Note 2

NOTES

1. In a 64K byte system, "TOP OF MEMORY = 77777" is printed.

2. This block of error information is printed only when the supplemental error information flag is set to 1.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4/C MEMORY DIAGNOSTIC
(DTOS Manual Mode; No Errors Found)

DTOS Mnemonic: N4CMD
DTOS Directory: HOST
DTOS Command: LOAD
Special Machine Requirements: None
Reference: Listing No. 096-001677
Estimated Program Run Time: 1 to 3 seconds per test. See note 4.

	Comments
Operator Input:	
*LOAD N4CMD	
Program Output:	
ACTIVE DIRECTORY = HOST PROCESSOR UNDER TEST = HOST	
LOAD: N4CMD N4CMD REV. 00 <Date>	
** PROGRAM EXEC **	
INPUT NEW VALUES FOR CF'S (LF=DEFAULT) ECM <0-4>?	Note 1
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 2 FOLLOWED BY A CARRIAGE RETURN>	Note 2
Program Output:	
SUPPLEMENTAL ERROR INFORMATION (Y/N)?	Question asked when ECM=0, 1, 2 or 3. See Note 3.
PRINT ERROR LOG AT CONCLUSION (Y/N)?	Question asked when ECM=4. See Note 3.
Operator Input:	
<Y OR N FOLLOWED BY A CARRIAGE RETURN>	Yes or No
Program Output:	
PATTERNS (0-17)?	
Operator Input:	
<LINE FEED OR OPTION SPECIFIED IN NOTE 4 FOLLOWED BY A CARRIAGE RETURN>	Note 4
Program Output:	
TEST NAME:	

IMPORTANT: When this diagnostic test is run using the LOAD command, the test will continue until stopped by the operator. See Program Termination below.

PROGRAM TERMINATION

Operator Input:

"CONTROL" C (Enters the program monitor -- see Note 5 below

A (Aborts the program and returns to DTOS)

NOTES

The following notes summarize infomation appearing in the text file portion of the program listings. For more detailed information, refer to the appropriate listing.

1. Control Flags Default* Settings

Description of CF	CF	Program Octal Value	Default
Error control mode	ECM	0	Print error, return to DTOS.
Supplementary error information	SEI	0	None
Error log print	LP	0	None
Patterns to be run	PATS	0	All

* Line Feed selects default.

2. ECM refers to the error control mode. The number entered affects the action taken when an error is encountered.

EMC	Action Taken
0	Print an error report and return to DTOS.
1	Print an error report and continue.
2	Print an error report and halt.
3	Print an error report and go to program monitor.*
4	Enter error in error log and continue.

* See note 5 below.

3. The following information it printed when an error is found:

```
*** ERROR ENCOUNTERED
TEST NAME:
BIT NUMBER(S) =
<UPPER OR LOWER BANK>
```

If yes is answered to the question concerning supplemental error report, the following information is also printed: failure address, expected data, actual data.

If yes is answered to the question concerning the error log, the the following information is printed at the conclusion of the testing: chip location (bank, bit), test names, failure count. See the appropriate listing for more detailed information.

4. Patterns refer to the bit pattern used to select tests. Thus, to select one or more tests, enter the octal number that sets the appropriate bits to 1. See the table below.

Bit Position	Test Name	Run Mode	Run Time (seconds)
15	Modifies Data = Address	Auto	2
14	Stuck Address Bit	Auto	1
13	Marching 1-0	Auto	2
12	Relocating ISZ-DSZ Test	Auto	3

Example: 007 selects all tests except the Relocating ISZ-DSZ Test.

Test times assume no memory errors are detected.

5. The following table summarizes the program monitor commands.

Command	Meaning	Action Taken
A	ABORT	Return to DTOS.
C	CLEAR	Clear error log.
D	DUMP	Print and clear error log.
E	EXIT	Return to main program.
F	FLAGS	Print control flags.
H	HALT	Halt program.
P	PRINT	Print error log.
R	RESET	Print CFs; input new values.
T	TERMINATE	Terminate the current test and return to program.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4 EXERCISER
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: N4EXER
DTOS Directory: HOST
DTOS Command: SELECT or CSELECT
Special Machine Requirements: None
Reference: Listing No. 096-001136

```
Operator Input:

*SELECT N4EXER

Program Output:

ACTIVE DIRECTORY =     HOST
PROCESSOR UNDER TEST = HOST

LOAD:
N4EXER   REV. 00
N4EXER   00 RUNNING
MMU      PRESENT
TOTAL # OF 1K'S = 64                                    Note 1

PASS 1
PASS 2
PASS 3
PASS 4

*

Operator Input:

*CSELECT N4EXER

Program Output:

INPUT DATA CHANNEL EXERCISER TO BE RUN
(0= STANDARD DISK, 1= ZEBRA DISK, 2= I/O TESTER)        Note 2

Operator Input:

<ENTER APPROPRIATE NUMBER: 0, 1, 2, FOLLOWED
     BY A CARRIAGE RETURN>

Program Output:

ENTER DISK TYPE (0-NON 3330 TYPE, 1- 3330 TYPE)         Note 3

Operator Input:

(ENTER APPROPRIATE NUMBER - 0 OR 1 FOLLOWED
     BY A CARRIAGE RETURN>

Program Output:

ENTER DISK DEVICE CODE

Operator Input:

<ENTER APPROPRIATE NUMBER - 33, 73, 27 OR 67>

Program Output:                                         Note 4
```

NOTES

1. TOTAL # 1K'S varies with system.

2. ZEBRA DISK means DGC model 6060,6061 or 6067 disc drive.

3. This question is asked only when a standard disc is indicated. Type 3330 refers to a DGC model 4231 disc drive.

4. The remaining program output is the same as that generated when the program is run using the SELECT command except that the program outputs an "S" at the end of the first pass and a "P" approximately every three minutes thereafter.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4 LOGIC TEST
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: N4LGCTST
DTOS Directory: HOST
DTOS Command: SELECT or CSELECT
Special Machine Requirements: None
Reference: Listing No. 096-001137

Operator Input:

*SELECT N4LGCTST

Comments

Program Output:

ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST

LOAD:

N4LGCTST REV. 00
PASS
PASS
PASS
PASS

*

Operator Input:

*CSELECT N4LGCTST

Program Output:

INPUT DATA CHANNEL EXERCISER TO BE RUN
(0= STANDARD DISK, 1= ZEBRA DISK, 2= I/O TESTER Note 1

Operator Input:

<ENTER APPROPRIATE NUMBER - 0,1,2 FOLLOWED BY A CARRIAGE RETURN>

Program Output:

ENTER DISK TYPE (0-NON 3330 TYPE, 1- 3330 TYPE) Note 2

Operator Output:

<ENTER APPROPRIATE NUMBER - 0 OR 1 FOLLOWED BY A CARRIAGE RETURN>

Program Output:

ENTER DISK DEVICE CODE

Operator Input:

<ENTER APPROPRIATE NUMBER - 33, 73, 27 or 67>

Program Output: Note 3

NOTES

1. ZEBRA DISK means DGC model 6060, 6061 or 6067 disc drive.

2. This question is asked only when a standard disc is indicated. 3330 type refers to a DGC model 4231 disc drive.

3. The remaining program output is the same as that generated when the program is run using the SELECT command except that the program outpus an "S" at the end of the first pass and a "P" approximately every three minutes thereafter.

SAMPLE PROGRAM RUN SUMMARY
BASIC INPUT/OUTPUT TEST
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: BASICIOT
DTOS Directory: HOST
DTOS Command: SELECT or CSELECT
Special Machine Requirements: Multi-mode I/O Tester Board, No. 005-004283
Reference: Listing No. 096-001133

Operator Input:

*SELECT BASICIOT

Program Output:

SELECT BASICIOT

ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST

LOAD:
BASICIOT REV. 00

BASICIOT REV. 00

PASS 1

*

Operator Input:

*CSELECT BASICIOT

Program Output:

CSELECT BASICIOT
INPUT DATA CHANNEL EXERCISER TO BE RUN
(0= STANDARD DISK, 1= ZEBRA DISK,2= I/O TESTER) Note 1

Operator Input:

<ENTER APPROPRIATE NUMBER - 0,1,2 FOLLOWED
BY A CARRIAGE RETURN>

Comments

Program Output:

ENTER DISK TYPE (0= NON 3330 TYPE, 1= 3330 TYPE) Note 2

Operator Input:

<ENTER APPROPRIATE NUMBER - 0 OR 1 FOLLOWED
BY A CARRIAGE RETURN>

Program Output:

ENTER DISK DEVICE CODE

Operator Input:

<ENTER APPROPRIATE NUMBER - 33, 73, 27 OR 67>

Program Output: Note 3

NOTES

1. ZEBRA DISK means DGC model 6060, 6061 or 6067 disc drive.

2. This question is asked only when a standard disc is indicated. Type 3330 refers tc a DGC model 4231 disc drive.

3. The remaining program output is the same as that generated when the program is run using the SELECT command except that the program outputs an "S" at the end of the first pass and a "P" approximately every three minutes thereafter.

SAMPLE PROGRAM RUN SUMMARY
REAL-TIME CLOCK TEST
(DTOS Auto Mode; No Errors Found)

DTOS Mnemonic: RTC TST
DTOS Directory: HOST
DTOS Command: SELECT or CSELECT
Special Machine Requirements: NOVA 4/C with real-time clock option
Reference: Listing No. 096-000154-13

Operator Input:

*SELECT RTC TST

Program Output:

SELECT RTC TST

ACTIVE DIRECTORY = HOST
PROCESSOR UNDER TEST = HOST
LOAD:
RTC TST REV. 13
RTC TST 13 RUNNING

PASS 1
PASS 2

*

Operator Input:

*CSELECT RTC TST

Program Output: Comments

CSELECT RTC TST
INPUT DATA CHANNEL EXERCISER TO BE RUN Note 1
(0= STANDARD DISK, 1= ZEBRA DISK, 2= I8/O TESTER)

Operator Input:

<ENTER APPROPRIATE NUMBER - 0, 1 OR 2 FOLLOWED
BY A CARRIAGE RETURN>

Program Output:

ENTER DISK TYPE (0- NON 3330 TYPE, 1- 3330 TYPE) Note 2

Operator Input:

<ENTER APPROPRIATE NUMBER - 0 OR 1 FOLLOWED
BY A CARRIAGE RETURN>

Program Output:

ENTER DISK DEVICE CODE

Operator Input:

(ENTER APPROPRIATE NUMBER - 33, 73, 27 OR 67>

Program Output: Note 3
NOTES

1. ZEBRA DISK means DGC model 6060, 6061 or 6067 disc drive.

2. This question is asked only when a standard disc is indicated. Type 3330 refers to a DGC model 4231 disc drive.

3. The remaining program output is the same as that generated when the program is run using the SELECT command except that the program outputs an "S" at the end of the first pass and a "P" approximately every three minutes thereafter.

CHAPTER 8
MANUAL TESTING

Chapters 3 through 7 of the troubleshooting section should isolate most malfunctions associated with the NOVA 4/C computer. The remainder of the troubleshooting is directed to system problems, namely, input/output.

DTOS LOADING FAILURE

If you cannot load DTOS as specified in Chapter 7 follow the steps listed below. If a fault is found as you proceed through the steps, take corrective action and attempt to load DTOS again.

1. Disconnect the loading unit (disc or tape drive) and power it up off-line.

   Refer to the documentation for the device. Check to ensure that all functions that can be performed off-line are responding properly. (For example, load the tape drive with a scratch tape and advance the tape to the beginning of tape position; advance the tape; rewind it.) If the unit fails to perform properly, either troubleshoot or replace the unit.

2. Examine the device cable. Is it connected properly? Are there any loose wires? If so, replace the device cable.

3. Examine the condition of the paddleboard cable and connectors. If they appear to be without fault, slip the paddleboard connectors off the appropriate backpanel pins and then reinsert them, making sure they are properly seated.

4. Replace the CPU board.

5. Replace the bus terminators (16-slot chassis only).

6. Replace the controller board if the unit is operating properly off-line and the device cable and paddleboard assembly appear to be in good condition and properly connected.

7. Move the controller board to a different slot, making sure the priority chain is maintained by inserting jumpers across the open slot. See the 5- or 16-slot installation data sheets.

8. Replace the paddleboard assembly and the device cable.

If the above procedures fail to repair the malfunction, call DGC Field Service for assistance.

RELIABILITY/DIAGNOSTIC TEST FAILURE

Successful completion of the CPU self-test and the loading of DTOS indicates that the main portion of the NOVA 4/C computer is operating properly and the input/output transactions between the disc (tape) drive controller, the CPU and memory were accomplished without fault.

After replacing the field replaceable units specified in Chapter 7, follow the steps listed below.

1. Remove all I/O controllers from the chassis, except the disc (tape) drive controller that is used as the DTOS loading device. Make sure the priority chain is maintained on the backpanel by placing jumpers across the slots that previously held I/O controllers. See the 5- or 16-slot installation data sheets. Also, make sure the load balancing rules for the 16-slot chassis are followed as shown in the 16-slot installation data sheets.

2. Remove the paddleboard connectors on the backpanel for all unused I/O controllers.

3. Load DTOS and run the failing reliability or diagnostic test.

4. If the test passes, add one I/O controller with its associated paddleboard connectors and rerun the test. Continue adding I/O controller boards until you isolate the malfunctioning controller.

If the above steps fail to correct the problem, call DGC Field Service for assistance.

USER PROGRAM FAILURE

A user program failure after successful completion of the NOVA 4/C reliability and diagnostic testing points to either a software problem or an I/O controller/device malfunction.

When this situation occurs, recheck any panic codes or error reports generated by the operating system. If these reports fail to indicate the source of the malfunction, follow the steps listed below.

1. Load DTOS.

2. Enter LOAD N3MORT L on the system terminal keyboard. (This is the DTOS mnemonic for NOVA 3 Multi-programming Reliability Test, Long version.)

3. Allow the program to run for a minimum of 30 minutes. When the program detects an error, it sends an error message to the terminal, as shown in the following sample program run summary.

   NOTE: To stop the reliability test, press the BREAK key. This places the CPU in console mode.

4. If an error occurs, run the diagnostics for the device indicated. See the appropriate device documentation. Take corrective action and rerun the user program that failed.

If the user program fails again, run the NOVA 3 Multi-programming Reliability Test, Peripheral version (DTOS mnemonic, N3MURT P), following the same steps as outlined above.

SAMPLE PROGRAM RUN SUMMARY
NOVA 3 MUTLTI-PROGRAMMING RELIABILITY TEST
LONG OR PERIPHERAL VERSION
(DTOS Auto Mode; Error Found)

DTOS Mnemonic: N3MORT L (Long)
N3MORT P (Peripheral)
DTOS Directory: HOST
DTOS Command: LOAD
Special Machine Requirements: none
References:
Listing Long: 096-000348
Listing Peripheral: 096-000508

NOTE: All input/output devices should be placed on-line. Disc drives and tape units should be loaded with scratch disc packs or tapes to prevent data loss.

Operator Input:	Comments
*LOAD N3MORT L	Note 1
Program Output:	
LOAD:	
N3MORT L REV. 04	
@200R	
N3MORT LONG - REV 04	
TOTAL # 1K'S=	Note 2
TEST RUN LIST	Note 3
TST# DESCRIPTION	
0 CHKRBRD RAN	
1 SC MEMORY TEST	
2 ARITHMETIC TEST	
4 MUL/DIV TEST	
11 6060/61 DISK(PRI)	
15 REAL TIME CLOCK	
16 ITY TEST	
DEV.#27 6060/61 DISK	
DSK# #CYLS #SEC/S #SURF	
0 815 24 19	
DEV.#33 M.H.DISK	
DSK# #CYCLES #SEC/S #SURF	
0 408 12 4	
R/T(HRS,MINS,ERTOT)=0 5	Note 4
PROGRAM #11 6060/61 DISK(PRI)	Note 5
AC'S 010000 017377 060201	
SCRLO/HI 026000 031777 USER B DCHLO/HI 056000 061777	
MEM ALLOCATION TABLE	
PHYS LOGICAL PHYS LOGICAL	
74 026000 24 030000	
CYL # ZBDST ZBCST	
101012 026114 056114	
ZBSTA ZBDDA ZBDDC	
060201 000000 017071	
R/T(HRS,MINS,ERTOT)= 0 7 1	Note 6

NOTES

1. When running peripheral version, substitute N3MORT P.
2. Number of 1K's varies with the size of memory.
3. The tests run vary with the system configuration.
4. This message indicates the program ran for 5 minutes without errors.
5. This message indicates an error was found when testing the 6060/61 disc drive, unit 0. In this case, run the 6060/61 diagnostics.
6. This message indicates the program ran 7 minutes before it encountered the failure indicated above.

CHAPTER 9
16-SLOT POWER SUPPLY OPERATION

INTRODUCTION

The NOVA 4 16-slot power supply converts a 120 or 220/240 ac voltage source to the five regulated dc voltages required by the NOVA 4 computers. It also generates the system clocks. A battery backup option generates the regulated dc memory voltages from a +12 volt battery during an ac power failure.

The power supply consists of a VNR (voltage non-regulated) unit and a printed circuit board. The VNR unit supplies both non-regulated dc voltage to the power supply printed circuit board and ac voltage to the fan module via the internal cable. The power supply printed circuit board supplies the regulated dc voltages and system clocks to the system printed circuit boards via the backpanel.

A line cord with a 12-pin connector determines the operating voltage for the power supply.

FUNCTIONAL OVERVIEW

The 16-slot power supply uses a forward off-line switching regulator to produce the high power outputs required by the NOVA 4 computers. The major components of this off-line switching regulator are a rectifier and filter, a buck regulator, and a dc to dc converter.

Figure 9.1 shows the interconnection of these components.

The rectifier and filter convert power from the ac line to a high voltage dc source. The voltage varies with the line, but is typically 300 volts.

The buck regulator takes power from the filter and provides a constant voltage for the dc to dc converter. It monitors the output voltage, and delivers more current as the load increases to keep the output in regulation. The buck regulator includes a high voltage switch and a pulse width modulator. The switch alternately opens and closes the path between the filter and the dc to dc converter. The pulse width modulator opens and closes the switch at a constant 40 Khz rate, but varies the duty cycle (the ratio between the "on" time and the "off" time) to achieve regulation.

The dc to dc converter takes power from the buck regulator and produces the low voltage output. It includes an H-bridge chopper, a power transformer and a rectifier and filter. The chopper converts regulated dc power to a high voltage square wave for the power transformer. It does this by alternately closing a current path in one direction and then the opposite direction between the buck regulator and the transformer's primary winding. The transformer converts the high voltage/low current input to a low voltage/high current output, which the rectifier and filter convert back to dc.

To summarize, the off-line forward switching regulator performs five power transformations to convert 110/220VAC to 5VDC. As you scan Figure 9.1 from left to right, these transformations are:

120 or 220/240 VAC (rms) - 300VDC - 180VAC (peak) - 5VAC - 5VDC

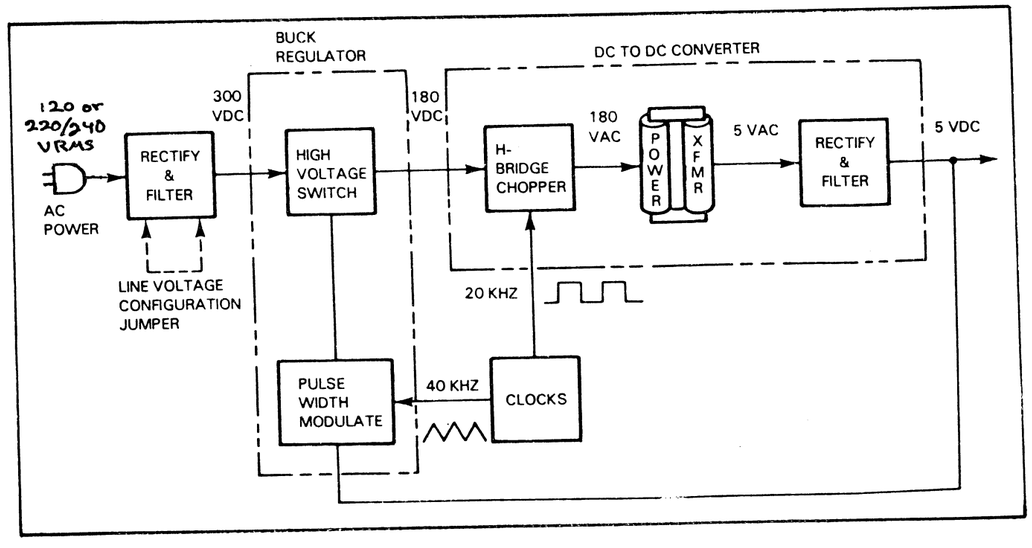


Figure 9.1 Off-Line Switching Regulator Block Diagram

OPERATION

We can now take a look at the actual functional blocks included in the NOVA 4 power supply. These blocks are distributed between the VNR unit and the power supply circuit board. We will pay particular attention to the signals that flow in and out of these modules. This may help you to more easily and accurately identify a failing field replaceable unit.

VNR Unit

The VNR (voltage-non-regulated) unit provides high voltage and low voltage dc power for the power supply board. It can also generate battery backup power when that option is configured. Figure 9.2 shows the component parts of the VNR unit. The easiest way to understand them is to follow a power on/off sequence.

When you first turn on the power switch, current flows from the ac power line, through the line fuse(s) and to the low voltage power transformer. The transformer output is rectified and filtered to provide +30VNR and -30VNR for the control circuits on the power supply board. The transformer also powers the fans and drives a low voltage ac signal (ACS) to the high state. This signal goes to the real-time clock circuits.

Current also flows through a very large resistor and into the high voltage rectifier and filter. The resistor limits the current flow as the filter capacitors charge, which keeps them from blowing the line fuse(s). When the capacitors are sufficiently charged, the voltage monitor drives the high voltage sense (HVS') signal to the low state. The supply board responds by closing the relay, which short circuits the resistor. This makes full power available to the off-line switching regulator, which completes the power-on sequence.

When you turn the power switch off, the fan module drives the on-switch (ONSW) signal to the low state. Following a short delay (to allow the CPU to save critical information), the supply board opens the relay, which disconnects the VNR unit from the ac power line.

The optional battery backup module generates 12 volt dc power for special battery backup circuits on the power supply board. These circuits maintain critical memory voltages when a power failure occurs in order to save data stored in main memory. The battery can support main memory for 90 minutes. If that is not enough time, you can connect a larger external battery (an automotive battery, for example). The backup option includes a battery charger that is powered by the low voltage dc supply. The charger is enabled whenever the relay is turned on.

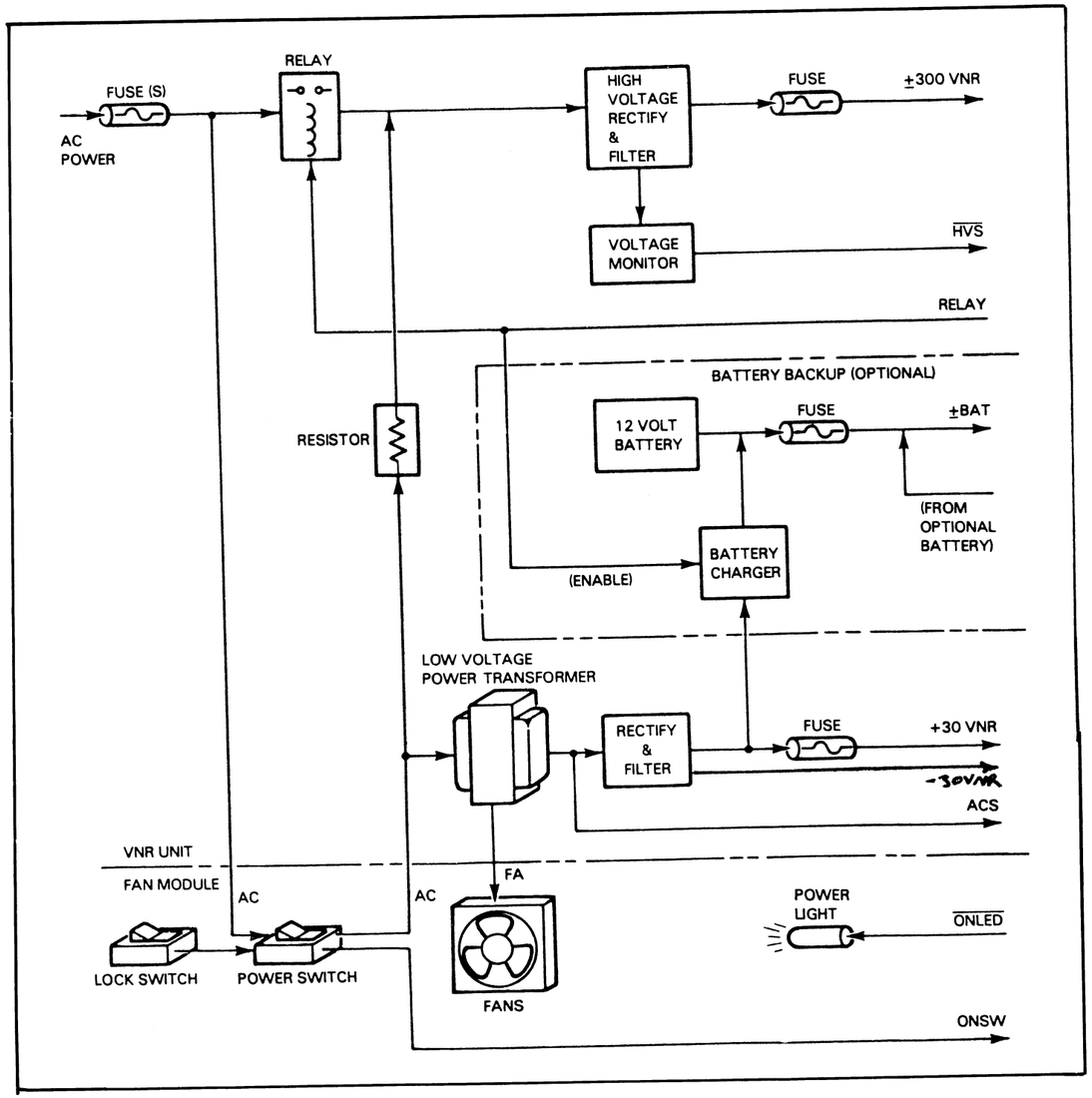


Figure 9.2 VNR Unit and Fan Module Block Diagram

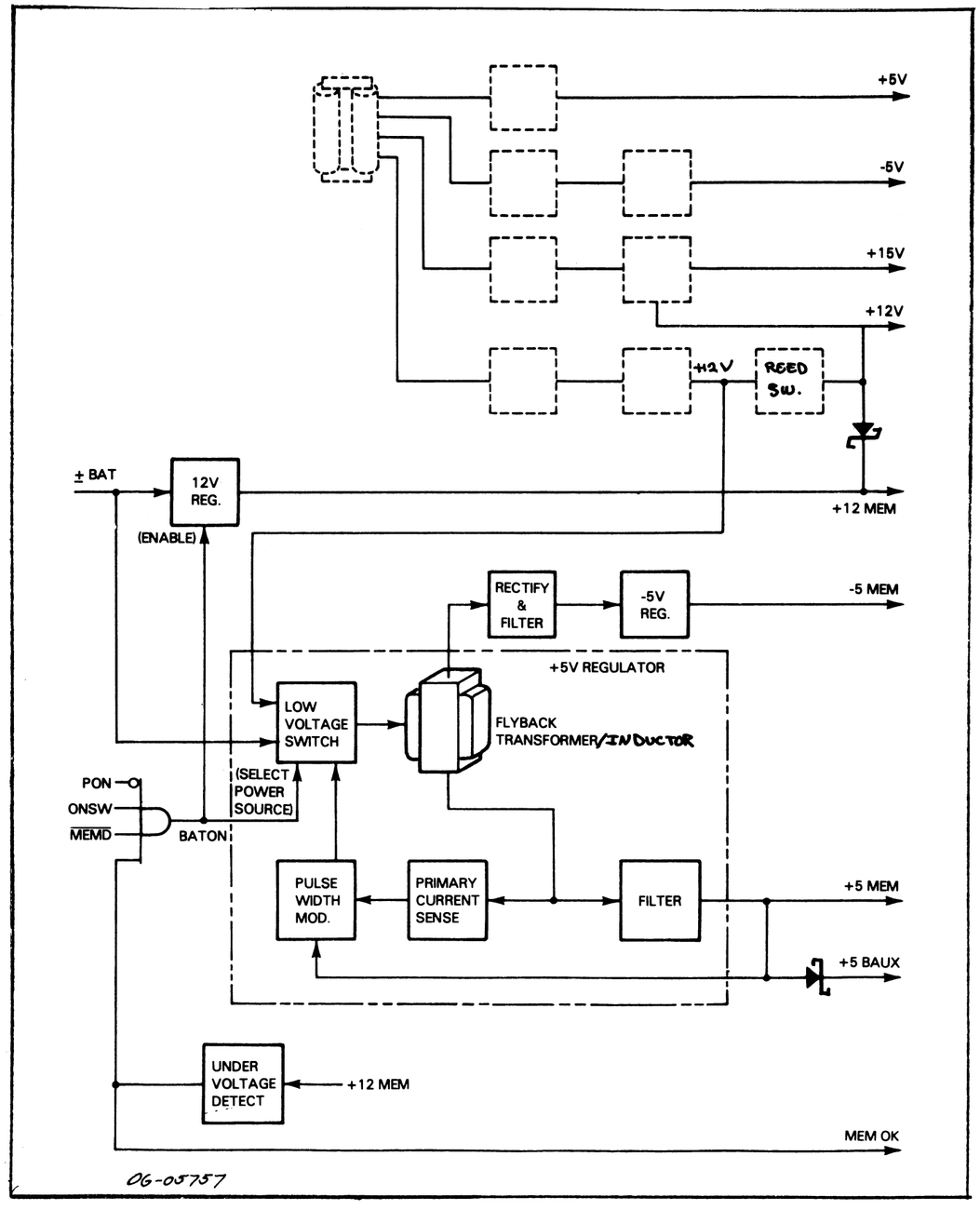


Figure 9.4 Battery Backup Block Diagram

The -5V regulator draws power from the +5V regulator via the flyback transformer. It is a simple linear series pass design and has built-in current limiting.

The battery on (BATON) signal controls battery backup operation. When the supply operates normally, the PON signal is driven to the high state and the BATON is driven to the low state. This turns off the +12 volt regulator, and current flows from the +12V supply, through the Schottky diode and to the +12 MEM output. At the same time, the low voltage switch selects the +12V supply, which in turn powers the +5 MEM-P and -5 MEM-P outputs.

When a power failure occurs, the PON signal is driven to the low state. If the failure did not occur because of a memory disaster, the BATON signal is driven to the high state. This switches the regulators over to battery operation. As long as the battery retains sufficient charge, the +12 MEM output stays in regulation and the MEM OK signal is in the high state. But when the battery discharges to a dangerously low level, the under-voltage dectector drives the MEM OK signal to the low state, which in turn drives the BATON signal to the low state. This shuts the supply down entirely. The entire supply also shuts down when the power switch is turned off.

Table 9.2 16-slot chassis power supply specifications with battery backup

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+5.10V	+5.20V	7.5A	100A
+12V	+12.5V	+12.1V	0	12.5A *
+15V	+14.5V	+15.5V	0	1.5A *
-5V	-4.9V	-5.1V	0	3A
-11V	-11.0V	-12.5V	0	0.02A
+5 MEM	+4.8V	+5.1V	0.25A	4.5A *
+12 MEM	+11.7V	+12.1V	0	6A *
-5 MEM	-4.9	-5.1 V	0	0.3A

* The sum of the currents on +12V, +15V, +12 MEM, and 0.55 times the sum of the currents on +5 MEM and -5 MEM must NOT exceed 12.5 Amps.

INTERCONECTION WITH SYSTEM

The 16-slot power supply board communicates with the rest of the system via jacks 17 and 35 to the backpanel. Tables 9.3 through 9.5 list each signal either generated or received by the power supply board together with the jack locations of the signal. See the 16-slot backpanel schematic, DGC No. 001-001563, for the locations of signals on the backpanel.

Table 9.3 Voltage Signals

Signal	Jack Pin	Source	Destination	Description
GND	J17 even pins J35 pins 1-2, 4, 37-42	Power Supply	Backpanel	Power or logic ground
+5V	J17 odd pins	Power Supply	Backpanel	+5V source
+5 MEM-P	J35 pins 33-36	Power Supply	Backpanel	Same as +5V if battery backup not configured
-5V	J35-27 J35-28	Power Supply	Backpanel	-5V source
-5 MEM-P	J35-19	Power Supply	Backpanel	Same as -5V if battery backup not configured
-11V	J35-25	Power Supply	Backpanel	EIA interface voltage
+12V	J35 pins 43-46	Power Supply	Backpanel	+12V source
+12 MEM	J35 pins 29-32	Power Supply	Backpanel	Same as +12V if battery backup not configured
+15V	J35-49 J35-50	Power Supply	Backpanel	+15V source

Table 9.4 Power supply status signals

Signal	Jack Pin	Source	Destination	Description
$\overline{\text{DATA 15}}$	J35-3	Power Supply	Backpanel	Reserved for future use
$\overline{\text{MEMD}}$	J35-21	Backpanel	Power Supply	Failure on -5 MEM
MEMOK	J35-23	Power Supply	Backpanel	+12 MEM voltage ok
$\overline{\text{ONLED-P}}$	J35-11	Power Supply	Backpanel	All DC output voltages ok
$\overline{\text{PWR FAIL}}$	J35-9	Power Supply	Backpanel	Power switch off or DC power failure
PWR OK	J35-16	Power Supply	Backpanel	All DC output voltages ok
$\overline{\text{SC DET}}$	J35-47	Power Supply Backpanel	Backpanel Power Supply	Short circuit on +5V, +5 MEM, +12V, or +12 MEM

Table 9.5 Clock Signals

Signal	Jack Pin	Source	Destination	Description
$\overline{\text{B10CLK}}$	J35-6	Power Supply	Backpanel	10 MHz square wave
$\overline{\text{B20CLK}}$	J35-14	Power Supply	Backpanel	20 Mhz square wave
$\overline{\text{B40CLK}}$	J35-10	Power Supply	Backpanel	40 MHz square wave
$\overline{\text{ENB10CLK}}$	J35-15	Power Supply	Backpanel	10 MHz pulse train
LCLK	J35-17	Power Supply	Backpanel	50/60 Hz square wave (AC line frequency)
$\overline{\text{PSCLK}}$	J35-5	Backpanel	Power Supply	Reserved for future use
$\overline{\text{5 MHz CLK}}$	J35-7	Power Supply	Backpanel	5 MHz square wave
500 Hz	J35-18	Power Supply	Backpanel	500 Hz square wave

Test Points

Table 9.6 lists and explains the signals that appear on the test points (J1) on the front of the 16-slot power supply board.

Table 9.6 Test point signals

Signal	J1 Pin	Description
+15V	8	Same as +15V supply on backpanel.
+12V	10	Same as +12V supply on backpanel.
+5V	15	Same as +5V supply on backpanel.
+5 AUX	7	Internal +5V supply for the power supply logic. (All supply functions are disabled when there is no +5 AUX. The VNR unit supplies +30V for the +5AUX regulator.)
-5V	6	Same as -5V supply on backpanel.
VREF	14	Internal +5.80V reference for all regulators. (All internal and external supply voltages go out of regulation if VREF fails.)
GND	9	Power and logic ground.
HVS	4	High voltage from the VNR unit exceeds 260V. (All external supply voltages except -11V shut down if high voltage fails and battery backup comes on-line if configured.)
PON	11	External supply voltage regulators are enabled. (Goes to low state if HVS is in low state, an emergency condition such as a memory disaster occurs, an internal failure occurs, or power switch turned off. Battery backup comes on-line when PON goes to low state if power switch is on.)
POK	5	All external supply voltages ok.
$\overline{\text{PWR FAIL}}$	3	POK or HVS in low state or power switch is turned off.
$\overline{\text{PWM}}$	1	40 KHz pulse train from pulse width modulator. Clocks the main switching regulator which powers the external supply voltage regulators.
20 K	16	20 KHz square wave. Clocks the circuits which transform high voltage from the main switching regulator to low voltages for the external supply voltage regulators.
Q30-C	12	20 KHz drive signal in the power transformation circuits mentioned above.
Q29-C	13	20 KHz drive signal in the power transformation circuits mentioned above.
CURRENT	2	Voltage proportional to current flow in primary winding of power transformer that converts high voltage from the main switching regulator to low voltage for the external supply voltage regulators.

CHAPTER 10
5-SLOT POWER SUPPLY OPERATION

INTRODUCTION

The NOVA 4 5-slot power supply converts a 100/120 or 220/240 ac voltage power source to the five regulated dc voltages required by the NOVA 4 computers. It also generates the system clocks. A battery backup option generates the regulated dc memory voltages from a +6 volt battery during an ac power failure.

The entire power supply, including the battery backup option and battery, is contained on a single printed circuit board. This board supplies the regulated dc voltages and system clocks to the printed circuit boards via the backpanel and provides ac power for the fan modules via the internal cable.

A line cord with a 12-pin connector is used to determine the operating voltage for the power supply.

NOTE: Throughout this chapter, reference designators (e.g., C1 and T1) refer to the 5-slot power supply logic schematic, DGC No. 001-001616. Thus when reading this chapter, it is helpful to refer to the schematic.

ORGANIZATION

The 5-slot power supply, like the 16-slot power supply, uses a forward off-line switching regulator to produce the high power outputs required by the NOVA 4 computers. The major components of the 5-slot power supply's off-line switching regulator are a VNR source, a pulse width modulation control, an inverter, and a dc regulator.

In addition to the off-line switching regulator, the 5-slot power supply includes a line filter, an auxiliary voltage supply, soft start logic, several voltage regulators, various fault detection circuits, and the system clock circuitry.

Figure 10.1 shows the interconection of all these components.

OPERATION

Off-Line Switching Regulator

The ac line voltage passes through a line filter to the VNR source where it is converted into a high dc voltage source. Although this dc voltage source varies from 259 VNR to 337 VNR with the line voltage, it is referred to as 300 VNR.

For 100/120 volt operation, the 300 VNR source rectifies and doubles the ac line source by connecting the junction of C1 and C2 (J1-9) to the neutral side of the line (J1-8) to provide a 300 VNR ac source; for 220/240 operation, it simply rectifies the ac line source.

The pulse width modulation control governs the operation of the inverter, and, in turn, of the dc regulator, by controlling the amount of power through the inverter. It opens and closes the power path once every 50 us (at a 20 KHz rate) and varies the ratio between the "open" time and the "closed" time (the duty cycle) in accordance with the variation on the +5V output. As the line voltage decreases or the +5V output load increases, the pulse width modulation control increases the "closed" time to transfer more power. In this way, the pulse width modulation control regulates the +5V output of the dc regulator.

Inverter

The inverter receives power from the 300 VNR source and transforms it into the ac voltage outputs which power the dc regulator. Its main component is transformer T1. T1 operates at 20 KHz with a variable duty cycle. Its maximum duty cycle is just less than 50 percent.

DC Regulator

The dc regulator receives ac voltages from the inverter and converts them into five different low dc voltage outputs: +5V, +12V, +15V, -5V, and -11V. It consists of rectifiers, an inductor L1, various filter circuits, and two voltage regulators.

The +5V output feeds back to the pulse width modulation control to regulate the duty cycle of the inverter, which, in turn, regulates all the outputs of the dc regulator.

The +12V output passes through a simple series pass regulator to produce a very well regulated +12V supply.

The +15V output is derived from T1 and the +5V in the dc regulator. It has no additional regulation. Since the pulse width modulation control removes all line variations from +5V, line variations will not effect the +15V output. Load variations on either the +5V or +15V outputs do effect the +15V output; however, their effect is relatively small.

The -5V and -11V receive additional regulation. The -5V output is regulated by a +5V three terminal regulator with its positive output grounded. The -11V output is regulated by a -12V three terminal regulator.

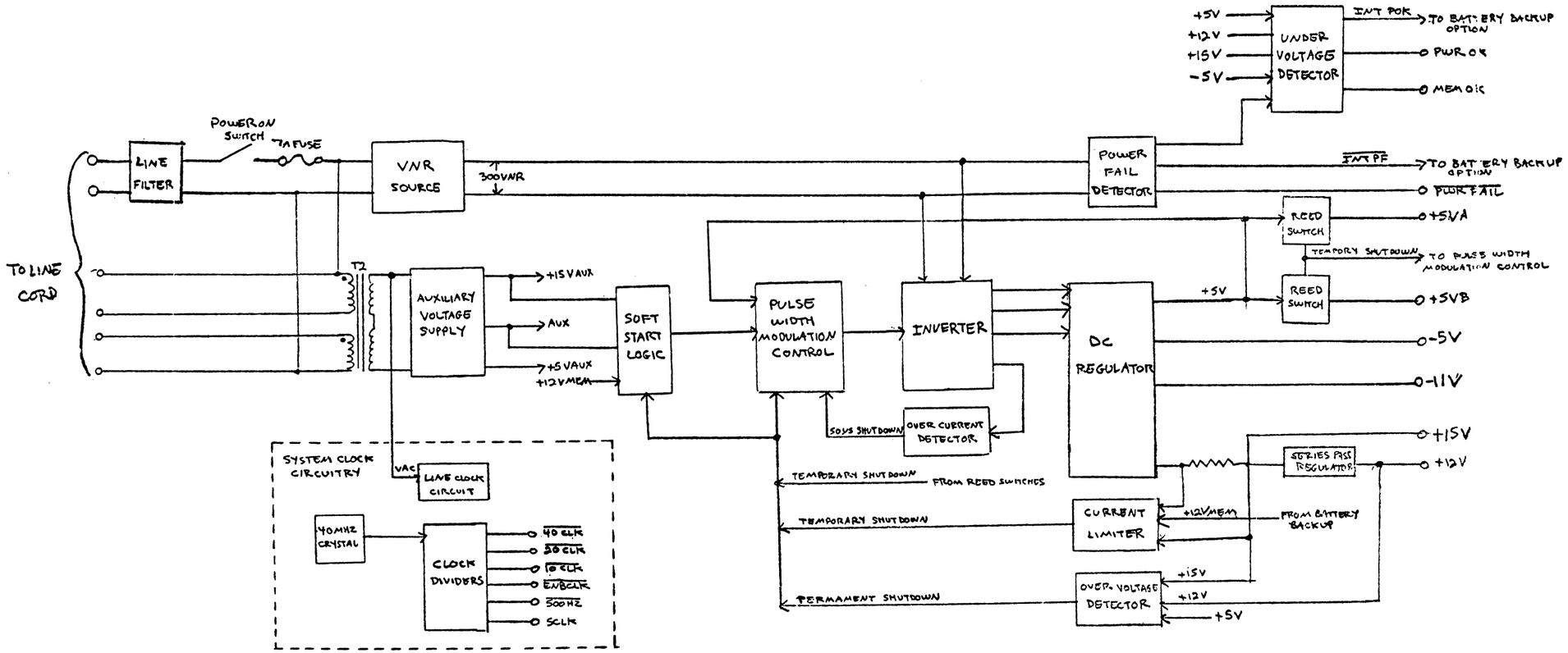


Figure 10.1 Basis 5-Slot Power Supply Block Diagram

Auxiliary Voltage Supply

The ac line voltage powers the transformer T2 to produce an auxiliary voltage which functions as a control voltage for the power supply. This voltage goes through a 3-terminal voltage regulator to produce the +15V AUX and VAUX. The auxiliary voltage supply also produces +5V AUX. These voltages power most of the power supply circuits and also provide voltage references.

Soft Start Logic

The soft start logic allows the output voltages of the power supply to come up slowly and not overshoot when the system is powered up. Its main component is a capacitor with a large time constant. This capacitor must charge up before the pulse width modulation control can switch full power to the inverter. Most of the faults which shut down the pulse width modulation control also discharge this capacitor to allow the output voltages to come up slowly when the fault is removed.

Fault Detection Circuits

Various circuits monitor the operation of the power supply, checking for under voltage, over voltage, and over current conditions.

Under Voltage Detection

The under voltage detector continually monitors the +5V, -5V, +12V and the +15V outputs. When any of these outputs falls below the minimum operating level (see Table 10.1), it drives the INT POK signal to a low state.

The power fail detector monitors the 300 VNR source for under voltage conditions on the ac line source. When it detects an under voltage condition, it pulls the INTPF to the low state. This signal drives the PWR FAIL signal to the low state to inform the system of an impending ac power failure. Approximately 22 ms later, INT POK is driven to the low state and stays in the low state for 155 ms or longer depending on how long the power failure lasts.

Whenever, INT POK goes to a low state, it drives PWR OK to a low state to reset the CPU. If battery backup is not present and the line fails, PWR OK stays in the low state, and later, it drives MEM OK to the low state. If battery backup is present, PWR OK stays in the low state and MEM OK stays in the high state as long as the battery lasts.

Table 10.1 5-Slot chassis power supply specifications

Output	Voltage		Current	
	Min	Max	Min	Max
+5V	+4.95V	+5.2V	5A	35A
+12V	+11.7V	+12.7V	0	5A *
+15V	+14.0V	+16.0V	0	5A *
-5V	-4.75V	-5.25V	0	1.5A
-11V	-11.0V	-12.5V	0	0.025A
+5 MEM	+4.95V	+5.2V	0	1A
+12 MEM	+11.3V	+12.7V	0	3A *
-5 MEM	-4.75	-5.25V	0	0.05A

* The sum of the maximum currrents on the +12V, +15V, and the +12 MEM lines must NOT exceed 5 Amps. In battery backup mode the maximum current specification for +12 MEM is 0.3 Amps.

Over Voltage Detection

The over voltage detector protects against over voltage conditions on the +5V, +12V, and +15V outputs. If any of these outputs goes above the shut down level (see Table 10.2), this detector shuts the pulse width modulation control down permanently. The pulse width modulator control will not start again until the power supply is turned off and on again using the front console power switch. This over voltage fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the system is powered up again.

Table 10.2 Over voltage shutdown levels

Output	Shutdown Voltage
+5V	5.66 +/- 1%
+12V	13.56 +/- 5%
+15V	17.3 +/- 5%

Over Current Detection

The main over current protection device is a cycle by cycle current limiter. It consists of a current sense transformer T3 in the inverter and an over current detector. The over current detector monitors the current in the secondary winding of this transformer. When the current flowing in this winding is too great, the over current detector shuts the pulse width modulation control down for one cycle (50 usec).

A secondary over current protection device, the current limiter, monitors the current on the +12V, +15V, and +12V MEM outputs. When the sum of the current on these three outputs goes above 5 Amps, the current limiter temporarily shuts down the pulse width modulation control. Although the shutdown time will vary with the load on these outputs, it is typically 0.5 sec. This over current fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the fault condition is removed.

Two reed switches with a one turn winding around them function as current sensors for the +5V outputs. When the current on either of the two +5V outputs, goes above 20-25 Amps, the reed switches temporarily shut down the pulse width modulation control. This over current fault also discharges the capacitor in the soft start logic to allow the voltage outputs to come up slowly when the fault condition is removed.

BATTERY BACKUP OPTION

Introduction

The battery backup option generates 6-volt dc power for the optional battery backup circuitry. This circuitry maintains the following critical memory voltages when a power failure occurs: +5V MEM, +12V MEM, and -5V MEM. These voltages are needed to refresh data stored in the dynamic RAM main memory. In addition, the battery backup circuitry powers the systems clocks and the front console lights, and provides a memory status signal (MEM OK) to indicate when the memory voltages are above the minimum operating levels.

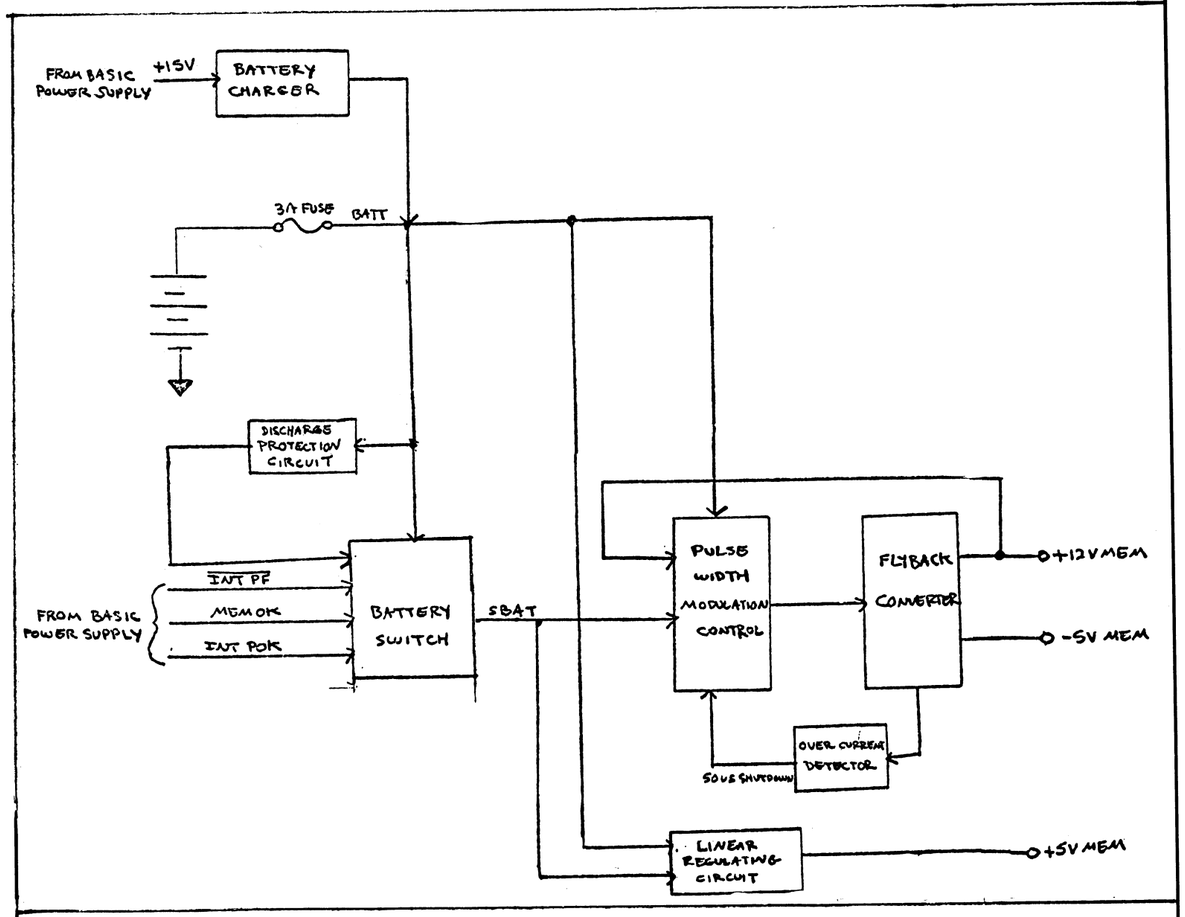


Figure 10.2 Battery Backup Block Diagram

Besides the battery, the battery backup option consists of a battery switch, a linear regulating circuit, a pulse width modulation control, flyback converter, several protection circuits, and a battery charger. Figure 10.2 shows the interconnection between these components.

Operation

The battery switch monitors the state of the $\overline{\text{INT PF}}$, the MEM OK, and the INT POK signals to determine when ac power fails and when ac power recovers. If $\overline{\text{INT PF}}$ goes to the low state when MEM OK is in the high state, power is failing. The battery switch turns on the battery to supply power (BATT) to the rest of the battery backup circuitry. When the power recovers, $\overline{\text{INT PF}}$ goes to the high state. Shortly, the voltage outputs from the basic power supply come up and cause INT POK to go to the high state. If the battery is on when the outputs recover, MEM OK is in the high state; if the battery is off, MEM OK goes to the high state. When both INT POK and MEM OK are in the high state, the battery switch turns off the battery.

The linear regulating circuit regulates the battery's output voltage to produce the +5V MEM output. This circuit is a series pass regulator with current limiting.

The pulse width modulation control governs the amount of power supplied to the flyback converter. It opens and closes the power path between the battery and the flyback converter once every 50 us (at a 20 KHz rate) and varies the ratio between the "open" time and the "closed" time (the duty cycle) in accordance with the variation on the +12V MEM output of the flyback regulator. In this way, the pulse width modulation control regulates the +12V MEM output.

The flyback converter transforms the 6V dc output from the battery into a regulated +12V MEM output and a -5V MEM output.

The over current detector is a cycle by cycle current limiter. When it detects an over current condition, it shuts down the pulse width modulation control for one cycle (50 us).

The discharge protection circuit monitors the voltage level of the battery. When it drops below 5.4 volts, the discharge protection circuit turns off the battery to prevent it from degrading.

The battery charger recharges the battery when basic power supply is operating.

INTERCONNECTION WITH SYSTEM

The 5-slot power supply board communicates with the rest of the system via the jack J1 to the backpanel. Tables 10.3 through 10.5 list each signal either generated or received by the power supply board together with the jack locations of the signal. See the 5-slot backpanel schematic, DGC No. 001-0001619, for the locations of signals on the backpanel.

Table 10.3 Voltage signals

Signal	Jack Pin	Source	Destination	Description
GND	J1 pins 1, 2, 4, 8, 35-42, 51, 52, 55-64, 79-88	Power Supply	Backpanel	Power or logic ground
+3V	J1-31, J1-32	Power Supply	Backpanel	+3V source for backpanel bus terminators
+5VA	J1 pins 91-100	Power Supply	Backpanel	+5V source
+5VB	J1 pins 67-76	Power Supply	Backpanel	+5V source
+5 MEM	J1-33, J1-34			Same as +5V if battery backup not configured
-5V	J1-27 J1-28	Power Supply	Backpanel	-5V source
-5 MEM	J1-19	Power Supply	Backpanel	Same as -5V if battery backup not configured
-11V	J1-24	Power Supply	Backpanel	EIA interface voltage
+12V	J1 pins 43-46	Power Supply	Backpanel	+12V source
+12 MEM	J1 pins 47-50	Power Supply	Backpanel	Same as +12V if battery backup not configured
+15V	J1-53, J1-54	Power Supply	Backpanel	+15V source

Table 10.4 Power supply status signals

Signal	Jack Pin	Source	Destination	Description
$\overline{\text{MEMD}}$	J1-21	Backpanel	Power Supply	Unused
MEM OK	J1-23	Power Supply	Backpanel	+5 MEM voltage ok
$\overline{\text{ONLED-P}}$	J1-11	Power Supply	Backpanel	All dc output voltages ok
$\overline{\text{PWR FAIL}}$	J1-9	Power Supply	Backpanel	Power switch off or ac power failure
PWR OK	J1-16	Power Supply	Backpanel	All ac output voltages ok

Table 10.5 Clock signals

Signal	Jack Pin	Source	Destination	Description
$\overline{\text{B10CLK}}$	J1-6	Power Supply	Backpanel	10 MHz square wave
$\overline{\text{B20CLK}}$	J1-14	Power Supply	Backpanel	20 MHz square wave
$\overline{\text{B40CLK}}$	J1-10	Power Supply	Backpanel	40 MHz square wave
$\overline{\text{ENB10CLK}}$	J1-15	Power Supply	Backpanel	10 MHz pulse train
LCLK	J1-17	Power Supply	Backpanel	50/60 Hz square wave (ac line frequency)
$\overline{\text{5 MHz CLK}}$	J1-7	Power Supply	Backpanel	5 MHz square wave
500 Hz	J1-18	Power Supply	Backpanel	500 Hz square wave

CHAPTER 11
CPU OPERATION

INTRODUCTION

The NOVA 4/C CPU board is a multi-fuctnion board consisting of a central processing unit (CPU), main memory, a virtual console, and an asynchronous communications interface. A real-time clock is optional.

CPU - governs the system's activities by executing assembly language instructions. It executes the NOVA instruction set enhanced with load and store byte instructions and, optionally, signed multiply and divide instructions. The CPU operates in two modes: run and console. In run mode, it executes instructions stored in main memory. In console mode, it executes instructions stored in the virtual console.

Main memory - provides either 32K bytes (16K words) to 64K bytes (32K words) of dynamic random access memory.

Virtual console - allows a user to examine and modify the system's state using a terminal (system terminal) connected to the resident asynchronous interface.

Asynchronous interface - a programmed I/O controller which contains both a transmitter and a receiver. It provides full-duplex communication between a serial asynchronous terminal and the CPU.

Real-time clock - an option which provides the system with four program selectable time bases.

The major units of the CPU board are interconnected by three 16-bit buses: ALUIN, ALUOUT, MBUS. The CPU board, in turn, is connected to the system controllers by the 48-line I/O bus. This bus consists of the 16-bit DATA bus, which transfers all data, plus 32 lines which carry programmed I/O, program interrupt, data channel, and system control signals. Figure 11.1 shows the interconnection of these buses and the major units of the CPU board.

CPU

The two major components of the CPU are a control processor and a data manipulation unit.

The control processor executes the NOVA 4/C instruction set by interpreting each assembly language instruction as a macroinstruction. It decodes the macroinstruction and then executes the sequence of microinstructions needed to perform the specified function. When executed, these microinstructions control the data paths and the operation of the data manipulation unit as well as the operation of main memory and input/output.

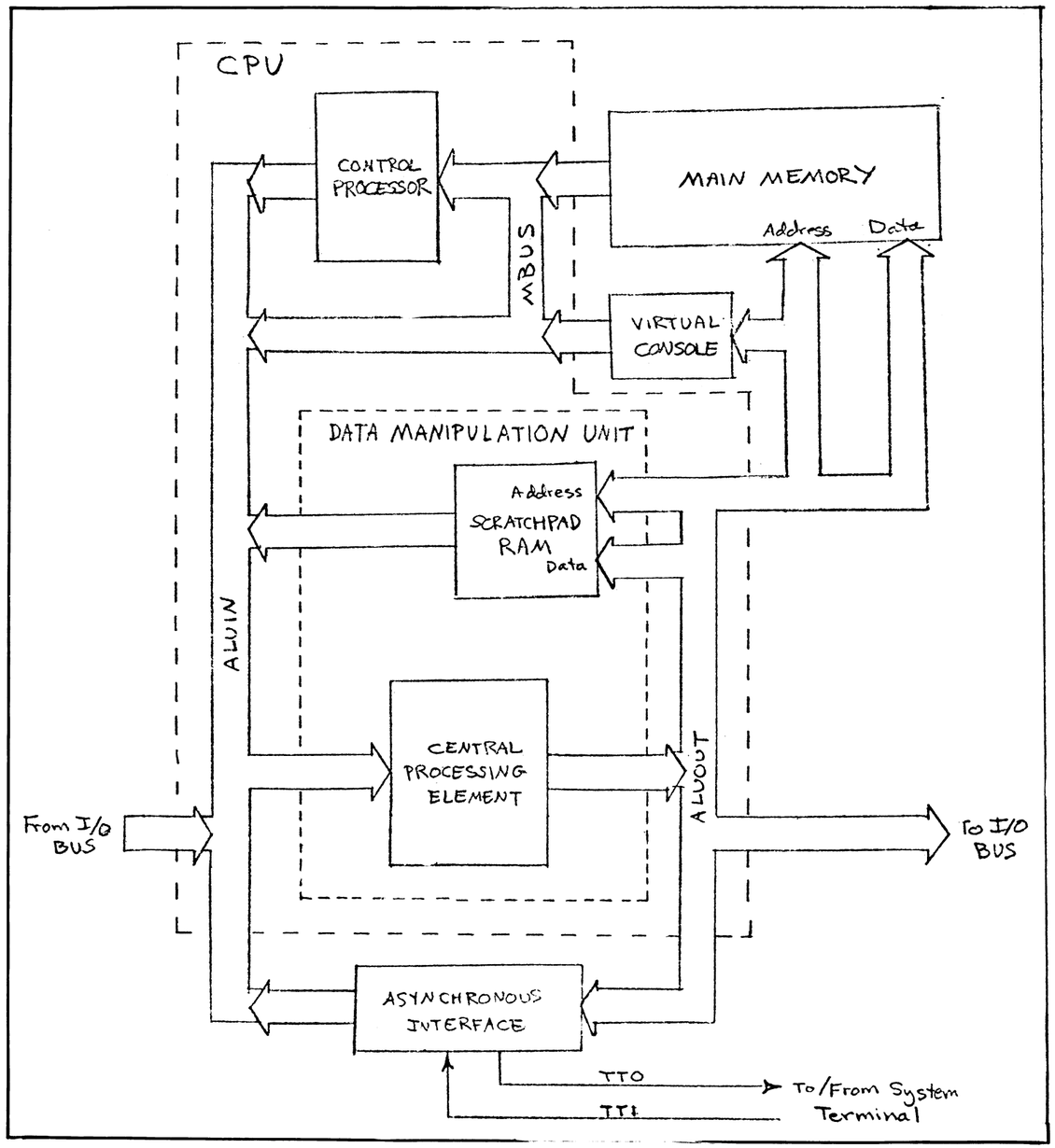


Figure 11.1 CPU Board Block Diagram

Control Processor

The control processor consists of the following major units:

- System timing logic
- Instruction register
- Starting address generator (SAGE)
- I/O and EA decode logic
- Microsequencer
- Control store
- Two microinstruction registers
- ALC decode logic
- Control decode logic
- Test logic

Figure 11.2 shows the interconnection of these units.

System Timing Logic

The system timing logic generates the following system clocks from the $\overline{\text{B40CLK}}$ (EXT40CLK) clock supplied by the power supply. (The $\overline{\text{B40CLK}}$ generated by the power supply is called EXT40CLK on the CPU board and is inverted before being used.)

- BUFACLK
- BUFBCLK
- $\overline{\text{B40CLK}}$
- 10CLK
- $\overline{\text{5CLK}}$

BUFACLK and BUFBCLK are nominally 200 ns clocks which provide the microinstruction cycle timing. BUFACLK is the complement of BUFBCLK. In other words, they are 100 ns out of phase. BUFACLK, together with $\overline{\text{B40CLK}}$, 10CLK, and $\overline{\text{5CLK}}$ provide the timing for main memory.

Instruction Register

This register stores the instructions which the control processor receives from memory in run mode and from the virtual console in console mode.

Starting Address Generator (SAGE)

The SAGE determines the starting address for the next sequence of microinstructions to be executed and supplies this address to the control store via the microinstruction sequencer. Before the control processor begins a new sequence of microinstructions, the SAGE examines the state of the service request lines listed below. These lines are listed in order of priority with a service request from the data channel having the highest priority and a service request from an instruction having the lowest priority. A non-maskable interrupt from the memory refresh logic is an exception to this priority structure. Such an interrupt takes highest priority.

1. Data channel
2. I/O or non-maskable interrupt
3. Instruction

If a service request is present, the SAGE generates the appropriate starting address for the service request with the highest priority.

I/O and EA Decode Logic

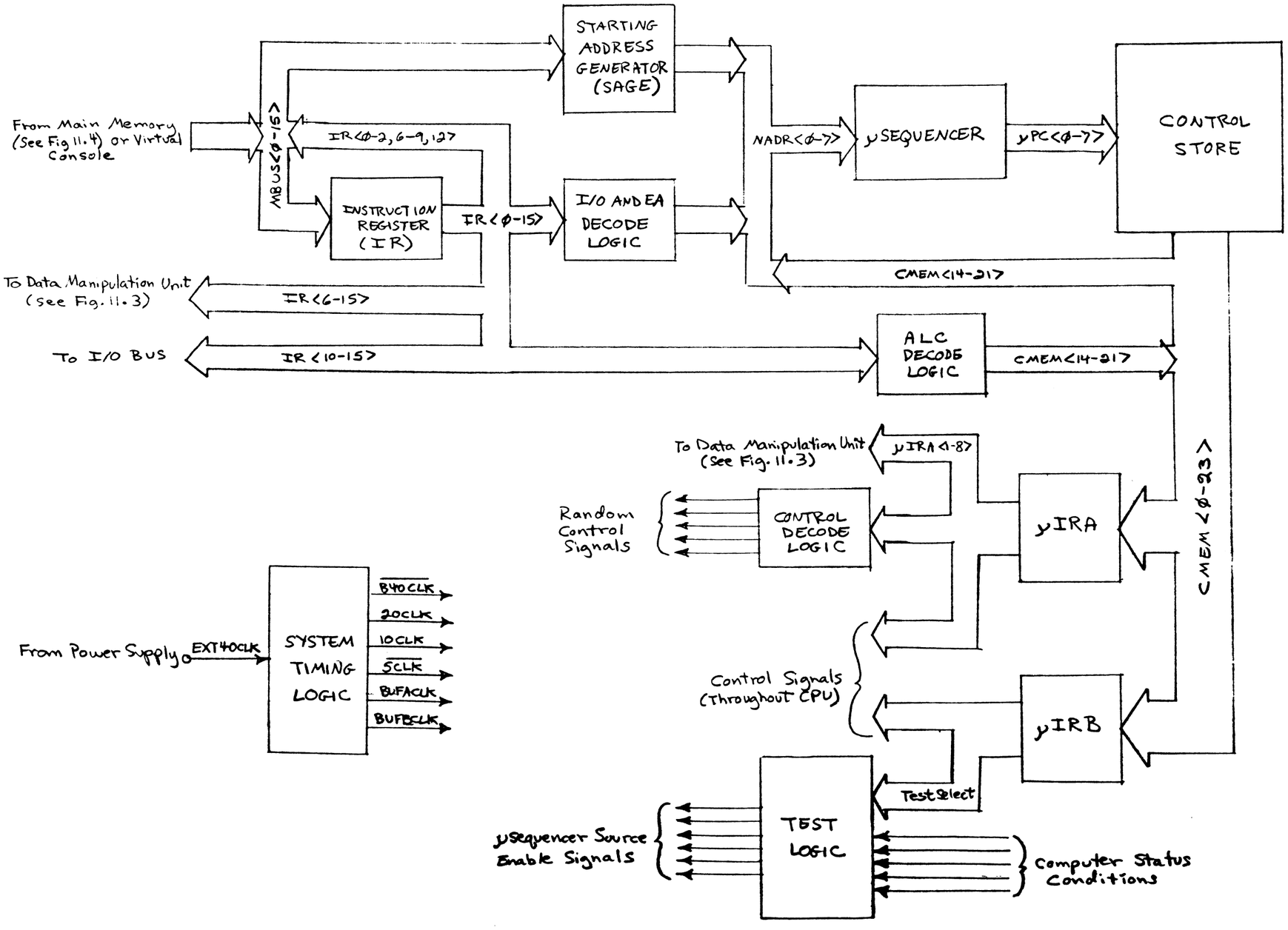
This logic supplements the decoding of I/O instructions and memory reference instructions done by the SAGE. After the SAGE selects the sequence of microinstructions needed to execute the I/O instruction or memory reference instruction, the I/O and EA decode logic determines which branch in the sequence the control processor executes. The I/O and EA decode logic supplies the starting address of this branch to the control store.

Microinstruction Sequencer

The microinstruction sequencer supplies the control store with the eight high-order address bits of the next microinstruction in the sequence to be executed.

Each microinstruction specifies a state change condition (a test) that determines what information the microinstruction register uses to generate the address. This information determines the address of the instruction "after the next instruction" to be executed. If the control processor finds that the specified condition is true, the microinstruction sequencer uses the information specified by the true field of the current microinstruction; otherwise, it uses the information specified by the false field.

Figure 11.2 Control Processor Block Diagram



Control Store

The control store contains 48-bit microinstructions stored in six 512 word by 8-bit ROMs organized in two banks (pages) of three ROMs. Each microinstruction is divided into two 24-bit parts - an A half and a B half. These halves are stored in two consecutive ROM locations and are selected by the address supplied by the microinstruction sequencer together with BUFACLK (BUFACLK supplies the low-order address bit). The control store sends the addressed microinstruction to the microinstruction registers via the CMEM bus.

Microinstruction Registers

Two microinstruction registers, the uIRA and the uIRB, each store half of the microinstruction currently being executed. When the control store receives the address of a microinstruction, it sends the A half of the microinstruction to the uIRA, and 100 ns later, it sends the B half to the uIRB. The uIRA distributes the control information contained in the A half to the data manipulation unit, the control decode logic, and various other components on the CPU board. This information governs the flow of data throughout the system. The uIRB distributes the control information contained in the B half to the test logic and to various other components in the control processor. This information governs the order in which the microinstructions are executed.

ALC Decode Logic

This logic decodes bits 5-9 and 12 of an arithmetic-logic (ALC) instruction and sends the results to the uIRA register via the CMEM bus. These results replace the 10-high order bits of the A-half of the current microinstruction.

Control Decode Logic

This logic decodes portions of the microinstruction stored in the uIRA to produce control information which governs the flow of data throughout most of the major components on the CPU board.

Test Logic

This logic determines if the state change condition (test) specified by the current microinstruction is true or false. It uses information supplied by the control store, the uIRB, the data manipulation unit, and the CPU logic governing the virtual console and I/O operations.

Data Manipulation Unit

The data manipulation unit performs arithmetic and logical functions on the data designated by the current microinstruction. It consists of the following major components:

- Central processing element
- Memory address register
- Read data register
- Write data register
- Scratchpad RAM

Figure 11.3 shows the interconnection of these components.

Central Processing Element

The central processing element consists of four 4-bit microprocessor slices which are cascaded to form a 16-bit unit. The major sections of the central processing element are: a high-speed arithmetic/logic unit (ALU) and a 16 word by 16-bit register file. The register file contains sixteen registers including the following program-accessible registers: the four accumulators, the stack pointer, and the frame pointer.

The register file has two ports: A and B. Data in any of its registers can be read from the A-port using the 4-bit A address provided by the A-port address logic, REGA<0-3>. Similarily, data in any of the above 16 registers can be read from the B-port using the 4-bit B address provided by the B-port address logic, REGB<0-3>. When enabled, new data is always written into the register specified by the B address.

The high speed ALU performs arithmetic and logical operations on the two 16-bit inputs designated R and S. The R input field is driven by a 2-input multiplexor while the S input field is driven by a 3-input multiplexor. The operation performed by the ALU is specified by information supplied by uIRA<14-22>.

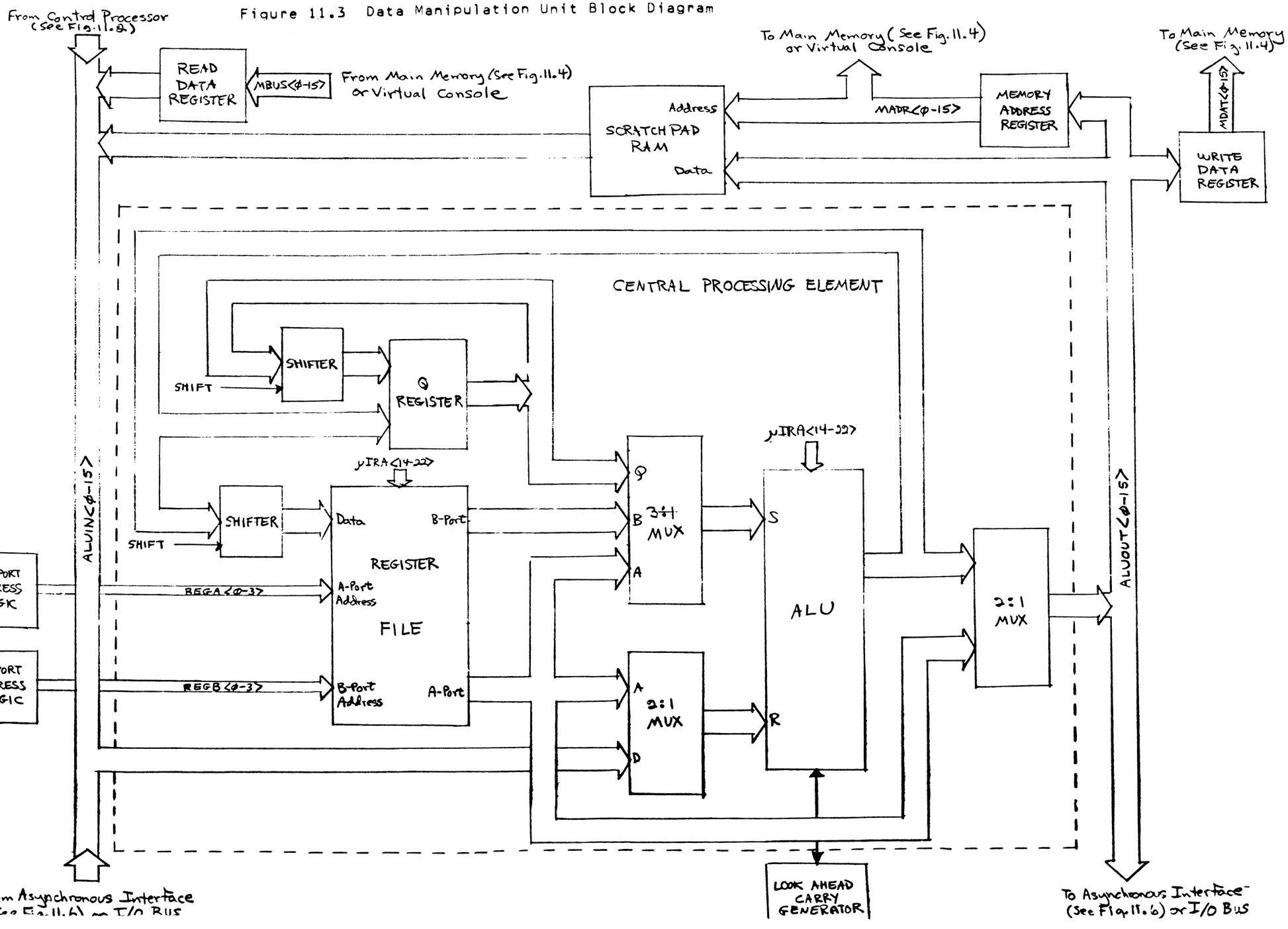
The look-ahead carry generator is a support component for the central processing element.

Memory Address Register

This register stores the 15-bit address for the main memory and the virtual console and the 4-bit address for the scratchpad RAM. It receives the address from the control processing element via the ALUOUT bus and sends it to main memory, the virtual console, or the scratchpad RAM via the MADR bus.

When the battery backup option operates, the row address section of the memory address register functions as a counter and supplies the row addresses for memory refreshing.

Figure 11.3 Data Manipulation Unit Block Diagram



Write Data Register

This register stores the 16-bit data word to be written into main memory. It receives the data word from the control processing element via the ALUOUT bus and sends it to main memory via the MDAT bus.

Read Data Register

This register stores the 16-bit data word read from main memory or the virtual console. It receives the data word from main memory or the virtual console via the MBUS.

Scratchpad RAM

This RAM provides 256-words of temporary storage which is used for various purposes. It provides:

- Storage during console mode
- Program-accessible data switch register
- Buffers for data transfers between accumulators and the resident asychronous interface
- Counter for the real-time clock option.

MAIN MEMORY

The major component of main memory is a dynamic RAM array which is located on the CPU board. RAM arrays are available with either 32K bytes (16K words) or 64K bytes (32K words). Both arrays use 16,384 x 1 bit RAM elements.

The 32K byte array contains one bank (bank 0) of 16 RAM elements while the 64K byte array contains two banks (bank 0 and bank 1) each having 16 RAM elements.

The control processor in the CPU initiates all main memory operations, including memory refresh operations except during battery backup.

Architecture

In addition to the RAM array, main memory contains:

- Memory timing logic
- Row and column select logic
- Row address logic
- Column address logic
- Address gate
- Memory bus driver

Figure 11.4 shows the interconnection of these components.

Memory Operations

The memory carries out three operations: read, write, and refresh. The CPU starts each of these operations. The CPU starts a read or write operation in main memory when either the current microinstruction specifies such an operation or the SAGE decodes an ALC instruction. In the case of an ALC instruction, the CPU starts a read operation to fetch the next instruction so that the CPU can maintain an instruction execution time of 400 ns. The CPU starts a refresh operation approximately every 12.8 us, except when the battery backup option is being switched off or on. In this case, the CPU begins a burst refresh operation.

Row and Column Selection

A read or write operation begins in the data manipulation unit. First, the control processing element sends the 15-bit address to the memory address register via ALUOUT<1-15>. This address contains the bank select bit and the row and column address as shown in Figure 11.5

The memory address register latches the address and places it on the MADR bus and the ROW6 and COL5 lines. Meanwhile, the memory timing logic enables the row address gate by driving ROW to the high state. As a result, when the address appears on the MADR bus, the row address bits (MADR<10-15> and ROW 6) pass through the row address gate to the address gate and from there to the RAM array.

Figure 11.4 Main Memory Block Diagram

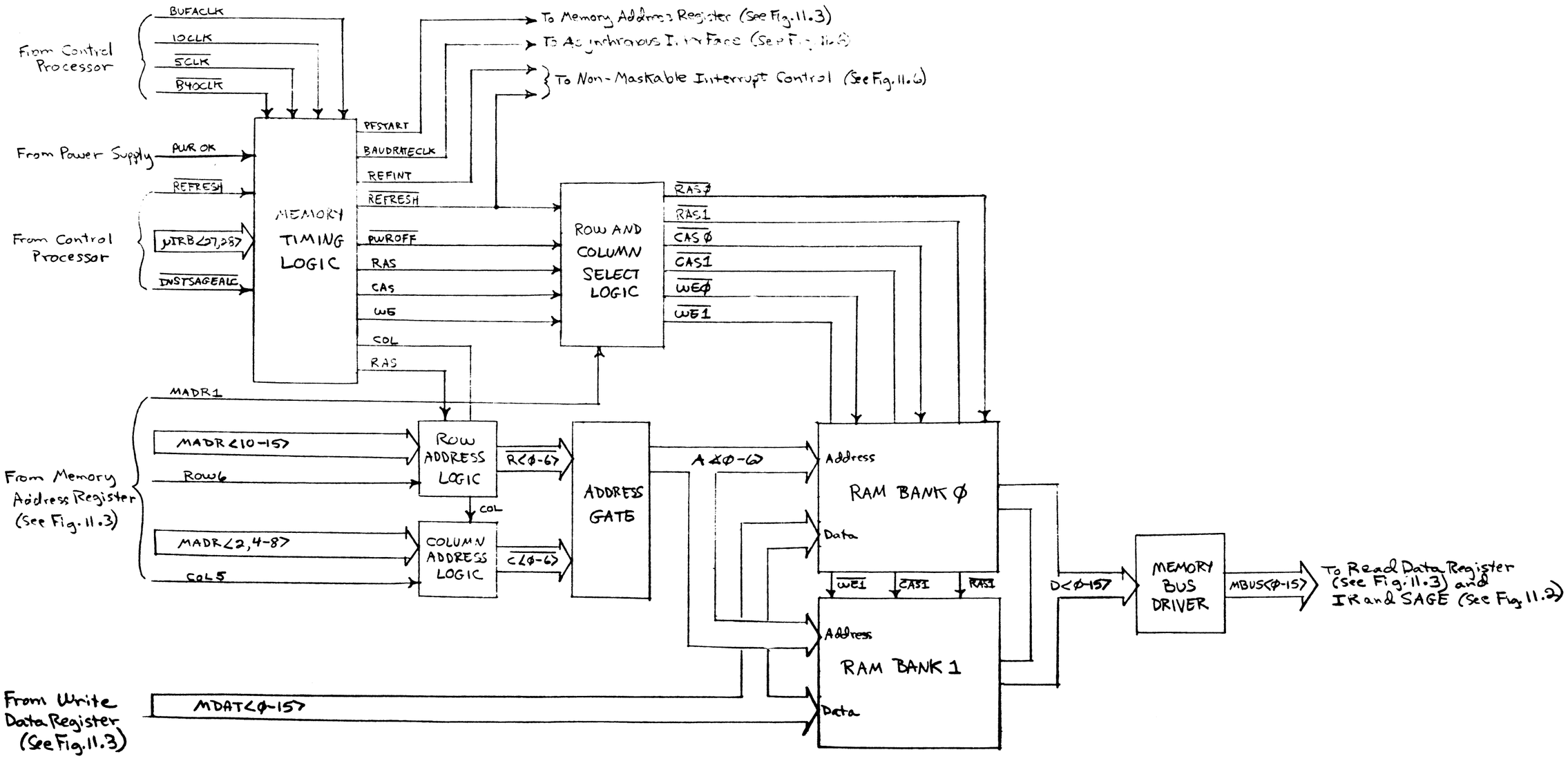
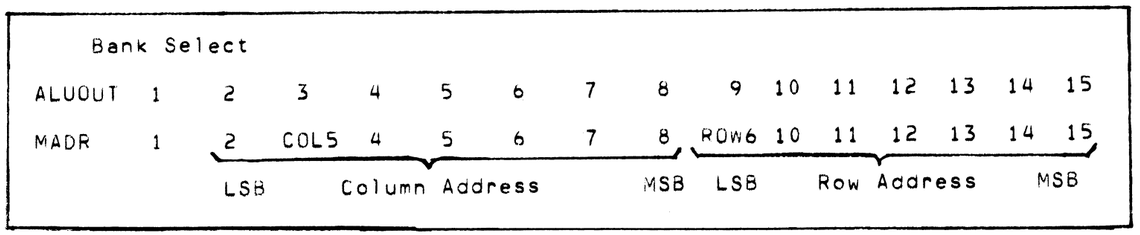


Figure 11.5 Meaning of memory address bits



When the memory timing logic drives RAS to the high state, the row and column select logic uses the high-order address bit, MADR1, to select the appropriate RAM bank. If MADR1 is in the low state, the row and column select logic drives $\overline{RAS0}$ to the low state; otherwise, it drives $\overline{RAS1}$ to the low state. The low state of $\overline{RAS0}$ latches the row address into bank 0; whereas, the low state of $\overline{RAS1}$ latches the row address into bank 1. When a 32K byte memory is addressed, MADR1 is always in a low state; and, consequently, the row address is always latched into bank 0.

Soon after the row address is latched into the appropriate bank, the memory timing logic disables the row address gate and enables the column address gate. As soon as the column address gate is enabled, the column address bits (MADR<2,4-8> and COL5) pass through the column address gate to the address gate and from there to the RAM array.

When the memory timing logic drives CAS to the high state, the row and column select logic drives both $\overline{CAS0}$ and $\overline{CAS1}$ to the low state. The low state of $\overline{CAS0}$ latches the column address into bank 0 and the low state of $\overline{CAS1}$ latches the column address into bank 1. $\overline{CAS0}$ and $\overline{CAS1}$ cannot go to the low state when the CPU is refreshing memory or when a power failure occurs.

Read

When uIRB27 is driven to the high state and uIRB28 to the low state, main memory begins a read operation. The memory timing logic drives WE to the low state and sends it to the row and column select logic. This logic then drives $\overline{WE0}$ and $\overline{WE1}$ to the high state to enable reading the RAM array. When the column address is latched into the RAM array, the array places the data in the addressed location on the D<0-15> lines. From there, the data is driven onto MBUS<0-15> by the memory bus driver.

Next the data is latched into the read data register in the data manipulation unit. The read data register sends the data to the data processing element via ALUIN<0-15>.

Appendix D shows the timing for a read operation.

Write

Before the CPU starts a write operation, the control processing element sends the data to the write data register via ALUOUT<0-15> and it sends the address to the memory address register. The write data register supplies the data to the RAM array via MDAT<0-15>.

When both uIRB27 and uIRB28 are driven to the high state, main memory begins a write operation. The memory timing logic drives WE to the high state and sends it to the row and column select logic. This logic then drives $\overline{WE0}$ and $\overline{WE1}$ to the low state to enable writing the RAM array. When the column address is latched into the RAM array, the array writes the data on MDAT<0-15> into the addressed location.

Appendix D shows the timing for a write operation.

Refresh

Main memory carries out three refresh operations: normal, burst, and battery. Each normal and battery refresh operation refreshes one row in both banks of the RAM array whereas each burst refresh operation refreshes all the rows in the RAM array.

During normal operation, the memory timing logic starts a normal refresh operation approximately every 12.8 us. It starts the operation by changing the state of REFINT to generate a refresh interrupt request. This interrupt request causes a non-maskable interrupt which is serviced as soon as the control processor finishes executing the current sequence of microinstructions.

When the interrupt is serviced, the control processing element places the address of the row to be refreshed on the ALUOUT bus. This address is latched into the memory address register and passed to main memory via the MADR bus. Main memory selects the addressed row in the RAM array in the same way it selects a row during a read or write operation. Column selection is disabled and both banks are enabled.

When the battery backup option switches on, and again, when it switches off, the control processor starts a burst refresh operation to ensure that all the rows are refreshed within 2 ms.

At the start of a burst refresh operation, the control processing element places the address of the row to be refreshed on the ALUOUT bus. This address is latched into the memory address register and passed onto main memory. Main memory carries out the refresh operation in the same way it carries out a normal refresh operation. The control processor places the address of the next row on the ALUOUT bus 400 ns after it sent out the first row address. It continues to send out a new row address every 400 ns until all the rows have been refreshed.

Between these two burst refreshes, while the battery backup operates, the memory timing logic starts a battery backup refresh operation every 12.8 us. During this time, the memory address register provides the row addresses for the refresh operations. The row address section of this register is actually a presettable counter; however, it only functions as a counter during a power failure.

At the beginning of a battery refresh, the memory timing logic drives PFSTART to the high state to start the refresh operation. When PFSTART goes to the low state, the memory address register increments the row address by one. The register supplies this address to main memory via the MADR bus. Main memory carries out the refresh operation in the same way it carries out a normal refresh operation.

Appendix D shows the timing for the refresh operations and a refresh interrupt.

VIRTUAL CONSOLE

The virtual console resides in a 512-word by 16-bit ROM. This ROM also contains the assembly language instructions needed to implement the computer self-test. The memory address register provides addresses to this ROM via the MADR bus.

When the control processor operates in console mode, the virtual console ROM supplies the instructions which the control processor executes. When the virtual console ROM is enabled, it sends instructions to the IR and the SAGE via the MBUS. Data from the virtual console ROM goes to the read data register. The virtual console can access main memory by temporarily enabling the RAM array to use the MBUS.

ASYNCHRONOUS INTERFACE AND REAL-TIME CLOCK

The asynchronous interface is a programmed I/O controller which provides full-duplex communications between the CPU and a serial, asynchronous terminal via either a 20mA current loop or an EIA RS-232C communications line.

The major component of the interface is a Universal Asynchronous Receiver/Transmitter (UAR/T). The interconnection between the UAR/T and the rest of the components of the interface is shown in Figure 11.6.

The UAR/T, which contains both a transmitter and receiver, is the communications link between the interface and the terminal. Jumpers select its line characteristics. The BAUDRATECLK clock from the memory timing logic provides the baud rate. The frequency of this clock is selected by a jumper in the memory timing logic. BAUDRATECLK supplies the UAR/T's transmitter and receiver clock inputs.

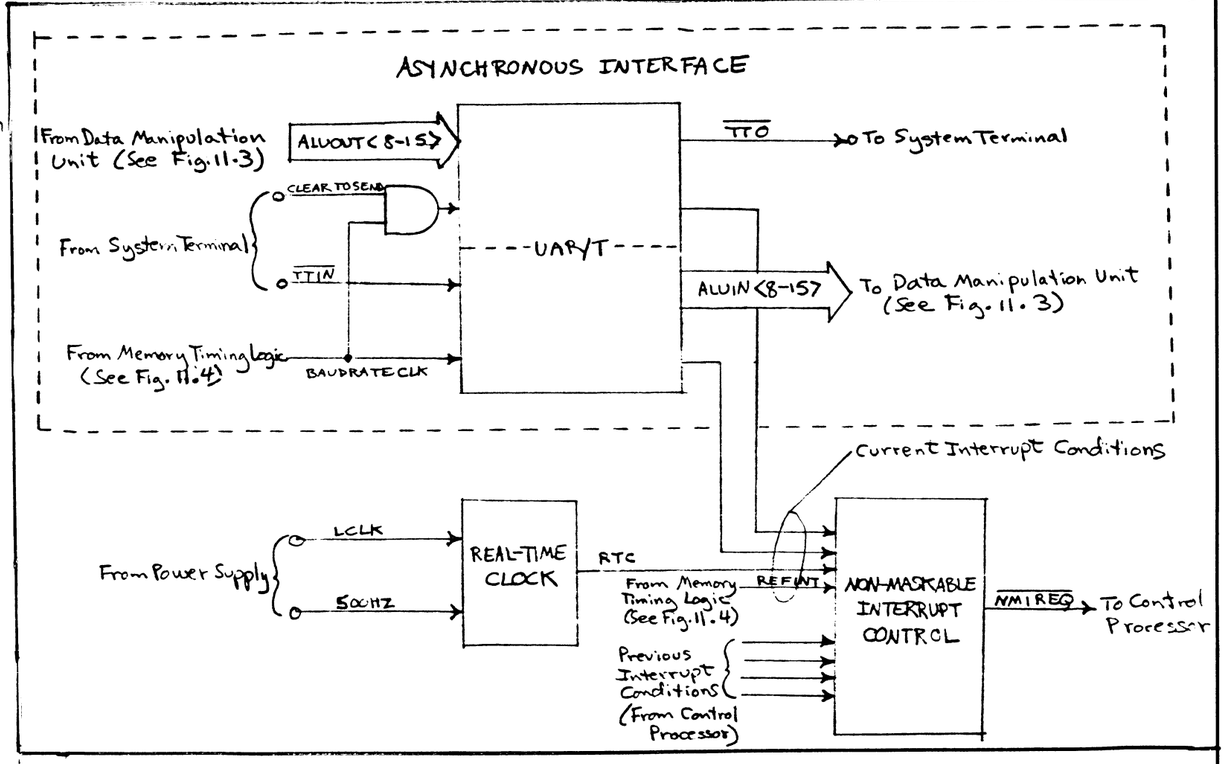
When communicating with the terminal, the UAR/T transmits and receives character codes in serial form. When communicating with the CPU under program control, the UAR/T's transmitter receives data in parallel form from the ALUOUT bus and the receiver places data in parallel form on the ALUIN bus.

The modem control signal, Clear to Send, is connected to the UAR/T's transmitter clock input line and inhibits data transmission when at the low state.

The real-time clock option provides four program-selectable time bases: power line frequency, 10 Hz, 100 Hz, and 1000 Hz.

Both the interface and the real-time clock option use a non-maskable interrupt control which is independent of the standard I/O interrupt facility. The Busy and Done flags and the priority mask bits for these devices are located in the I/O flag register, which resides in the data manipulation unit.

Figure 11.6 Asynchronous Interface and Real-Time Clock Block Diagram



The non-maskable interrupt control compares previous interrupt conditions (which are stored in the RF register in the control processor) with current interrupt conditions. Whenever a current condition differs from the corresponding previous condition, the interrupt control generates a non-maskable interrupt. Next, the control processor equalizes both sets of interrupt conditions so the interrupt control can detect future interrupt conditions. An interrupt condition occurs when main memory generates a refresh interrupt request, the interface receives a start bit, the receiver buffer contains a character, the transmitter buffer is empty, or the real-time clock changes state.

INTERCONNECTION WITH SYSTEM

The CPU board communicates with the rest of the system via its A and B connectors to the backpanel. Tables 11.1 through 11.9 list each signal either generated or received by the CPU board together with the backpanel location of the signal.

Table 11.1 Clock signals

Signal	Backpanel Pin	Source	Destination	Description
$\overline{\text{B40CLK}}$ (EXT40CLK)	A36	Power Supply	CPU	40 MHz square wave
LCLK	A88	Power Supply	CPU	50/60 Hz square wave (AC line frequency)
500HZ	A90	Power Supply	CPU	500 Hz square wave

Table 11.2 Memory control signals

Signal	Backpanel Pin	Source	Destination	Description
MEMOK	A96	Power Supply	CPU	+12MEM voltage OK
$\overline{\text{MEMDIASTER}}$	B96	CPU	Power Supply	Failure on -5MEM

Table 11.3 Data channel and interrupt signals *

Signal	Backpanel Pin	Source	Destination	Description
$\overline{\text{DCHA}}$	A60	CPU	I/O	Data channel acknowledge
DCHI	B37	CPU	I/O	Data channel input
DCHO	B33	CPU	I/O	Data channel output
$\overline{\text{DCHMO}}$	B17	I/O	CPU	Data channel mode select
$\overline{\text{DCHR}}$	B35	I/O	CPU	Data channel request
FASTDCH	A95	CPU	I/O	High speed device
INTA	A40	CPU	I/O	Interrupt acknowledge
$\overline{\text{INTR}}$	B29	I/O	CPU	Interrupt request
$\overline{\text{MSKO}}$	A38	CPU	I/O	Mask out
$\overline{\text{RQENB}}$	B41	CPU	I/O	Request synchronizing clock
$\overline{\text{SELB}}$	A82	I/O	CPU	Selected device busy
$\overline{\text{SELD}}$	A80	I/O	CPU	Selected I/O device done

* See "Interface Designer's Reference" (DGC No. 015-000031) for more information on how the I/O signals function.

Table 11.4 I/O device code *

Signal	Backpanel Pin	Source	Destination	Description
$\overline{DS0}$	A72	CPU	I/O	Device select bit 0
$\overline{DS1}$	A68	CPU	I/O	Device select bit 1
$\overline{DS2}$	A66	CPU	I/O	Device select bit 2
$\overline{DS3}$	A46	CPU	I/O	Device select bit 3
$\overline{DS4}$	A62	CPU	I/O	Device select bit 4
$\overline{DS5}$	A64	CPU	I/O	Device select bit 5

* See the "Interface Designer's Reference" (DGC No. 015-000031) for more information on how the I/O signals function.

Table 11.5 I/O function signals *

Signal	Backpanel Pin	Source	Destination	Description
CLR	A50	CPU	I/O	Clear
DATIA	A44	CPU	I/O	Data in A
DATIB	A42	CPU	I/O	Data in B
DATIC	A54	CPU	I/O	Data in C
DATOA	A58	CPU	I/O	Data out A
DATOB	A56	CPU	I/O	Data out B
DATOC	A48	CPU	I/O	Data out C
IORST	A70	CPU	I/O	I/O reset
IOPLS	A74	CPU	I/O	I/O pulse
STRT	A52	CPU	I/O	Start

* See "Interface Designer's Reference" (DGC No. 015-000031) for more information on how the I/O signals function.

Table 11.6 I/O data bus signals *

Signal	Backpanel Pin	Source	Destination	Description
$\overline{DATA0}$	B62	CPU I/O	I/O CPU	High-order data bit
$\overline{DATA1}$	B65	CPU I/O	I/O CPU	Data bit
$\overline{DATA2}$	B82	CPU I/O	I/O CPU	Data bit
$\overline{DATA3}$	B73	CPU I/O	I/O CPU	Data bit
$\overline{DATA4}$	B61	CPU I/O	I/O CPU	Data bit
$\overline{DATA5}$	B57	CPU I/O	I/O CPU	Data bit
$\overline{DATA6}$	B95	CPU I/O	I/O CPU	Data bit
$\overline{DATA7}$	B55	CPU I/O	I/O CPU	Data bit
$\overline{DATA8}$	B60	CPU I/O	I/O CPU	Data bit
$\overline{DATA9}$	B63	CPU I/O	I/O CPU	Data bit
$\overline{DATA10}$	B75	CPU I/O	I/O CPU	Data bit
$\overline{DATA11}$	B58	CPU I/O	I/O CPU	Data bit
$\overline{DATA12}$	B59	CPU I/O	I/O CPU	Data bit
$\overline{DATA13}$	B64	CPU I/O	I/O CPU	Data bit
$\overline{DATA14}$	B56	CPU I/O	I/O CPU	Data bit
$\overline{DATA15}$	B66	CPU I/O	I/O CPU	Low-order data bit

Table 11.7 Front console signals

Signal	Backpanel Pin	Source	Destination	Description
CONRSTH	B51	Front Console	CPU	From front console reset switch
CONLED	B49	CPU	Front Console	CPU in run mode
CONPL	B48	Front Console	CPU	Program load from device selected by CPU program load jumper register
CONLOCK	B40	Front Console	CPU	CPU and power supply locked
CONRSTL	B52	Front Console	CPU	From front console reset switch
PWROK	A4	Power Supply	CPU	DC voltages ok

Table 11.8 Asynchronous interface signals

Signal	Backpanel Pin	Source	Destination	Description
CLEARTOSEND	A93	System Console	CPU	System console ready to receive data
ITTO	A83	CPU	System Console	+15V current loop voltage
READERRUN	A89	CPU	System Console	Start reader
TTIN	A94	System Console	CPU	Serial input
TTOUT	A85	CPU	System Console	Serial output

* See "Interface Designer's Reference" (DGC No.015-000031) for more information on how the I/O signals function.

Table 11.9 Voltage signals (from power supply board)

Signal	Backpanel Pins
GND	A1, A2, A99, A100 B1, B2, B99, B100
+5MEM	B93, B94
-5MEM	B91
+5V	A3, A4, A97, A98 B3, B4, B97, B98
+15V	A10
+12MEM	B70, B71,B72
+12V	B87, B88, B90
-11V	B77

CHAPTER 12
REMOVING AND INSTALLING FRUS

INTRODUCTION

This chapter gives step by step instructions for removing and installing the FRUs. Please abide by the following in all procedures:

- Metric tools must be used in all the procedures.
- Extreme caution must be used in procedures that involve opening the power supply units. After powering down the system, you must wait AT LEAST 5 MINUTES before proceeding with the replacement.
- Do not attempt to remove or replace any component not included in these procedures.

Fourteen procedures are described in the order listed below.

1. Front Panel Replacement
2. Fan and Fan Module Replacement for 16-Slot Chassis
3. Fan Replacement for 5-Slot Chassis
4. Console PC Board Replacement for 16-Slot Chassis
5. Console PC Board Replacement for 5-Slot Chassis
6. PC Board Replacement
7. CPU Board Replacement
8. Power Supply PC Board Replacement
9. VNR Unit Replacement
10. Paddleboard and Terminator Replacement
11. 16-Slot Wiring Harness Replacement
12. 5-Slot Wiring Harness Replacement
13. Backpanel Replacement for 16-Slot Chassis
14. Backpanel Replacement for 5-Slot Chassis

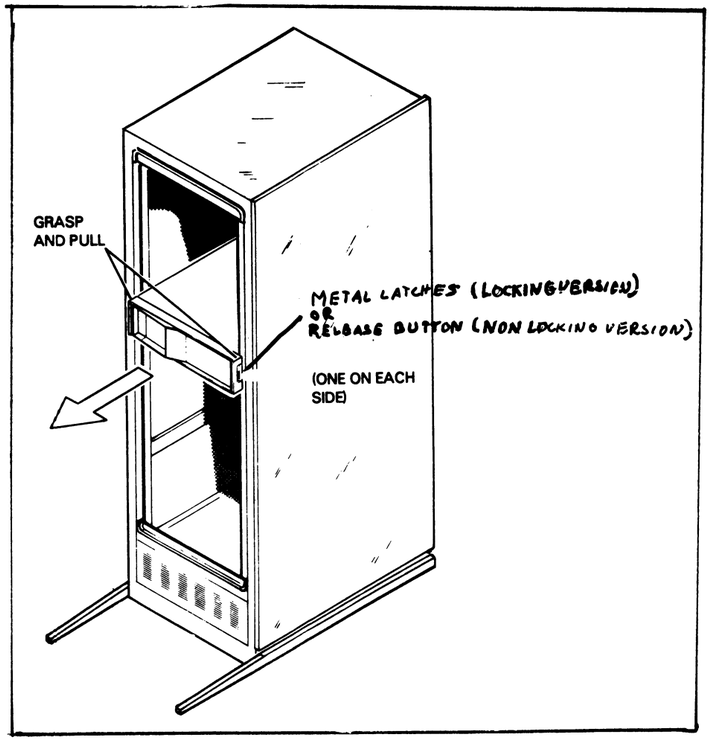
FRONT PANEL REPLACEMENT

There are two versions of the front panel assemblies, locking and nonlocking.

1. To remove a locking front panel, find the metal latch located at the center of each side of the front panel. Using a screw driver, push them in towards each other. This will release the latches and allow the front panel to be pulled off.

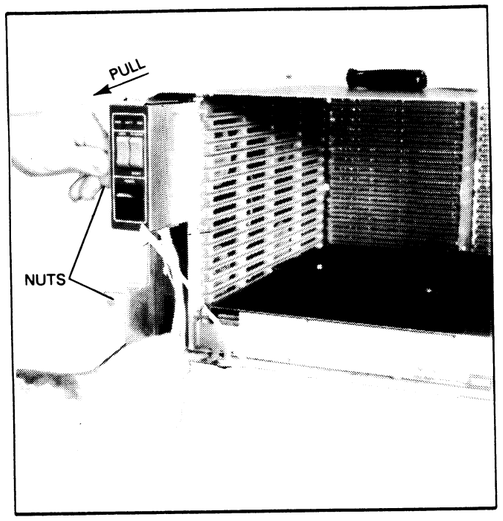
   To remove a nonlocking front panel, find the release button located at the center of each side of the front panel. Push them in towards each other and remove the front panel.

2. To replace the either a locking or nonlocking front panel, line up the guide pins and push until it locks in place.

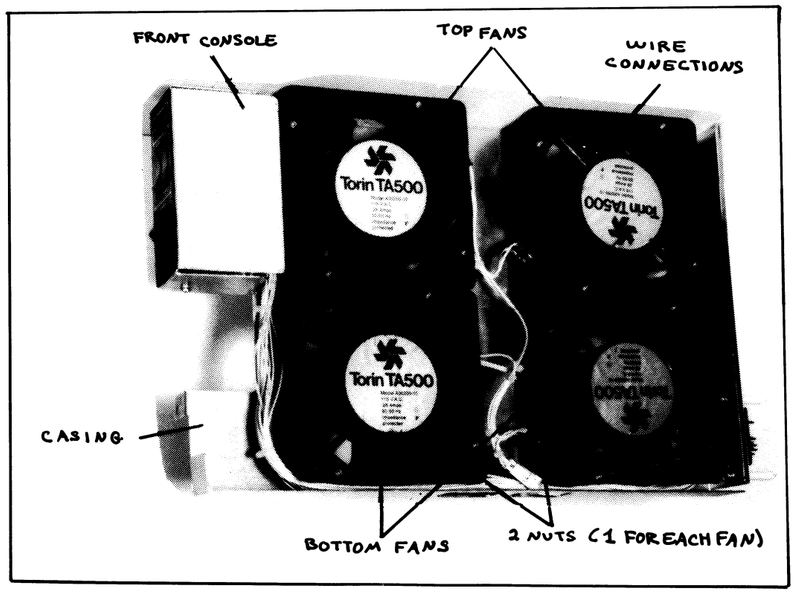


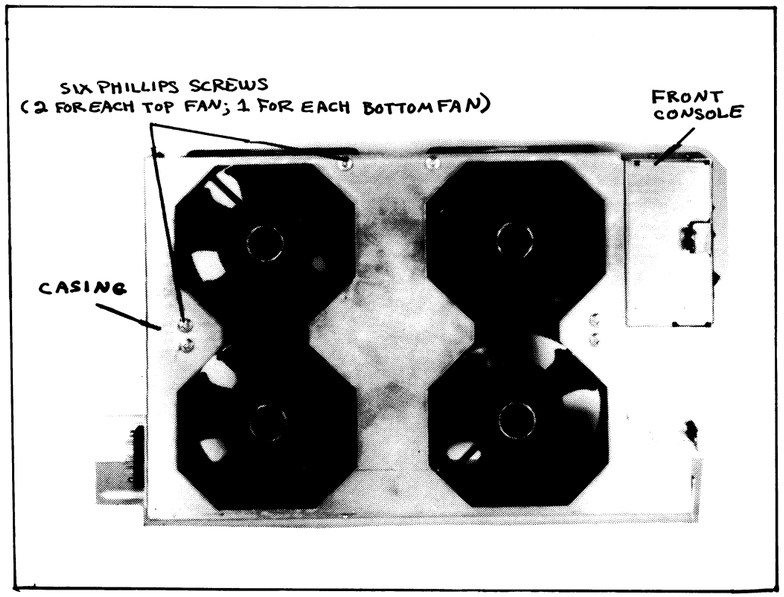
FAN AND FAN MODULE REPLACEMENT FOR 16-SLOT CHASSIS

1. Power down the system.
2. Remove the front panel. (See Front Panel Replacement procedure.)
3. Remove 2 nuts with lock washers located to the left of the console switches.
4. Grasp the fan module at the top and bottom and pull out.



5. To remove a fan:
   a. Place the fan on a table with the fan side up.
   b. Disconnect the two wires from the faulty fan. Note the position of the wire connectors on the fan so you can install the new fan in the same position.
   c. If the fan is a bottom fan, remove the nut, lock washer, and the washer on the stud holding the fan to the casing.
   d. Turn the module over and remove the self-tapping screw(s) holding the fan to the casing. (1 screw for a bottom fan; 2 screws for a top fan.)
   e. Carefully lift the fan module up. The faulty fan should remain on the table.
   f. Install the new fan. If it is a bottom fan, make sure it is on the stud properly, and then replace the washer, locking washer, and the nut.
   g. Carefully turn the module on its side, holding the new fan to make sure it stays in the correct position.
   h. Replace the self-tapping screw(s) which hold the fan to the casing. (1 screw for a bottom fan; 2 screws for a top fan).
   i. Reconnect the 2 wires to the new fan.





6. To replace the fan module:

   a. Remove the 3 screws on the console PC board assembly. (See the replacement procedure for the console PC board on the 16-slot chassis.)

   b. Remove the console PC board assembly. (See the replacement procedure for the console board on the 16-slot chassis.)

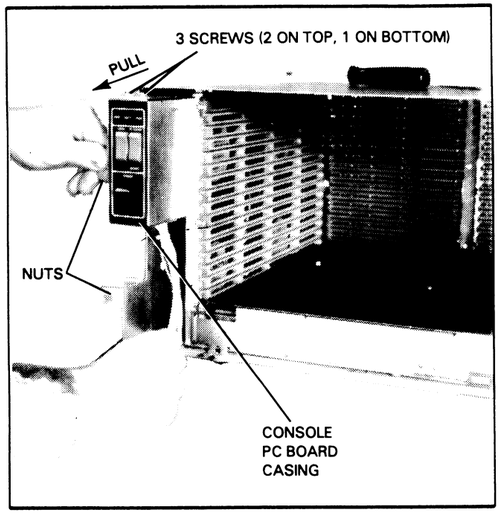
   c. Remove the console PC board casing from the new fan module.

   d. Install the console PC board in the casing of the new fan module. Replace the casing.

7. Slide the module in and push until it locks in place.

8. Replace the 2 nuts and lock washers.

9. Replace the front panel and power up the system.

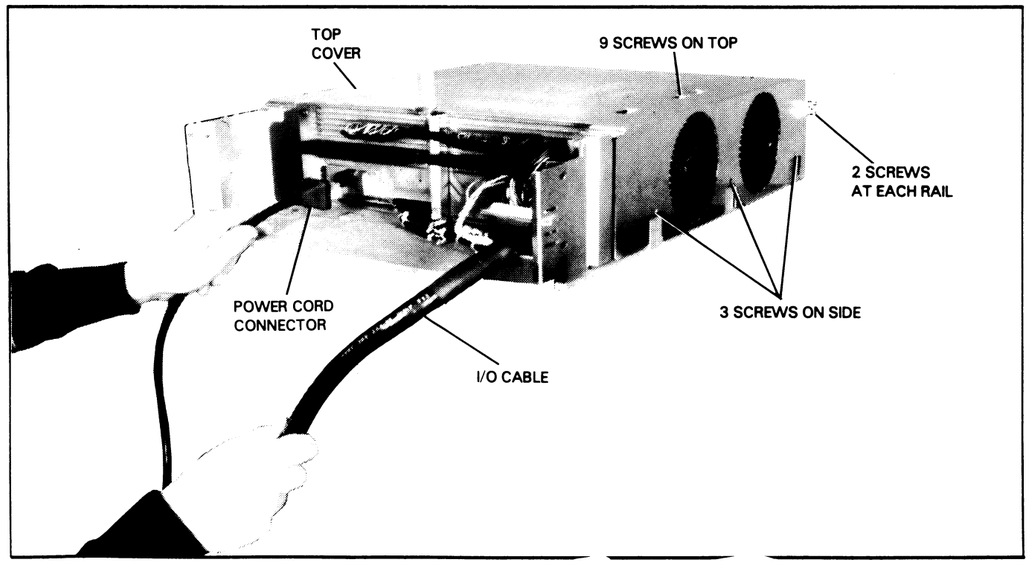


FAN REPLACEMENT FOR 5-SLOT CHASSIS

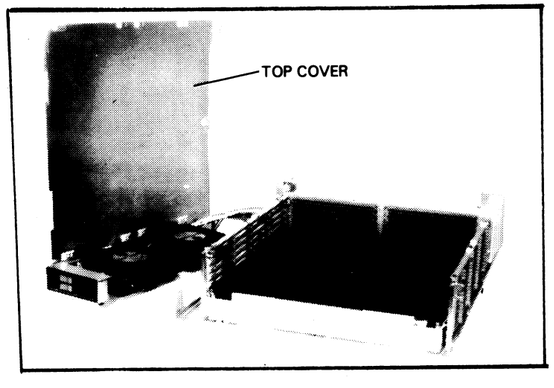
1. Power down the system, open the rear cabinet door, and unplug the ac source from the cabinet.
2. Remove the power cord connector and any I/O cables.
3. Remove the front panel. (See the Front Panel Replacement procedure.)
4. Remove the 8 screws which secure the chassis to the cabinet rails; there are 2 screws per rail.
5. Slide the chassis out from the front of the cabinet. The slides will support the chassis until it is about half way out of the cabinet.

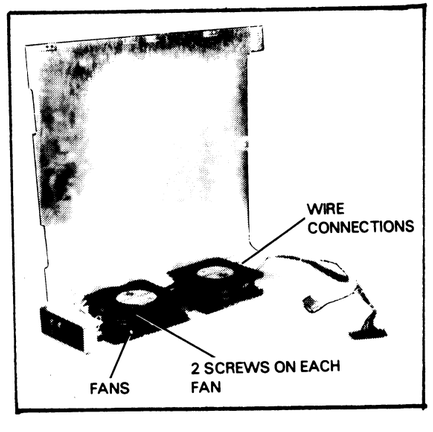
   CAUTION: The chassis weighs about 50 lbs (about 23 kgs) fully loaded. You may need help.

6. Place the chassis on a secure table.
7. Remove the top cover (9 screws on the top and 3 screws on the left or fan side).



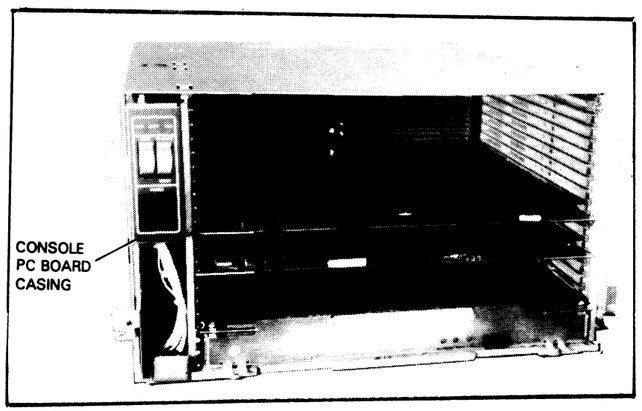
8. Lift the top cover up and over to the left so that it lies on its side. (See photo below.)
9. Disconnect the wires from the faulty fan that connect it to the power supply. Note the color scheme so you can replace them correctly.
10. Remove the 2 screws holding the fan to the cover and remove the fan.
11. Install the new fan and replace the 2 screws.
12. Reconnect the wires. (See the 5-Slot Wiring Harness Replacement procedure for the correct wire color scheme if necessary.)
13. Place the cover back in position over the chassis and replace the screws (9 on the top and 3 on the side).
14. Slide the chassis back into the front of the cabinet.
15. Replace the 8 screws which secure the chassis to the cabinet rails; there are 2 screws per rail.
16. Replace the front panel.
17. Replace the power cord connector at the rear, and replace all I/O cables.
18. Plug in the ac source, close the rear cabinet door, and power up the system.

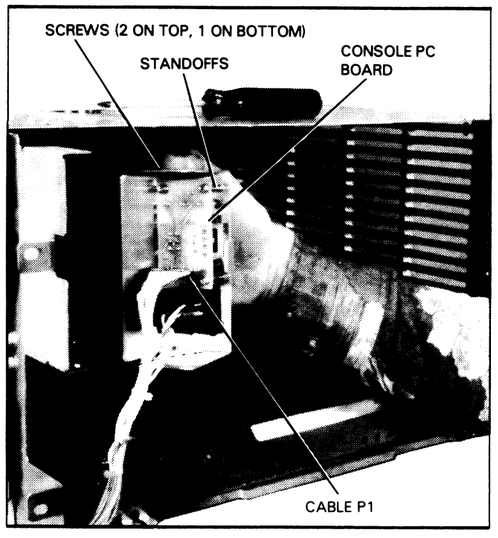




CONSOLE PC BOARD REPLACEMENT FOR 16-SLOT CHASSIS

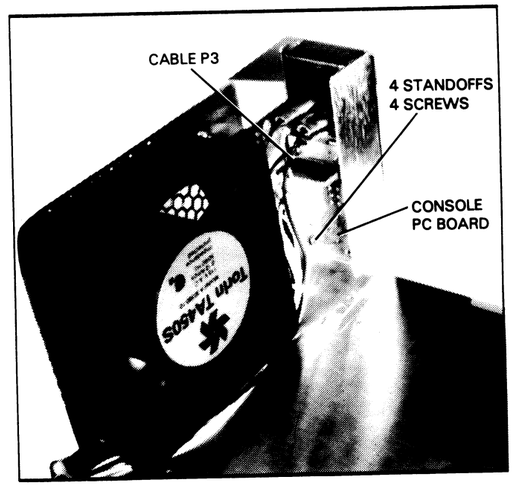
1. Power down the system and remove the front panel. (See Front Panel Replacement procedure.)
2. Remove the fan module. (See Fan and Fan Module Replacement procedure steps 3-4.)
3. Remove 3 screws, 2 on the top of the console PC board casing and 1 on the bottom. (Each screw has 1 lock washer.)
4. Unplug cable P1 on the back of the console PC board.
5. Remove the 4 screws which mount the PC board to its stand-offs. (Each screw has 2 lock washers.)
6. Mount the new PC board and replace the screws and lock washers.
7. Plug cable P1 into the new PC board.
8. Replace the 3 screws and lock washers on the PC board casing.
9. Replace the fan module and the front cover.





CONSOLE PC BOARD REPLACEMENT FOR 5-SLOT CHASSIS

1. Go to the fan replacement procedure for the 5-slot chassis and perform steps 1-8.
2. Unplug cable P3 on the back of the console PC board.
3. Remove the 4 screws which mount the PC board to its stand-offs. (Each screw has 2 washers.)
4. Mount the new PC board and replace the screws and washers.
5. Plug cable P3 into the new PC board.
6. Go to the fan replacement procedure for the 5-slot chassis and perform steps 13-18.



PC BOARD REPLACEMENT

1. Power down the system.

   IMPORTANT: If you are replacing the power supply PC board or the CPU board see to the replacement procedures for these boards.

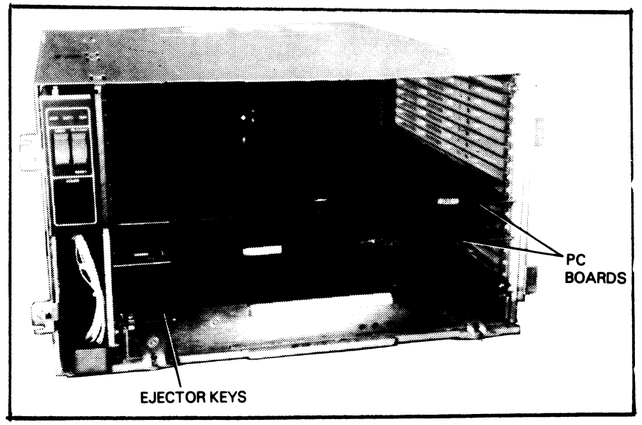
2. Remove the front panel. (See the Front Panel Replacement procedure.)

3. Locate the PC board that is to be replaced. (See your system's Configuration Chart for slot assignments.)

4. Use the ejector keys to remove the PC board.

5. Make sure the new board is tailored (jumpered) correctly and install the new board. Make sure it is seated properly. (The ejector keys should close completely.)

6. Replace the front panel and power up the system.



CPU BOARD REPLACEMENT

1. Power down the system.
2. Remove the front panel. (See Front Panel Replacement procedure.)
3. Remove the CPU board. (It is ALWAYS located in slot 1.)
4. Install the appropriate ROMs into the sockets at locations 29N and 33N on the new CPU board. (See the table and the diagram below for the ROM part numbers and locations.)
5. Install the correct jumpers on the new CPU using the diagram and the tables below showing the jumper positions.
6. Install the new CPU board in slot 1 of the chassis.
7. Replace the front panel and power up the system.
8. Check the new board by running the test that failed.

   a. If the test passes:

      - Power down the system.
      - Remove the front panel.
      - Remove the new CPU board.
      - On the new CPU board, solder the ROMs at locations 29N and 33N into their sockets.
      - Install the new CPU board in slot 1 of the system.
      - Replace the front panel and power up the system.

   b. If the test fails and reports the SAME error as before:

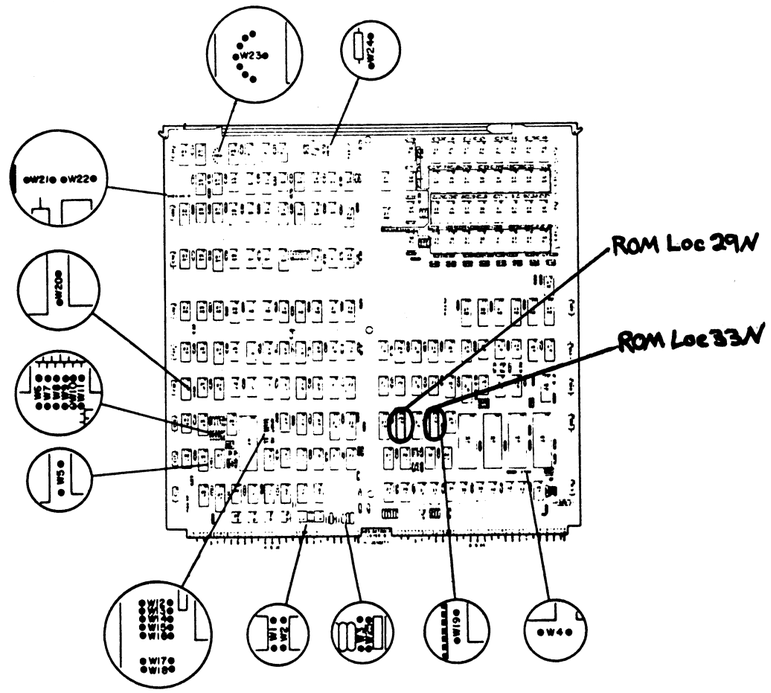
      - Power down the system.
      - Remove the front panel.
      - Remove the new CPU board.
      - Install the ORIGINAL CPU board in slot 1 of the system.
      - Replace the front panel and power up the system.

   c. If the test fails and does NOT report the SAME error as before, replace the new CPU board with another CPU board following steps 1 through 8.

Table 12.1 CPU board assembly numbers and rom part numbers

Assembly No.	ROM Part No. Loc 29N	Loc 33N	Description
005-12413	100-1831	100-1832	NOVA 4/C CPU with 32K byte (16K word) memory
005-12413	100-1833	100-1834	NOVA 4/C CPU with 32K byte (16K word) memory and real-time clock
005-12413	100-1835	100-1836	NOVA 4/C CPU with 32K byte (16K word) memory and multipy/divide option
005-12413	100-1837	100-1838	NOVA 4/C CPU with 32K byte (16K word) memory, real-time clock, and multipy/divide option
005-12415	100-1831	100-1832	NOVA 4/C CPU with 64K byte (32K word) memory
005-12415	100-1833	100-1834	NOVA 4/C CPU with 64K byte (32K word) memory and real-time clock
005-12415	100-1835	100-1836	NOVA 4/C CPU with 64K byte (32K word) memory and multiply/divide option
005-12415	100-1837	100-1838	NOVA 4/C CPU with 64K byte (32K word) memory, real-time clock, and multiply divide option

CPU ROM AND JUMPER LOCATIONS



STOP BIT JUMPERS

NUMBER OF STOP BITS	W15 JUMPER POSITION
1	IN
2	OUT

PARITY JUMPERS

TYPE OF PARITY	JUMPER POSITION W12	W16
EVEN	OUT	IN
ODD	IN	IN
NONE	OUT	OUT

CHARACTER LENGTH JUMPERS

CHARACTER LENGTH	JUMPER POSITION W13	W14
5 BITS	IN	IN
6 BITS	OUT	IN
7 BITS	IN	OUT
8 BITS	OUT	OUT

DEVICE CODE JUMPERS FOR FRONT PANEL AUTOMATIC PROGRAM LOAD

SELECT THE PROGRAM LOAD DEVICE CODE BY INSTALLING JUMPERS W11, W8, W6, W7, W9, W10, AS FOLLOWS:

JUMPER OUT = 1 JUMPER IN = 0

EXAMPLE JUMPERING FOR DEVICE CODE 27_8:

W11	W8	W6	W7	W9	W10
IN	OUT	IN	OUT	OUT	OUT

W4 IS NOT INSERTED IF THE PROGRAM LOAD DEVICE IS A HIGH SPEED DEVICE, OTHERWISE IT IS INSERTED.

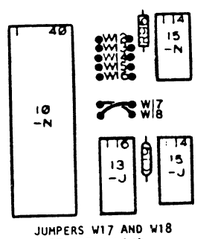
TYPE OF TRANSMISSION JUMPERS

TYPE OF TRANSMISSION	JUMPERS INSERTED*
20MA CURRENT LOOP	W1, W3
EIA RS232-C	W2

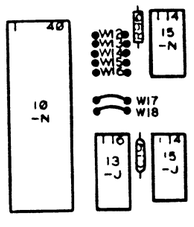
* JUMPER 25 IS INSERTED IF THE SYSTEM TERMINAL IS A TELETYPE, OTHERWISE IT IS NOT INSERTED.

* JUMPERS W17 AND W18 MUST ALSO BE INSERTED AS SHOWN BELOW.

20MA CURRENT LOOP

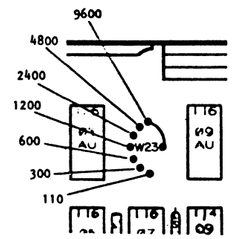


EIA RS232-C



JUMPERS W17 AND W18 MUST NOT TOUCH!

W23 IS INSERTED TO DETERMINE THE BAUD RATE AS SHOWN BELOW:
(9600 SHOWN)



W22 IS NEVER INSERTED.

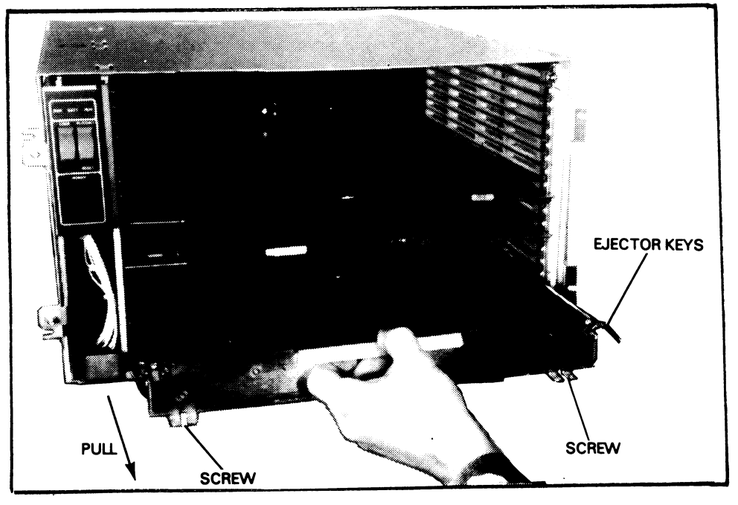
THE FOLLOWING JUMPERS ARE ALWAYS INSERTED:

W5
W19
W20
W21
W24

POWER SUPPLY PC BOARD REPLACEMENT

1. Power down the system. Unplug the ac source from the cabinet.
2. If this is a 5-slot chassis, open the rear cabinet door and remove the power cord connector and the wiring harness cable P1.
3. Remove the front panel. (See Front Panel Replacement pocedure.) The power supply PC board assembly is located in slot 0 of the chassis.
4. Remove the 2 screws which secure the power supply assembly to the chassis.
5. Remove the assembly using the ejector keys.

NOTE: If you are replacing the power supply PC board for any 16-slot chassis, or a 5-slot chassis without the battery back-up option, proceed to step 16. If you are replacing the power supply PC board for a 5-slot chassis with the battery back-up option, WAIT FOR 5 MINUTES to allow the capacitors to discharge, and continue with step 6.



6. Remove the 5 screws on the top of the power supply assembly (one in each corner and one in the center) and remove the top cover.

7. Locate the battery in the front-left corner of the board.

8. Disconnect the two wires (red and black, positive and negative respectively) that connect the battery to the PC board.

9. Remove the 4 screws that secure the battery bracket and remove the battery. Replace the bracket (4 screws).

10. Replace the top cover (5 screws).

11. Remove the 5 screws on the top of the new power supply assembly and remove the top cover.

12. Locate the battery bracket in the front-left corner of the board and remove it (4 screws).

13. Install the battery from the old assembly into the bracket of the new assembly.

14. Replace the bracket (4 screws) and connect the wires.

15. Replace the top cover (5 screws).

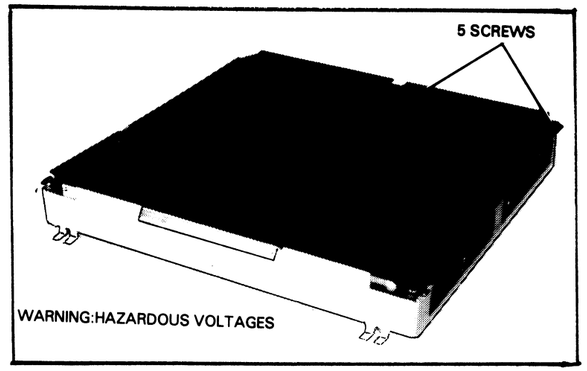
16. Install the new power supply PC board assembly into the chassis.

17. If this is a 5-slot chassis, replace the power cord and cable P1. Close the rear cabinet door.

18. Replace the 2 screws at the front of the assembly.

19. Replace the front panel.

20. Plug in the ac source. Power up the system.



VNR UNIT REPLACEMENT

1. Power down the system, open the rear cabinet door, and unplug the ac source from the cabinet. Wait AT LEAST 5 minutes before proceeding.

2. Unplug the power cord connector on the back of the VNR unit.

3. Loosen the 2 fasteners on the right side of the VNR unit (1/4 ccw turn).

   Note: There may also be 2 shipping screws on the right side of the VNR unit as well as the fasteners. These screws should be removed and discarded.

   Pull the VNR unit on the right side so that it swings out on its hinges.

4. Remove the 4 screws on the inside cover. Remove the cover.

5. Unplug cable P4 located at the bottom right section of the unit.

6. Remove the battery bracket (4 screws). Disconnect the battery wires and remove the battery. Replace the battery bracket (4 screws).

7. Replace the inside cover (4 screws).

8. Remove the 4 screws located on the inside of the hinge.

9. Secure the new VNR unit to the chassis by replacing the 4 screws on the inside of the hinge.

10. Remove the 4 screws on the inside cover. Remove the cover.

11. Remove the battery bracket (4 screws). Insert the battery from the old VNR unit and connect the wires. (The polarity of the wires is etched on the PC board.)

12. Connect cable P4 located at the bottom right section of the unit.

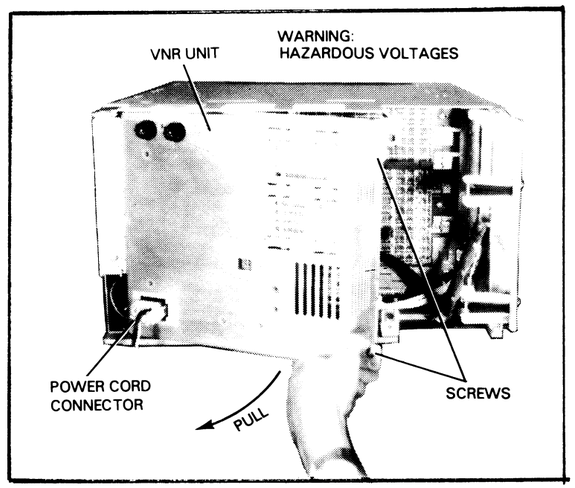
13. Replace the inside cover (4 screws).

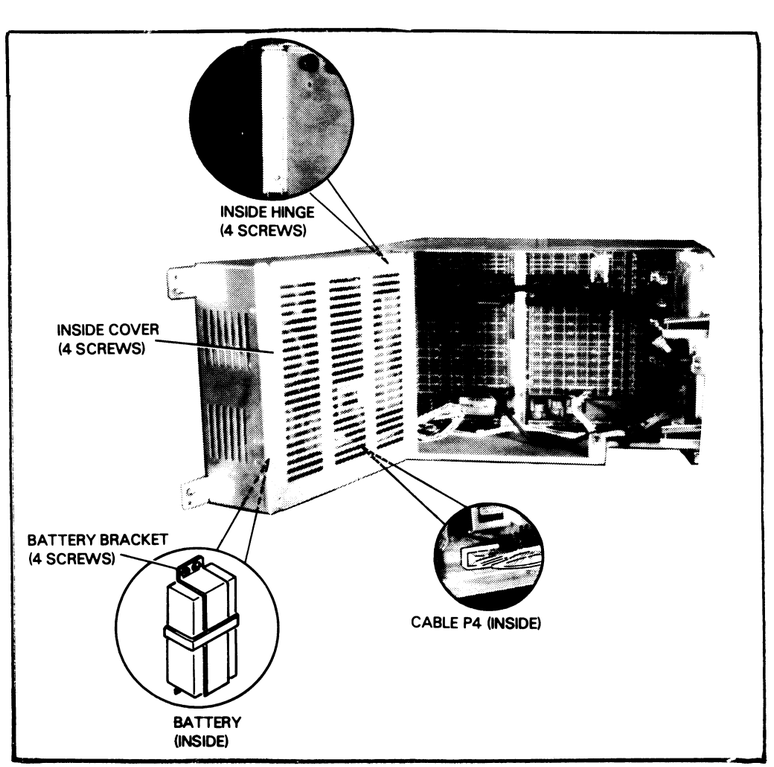
14. Push the VNR unit in towards the chassis and tighten the 2 fasteners.

15. Connect the power cord connector, P1/J1, on the back of the VNR unit.

16. Plug in the ac source. Close the rear cabinet door.

17. Power up the system.





PADDLEBOARD AND TERMINATOR REPLACEMENT

1. Power down the system.

2. Open the rear cabinet door. If it is a 16-slot chassis, you must swing the VNR unit out of the way. (See the VNR Unit Replacement procedure.)

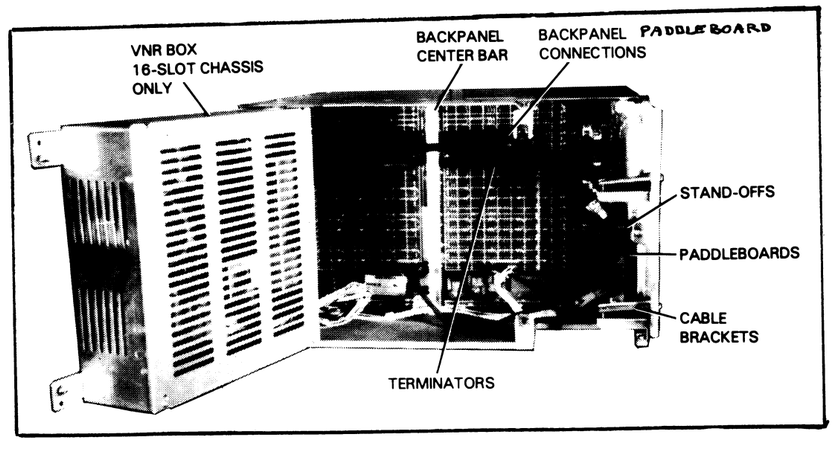
3. A 5-slot chassis does not have any terminators. The terminators on a 16-slot chassis simply pull off and push on the backpanel. (Be careful not to bend backpanel pins.) They must be located on the pins of slot 2 and positioned so that their connection starts at the center bar of the backpanel.

4. The paddleboards are mounted on a bracket on the right (fan) side of the chassis. They are supported by a pair of stand-offs between each board and a pair between the first board and the bracket. You can remove the stand-offs by hand.

   Their connectors to the backpanel pull off and push off. (Be careful not to bend backpanel pins.) They must be positioned so that their connection starts at the center bar of the backpanel.

   The I/O cables are supported by strain relief brackets. There are two brackets per chassis. The brackets each contain one screw on the top to tighten them. The brackets are adjustable to accommodate different size cables.

5. Reposition the VNR unit if this is a 16-slot chassis. Clo e the rear cabinet door and power up the system.



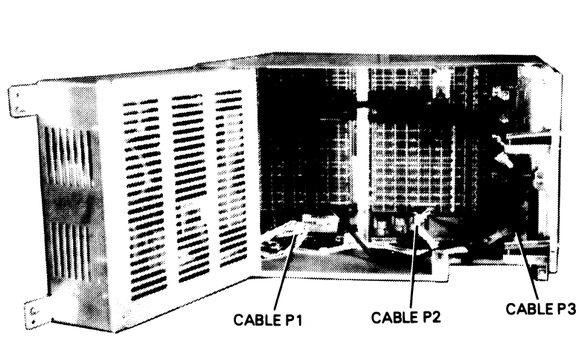
16-SLOT WIRING HARNESS REPLACEMENT

1. Go to the replacement procedure for the VNR unit and perform steps 1-5.

2. Remove the 2 screws on cable P1. Unplug cables P1, P2, and P3, and remove the wiring harness. (See the illustration below and wiring diagram No. 001-001607.)

3. Plug in cables P1, P2, and P3 of the new wiring harness in the proper sockets. (See the illustration below and wiring diaram No. 001-001607.) Replace the 2 screws on cable P1.

4. Go to the replacement procedure for the VNR unit and perform steps 12-17.



REFER TO WIRING DIAGRAM NO.
001-001607 FOR MORE INFORMATION.

5-SLOT WIRING HARNESS REPLACEMENT

1. Go to the fan replacement procedure for the 5-slot chassis and perform steps 1-8.

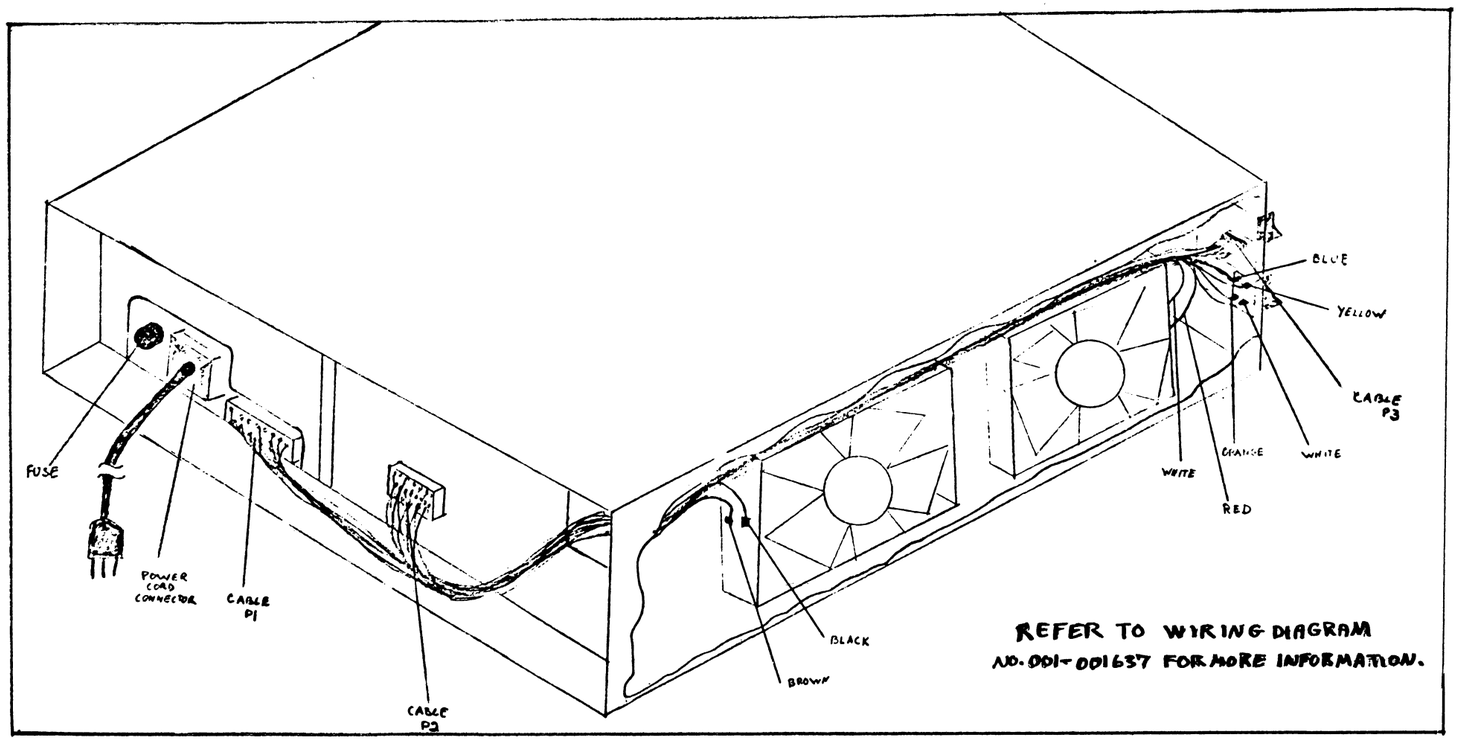
2. Remove cable P3 from the console PCB, the 4 wires from the power switch, and the 4 wires from the fans (2 wires per fan). (See the illustration below and wiring diagram No. 001-001637.)

3. Pull these cables of the harness through the slot in the backpanel. Remove the wiring harness cables connected to the backpanel, P2 and P1.

4. Being very careful to follow the color scheme shown in the picture below, connect the new wiring harness to the fans (2 wires per fan), the power switch (4 wires), and the console PCB (cable P3).

5. Pull the 2 remaining cables of the harness (P1 and P2) through the slot in the backpanel and plug them in the appropriate locations. (See the illustration below and wiring diagram No. 001-001637.)

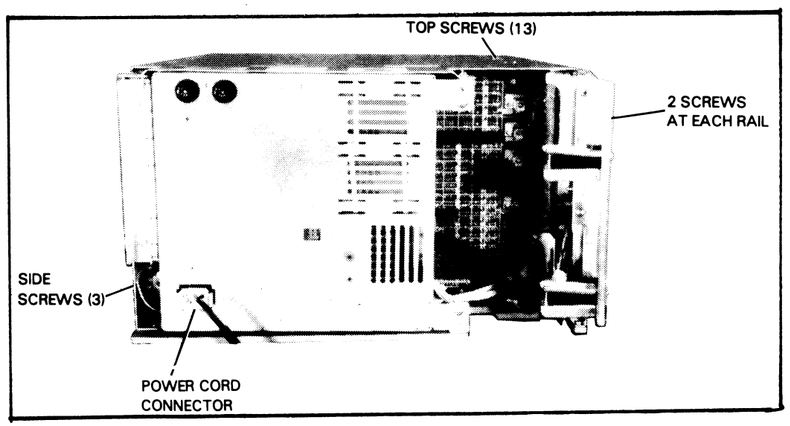
6. Go to the fan replacement procedure for the 5-slot chassis procedure and perform steps 13-18.

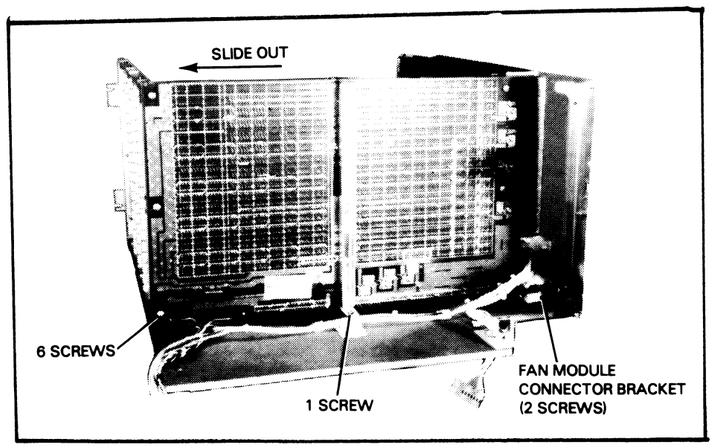


BACKPANEL REPLACEMENT FOR 16-SLOT CHASSIS

CAUTION: This procedure requires at least two people. The chassis weighs about 110 lbs. (about 50 Kgs.) fully loaded.

1. Power down the system and unplug the ac source.
2. Remove the front panel. (See the Front Panel Replacement procedure.)
3. Remove all PC boards in the chassis. (See the replacement procedures for the power supply board, the CPU, and other PC boards.)
4. Remove the fan module. (See the Fan and Fan Module Replacement procedure.)
5. Open the rear cabinet door and remove the power cord from the VNR unit.
6. Swing out the VNR unit. (See the VNR Unit Replacement procedure.)
7. Remove all connectors, terminators, and paddleboard connectors from the backpanel. Note their location so you can reconnect them on the new backpanel.
8. Remove the 8 screws which secure the chassis to the cabinet rails; there are 2 screws per rail.
9. With one person on each side of the cabinet, slide the chassis out from the front of the cabinet. The slides will support the chassis until it is about half way out of the cabinet.
10. Place the chassis on a secure table.
11. Remove the top cover; there are 13 screws on the top and 3 screws on the left-hand side (where the fan module is located).
12. Remove the screw which holds the backpanel to the base of the chassis.
13. Remove the bracket which supports the fan module connector (2 screws).
14. Remove the 6 screws which secure the backpanel to the back of the chassis.
15. You should now be able to slide the backpanel out towards the right-hand side, away from the fan module.
16. Slide in the new backpanel and replace the 6 screws which secure it to the back of the chassis.
17. Replace the bracket that supports the fan module connector (2 screws).





18. Replace the screw that holds the backpanel to the base of the chassis.

19. Replace the top cover; there are 13 screws on the top and 3 screws on the left-hand side (where the fan module is located).

20. Slide the chassis back into the front of the cabinet.

21. Replace the 8 screws that secure the chassis to the cabinet rails.

22. Replace all connectors, terminators, and paddleboard connectors on the backpanel.

23. Return all the PC boards to their proper location in the chassis. (See your system's configuration chart and replacement procedures for the power supply board, the CPU, and other PC boards.)

24. Replace the fan module. (See the Fan and Fan Module Replacement procedure.)

25. Replace the front panel. (See the Front Panel Replacement procedure.)

26. Return the VNR unit to its proper position. (See the VNR Unit Replacement procedure.)

27. Reconnect the power cord to the VNR unit.

28. Plug in the ac source, close the rear cabinet door, and power up the system.

BACKPANEL REPLACEMENT FOR 5-SLOT CHASSIS

1. Power down the system, open the rear cabinet door, and unplug the ac source.

2. Remove the front panel. (See the Front Panel Replacement procedure.)

3. Open the rear cabinet door and remove the power cord connector and the wiring harness cable P1.

4. Remove all PC boards in the chassis. (See the replacement procedures for the power supply board, the CPU, and other PC boards.)

5. Remove all connectors, including paddleboard connectors, from the backpanel. Note their location so you can reconnect them on the new backpanel.

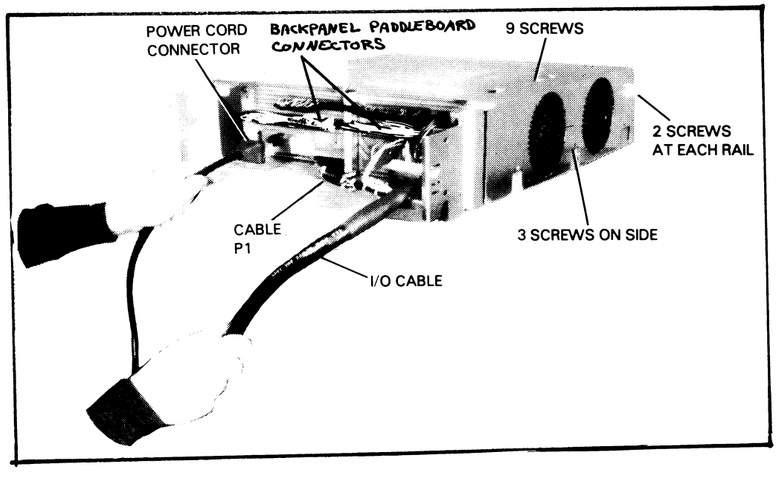
6. Remove the 8 screws which secure the chassis to the cabinet rails; there are 2 screws per rail.

7. Slide the chassis out from the front of the cabinet. The slides will support the chassis until it is about half way out of the cabinet.

   CAUTION: The chassis weighs about 50 lbs (about 23 kgs) fully loaded. You may need help.

8. Place the chassis on a secure table.

9. Remove the top cover; there are 9 screws on the top and 3 screws on the left or fan side.



10. Lift the top cover up and over to the left so that it lies on its side.

11. Remove the screw that holds the backpanel to the base of the chassis.

12. Remove the 4 screws that secure the backpanel to the back of the chassis.

13. You should now be able to slide the backpanel out towards the right side, away from the fans.

14. Slide in the new backpanel and replace the 4 screws which secure it to the back of the chassis.

15. Replace the screw in the base of the chassis.

16. Place the cover back in position over the chassis and replace the screws (9 on the top and 3 on the side).

17. Slide the chassis back into the front of the cabinet.

18. Replace the 8 screws which secure the chassis to the cabinet rails; there are 2 screws per rail.

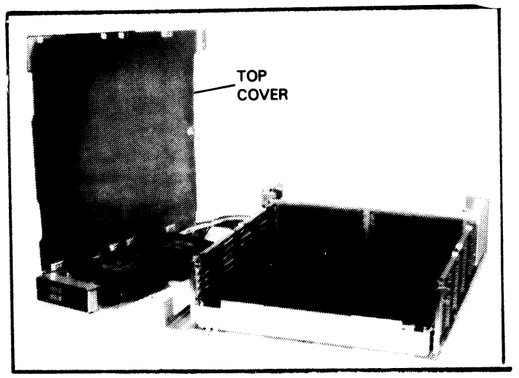
19. Replace all connectors, including paddleboard connectors, on the backpanel.

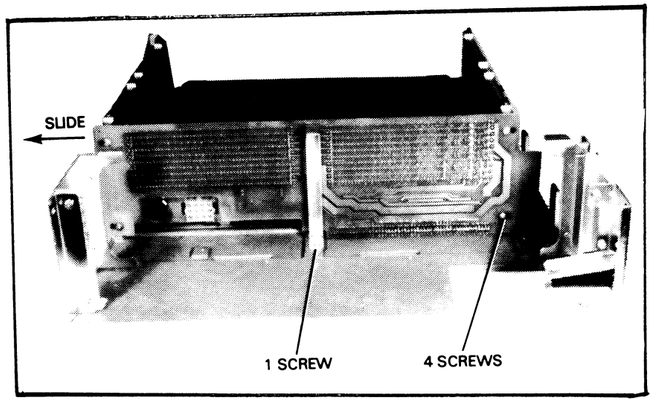
20. Return all the PC boards to their proper location in the chassis. (See your system's configuration chart and the replacement procedures for the power supply board, the CPU, and other PC boards.)

21. Replace the front panel.

22. Replace the power cord connector and cable P1 at the rear, and replace all I/O cables.

23. Plug in the ac source, close the rear cabinet door, and power up the system.





APPENDIX A
RDOS PANIC CODES

Panic Code No.	Description
1	Not used.
2	This panic is caused by an error in the operating system file SYS.DR. Failure may be caused by memory or disc subsystem prior to the write data operation on the disc media.
3	This panic is caused by a stack overflow inside the RDOS addressing space. Failure may be caused by a CPU/memory related problem or it may be the result of an I/O controller continually interrupting. In the latter case, the stack would overflow from continuous return blocks being pushed on the stack.
4	This panic can be caused by any one of the following: a. RDOS encountered a logical block address outside the boundaries of the disc. b. A device code is encountered in a table for which there is no corresponding device driver. c. A table address was found that pointed to the wrong memory address. Failure may be caused by the disc subsystem, memory or the CPU.
5	This panic is caused by a fatal error on the disc from which RDOS was booted. Failure is caused by the malfunctioning of the disc subsystem used to boot RDOS.
6	This panic is caused by the lack of an interrupt from the disc that was booted. Failure is caused by the malfunctioning of the disc subsystem used for last boot.
7	This panic can only occur when either the 6060, 6061 or 6067 disc subsystem is present. It indicates that the disc returned an illogical status to the operating system. Accumulator 0 contains the DIA status word; AC1 contains the DIB status word. Failure is caused by the malfunctioning of the disc subsystem.
8	Not used
9	Not used
10	This panic occurs when the operating system receives an interrupt from a device that is not recognized by the operating system. The operating system attempts to clear the interrupt 2000 times before it issues panic 10. Accumulator 2 contains the device code of the interrupting device causing the problem. If it is a non-existent device code, check pin B29 (INTR) of each open slot on the backpanel.
11	Not used
12	Not used
13	This panic is primarily related to either the operating system or the user software. Failure could be caused by memory.

Panic Code No.	Description
14	This panic can only occur in a dual processor system containing a 4240 Interprocessor Bus (IPB) Subsystem. It can be caused by an interrupt from the interval timer (indicating a failure in the other processor) or an illegal message from the other CPU. If accumulator 2 contains the octal number 064400, the interrupt was the cause of the failure. In either case, troubleshoot the 4240 IPB subsystem.
15	This panic is caused by a map violation in a user interrupt handler. Accumulator 0 contains the logical address at which the trap occurred. Failure could be caused by malfunctioning of MMPU on NOVA 4/X CPU.
16-20	Not used
21	This panic indicates an unrecoverable I/O error occurred on the RDOS master disc unit.

APPENDIX B
DTOS LOADING PROCEDURES

FROM MAGNETIC TAPE UNIT

1. Power up processor and tape drive.
2. Set SELECT switch on tape drive to unit 0.
3. Press RESET switch on tape drive.
4. Remove write-enable ring from tape; load and thread tape.
5. Press LOAD and then ON LINE switches on tape drive.
6. Enter 100022L on system terminal keyboard.
7. The system terminal will print or display the following message:

   TYPE IN THE ID NUMBER FOR THIS CPU AND CR
   (0-NOVA 1200, 1-NOVA 800, 2-NOVA II, 3-NOVA III, 4-NOVA IV OR
   5-ECLIPSE)

8. Enter 4 in the keyboard followed by a Carriage Return.
9. The system terminal will print or display the following message:

   TYPE IN CPU SUBTYPE AND CR
   (0-NOVA 4C, 1-NOVA 4S OR X)

10. Enter 0 in the keyboard followed by a Carriage Return.
11. The system terminal will print or display the following message:

TOP OF MEMORY =	(Number varies with system memory size)
HIDTOS REV --	(Revision number varies with system revision)
*	(This is the DTOS prompt; enter DTOS commands as specified in Section 2, Chapters 5 and 6)

FROM DISC OR DISKETTE

1. Power up processor and disc or diskette drive.
2. Insert disc cartridge, pack or diskette into drive assigned logical unit 0.
3. Recalibrate the drive as follows:

   a. For 6060/6061 and 6067 disc drives

      Press RESET switch on front console

   b. For diskette

      Open and close drive door
      Make sure the READY and TRACK 0 indicators are lit

   c. For other disc drives, use the virtual console to enter the following data in the locations indicated:

Location	Input
00000	063033 (for primary device) 063073 (for secondary device)
00001	065333 (for primary device) 065373 (for secondary device)
00002	063077
AC0	000000
AC1	003400

   Enter 00000R in the keyboard.

4. When the console prompt (:) appears, enter the following in the keyboard.

   For 6060, 6061 and 6067 disc drives:

   100027L (for primary device)
   100067L (for secondary device)

   For other disc drives:

   100033L (for primary device)
   100073L (for secondary device)

5. The system terminal will print or display the following message:

   TYPE IN ID NUMBER FOR THIS CPU AND CR
   (0-NOVA 1200, 1-NOVA 800, 2-NOVA II, 3-NOVA III, 4-NOVA IV
   OR 5-ECLIPSE)

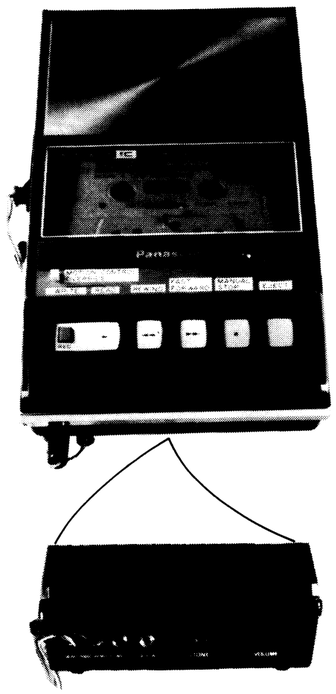
6. Enter 4 in the keyboard followed by a Carriage Return
7. The system terminal will print or display the following message:

   TYPE IN CPU SUBTYPE AND CR
   (0-NOVA 4C, 1-NOVA 4S OR X)

8. Enter 0 in the keyboard followed by a Carriage Return.
9. The system terminal will print or display the following message:

TOP OF MEMORY =	(Number varies with system memory size)
HIDTOS REV --	(Revision number varies with disc build operator input)
*	(This is the DTOS prompt; enter the DTOS commands as specified in Section 2, Chapters 5 and 6)

Figure D.1 Field Service Cassette Loader



APPENDIX C
FIELD SERVICE CASSETTE PROCEDURES

When you cannot run diagnostic test programs using DTOS, you can run them using the field service cassette. Load the diagositc programs following the procedure below and run them in the sequence given in the troubleshooting flowchart in chapter 5, "Diagnostic Testing".

Throughout the flowchart, action recommendations following each program test are made solely on a pass/fail basis. To determine if a test passed, refer to the Sample Program Run Summary for the particular test at the end of this appendix.

LOADING PROCEDURE

1. Plug the cassette cable into backpanel pins A68 to A100 in any I/O slot.
2. Load the NOVA 4 cassettte (DGC No. 005-009270) in the cassette loader.
3. Set the VOLUME control on the loader to between 5.5 and 6 (see figure C.1).
4. Power up the processor.
5. Load the Cassette Executive program into the top of memory as follows:

    o Using the Automatic Cassette Load

        a. Rewind the tape to the beginning.

        b. Press the READ key on the cassette loader (see figure C.1).

        c. When a tone sounds, press the F key on the system console. In a few seconds, the tone stops and the console prints the top memory address to be used by the diagnostic programs. For a 64KByte system, this top memory address is 77777(octal); for a 32KByte system it is 37777(octal). If the tone does not stop before 9 feet of tape have been read, the Cassette Executive program prabably did not load. In this case, repeat steps a through c. If the program fails to load after several attempts, use the cassette bootstrap as described below. You might also check to see if tne cassette bootstrap was loaded correctly. Note the automatic cassette load program loads the cassette bootstrap into memory starting at location 2.

- Using the Cassette Bootstrap

  a. Using the virtual console, enter the following data in the locations indicated.

Location	Input
1000	152440
1001	176440
1002	24402
1003	125401
1004	177526
1005	63600
1006	775
1007	62677
1010	175203
1011	771
1012	055177
1013	151400
1014	14177
1015	764
1016	4200

  b. Rewind the tape to the beginning.

  c. Press the READ key on the cassette loader. When a tone sounds, enter the following on the console:

     ↓1000R

  d. In a few seconds, the tone will stop and the console will print the top memory address to be used by the diagnostic programs). For a 64 KByte or larger system, the top memory address is 77777; for a 32 KByte system it is 37777. If the tone does not stop before 9 feet of tape have been read, the Cassette Executive program probably did not load. In this case, repeat steps a through d.

6. Load a diagnostic program from the cassette using the procedure below. If you do not have a listing of the programs on the cassette and their file numbers, the program in file 1 will print out such a listing. Load this program as described below, and run it starting at address 200 as described in step 7.

   a. Depress the READ switch on the loader, if it is not already depressed.

   b. Enter top memory address used by the diagnostics and press the R key on the console.

   c. When the console prints out a number sign, #, enter the file number of the program you want to run followed by a CARRIAGE RETURN.

   d. The console will print the file number of each file it comes to. You can keep the console from printing these numbers and advance the tape more quickly by holding down the MOTION CONTROL OVERRIDE and the FAST FORWARD keys on the cassette loader (see figure C.1). If the file numbers printed out are higher than the number you entered, rewind the tape by pressing the MOTION CONTROL OVERRIDE and the REWIND keys on the loader (see figure C.1).

   e. When the specified file is reached, it will be loaded into memory and the console will print the following message:

      ↓LOADED <file number><top memory address>
      ↓

7. Run the program by entering the following on the console:

   ↓<starting address>R

   IMPORTANT: All programs start at address 200 except for the N4CMD which starts at address 500.

8. To run another program, press the BREAK key on the console and repeat steps 5 through 7. If you cannot load a program, repeat the entire procedure by starting at step 1.

SAMPLE PROGRAM RUN SUMMARY
NOVA 4/C MEMORY DIAGNOSTIC
(No Errors Found)

DTOS Mnemonic: N4CMD
Special Machine Requirements: None
Reference: Listing No. 096-001677

Operator Input: Comments

!<ENTER TOP MEMORY ADDRESS USED FOLLOWED BY AN R>

#<ENTER FILE NUMBER OF N4MDU1 FOLLOWED BY A CARRIAGE RETURN>

Program Output:

. . . . . Note 1

LOADED <FILE NUMBER OF N4CMD><TOP MEMORY ADDRESS USED>

Operator Input:

!500R

Program Output:

LOAD: N4CMD
N4MCMD REV. 00 <Date>

** PROGRAM EXEC **

INPUT NEW VALUES FOR CF'S (LF=DEFAULT)
ECM <0-4>?

Operator Inout:

< 0 FOLLOWED BY A CARRIAGE RETURN>

Program Output:

SUPPLEMENTAL ERROR INFORMATION (Y/N)?

OPERATOR INPUT:

< N FOLLOWED BY A CARRIAGE RETURN>

Program Output:

PATTERNS (0-17)?

Operator Input:

<LINE FEED>

Program Output:

TESTING COMPLETED
*** END PROGRAM ***

PASS= 1

NOTES:

1. The program may output the number of each file which it passes before it reaches the specified file.

2. For information on the questions asked by the program and on error reporting, see the sample program run summaries for N4CMD in Part II, Chapter 7, "Diagnostic Testing."

SAMPLE PROGRAM RUN SUMMARY
NOVA 4 EXERCISER
(No Errors Found)

DTOS Mnemonic: N4EXER
Special Machine Requirements: None
Reference: Listing No. 096-001136

Operator Input:	Comments
!<ENTER TOP MEMORY ADDRESS USED FOLLOWED BY AN R>	
#<ENTER FILE NUMBER OF N4EXER FOLLOWED BY A CARRIAGE RETURN>	
Program Output:	
. . . . .	Note 1
LOADED <FILE NUMBER OF N4EXER><TOP MEMORY ADDRESS USED>	
Operator Input:	
!200R	
Program Output:	
N4EXER 00 RUNNING	
TOTAL # OF 1K'S = 128	Note 2
PASS 1	
PASS 2	
PASS 3	

NOTES:

1. The program may output the number of each file which it passes before it reaches the specified file.
2. TOTAL # 1K'S varies with system.
3. For information on error reporting, see the sample program run summary for N4EXER in Part II, Chapter 7, "Diagnostic Testing."

SAMPLE PROGRAM RUN SUMMARY
NOVA 4 LOGIC TEST
(No Errors Found)

DTOS Mnemonic: N4LGCTST
Special Machine Requirements: None
Reference: Listing No. 096-001137

Operator Input:	Comments
!<ENTER TOP MEMORY ADDRESS USED FOLLOWED BY AN R>	
#<ENTER FILE NUMBER OF N4LGCTST FOLLOWED BY A CARRIAGE RETURN>	
Program Output:	
. . . . .	Note 1
LOADED <FILE NUMBER OF N4LGCTST><TOP MEMORY ADDRESS USED>	
Operator Input:	
!200R	
!P	
Program Output:	
PASS	
PASS	
PASS	

NOTES:

1. The program may output the number of each file which it passes before it reaches the specified file.

SAMPLE PROGRAM RUN SUMMARY
BASIC INPUT/OUTPUT TEST
(No Errors Found)

DTOS Mnemonic: BASICIOT
Special Machine Requirements: Multi-mode I/O Tester Board No. 005-004283
Reference: Listing No. 096-001133

Operator Input:	Comments
↓<ENTER TOP MEMORY ADDRESS USED FOLLOWED BY AN R>	
#<ENTER FILE NUMBER OF BASICIOT FOLLOWED BY A CARRIAGE RETURN>	
Program Output:	
. . . . .	Note 1
LOADED <FILE NUMBER OF BASICIOT><TOP MEMORY ADDRESS USED>	
Operator Input:	
↓200R	
Program Output:	
BASICIOT REV. 00 <DATE>	
COMPUTER TYPE (0=NOVA 4, 1=NOVA 3, 2= MICRONOVA, 3=ECLIPSE)?	
Operator Input:	
0	
Program Output:	
HIT (CR) WHEN INTP AND DCHP JUMPERS IN PLACE	Note 2
Operator Input:	
<CARRIAGE RETURN>	
Program Output:	
PASS 1 PASS 2	

NOTES:

1. The program may output the number of each file which it passes before it reaches the specified file.

2. Before entering a carriage return, the make sure that the I/O Tester Board is inserted in an I/O slot, and that the harware priority jumpers are positioned correctly.

PROGRAM RUN SUMMARY
REAL-TIME CLOCK TEST
(No Errors Found)

DTOS Mnemonic: RTC TST
Special Machine Requirements: NOVA 4/C with real-time clock option
Reference: Listing No. 096-000154-13

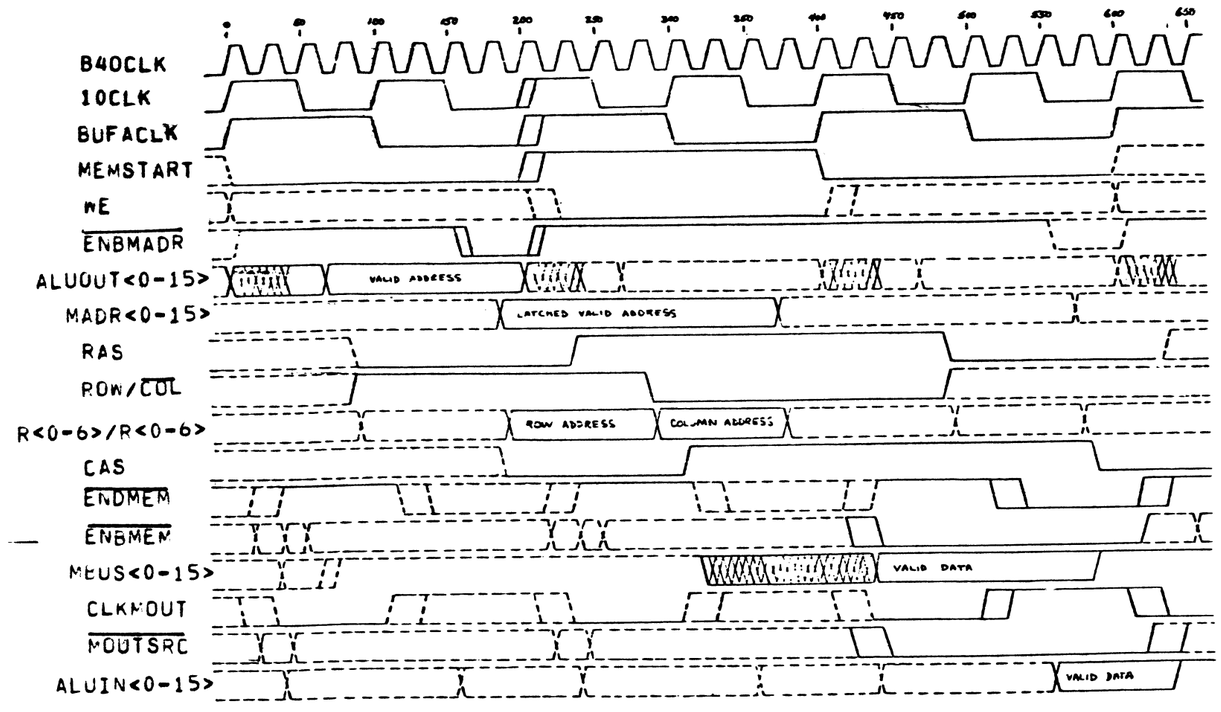
Operator Input:	Comments
↓<ENTER TOP MEMORY ADDRESS USED FOLLOWED BY AN R>	
#<ENTER FILE NUMBER OF RTC TST FOLLOWED BY A CARRIAGE RETURN>	
Program Output:	
. . . . .	Note 1
LOADED <FILE NUMBER OF RTC TST><TOP MEMORY ADDRESS USED>	
Operator Input:	
↓200R	
Program Output:	
RTC TST 13 RUNNING	
PASS 1	
PASS 2	
PASS 3	

NOTES:

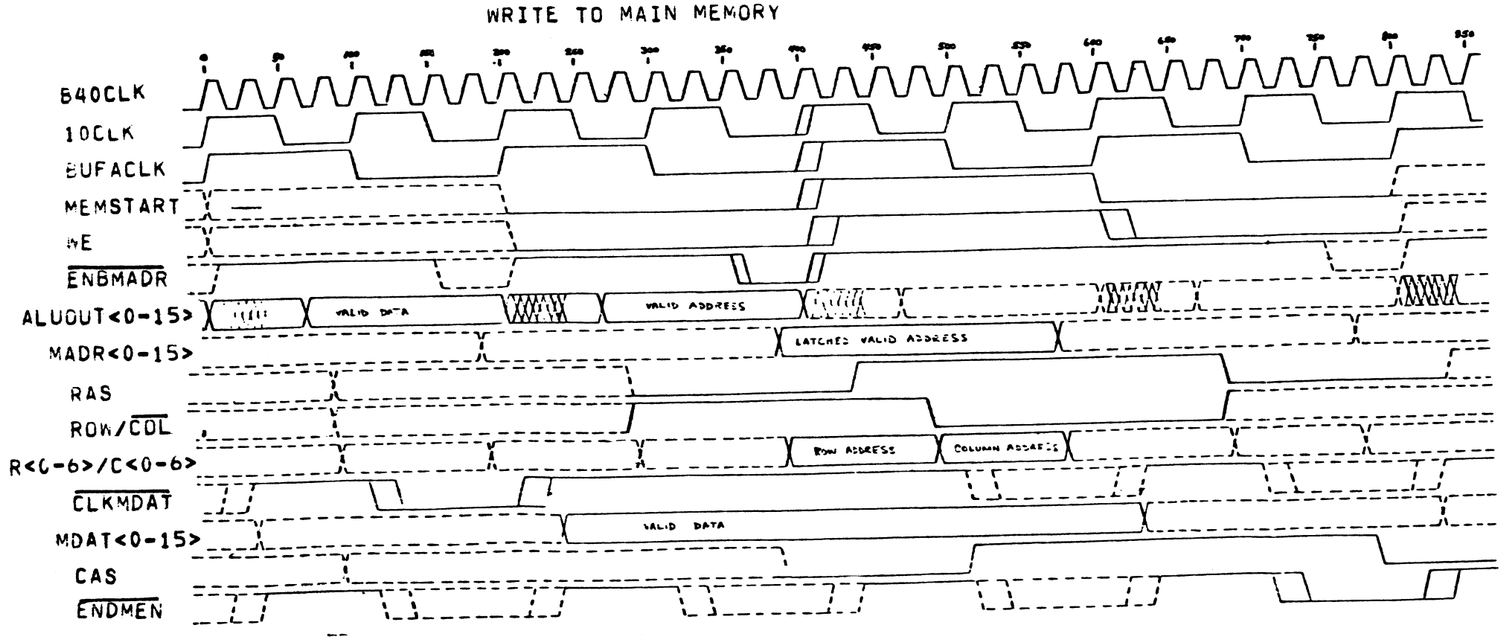
1. The program may output the number of each file which it passes before it reaches the specified file.

APPENDIX D
MAIN MEMORY TIMING DIAGRAMS

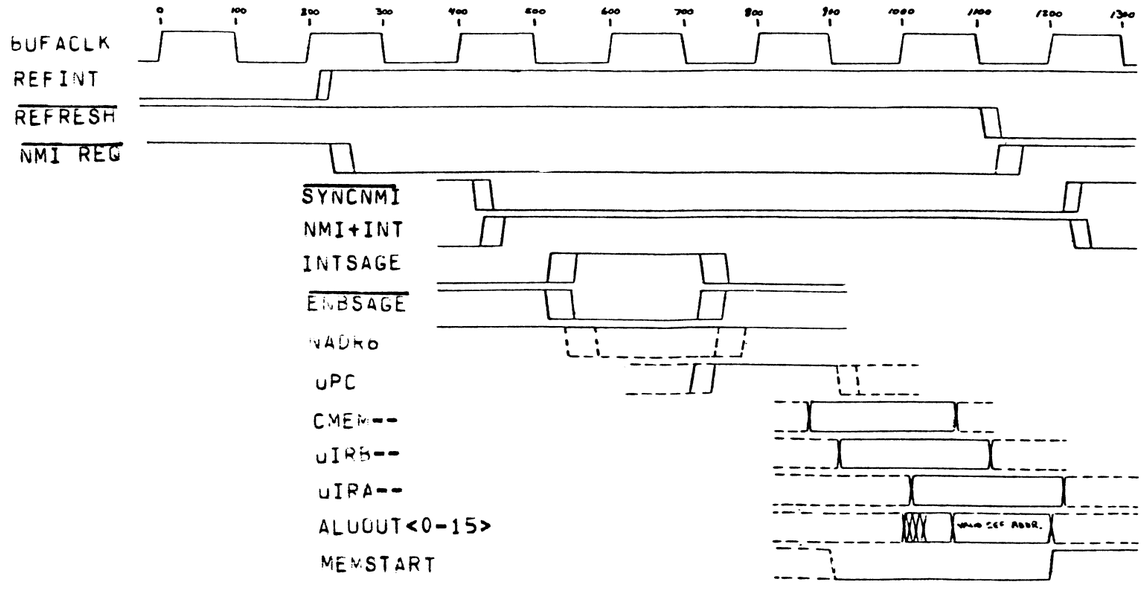
READ FROM MAIN MEMORY



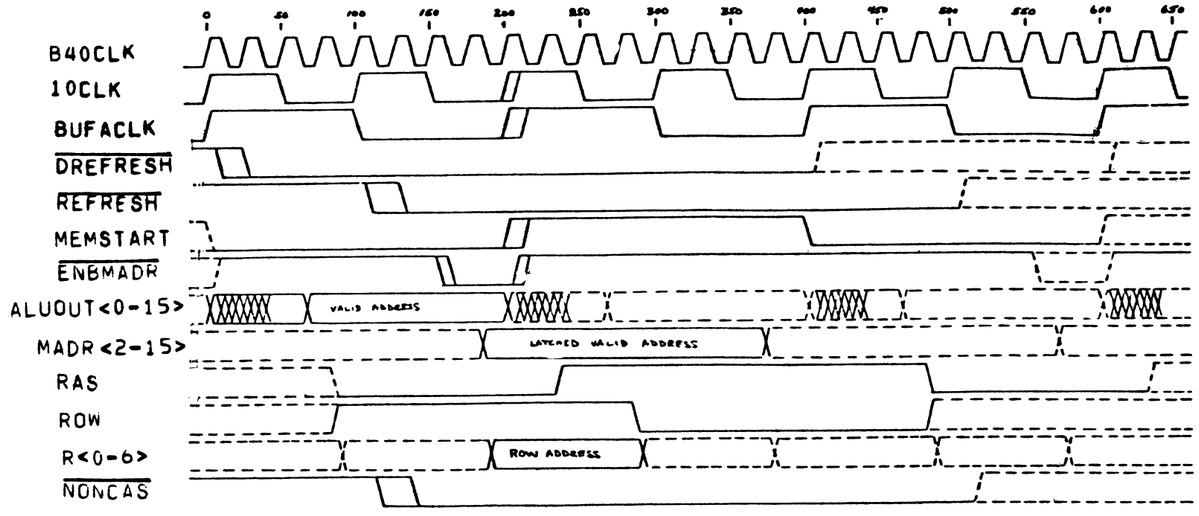
WRITE TO MAIN MEMORY



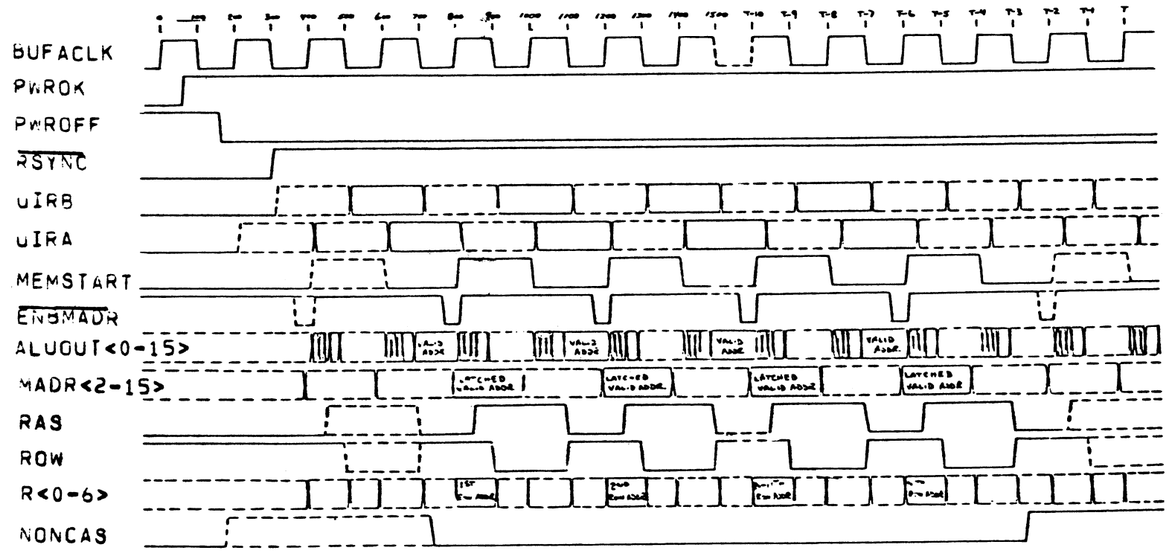
NORMAL REFRESH INTERRUPT



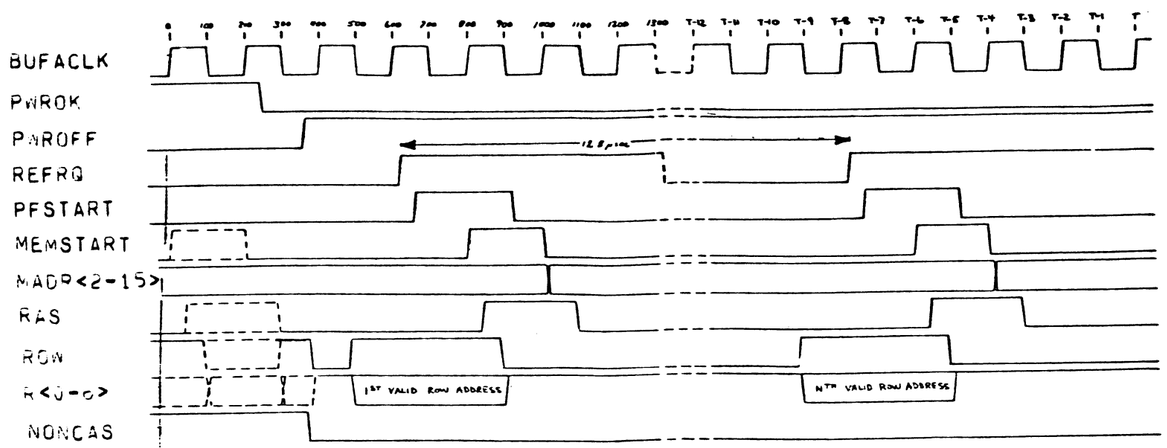
NORMAL REFRESH FOR MAIN MEMORY



BURST REFRESH (SWITCHING OUT OF BATTERY BACKUP)



BATTERY REFRESH (PERIODIC DURING BATTERY BACKUP)



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Installation Membership Form

Name _____ Position _____ Date _____

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Telephone: Area Code _____ No. _____ Ext. _____

1. Account Category

- ☐ OEM
- ☐ End User
- ☐ System House
- ☐ Government

2. Hardware

	Qty. Installed	Qty. On Order
M/600		
C/350, C/330, C/300		
S/250, S/230, S/200		
S/130		
AP/130		
CS Series		
N3/D		
Other NOVA		
microNOVA		
Other (Specify) _____		
_____		

3. Software

- ☐ AOS
- ☐ DOS
- ☐ SOS
- ☐ RDOS
- ☐ RTOS
- ☐ Other

Specify _____

4. Languages

- ☐ Algol
- ☐ DG/L
- ☐ Cobol
- ☐ ECLIPSE Cobol
- ☐ Business BASIC
- ☐ BASIC
- ☐ Assembler
- ☐ Interactive
- ☐ Fortran
- ☐ RPG II
- ☐ PL/1
- ☐ Other

Specify _____

5. Mode of Operation

- ☐ Batch (Central)
- ☐ Batch (Via RJE)
- ☐ On-Line Interactive

6. Communications

- ☐ RSTCP
- ☐ HASP
- ☐ RJE80
- ☐ SAM
- ☐ CAM
- ☐ 4025
- ☐ Other

Specify _____

7. Application Description

○ _____

8. Purchase

From whom was your machine(s) purchased?

- ☐ **Data General Corp.**
- ☐ Other

Specify _____

9. Users Group

Are you interested in joining a special interest or regional Data General Users Group?

○ _____

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