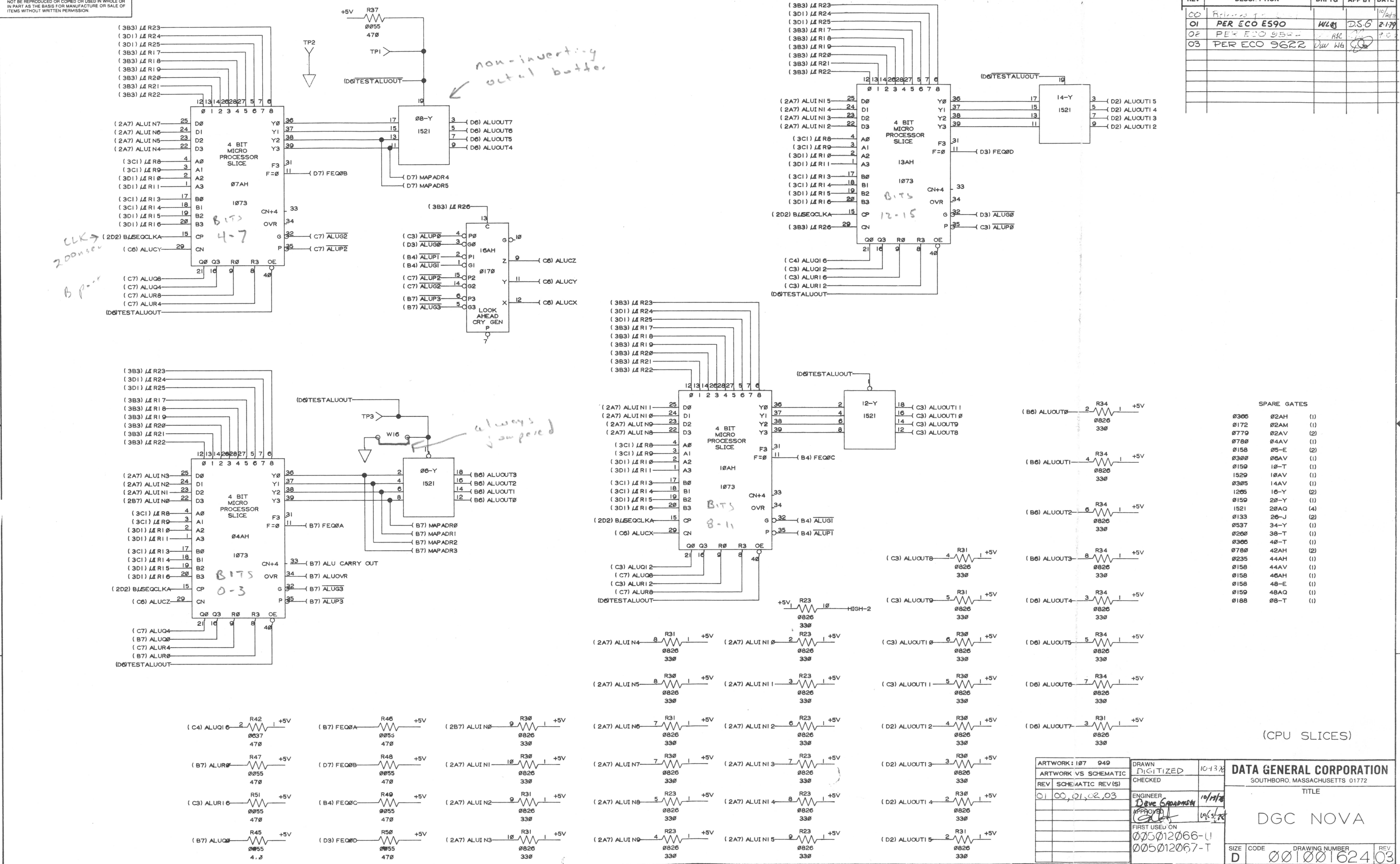


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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE
00	PER ECO 5590	WLG	DSG	2-17-79
01	PER ECO 5590			
02	PER ECO 5590			
03	PER ECO 5622			



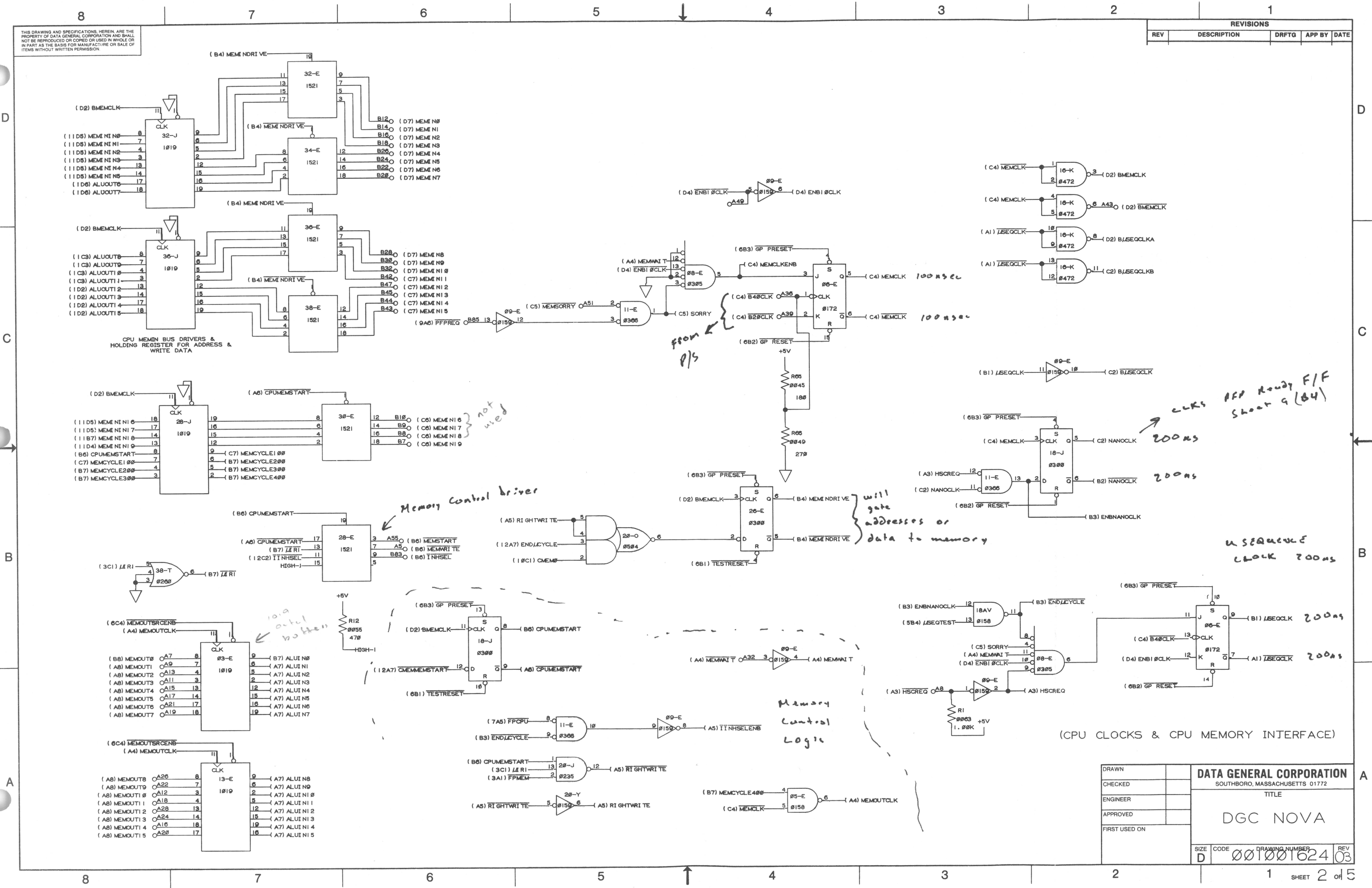
SPARE GATES

0366	02AH	(1)
0172	02AM	(1)
0779	02AV	(2)
0780	04AV	(1)
0158	05-E	(2)
0300	06AV	(1)
0159	10-T	(1)
1529	10AV	(1)
0305	14AV	(1)
1265	16-Y	(2)
0159	20-Y	(1)
1521	20AQ	(4)
0133	26-J	(2)
0537	34-Y	(1)
0200	38-T	(1)
0305	40-T	(1)
0780	42AH	(2)
0235	44AH	(1)
0158	44AV	(1)
0158	46AH	(1)
0158	48-E	(1)
0159	48AQ	(1)
0188	08-T	(1)

ARTWORK: 107 949	DRAWN: DIGITIZED 10-13-78	DATA GENERAL CORPORATION SOUTHBOOR, MASSACHUSETTS 01772
ARTWORK VS SCHEMATIC CHECKED	CHECKED	
REV: 01, 02, 03	ENGINEER: Dave Garabedian 10/17/78	TITLE: DGC NOVA
	APPROVED: [Signature] 10/17/78	SIZE: D
	FIRST USE ON: 005012066-U	DRAWING NUMBER: 001001624.03
		REV: 005012067-T

REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

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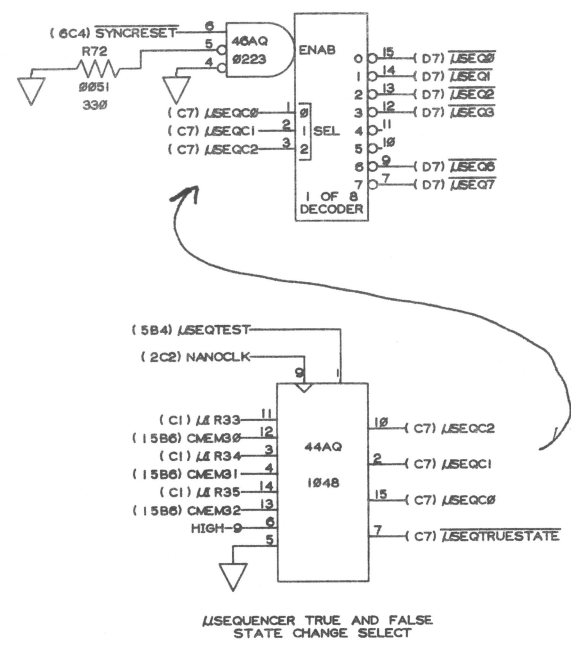


(CPU CLOCKS & CPU MEMORY INTERFACE)

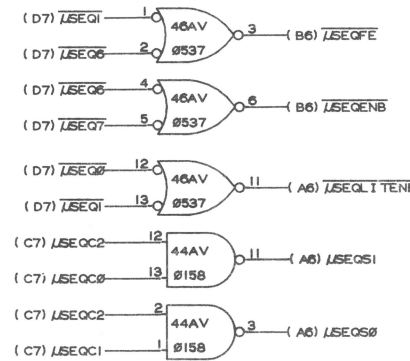
DRAWN		DATA GENERAL CORPORATION		A
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON		SIZE	CODE	DRAWING NUMBER
		D		001001624 03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

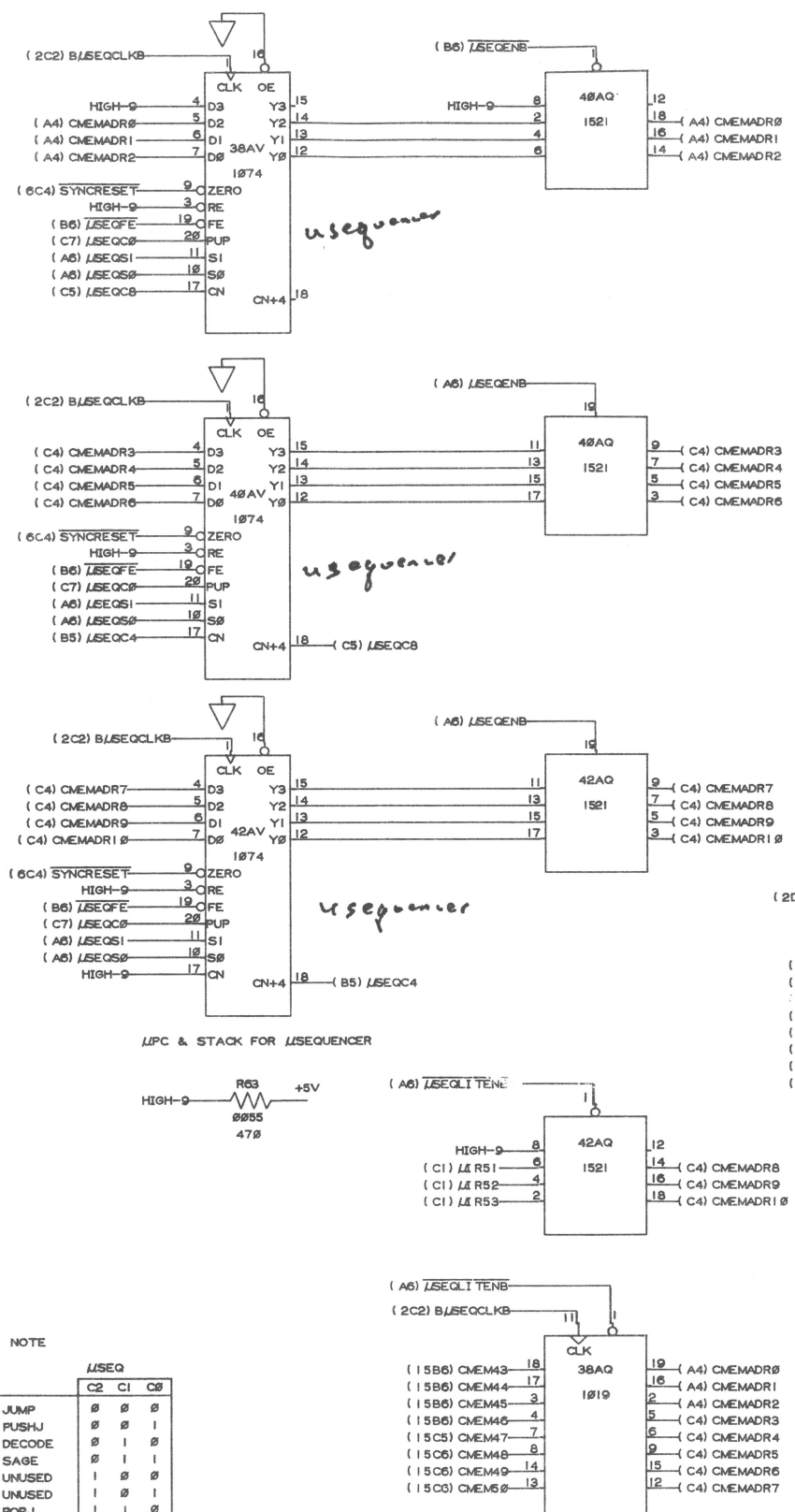


*useq test -> H = True  
pass MEM (30-32)  
L = False  
pass uIR (33-35)*

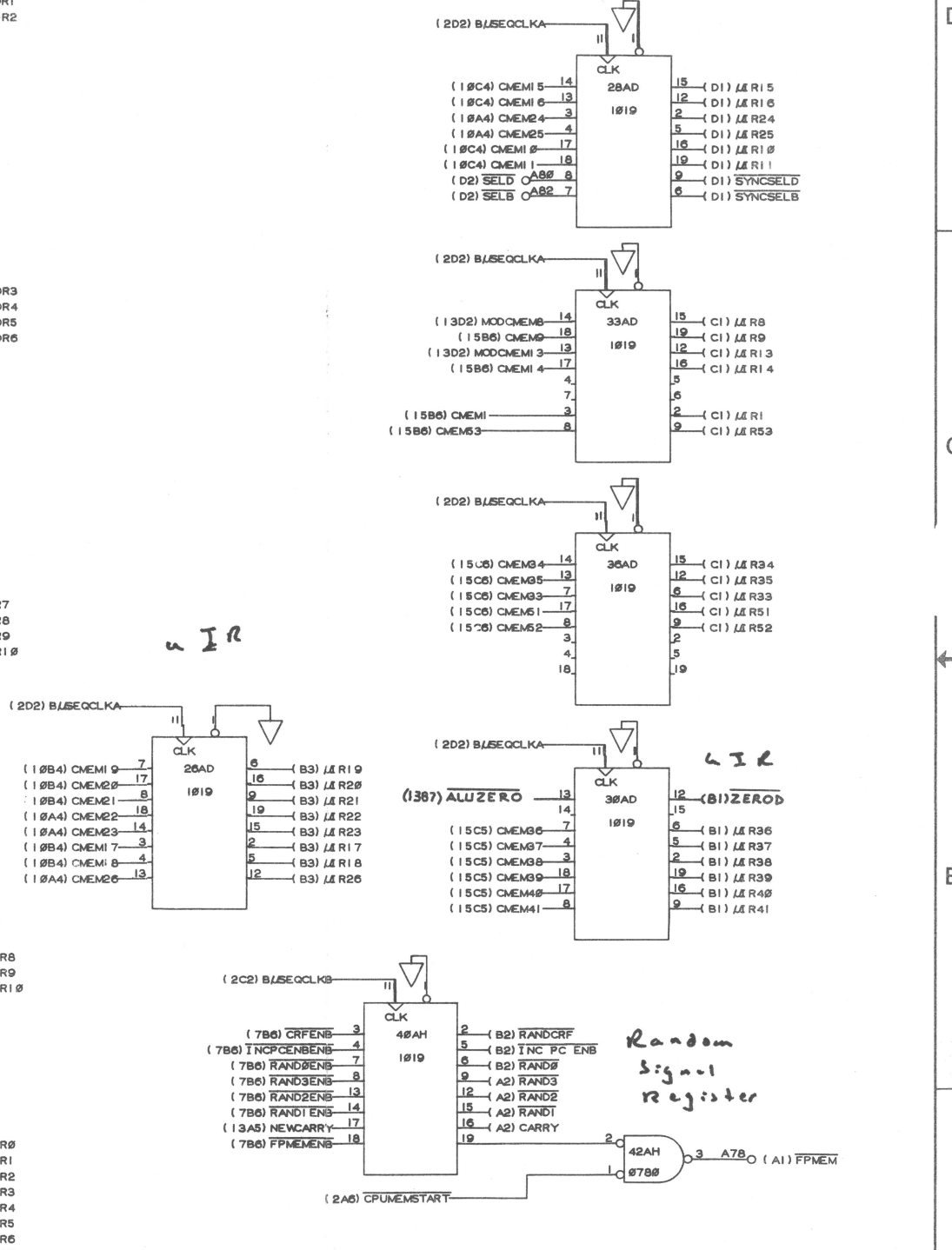


NOTE

	I/SEQ	C2	C1	C0
JUMP	0	0	0	0
PUSHJ	0	0	1	0
DECODE	0	1	0	0
SAGE	0	1	1	0
UNUSED	1	0	0	0
UNUSED	1	0	1	0
POPJ	1	1	0	0
CONTINUE	1	1	1	0



*used only for jump + pushj operation*



*Random signal register*

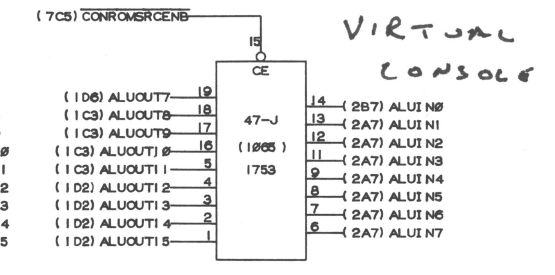
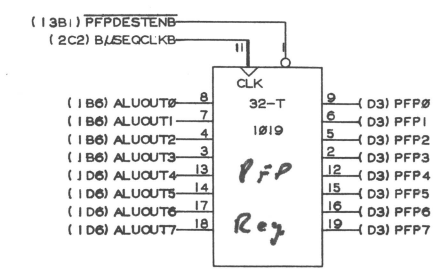
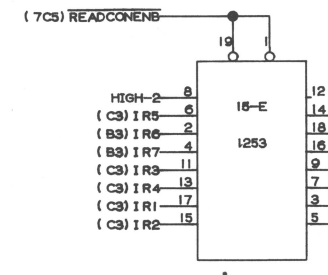
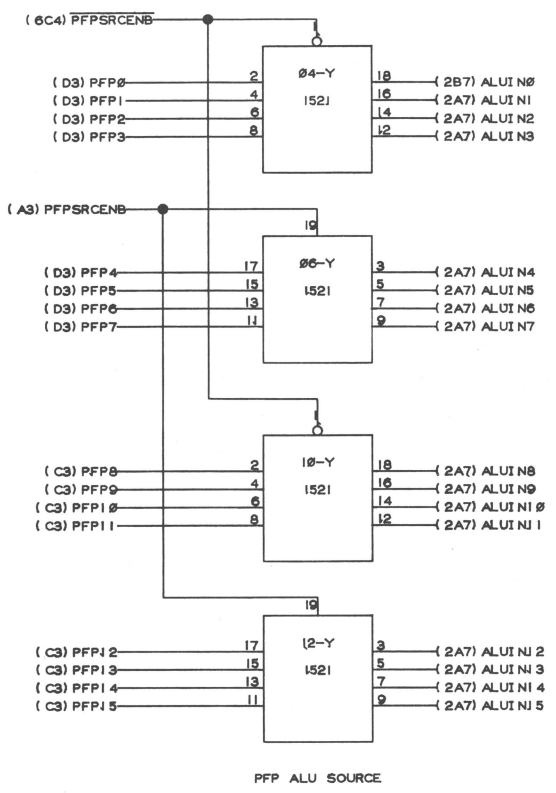
(MICRO IR AND MICRO SEQUENCER)

DRAWN		<b>DATA GENERAL CORPORATION</b> SOUTHBORO, MASSACHUSETTS 01772 TITLE <b>DGC NOVA</b>			
CHECKED					
ENGINEER					
APPROVED					
FIRST USED ON					
SIZE	D	CODE	001001624	REV	03

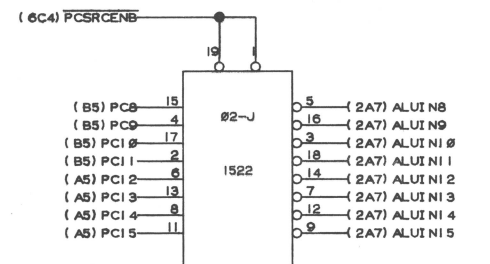
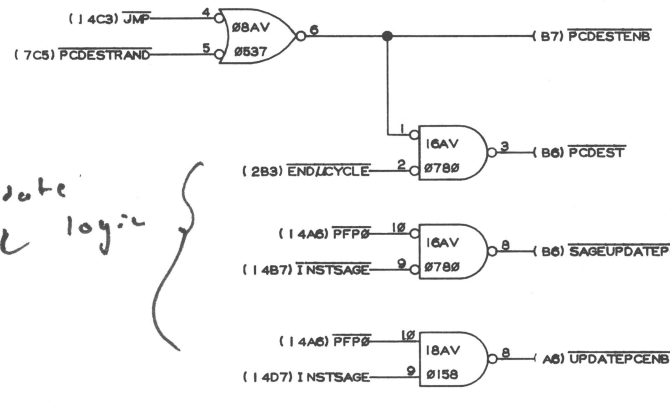
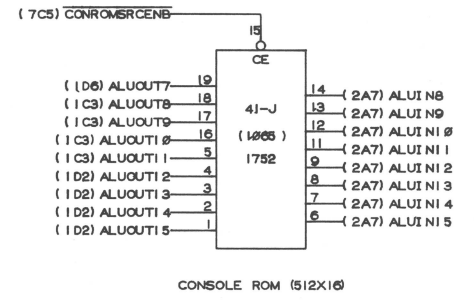
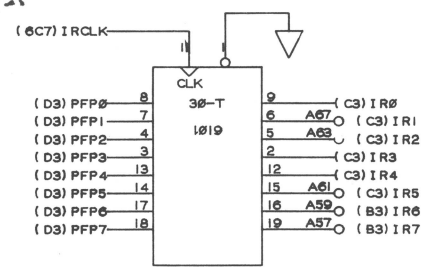
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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

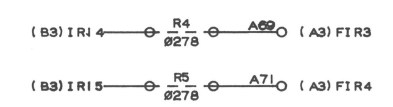
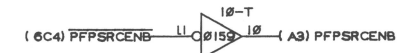
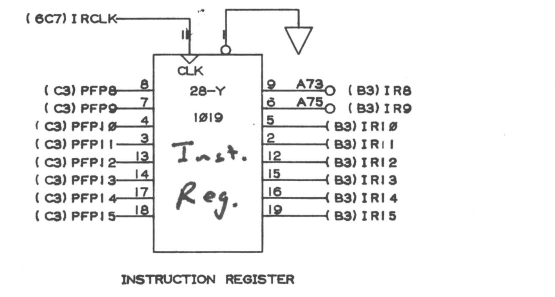
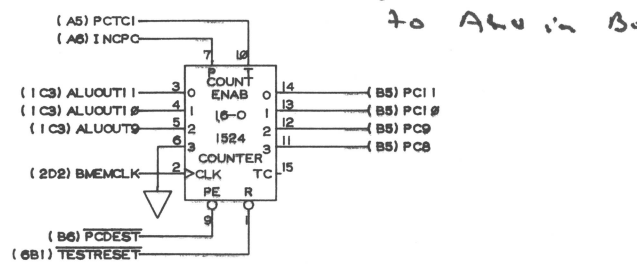
gates PFP to ALU in



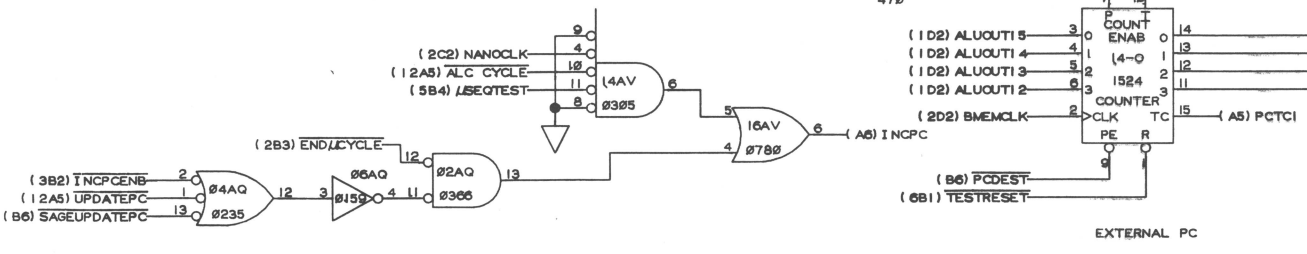
used during read switches



gate external PC to ALU in Bus



leave out



EXTERNAL PC Reg/Count

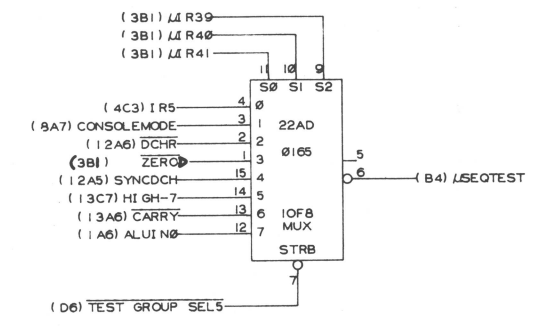
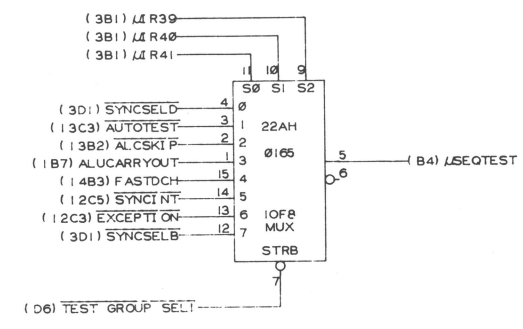
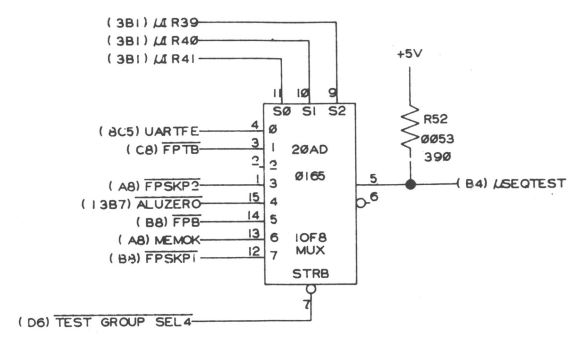
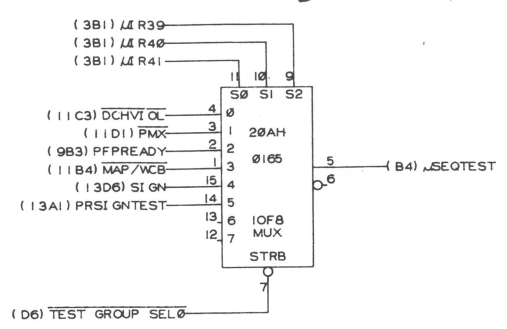
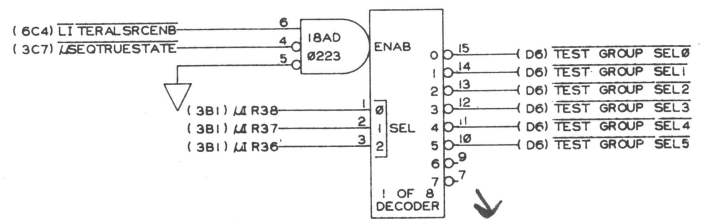
(PC, CONSOLE ROM, PFP SRC, PFP DEST IR)

DRAWN		<b>DATA GENERAL CORPORATION</b> SOUTHBORO, MASSACHUSETTS 01772 TITLE <b>DGC NOVA</b>
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		
SIZE	D	CODE 001001 DRAWING NUMBER 624 REV 03

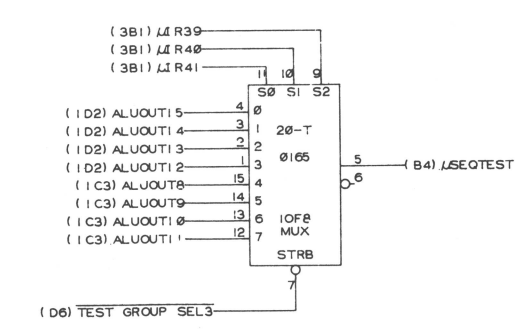
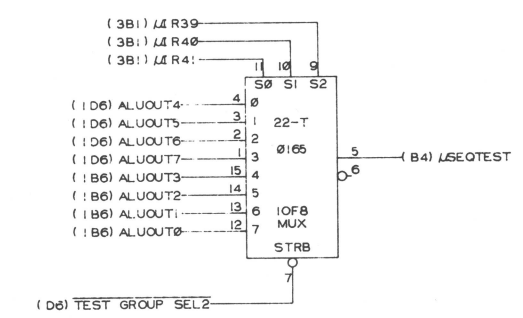
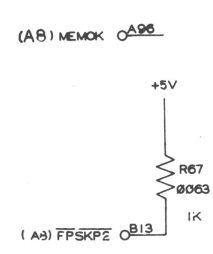
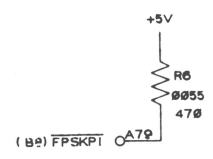
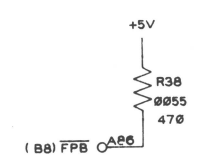
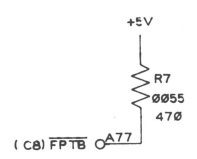


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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



SHEET 3 OF 9



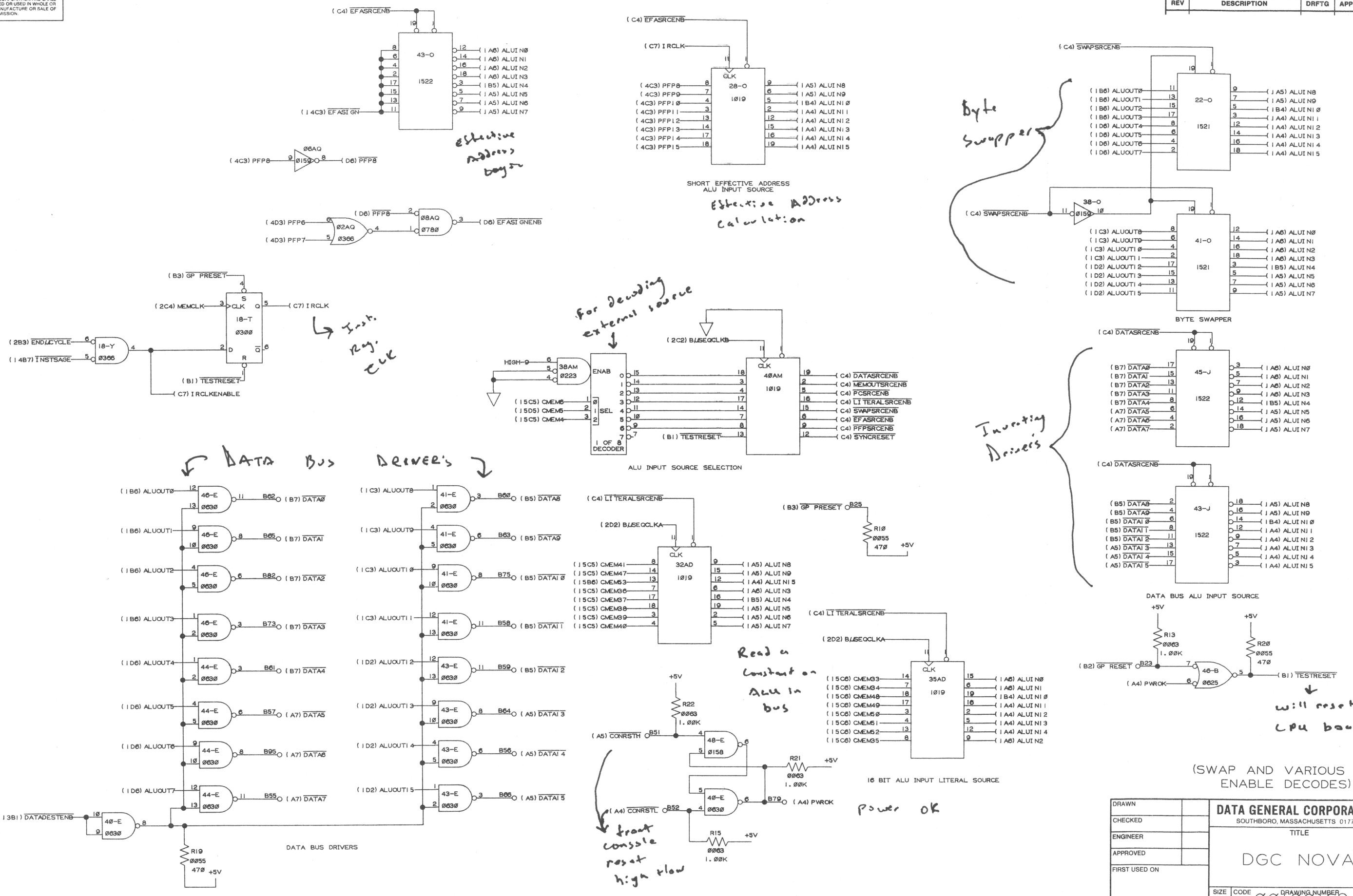
NOTE: TEST SELECTED BY THE SIGNAL TEST GROUP SELS ARE NEGATIVE ASSERTED ALL OTHER TESTS ARE POSITIVE ASSERTED

(DGC TEST MUX AND TEST CONDITIONS)

DRAWN		<b>DATA GENERAL CORPORATION</b>	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	001001624 03

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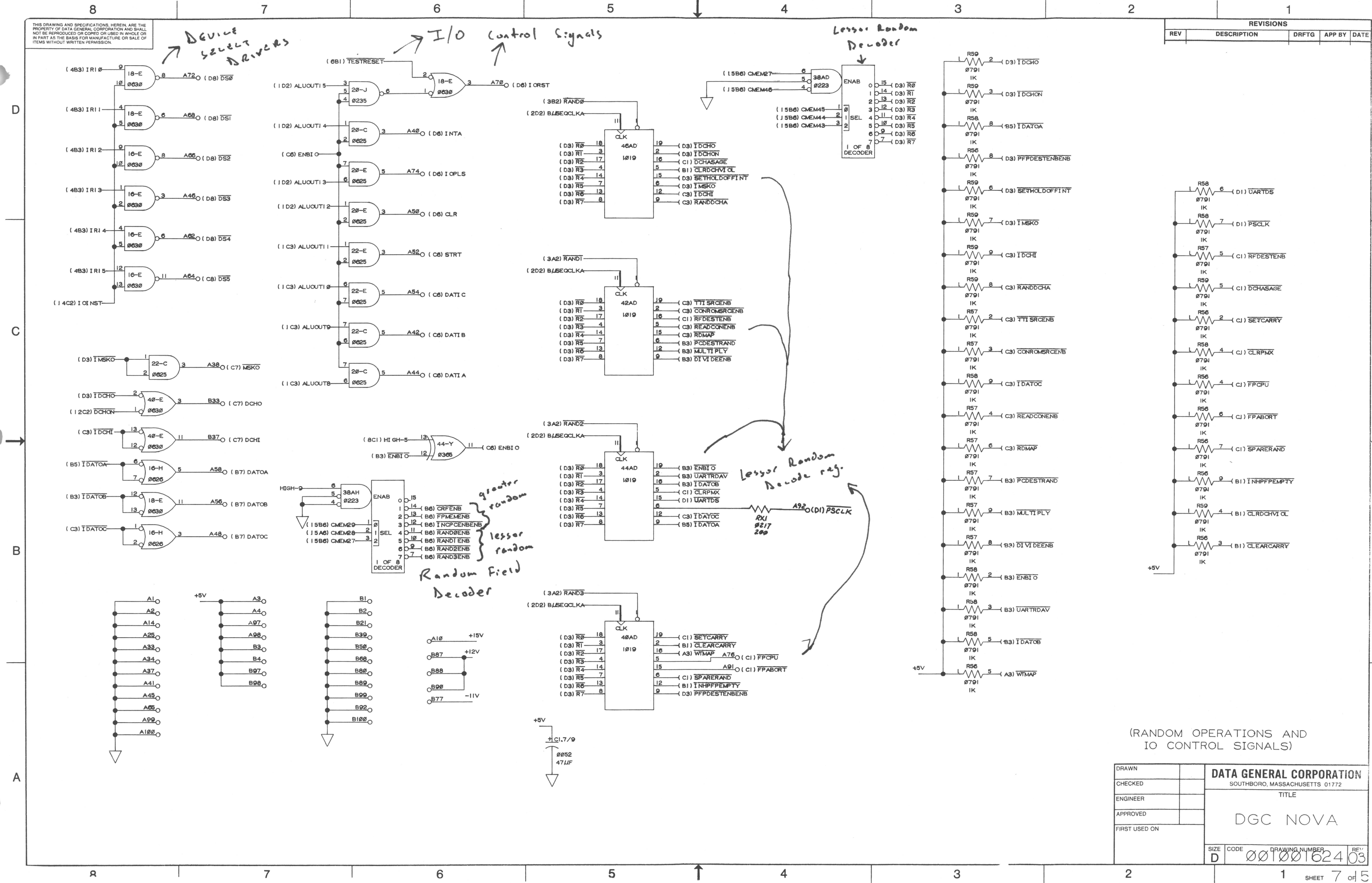
REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



DRAWN		<b>DATA GENERAL CORPORATION</b> SOUTHBORO, MASSACHUSETTS 01772 TITLE <b>DGC NOVA</b>			
CHECKED					
ENGINEER					
APPROVED					
FIRST USED ON					
SIZE	D	DRAWING NUMBER	001001624	REV	03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



(RANDOM OPERATIONS AND IO CONTROL SIGNALS)

DRAWN		<b>DATA GENERAL CORPORATION</b>		
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON		SIZE	CODE	DRAWING NUMBER
		D		001001624 03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

D

C

B

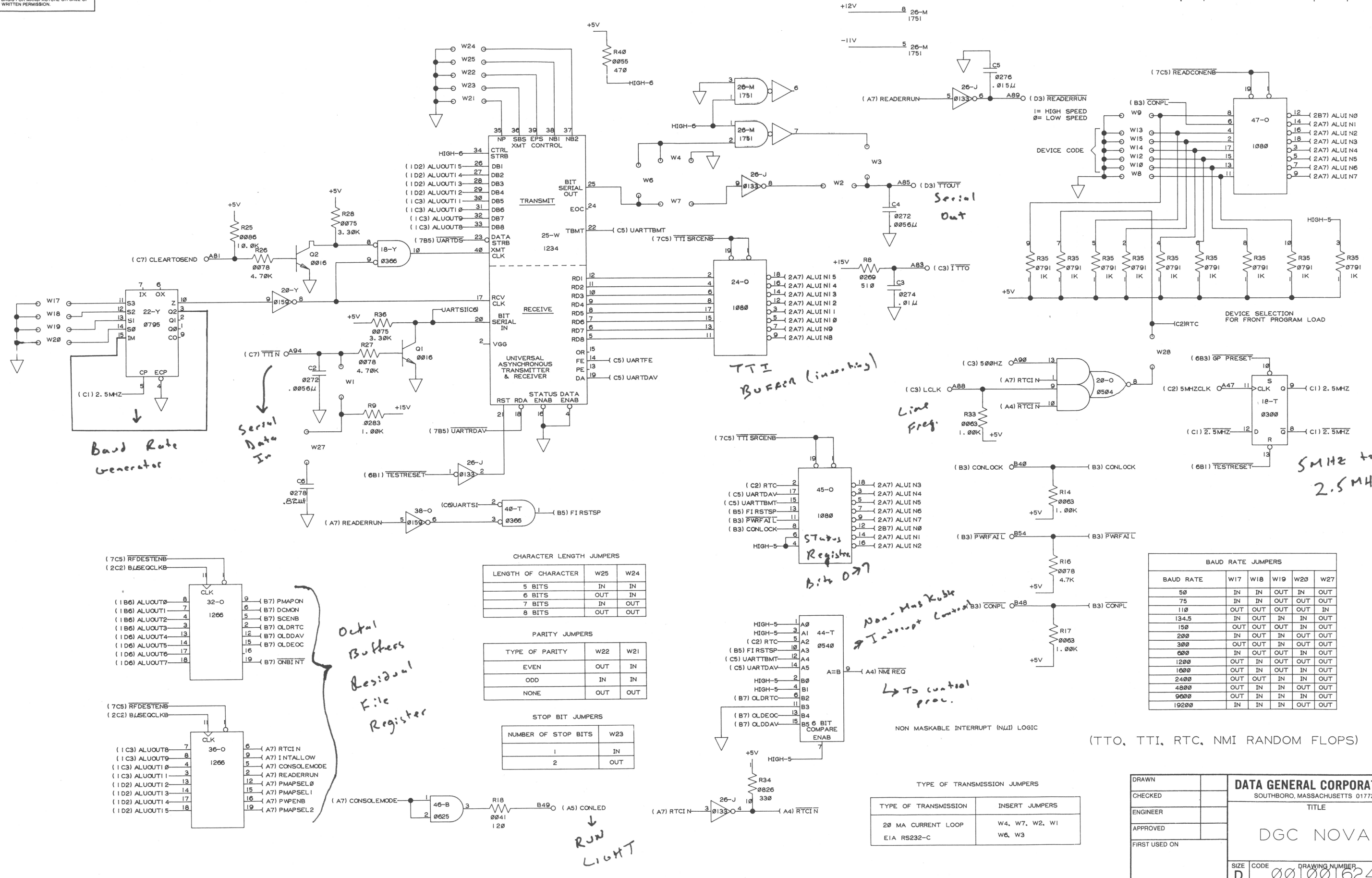
A

D

C

B

A



Baud Rate Generator

Serial Data In

Line Freq.

TTI Buffer (inserting)

Bit 0 > 7

Non-Maskable Interrupt Control  
→ To control proc.

Run Light

CHARACTER LENGTH JUMPERS

LENGTH OF CHARACTER	W25	W24
5 BITS	IN	IN
6 BITS	OUT	IN
7 BITS	IN	OUT
8 BITS	OUT	OUT

PARITY JUMPERS

TYPE OF PARITY	W22	W21
EVEN	OUT	IN
ODD	IN	IN
NONE	OUT	OUT

STOP BIT JUMPERS

NUMBER OF STOP BITS	W23
1	IN
2	OUT

TYPE OF TRANSMISSION JUMPERS

TYPE OF TRANSMISSION	INSERT JUMPERS
20 MA CURRENT LOOP	W4, W7, W2, W1
EIA RS232-C	W6, W3

BAUD RATE JUMPERS

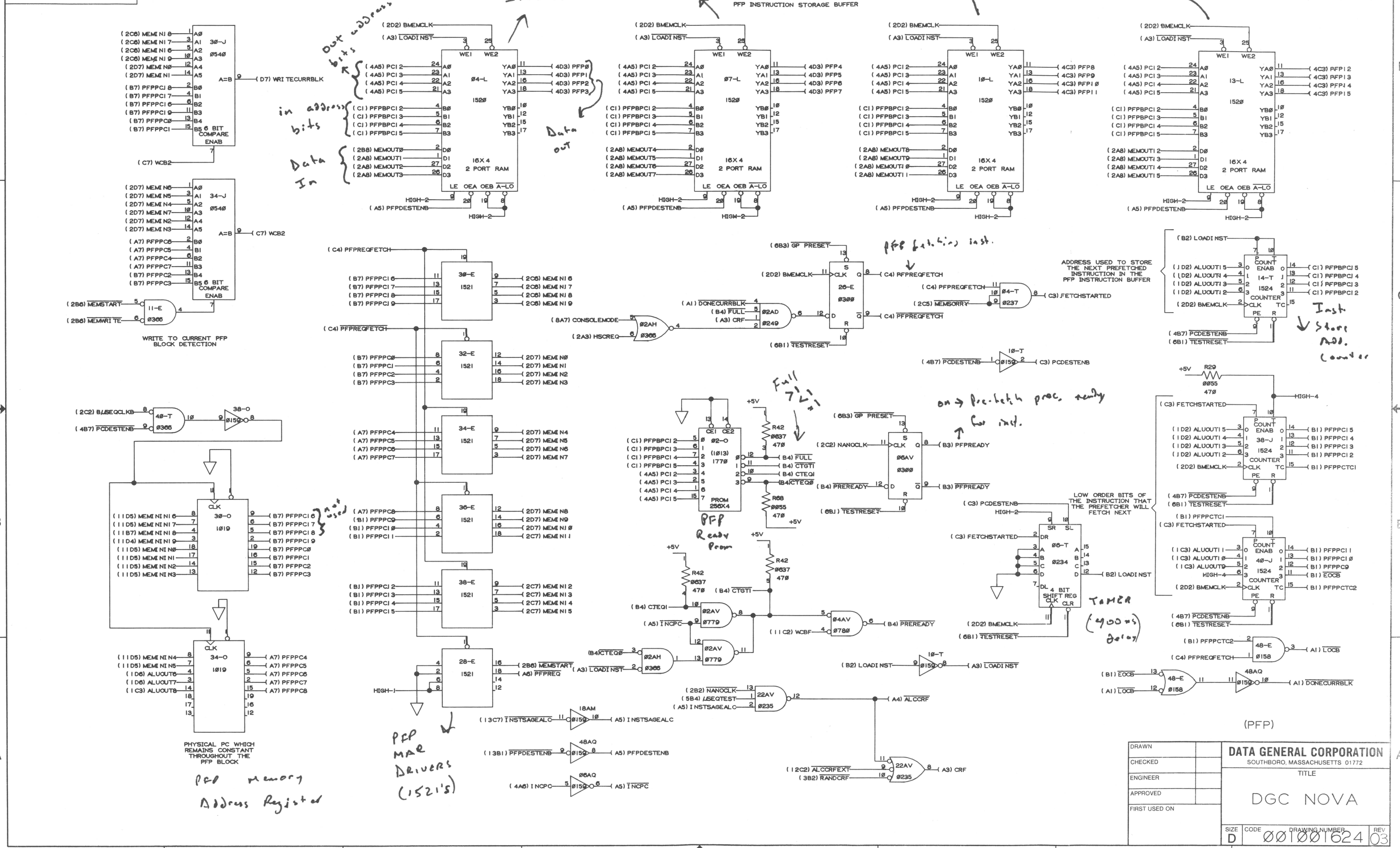
BAUD RATE	W17	W18	W19	W20	W27
50	IN	IN	OUT	IN	OUT
75	IN	IN	OUT	OUT	OUT
110	OUT	OUT	OUT	OUT	IN
134.5	IN	OUT	IN	IN	OUT
150	OUT	OUT	IN	IN	OUT
200	IN	OUT	IN	OUT	OUT
300	OUT	OUT	IN	OUT	OUT
600	IN	OUT	OUT	IN	OUT
1200	OUT	IN	OUT	OUT	OUT
1600	OUT	IN	OUT	IN	OUT
2400	OUT	OUT	IN	IN	OUT
4800	OUT	IN	IN	OUT	OUT
9600	OUT	IN	IN	IN	OUT
19200	IN	IN	IN	OUT	OUT

(TTO, TTI, RTC, NMI RANDOM FLOPS)

DRAWN		<b>DATA GENERAL CORPORATION</b> SOUTHBORO, MASSACHUSETTS 01772  TITLE  <b>DGC NOVA</b>	
CHECKED			
ENGINEER			
APPROVED			
FIRST USED ON			
SIZE	CODE	DRAWING NUMBER	REV
D		001001624	03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



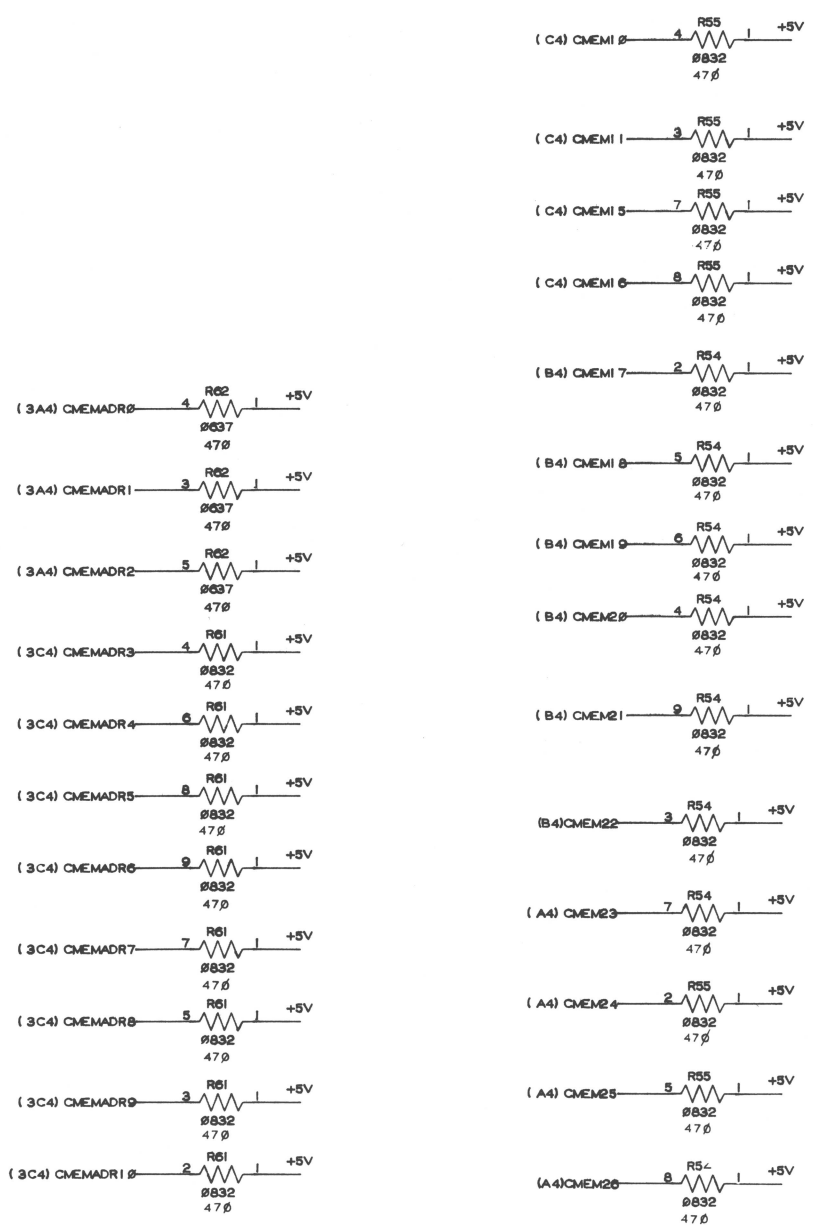
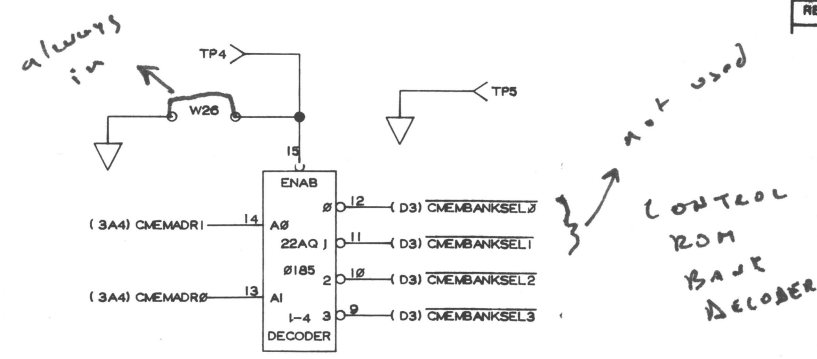
6/19/72

DRAWN		DATA GENERAL CORPORATION		
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON		SIZE	CODE	DRAWING NUMBER
		D	0010001624	REV 03



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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



(CONTROL ROMARRAY)

DRAWN		<b>DATA GENERAL CORPORATION</b>		
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON				
SIZE	D	CODE	DRAWING NUMBER	REV
			001001624	03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

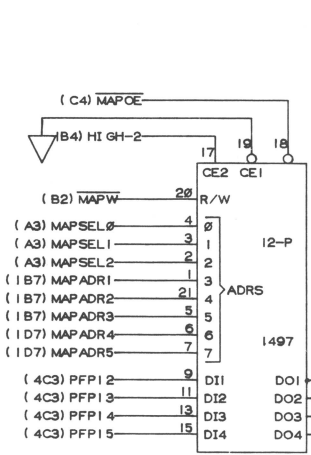
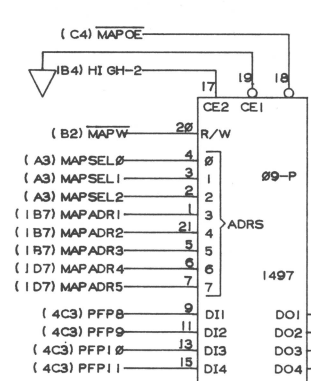
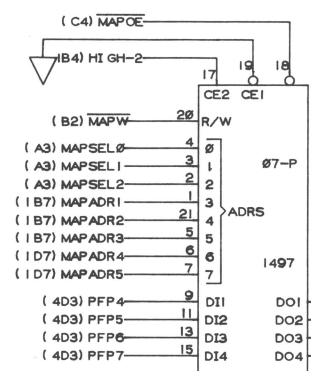
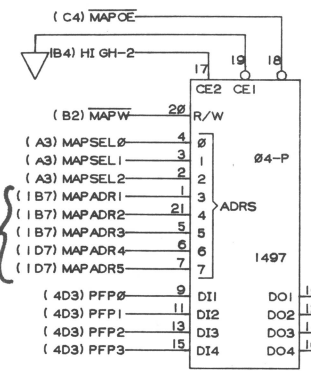
ALL OUT 1-5

Scratch Pad RAMS

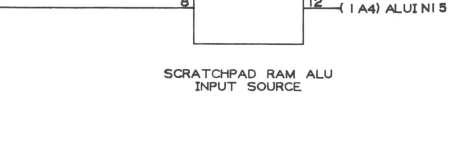
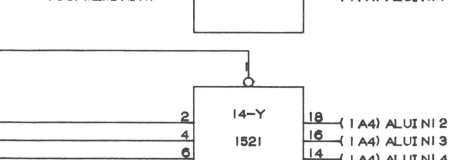
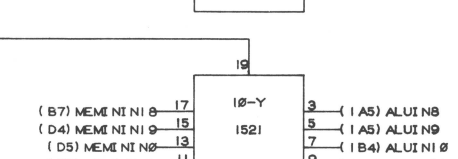
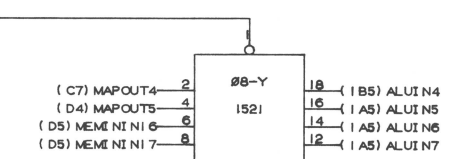
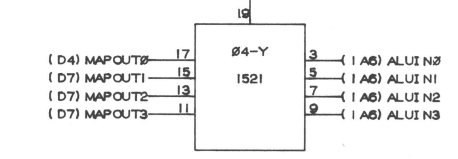
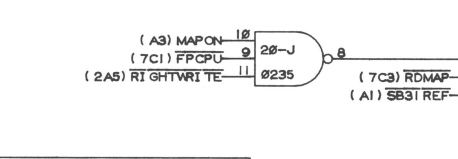
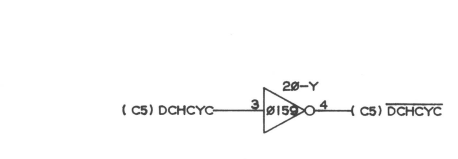
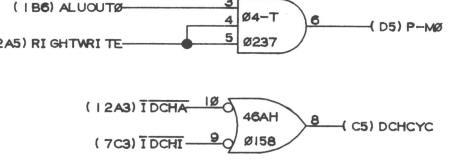
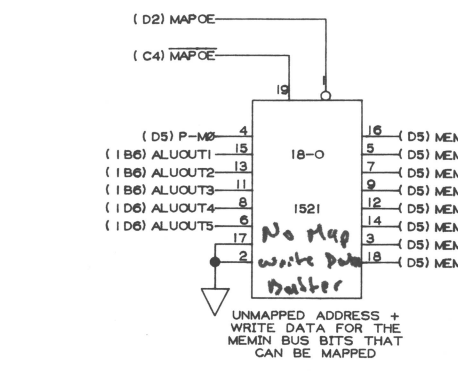
No Map write Data Buffer  
UNMAPPED ADDRESS + WRITE DATA FOR THE MEMIN BUS BITS THAT CAN BE MAPPED

MAPSEL

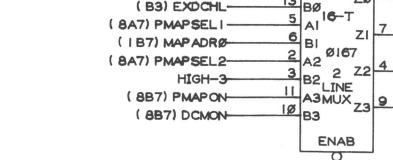
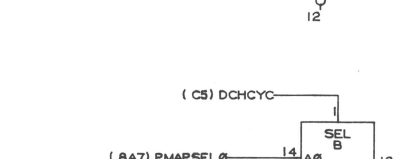
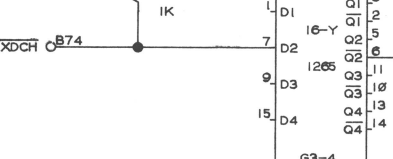
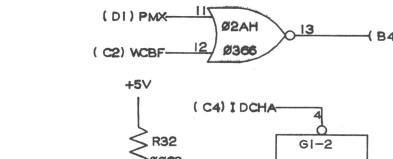
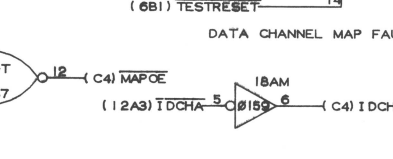
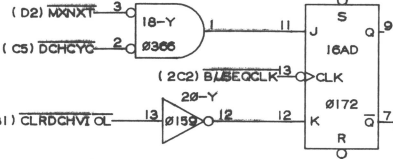
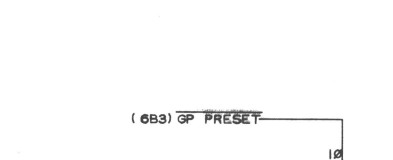
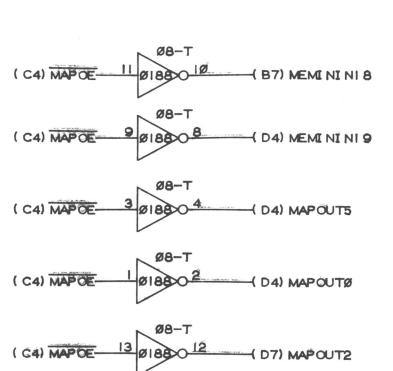
0	1	2	
0	0	0	Program A
0	0	1	DCH A
0	1	0	Program B
0	1	1	DCH B
1	0	0	Console
1	0	1	"
1	1	0	"
1	1	1	"



256X16 SCRATCHPAD RAM INCLUDES MAP ENTRIES



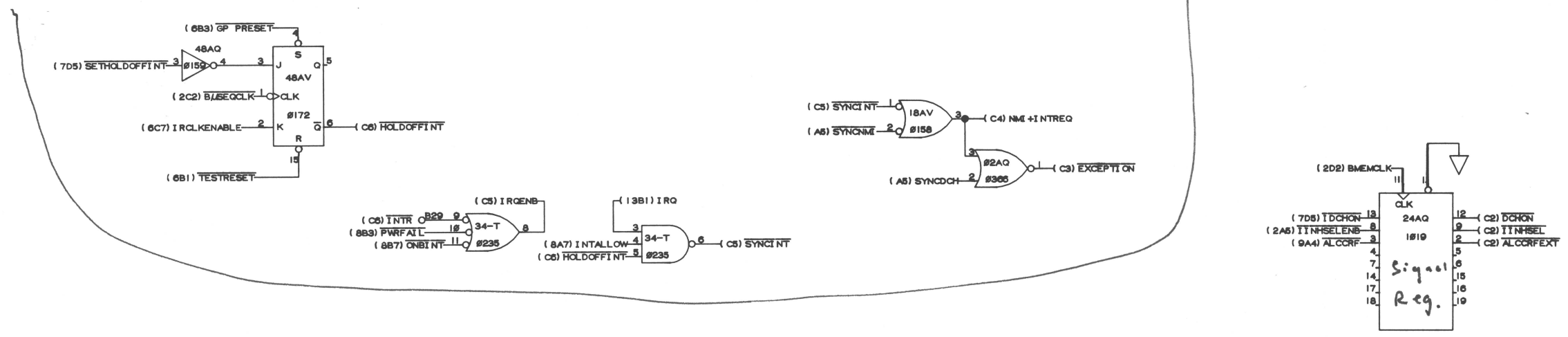
SCRATCHPAD RAM ALU INPUT SOURCE



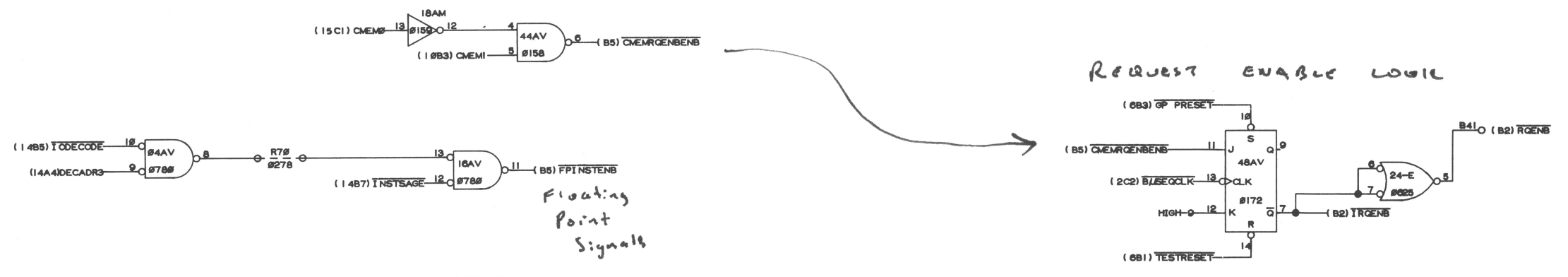
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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

### INTERUPT LOGIC



### REQUEST ENABLE LOGIC



Floating Point Signals

(MEMORY CONTROL, DATA CHANNEL LOGIC, INTERRUPT LOGIC)

### Data Channel signals



DRAWN		<b>DATA GENERAL CORPORATION</b>		
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON		SIZE	CODE	DRAWING NUMBER
		D		001001624103

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

Mult/Div. Logic

Used during ALL Inst.

ALL Fill IN LOGIC

ALL (stuff) Fill IN LOGIC

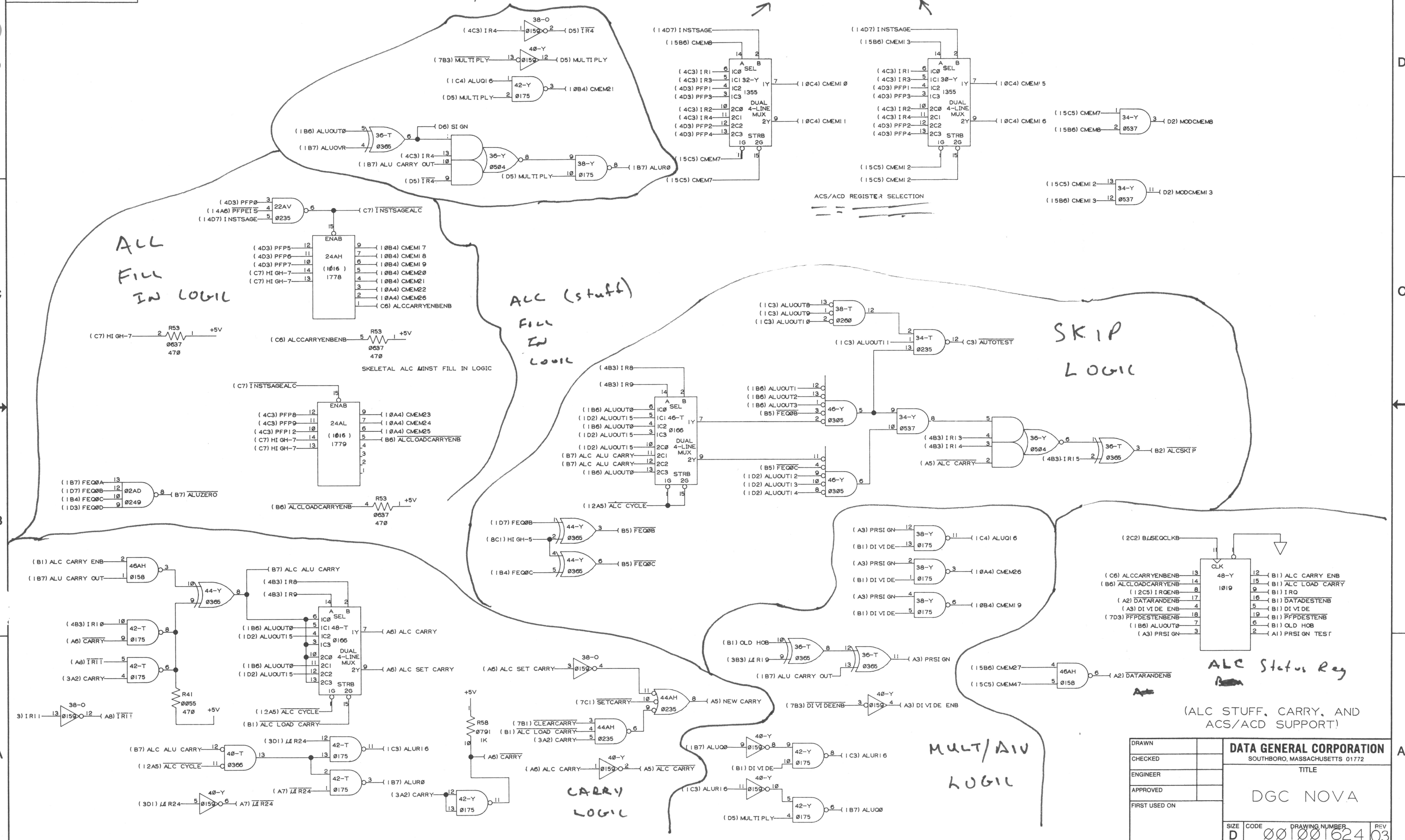
SKIP LOGIC

MULT/DIV LOGIC

CARRY LOGIC

ALC Status Reg

(ALC STUFF, CARRY, AND ACS/ACD SUPPORT)



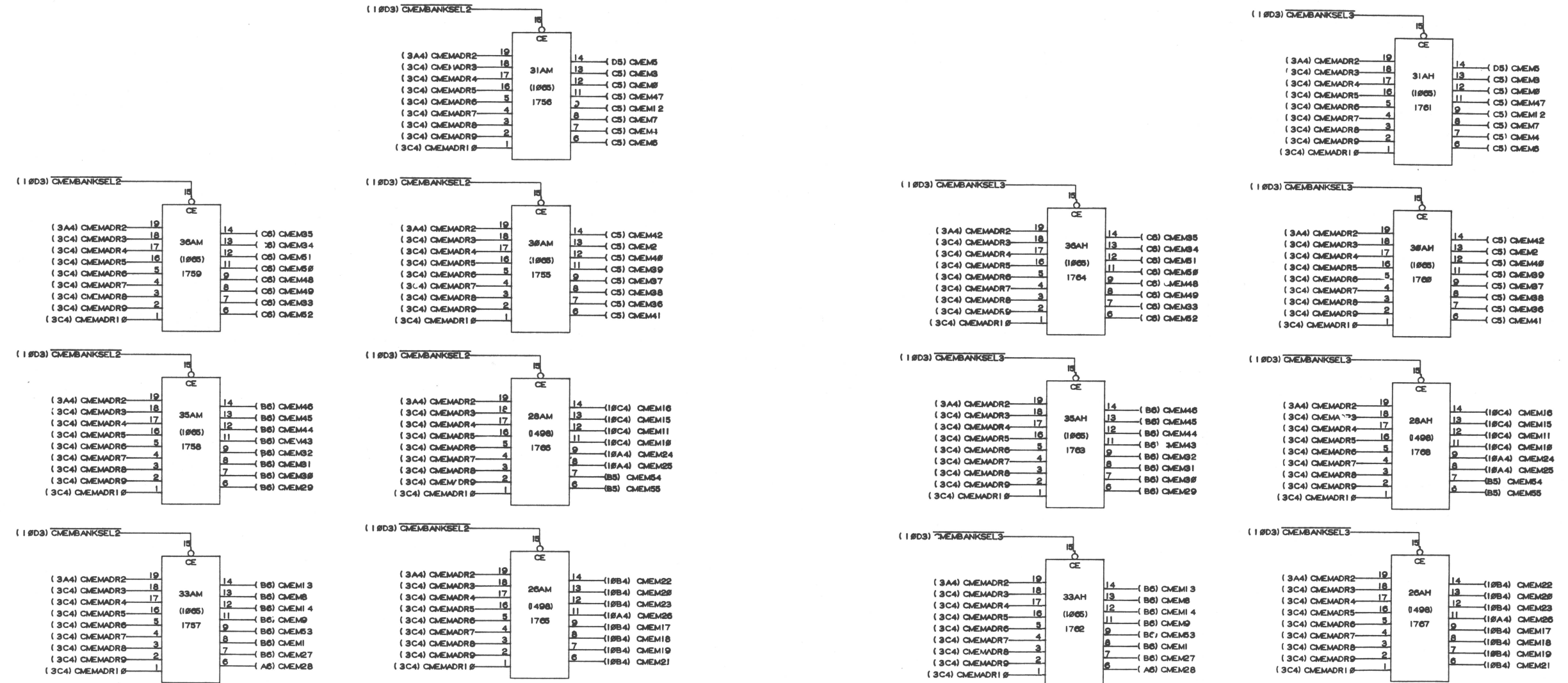
DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		REV	
SIZE	D	CODE	001001624 03





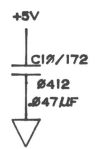
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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



Bank #2

CONTROL MEMORY ADDRESSES 2900<sub>8</sub> TO 2777<sub>8</sub>



CONTROL MEMORY ADDRESSES 3000<sub>8</sub> TO 3777<sub>8</sub>

Bank #3

(CONTROL ROMARRAY)

DRAWN		<b>DATA GENERAL CORPORATION</b> SOUTHBORO, MASSACHUSETTS 01772 TITLE <b>DGC NOVA</b> SIZE CODE 00100162403
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		
D	00100162403	REV