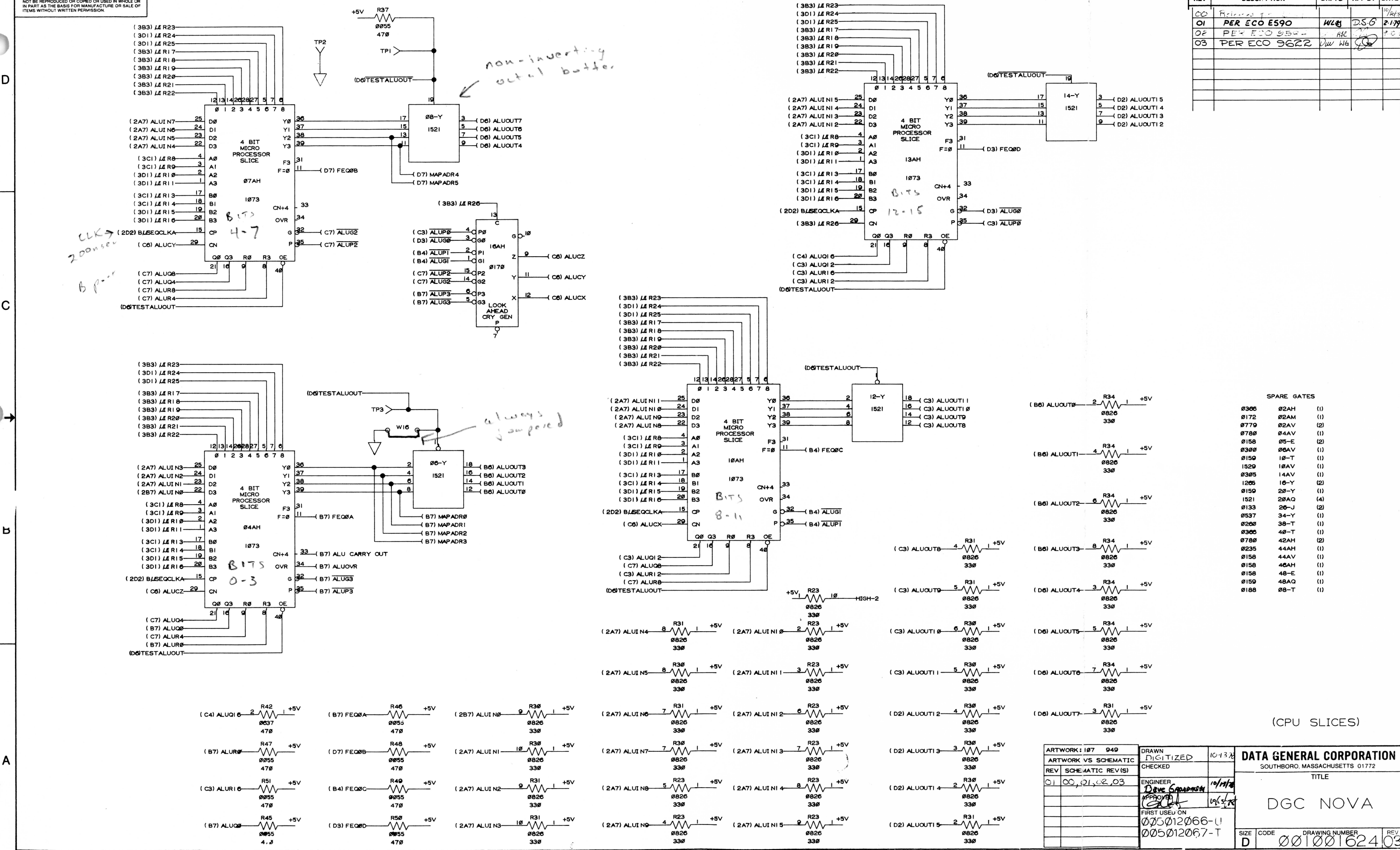


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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE
00	Released for			10/1/78
01	PER ECO E590	WLG	DSG	2-1-79
02	PER ECO 952		AKC	
03	PER ECO 9622	DW	Wg	



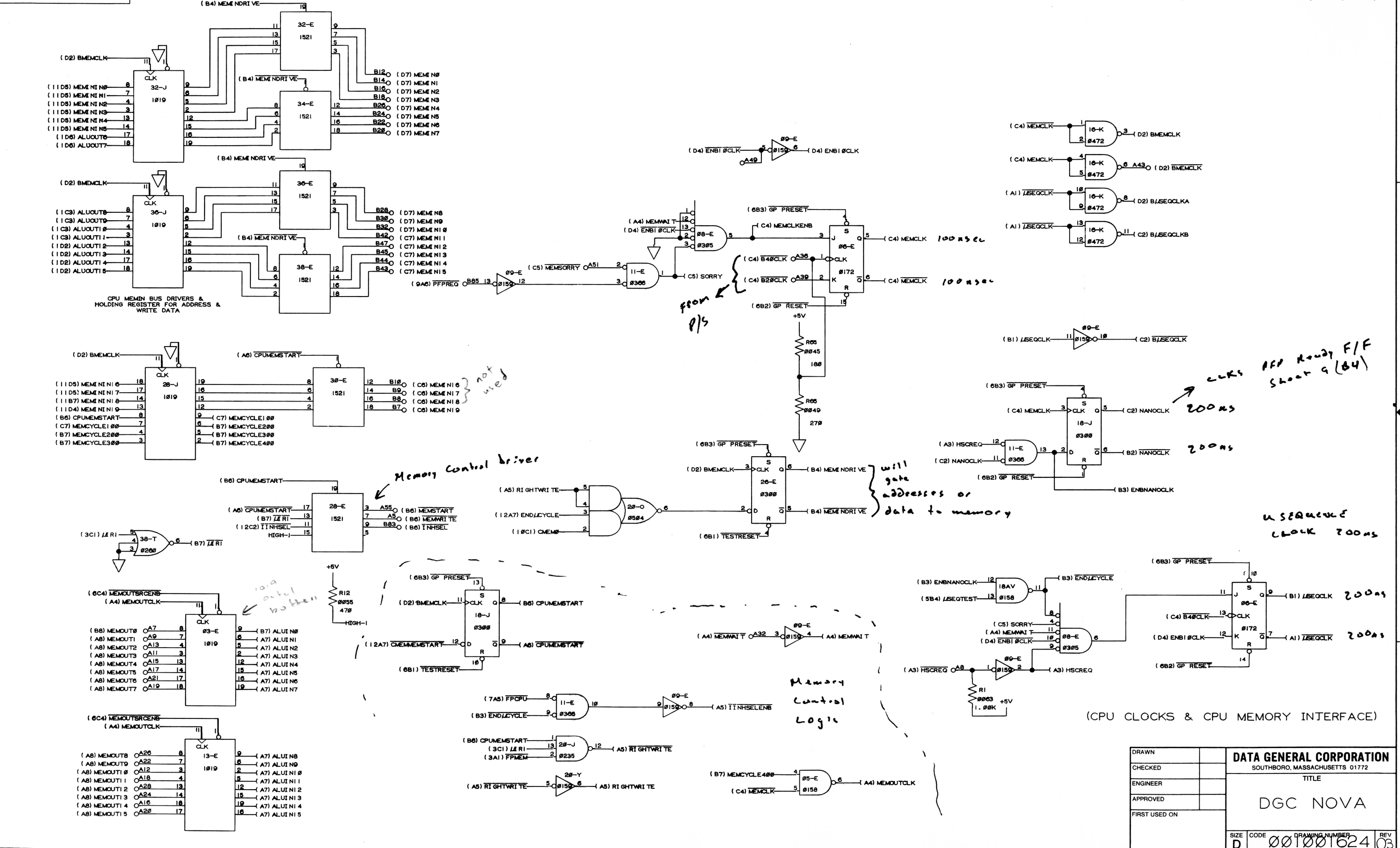
SPARE GATES

0306	02AH	(1)
0172	02AM	(1)
0779	02AV	(2)
0780	04AV	(1)
0158	05-E	(2)
0300	06AV	(1)
0150	10-T	(1)
0305	10AV	(1)
1205	16-Y	(2)
0150	20-Y	(1)
0133	20AQ	(4)
0537	20-J	(2)
0206	34-Y	(1)
0300	38-T	(1)
0780	40-T	(1)
0235	42AH	(2)
0158	44AH	(1)
0158	44AV	(1)
0158	46AH	(1)
0158	48-E	(1)
0150	48AQ	(1)
0188	08-T	(1)

ARTWORK: 107 949	DRAWN: DIGITIZED 10-13-78	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772
ARTWORK VS SCHEMATIC	CHECKED	
REV SCHEMATIC REV(S)	ENGINEER: Dave Scambata 10/1/78	TITLE: DGC NOVA
01 00, 01, 02, 03	APPROVED: [Signature]	SIZE: CODE: DRAWING NUMBER: REV: 001001624103
	FIRST USE ON: 005012066-U	
	005012067-T	

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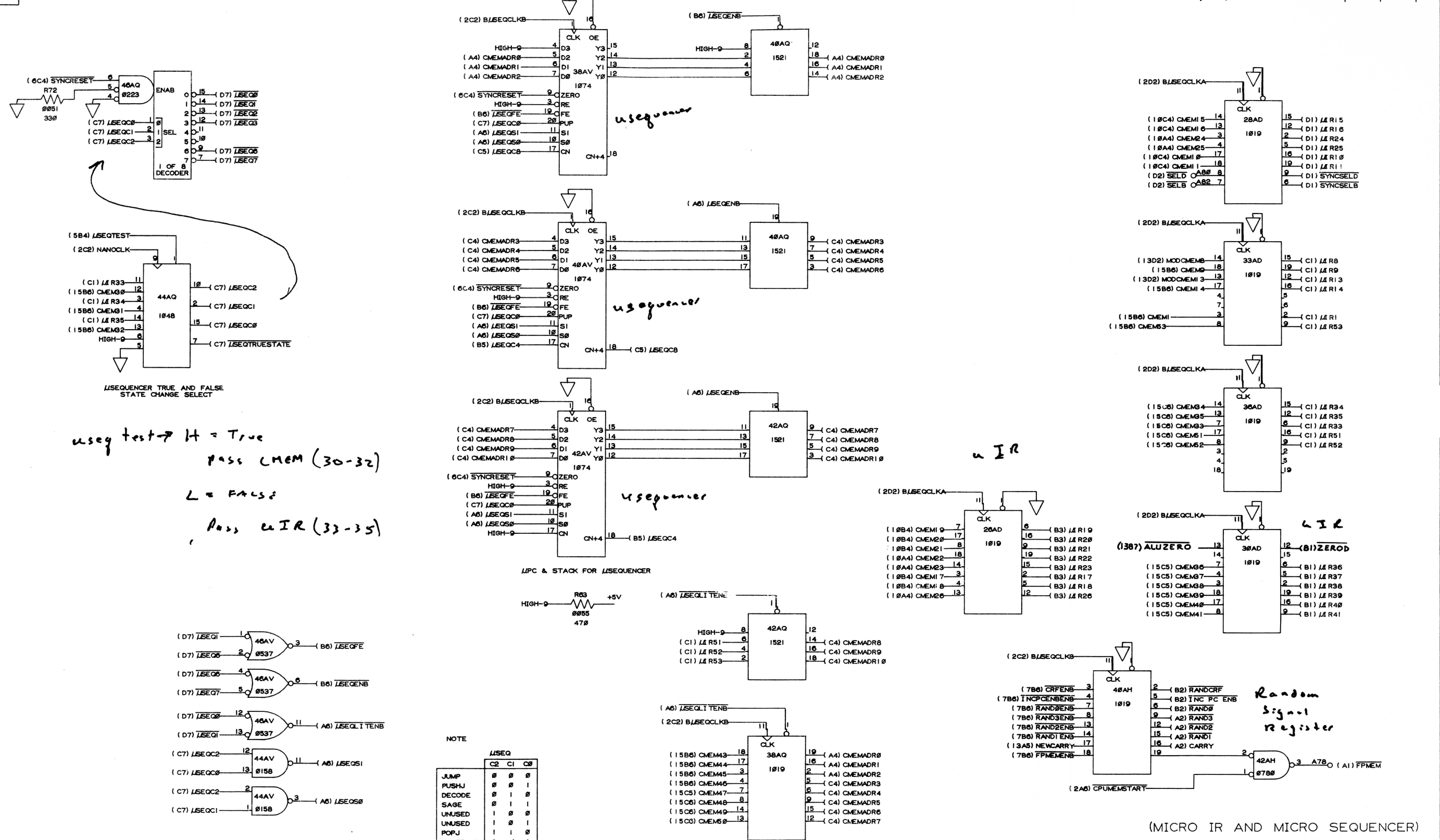
REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE



DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON			
SIZE	D	CODE	001001624
		DRAWING NUMBER	03

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



*u seq test -> H = True
pass MEM (30-32)
L = False
Pass u IR (33-35)*

*used only for
jump + push
operation*

NOTE

	ISEQ	C2	C1	C0
JUMP	0	0	0	0
PUSHJ	0	0	1	1
DECODE	0	1	1	1
SAGE	0	1	1	1
UNUSED	1	0	1	1
UNUSED	1	0	1	1
POPJ	1	1	1	1
CONTINUE	1	1	1	1

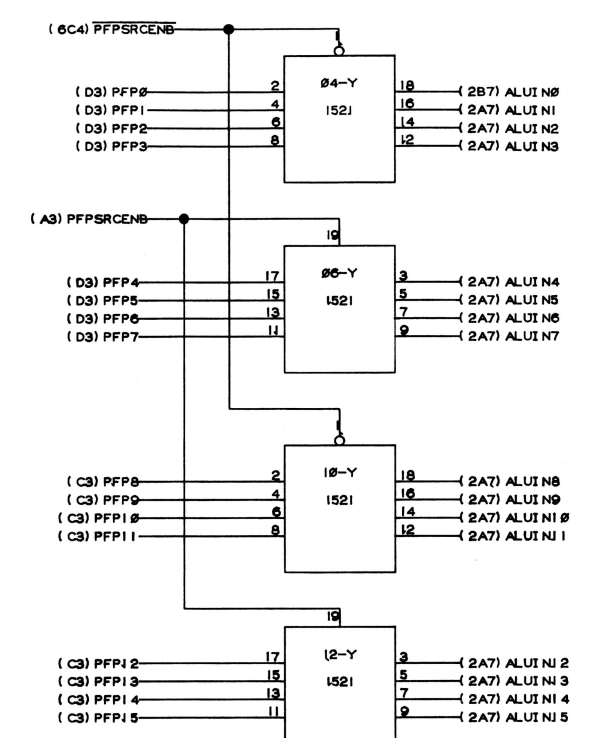
(MICRO IR AND MICRO SEQUENCER)

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	001001624
		DRAWING NUMBER	REV
			03

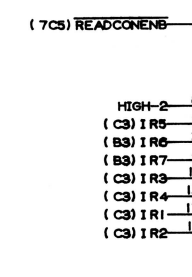
THIS DRAWING AND SPECIFICATIONS, HEREIN ARE THE PROPERTY OF DATA GENERAL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

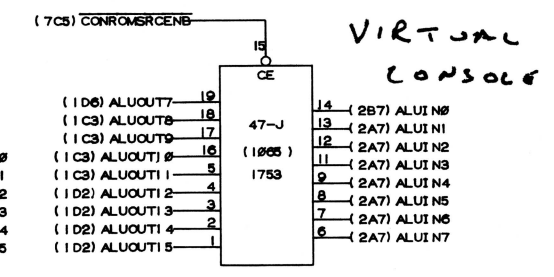
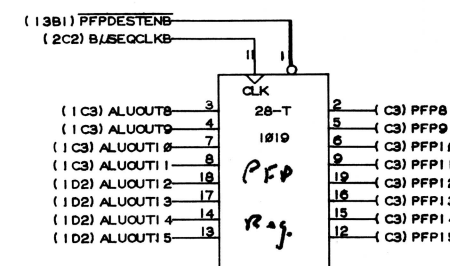
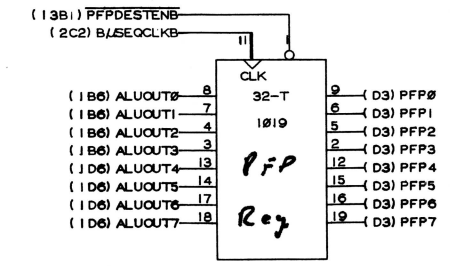
gates PFP to ALUin



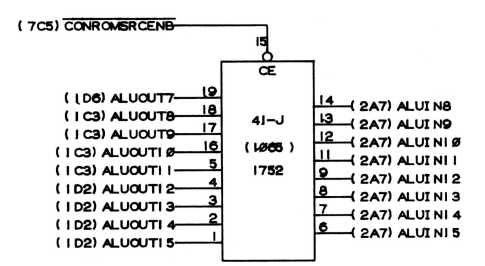
PFP ALU SOURCE



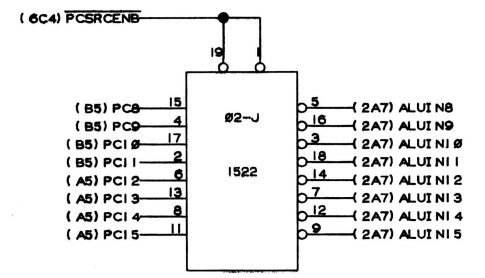
used during read switch int.



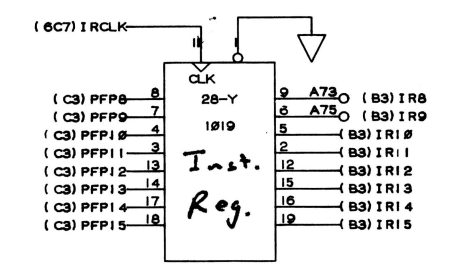
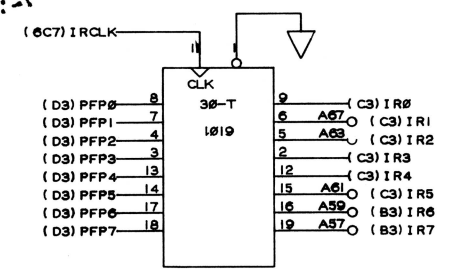
VIRTUAL CONSOLE



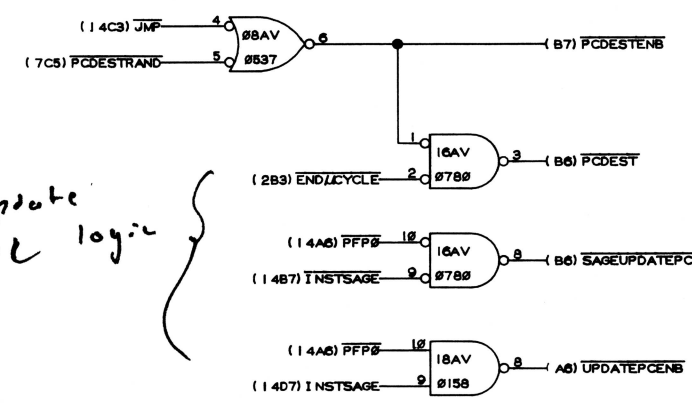
CONSOLE ROM (512X10)



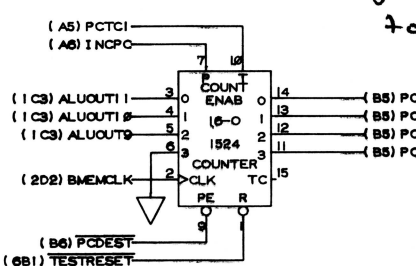
gate external PC to ALUin Bus.



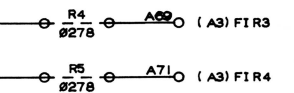
INSTRUCTION REGISTER



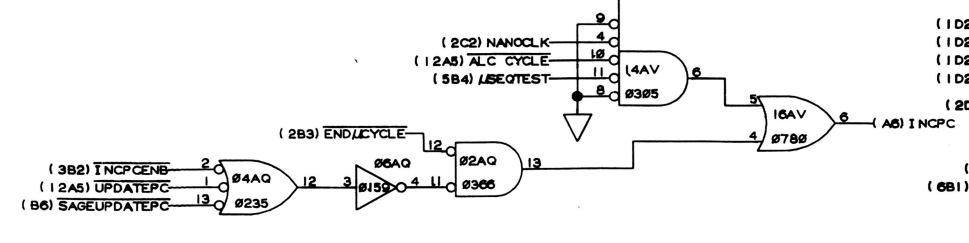
update PC logic



EXTERNAL PC Reg/Count



leave out



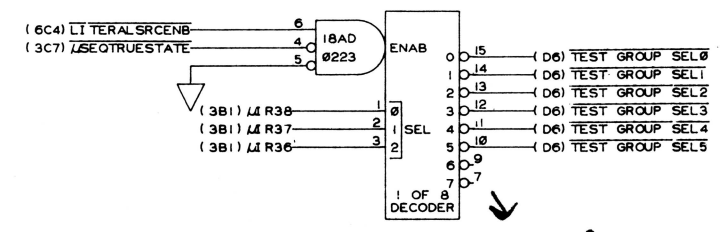
EXTERNAL PC

(PC, CONSOLE ROM, PFP SRC, PFP DEST IR)

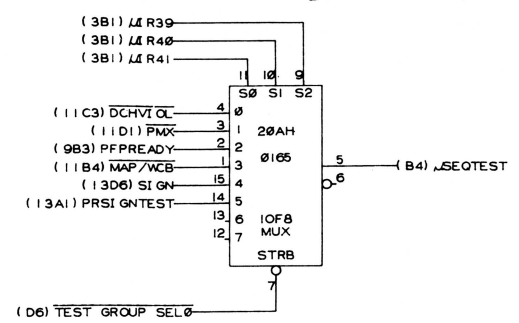
DRAWN		DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 TITLE DGC NOVA			
CHECKED					
ENGINEER					
APPROVED					
FIRST USED ON					
SIZE	D	DRAWING NUMBER	001001624	REV	03

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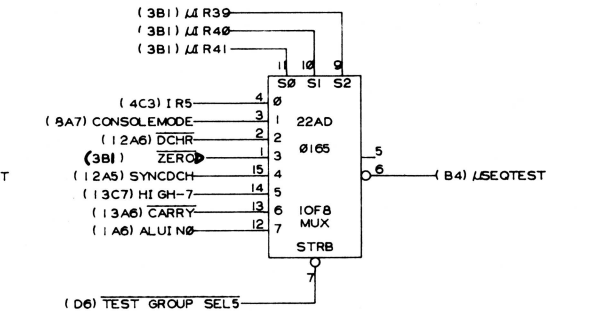
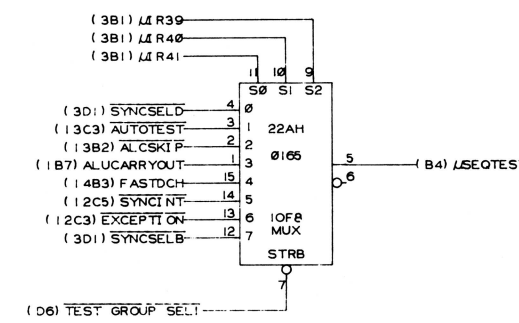
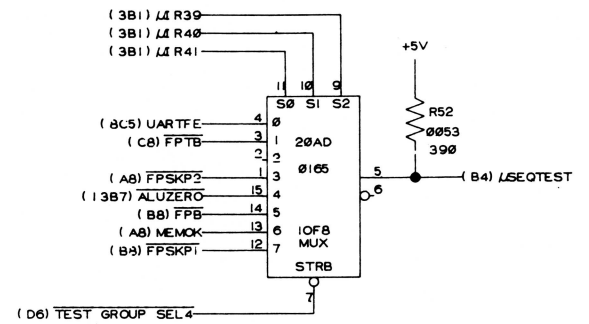
REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



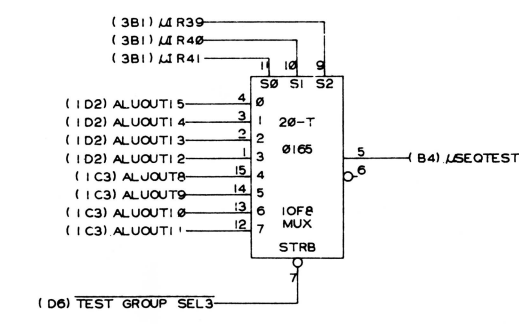
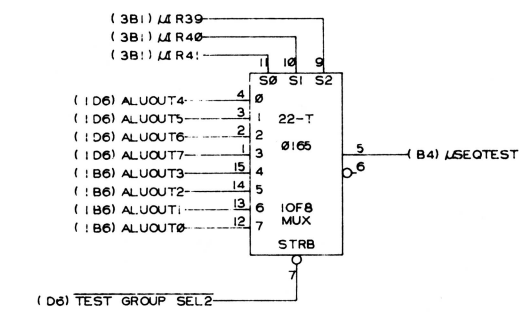
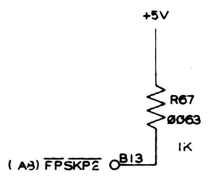
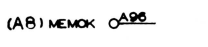
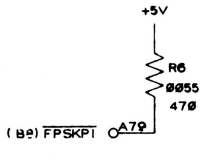
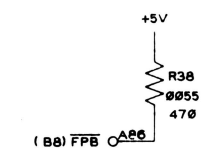
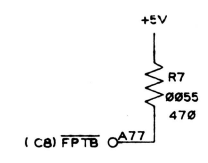
Test Group Decode - will select 1 of 8 Mux's.



Will select 1 of 3 signals to test



Sheet 3 of 9



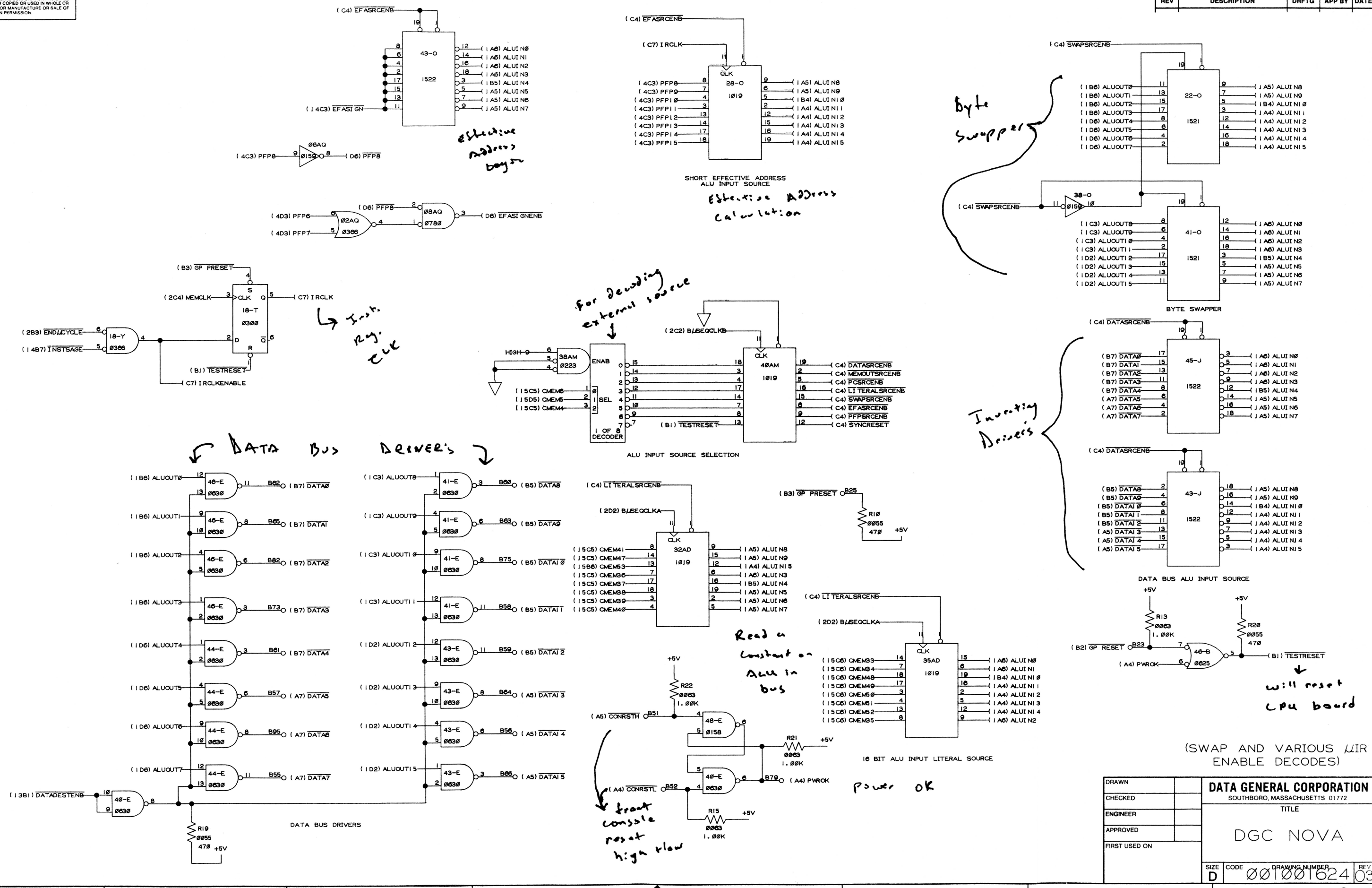
NOTE TEST SELECTED BY THE SIGNAL TEST GROUP SELS ARE NEGATIVE ASSERTED ALL OTHER TESTS ARE POSITIVE ASSERTED

(DGC TEST MUX AND TEST CONDITIONS)

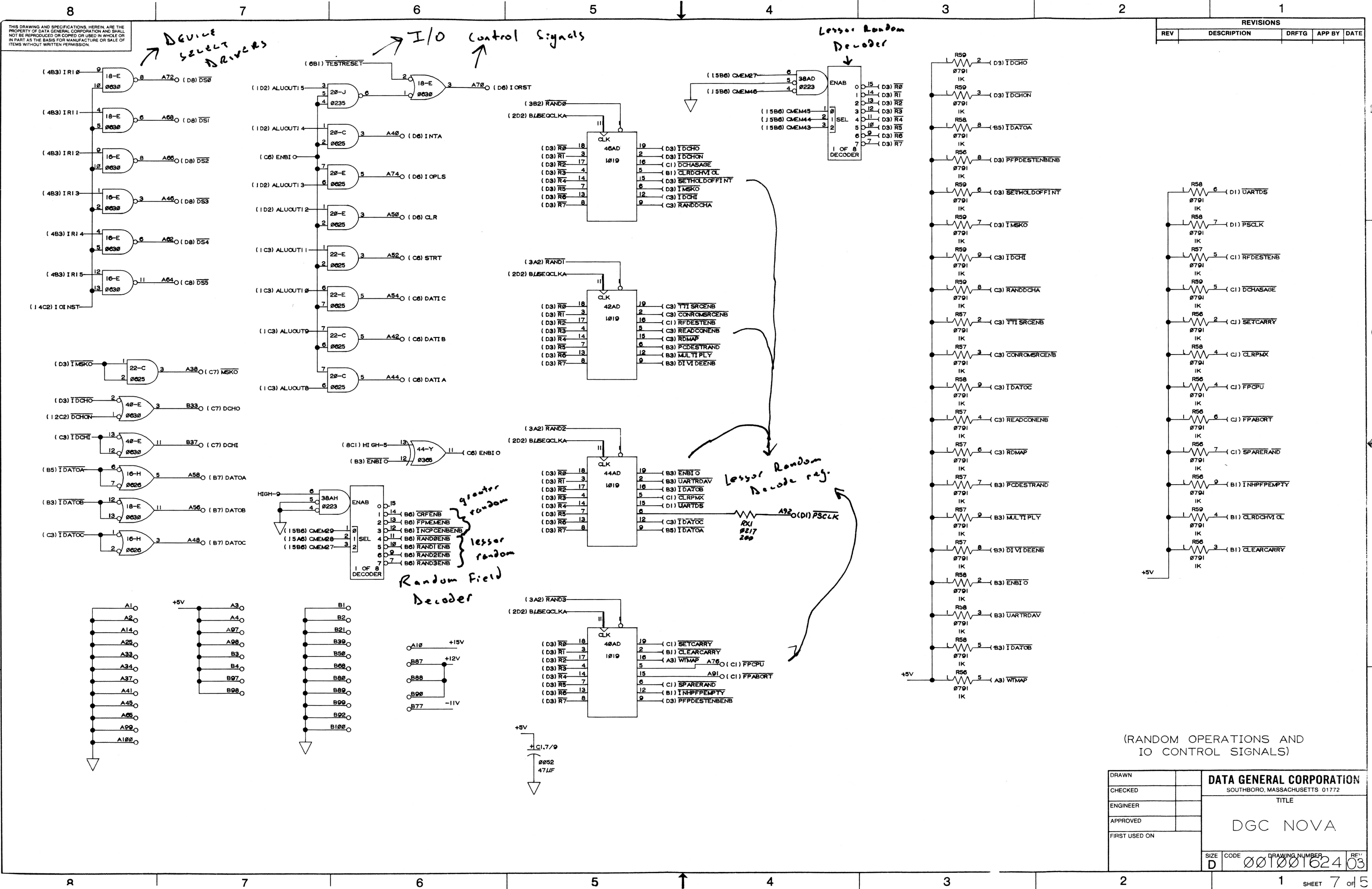
DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	001001624

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REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE



DRAWN		DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 TITLE DGC NOVA	
CHECKED			
ENGINEER			
APPROVED			
FIRST USED ON			
SIZE	CODE	DRAWING NUMBER	REV
D		001001624	03



REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

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Device Select Drivers

I/O Control Signals

Lesser Random Decoder

greater random
lesser random
Random Field Decoder

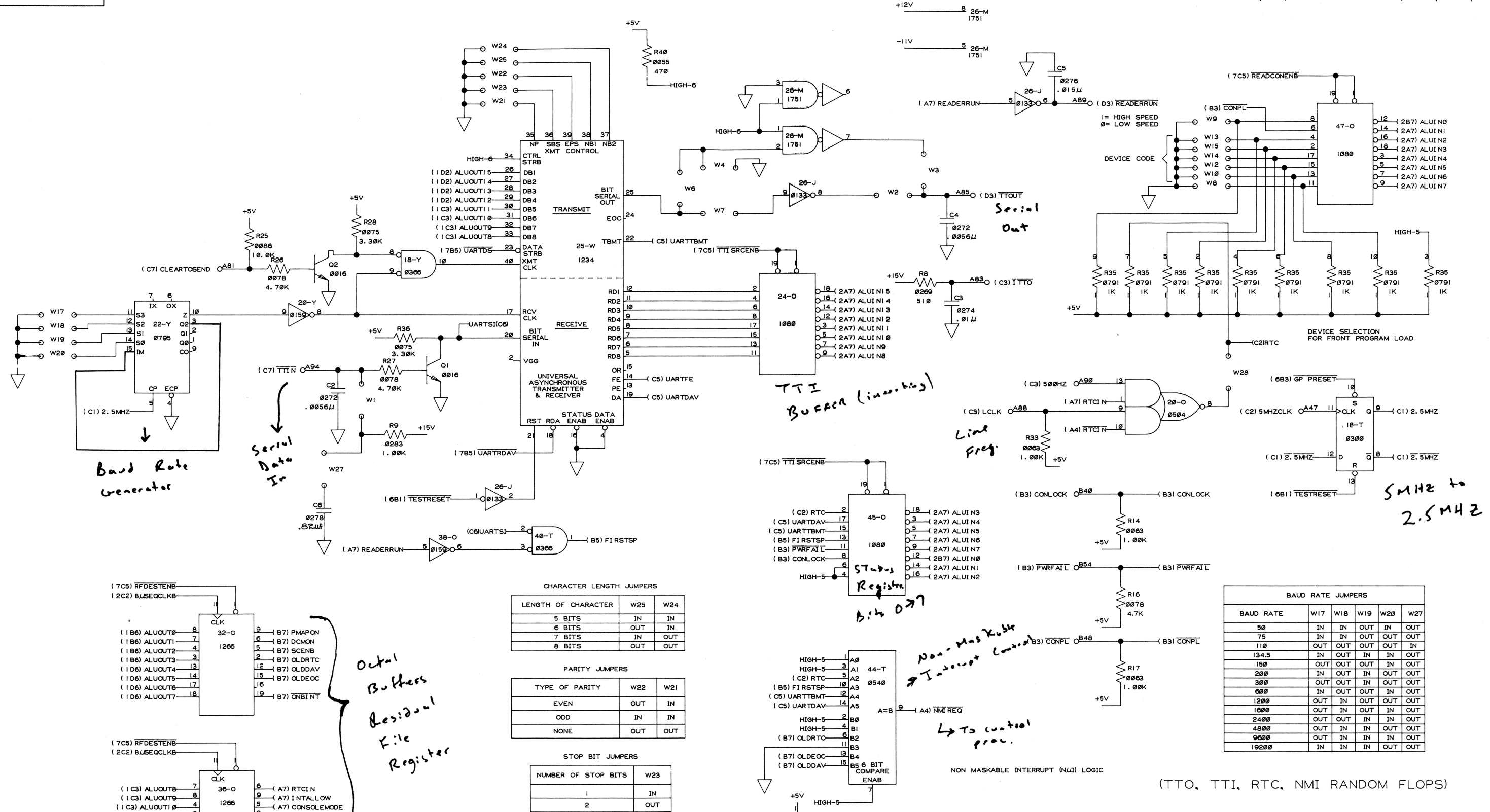
Lesser Random Decoder reg.

(RANDOM OPERATIONS AND I/O CONTROL SIGNALS)

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	00100162403

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



CHARACTER LENGTH JUMPERS

LENGTH OF CHARACTER	W25	W24
5 BITS	IN	IN
6 BITS	OUT	IN
7 BITS	IN	OUT
8 BITS	OUT	OUT

PARITY JUMPERS

TYPE OF PARITY	W22	W21
EVEN	OUT	IN
ODD	IN	IN
NONE	OUT	OUT

STOP BIT JUMPERS

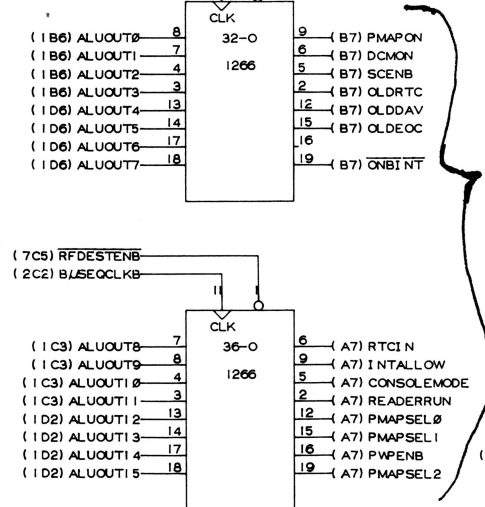
NUMBER OF STOP BITS	W23
1	IN
2	OUT

BAUD RATE JUMPERS

BAUD RATE	W17	W18	W19	W20	W27
50	IN	IN	OUT	IN	OUT
75	IN	IN	OUT	OUT	OUT
110	OUT	OUT	OUT	OUT	IN
134.5	IN	OUT	IN	IN	OUT
150	OUT	OUT	IN	OUT	OUT
200	IN	OUT	IN	OUT	OUT
300	OUT	OUT	IN	OUT	OUT
600	IN	OUT	IN	OUT	OUT
1200	OUT	IN	OUT	IN	OUT
1800	OUT	IN	OUT	IN	OUT
2400	OUT	IN	IN	OUT	OUT
4800	OUT	IN	IN	OUT	OUT
9600	OUT	IN	IN	OUT	OUT
19200	IN	IN	IN	OUT	OUT

TYPE OF TRANSMISSION JUMPERS

TYPE OF TRANSMISSION	INSERT JUMPERS
20 MA CURRENT LOOP EIA RS232-C	W4, W7, W2, W1 W6, W3



Detailed Buffer Register

(TTO, TTI, RTC, NMI RANDOM FLOPS)

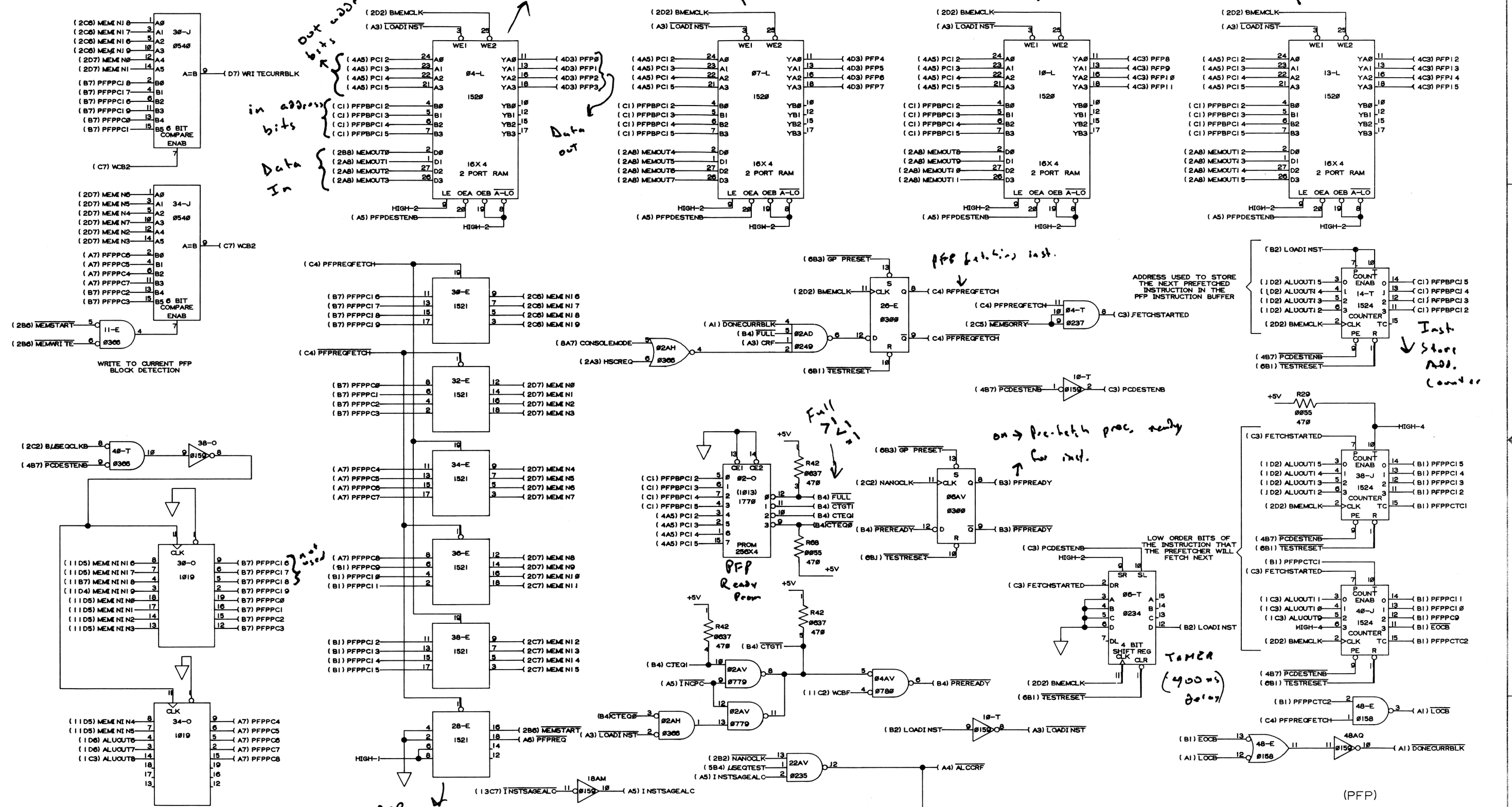
DRAWN	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01172 TITLE DGC NOVA SIZE CODE DRAWING NUMBER REV D 001001624 03
CHECKED	
ENGINEER	
APPROVED	
FIRST USED ON	

A

8 of 5

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



6/18/82
2/2

PFP memory address register

PFP MAE Drivers (1521's)

Full 7/21

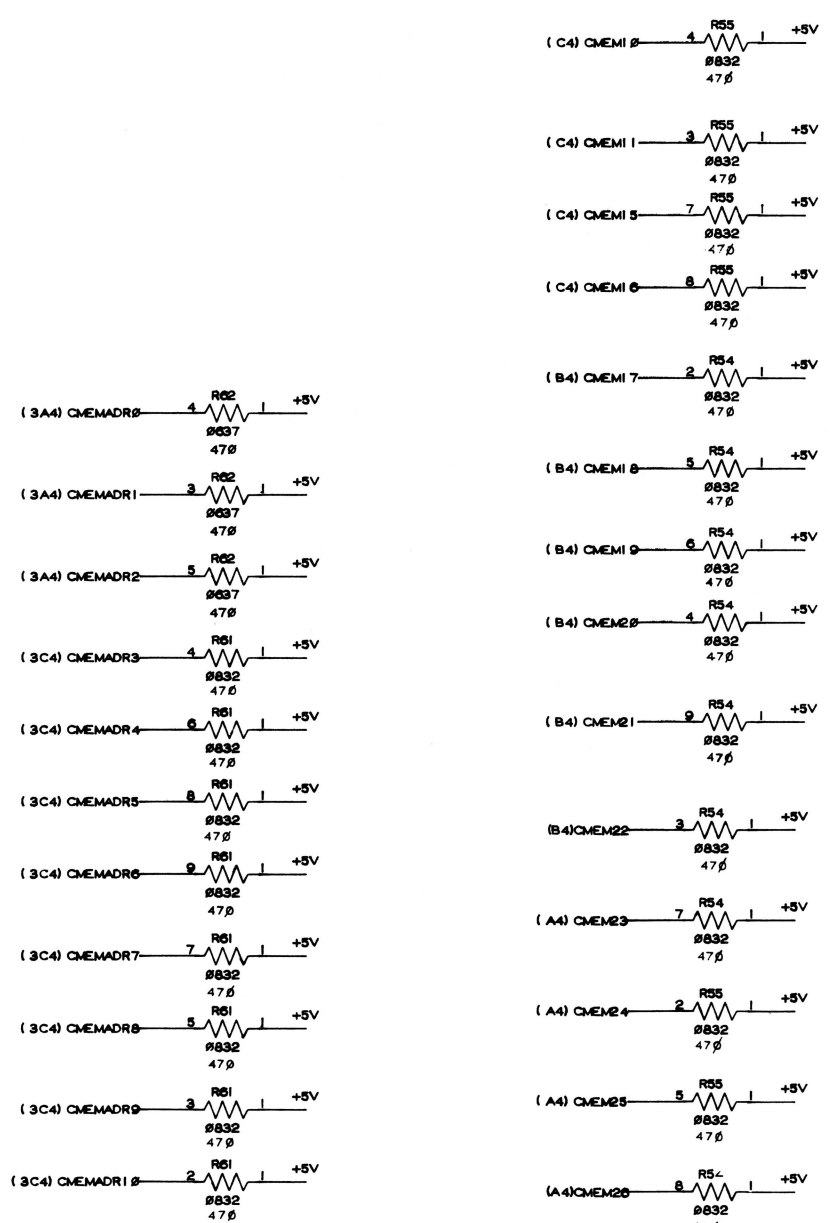
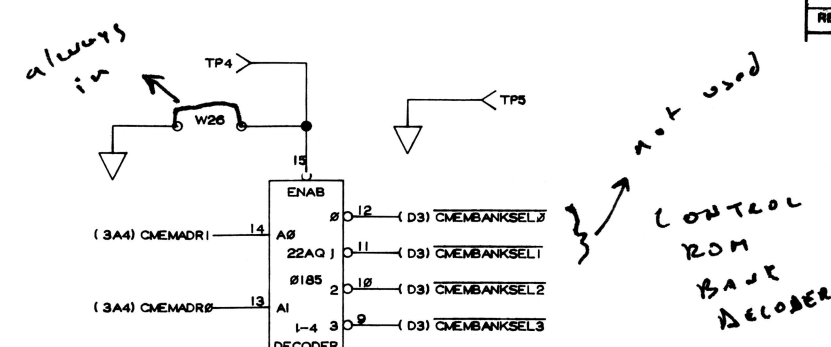
on -> pre-halt proc. ready for inst.

TAMER (400ms)

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	00100162403

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



(CONTROL ROMARRAY)

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON			
SIZE	CODE	DRAWING NUMBER	REV
D		001001624	03

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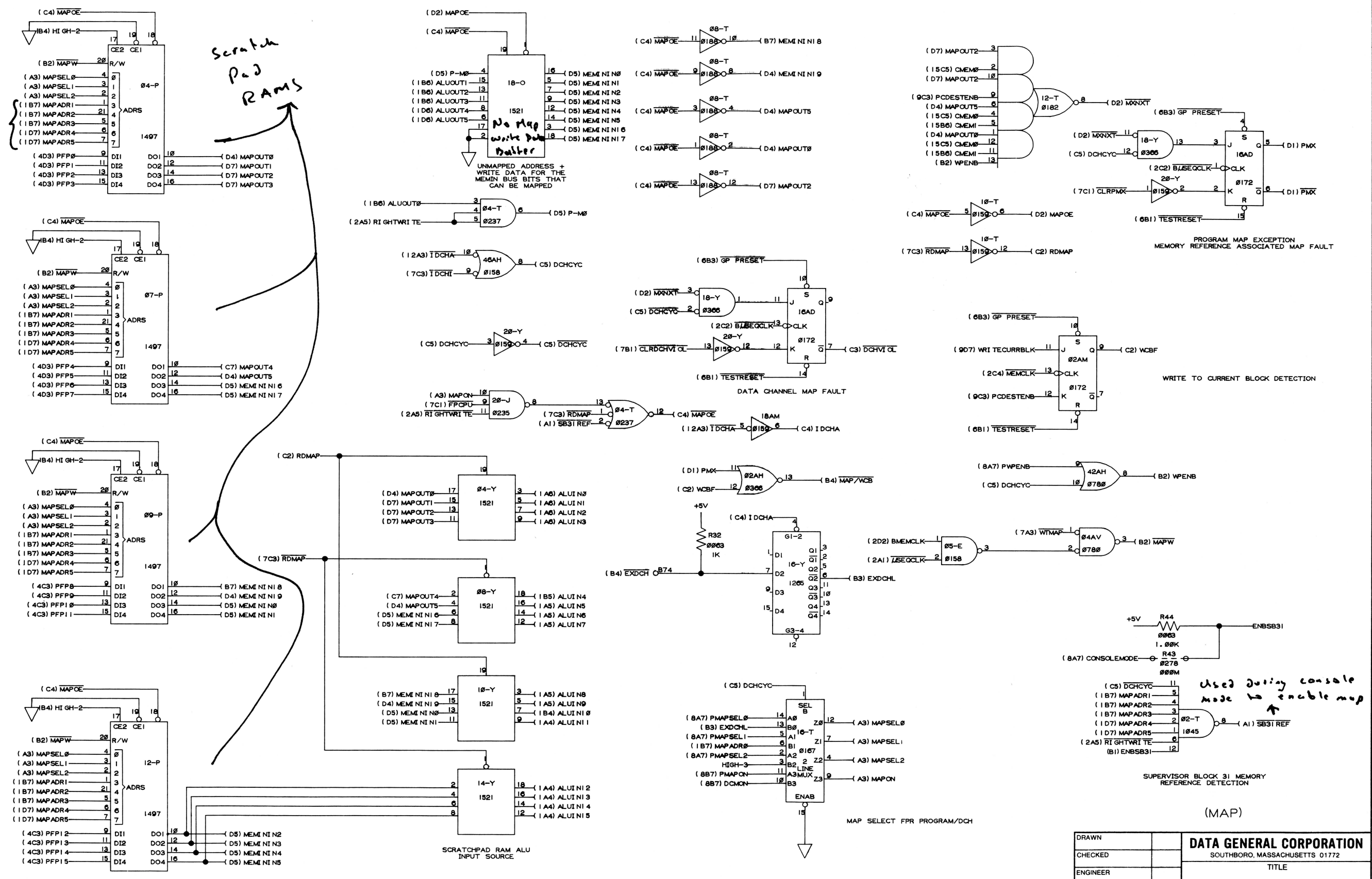
REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

ALL OUT 1-5

Scratch Pad RAMS

MAPSEL

0	1	2	
0	0	0	Program A
0	0	1	DCH A
0	1	0	Program B
0	1	1	DCH B
1	0	0	Console
1	0	1	"
1	1	0	"
1	1	1	"



DRAWN		DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 TITLE DGC NOVA	
CHECKED			
ENGINEER			
APPROVED			
FIRST USED ON			
SIZE	CODE	DRAWING NUMBER	REV
D		001001624	03

(MAP)

SUPERVISOR BLOCK 31 MEMORY REFERENCE DETECTION

MAP SELECT FPR PROGRAM/DCH

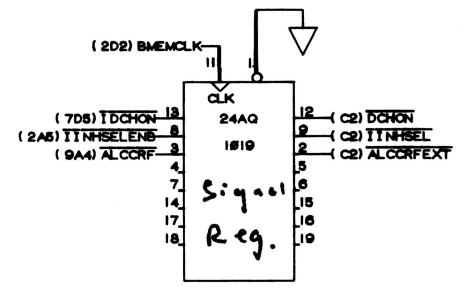
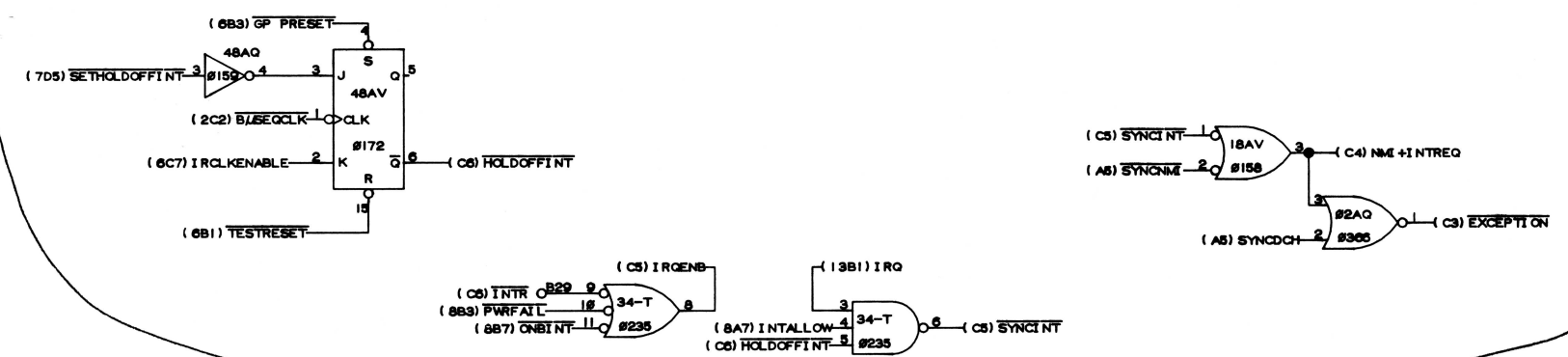
SCRATCHPAD RAM ALU INPUT SOURCE

256X16 SCRATCHPAD RAM INCLUDES MAP ENTRIES

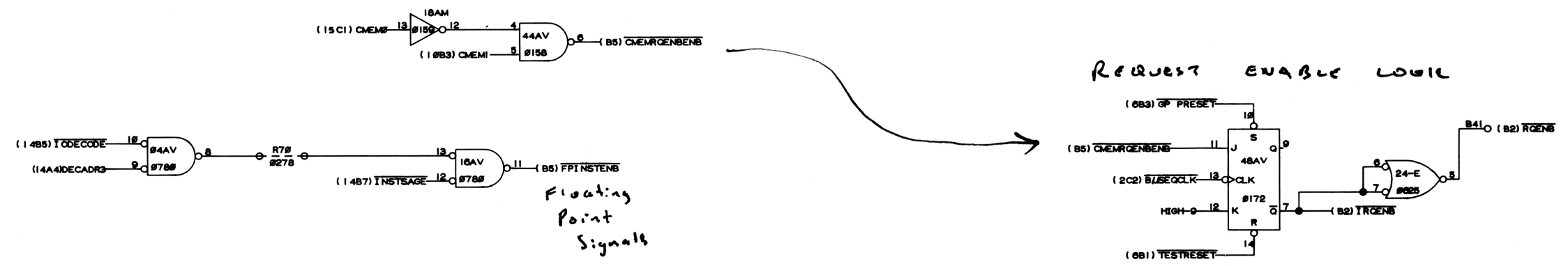
REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

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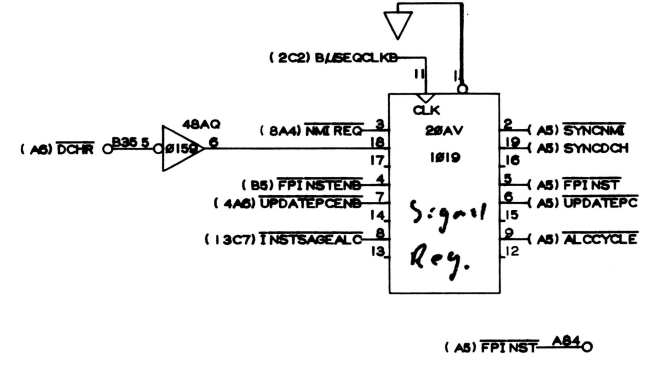
INTERUPT LOGIC



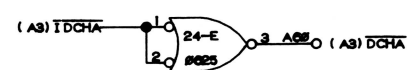
REQUEST ENABLE LOGIC



Floating Point Signals



Data Channel signals



(MEMORY CONTROL, DATA CHANNEL LOGIC, INTERRUPT LOGIC)

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		DGC NOVA	
FIRST USED ON		SIZE	CODE
		D	00100162403

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

Mult/Div. Logic

Used during ALL Inst.

ALL Fill IN LOGIC

ALL (stuff) Fill IN LOGIC

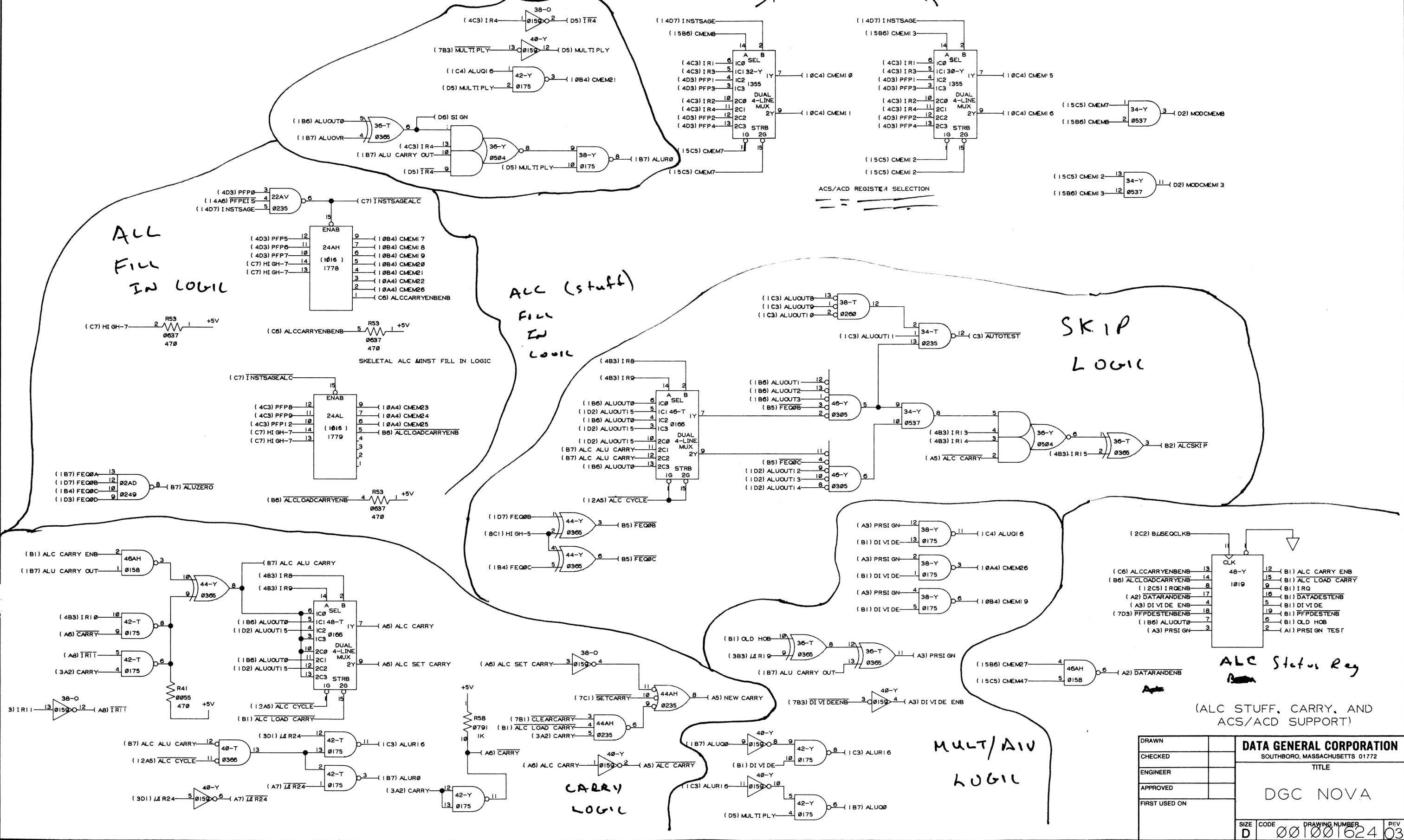
SKIP LOGIC

ALC Status Reg

MULT/DIV LOGIC

CARRY LOGIC

(ALC STUFF, CARRY, AND ACS/ACD SUPPORT)

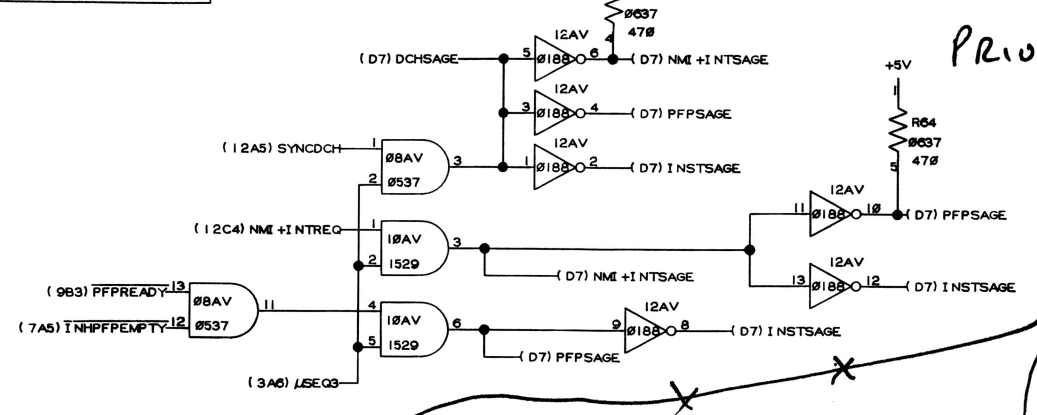


DRAWN		DATA GENERAL CORPORATION		
CHECKED		SOUTHBORO, MASSACHUSETTS 01772		
ENGINEER		TITLE		
APPROVED		DGC NOVA		
FIRST USED ON		SIZE CODE DRAWING NUMBER REV		
	D	001001624	03	

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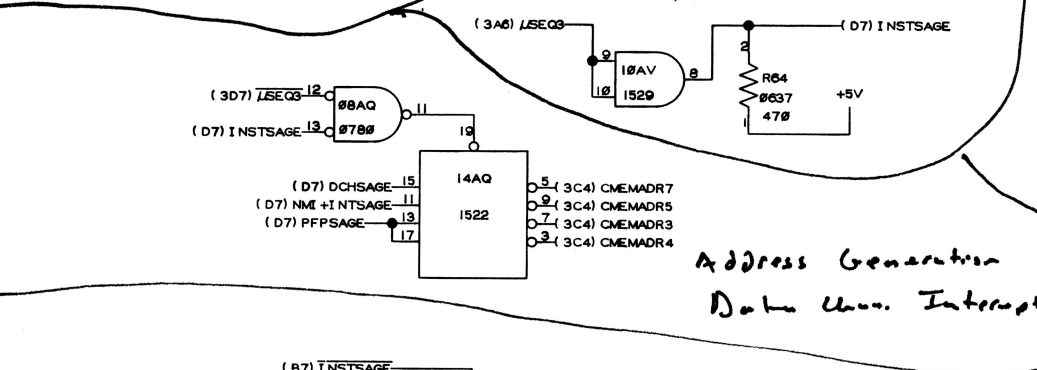
REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

SAGE PRIORITY LOGIC



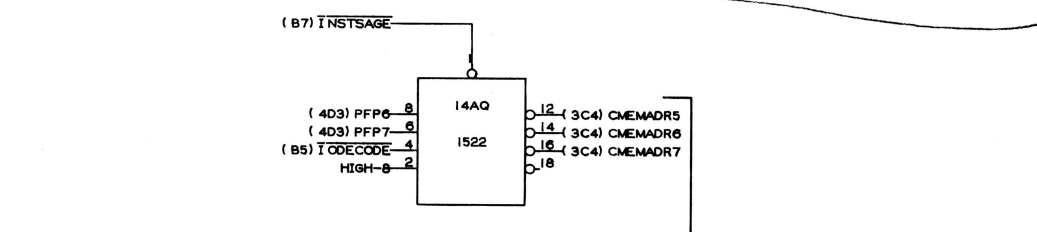
- SAGE PRIORITY LOGIC
- 1 DCH
 - 2 INTERRUPT OR NMI
 - 3 PFP EMPTY
 - 4 INSTRUCTIONS

Address Generation Data Chan. Interrupt

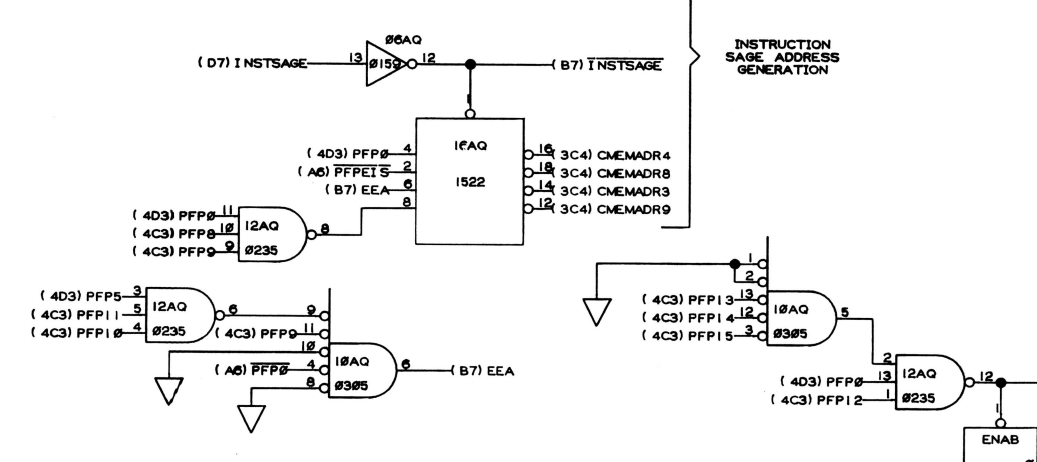


4x w/mult/div
4x w/o/mult/div
4x w/mult/div
4x w/o/mult/div

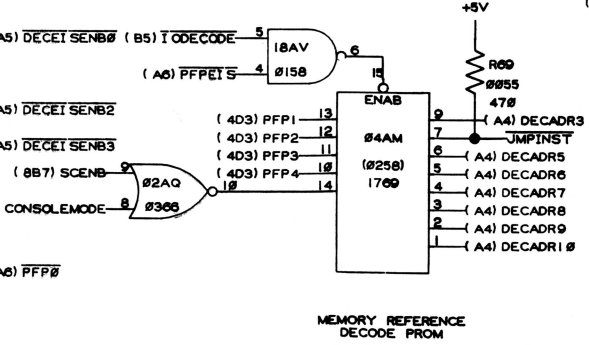
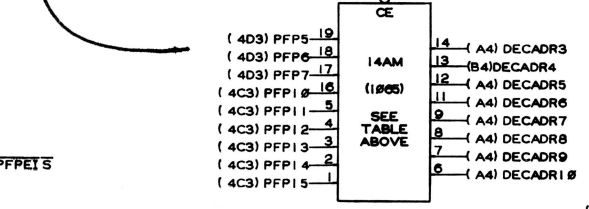
TABLE	
005012057	1754
005012785	1788
005012787	1750
005012786	1769



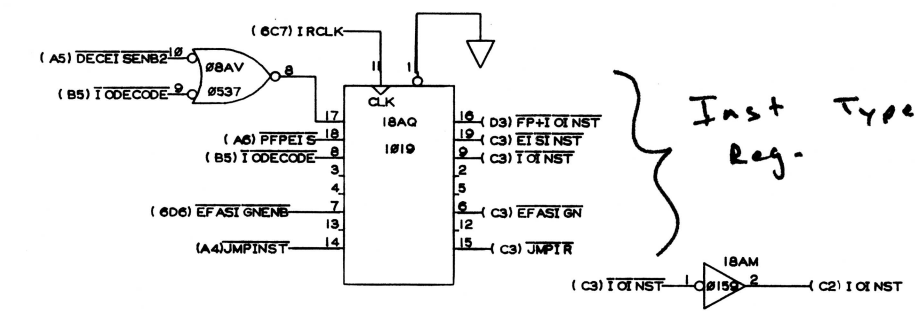
INSTRUCTION SAGE ADDRESS GENERATION



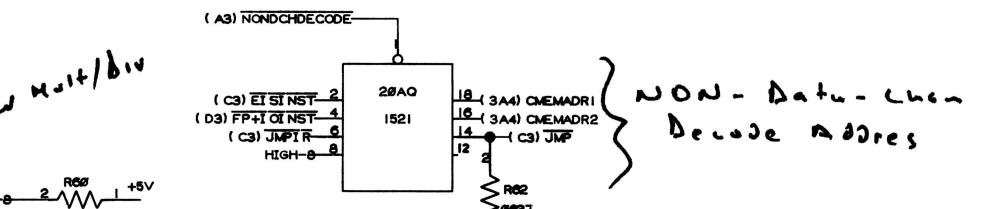
I/O DECODE FROM



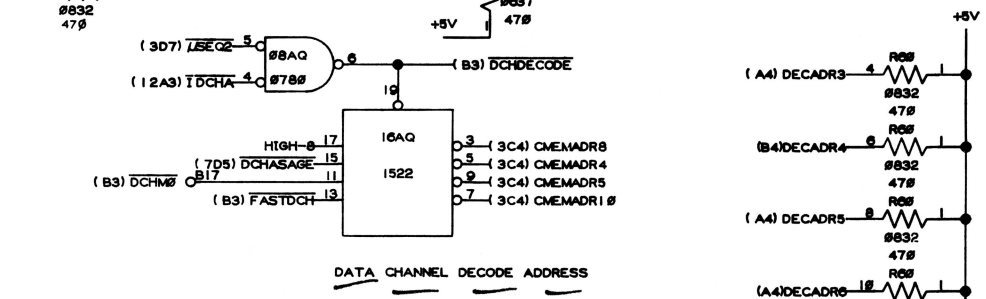
MEMORY REFERENCE DECODE FROM



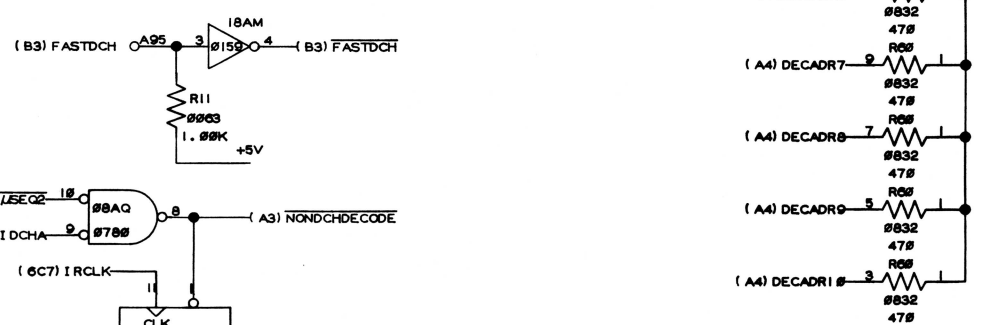
Inst Type Reg.



NON-DATA-CHAN DECODE ADDRESS



DATA CHANNEL DECODE ADDRESS



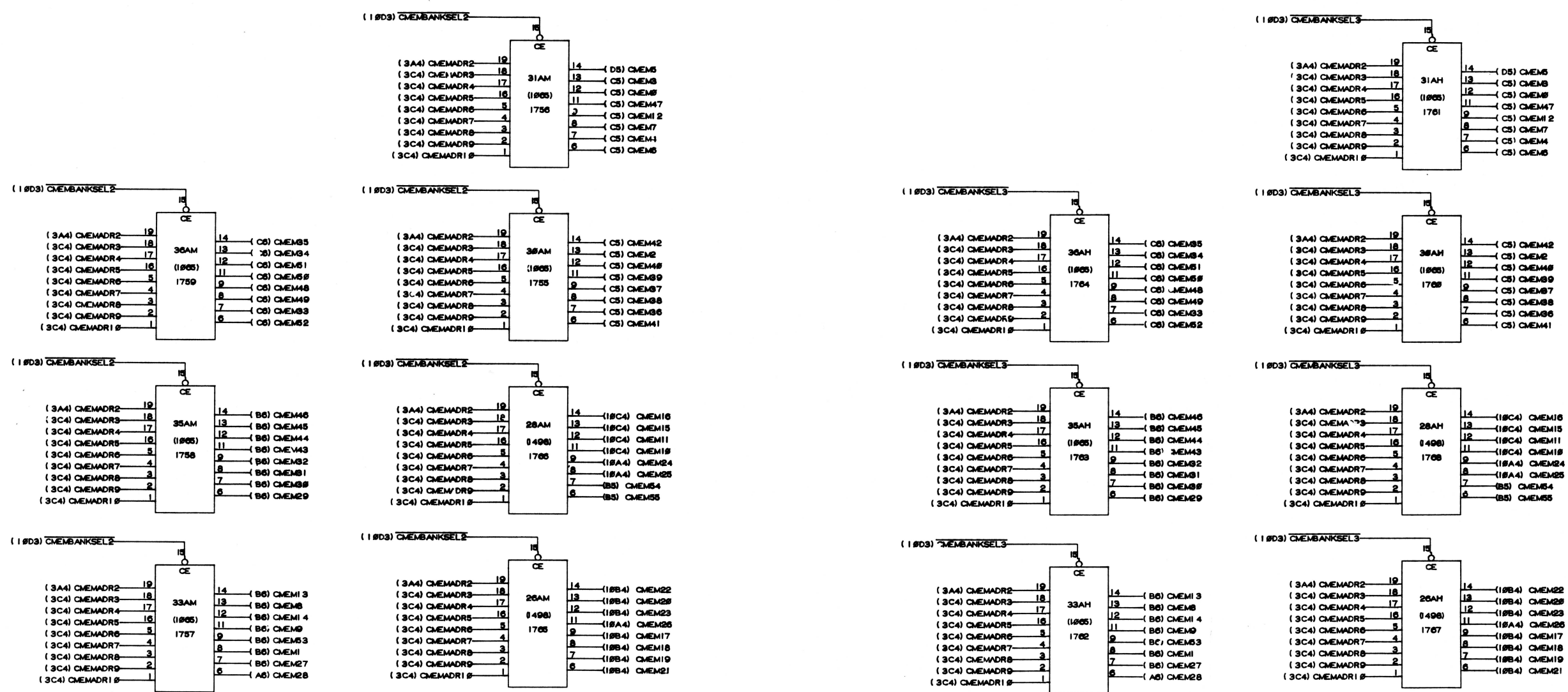
(DECODE SAGE)

Decode Address Register

DRAWN		DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 TITLE DGC NOVA
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		SIZE CODE 001001624 REV 03

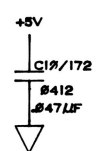
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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



Bank #2

CONTROL MEMORY ADDRESSES 2998₈ TO 2777₈



CONTROL MEMORY ADDRESSES 3698₈ TO 3777₈

Bank #3

(CONTROL ROM ARRAY)

DRAWN		DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772 TITLE DGC NOVA
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		
SIZE	D	CODE 001001624 DRAWING NUMBER 03 REV