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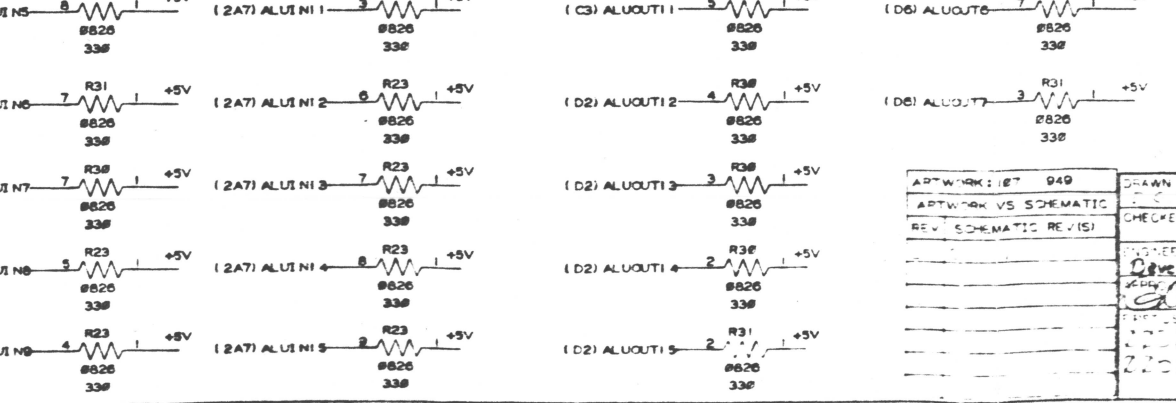
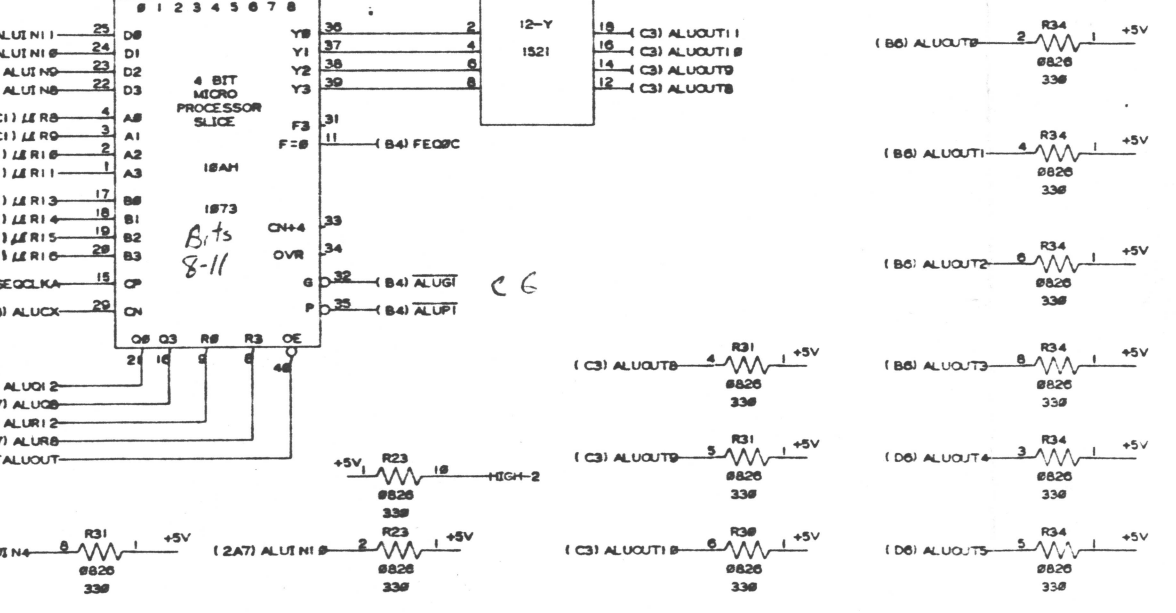
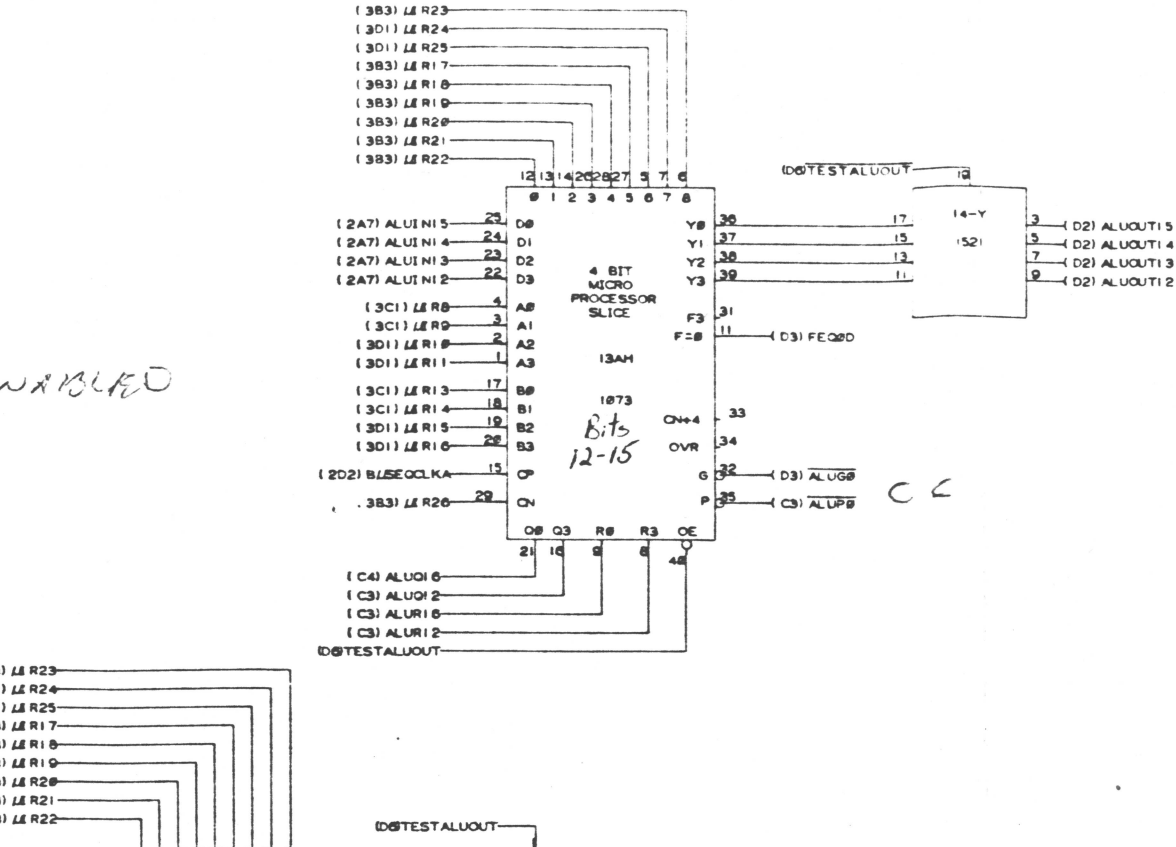
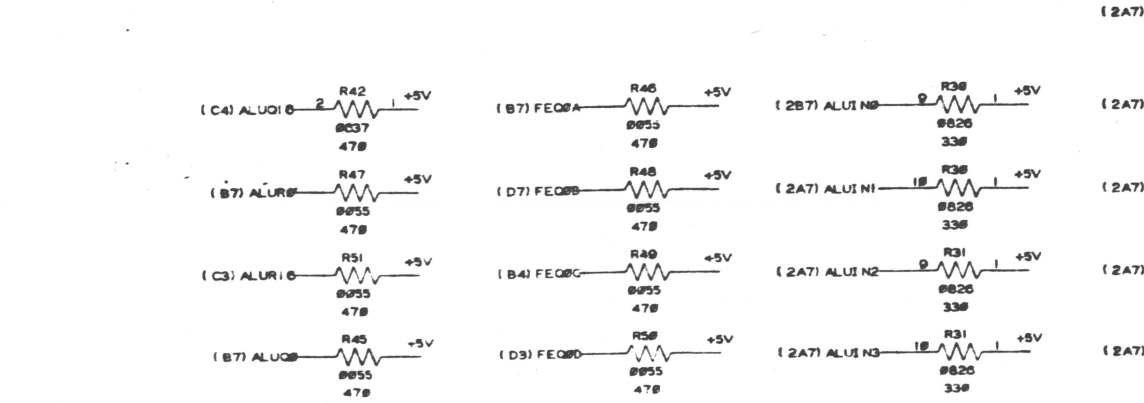
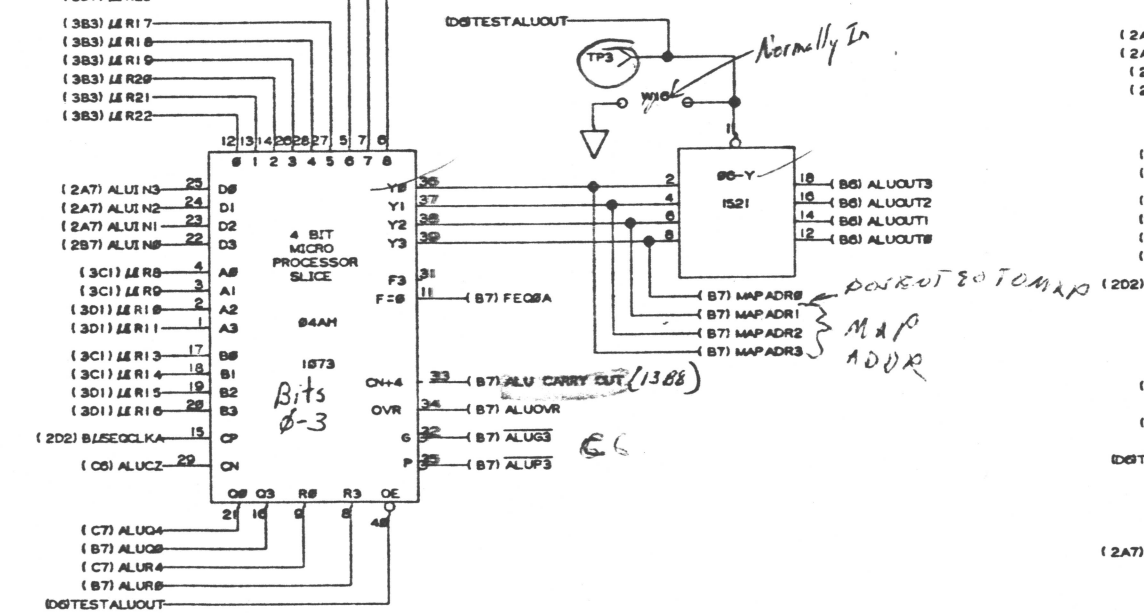
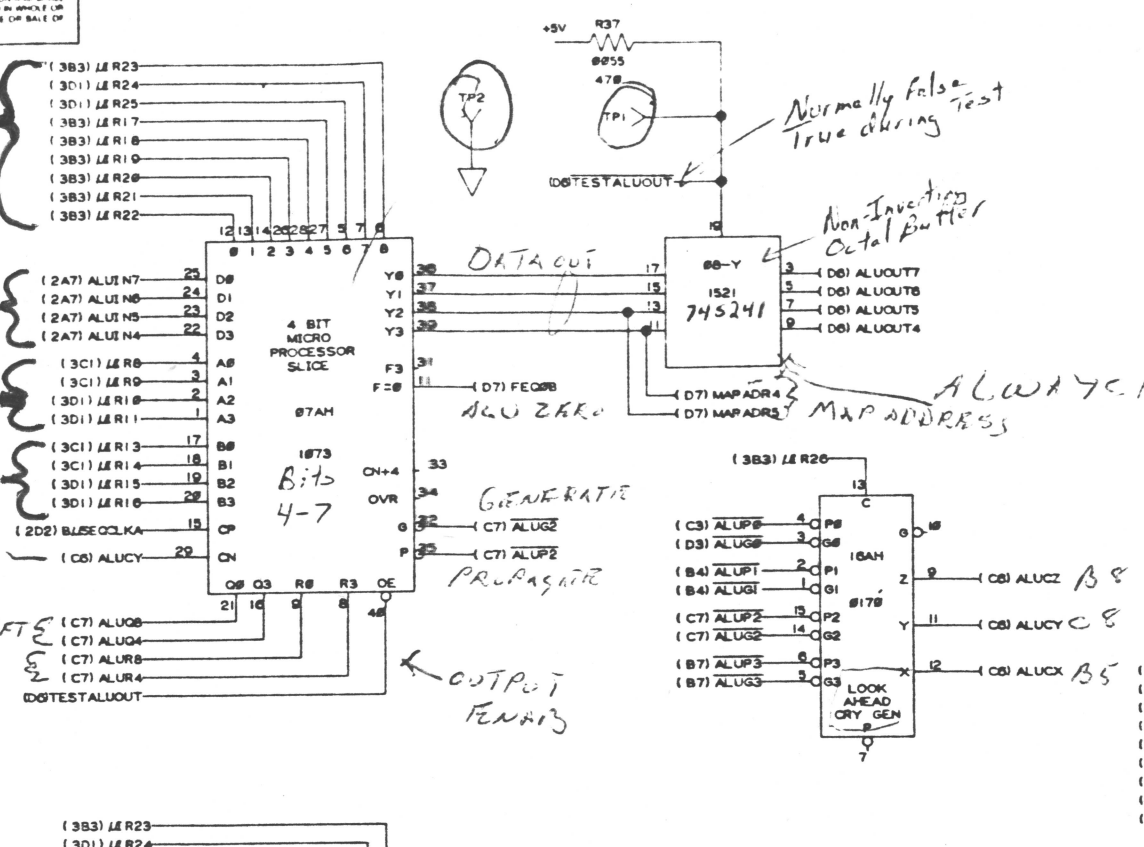
REVISIONS				
REV	DESCRIPTION	DRAFT	APP BY	DATE
01	PER ECO E590	WLG	DSG	8/17

ALU OPERATION
ALU IN DATA
AREG SELECT
ALU DEST
AREG SEL
CARRY IN

SHIFT
REGISTER
SHIFTER

B

A



SPARE GATES

8305	82AH	(1)
8172	82AM	(1)
8779	82AV	(2)
8788	84AV	(1)
8158	85-E	(2)
8368	86AV	(1)
8150	18-T	(1)
1520	18AV	(1)
8385	14AV	(1)
1205	18-Y	(2)
8150	28-Y	(1)
1521	28AQ	(4)
8133	26-J	(2)
8537	34-Y	(1)
8208	38-T	(1)
8388	48-T	(1)
8788	42AH	(2)
8235	44AH	(1)
8158	44AV	(1)
8158	46AH	(1)
8158	48-E	(1)
8150	48AQ	(1)
8188	88-T	(1)

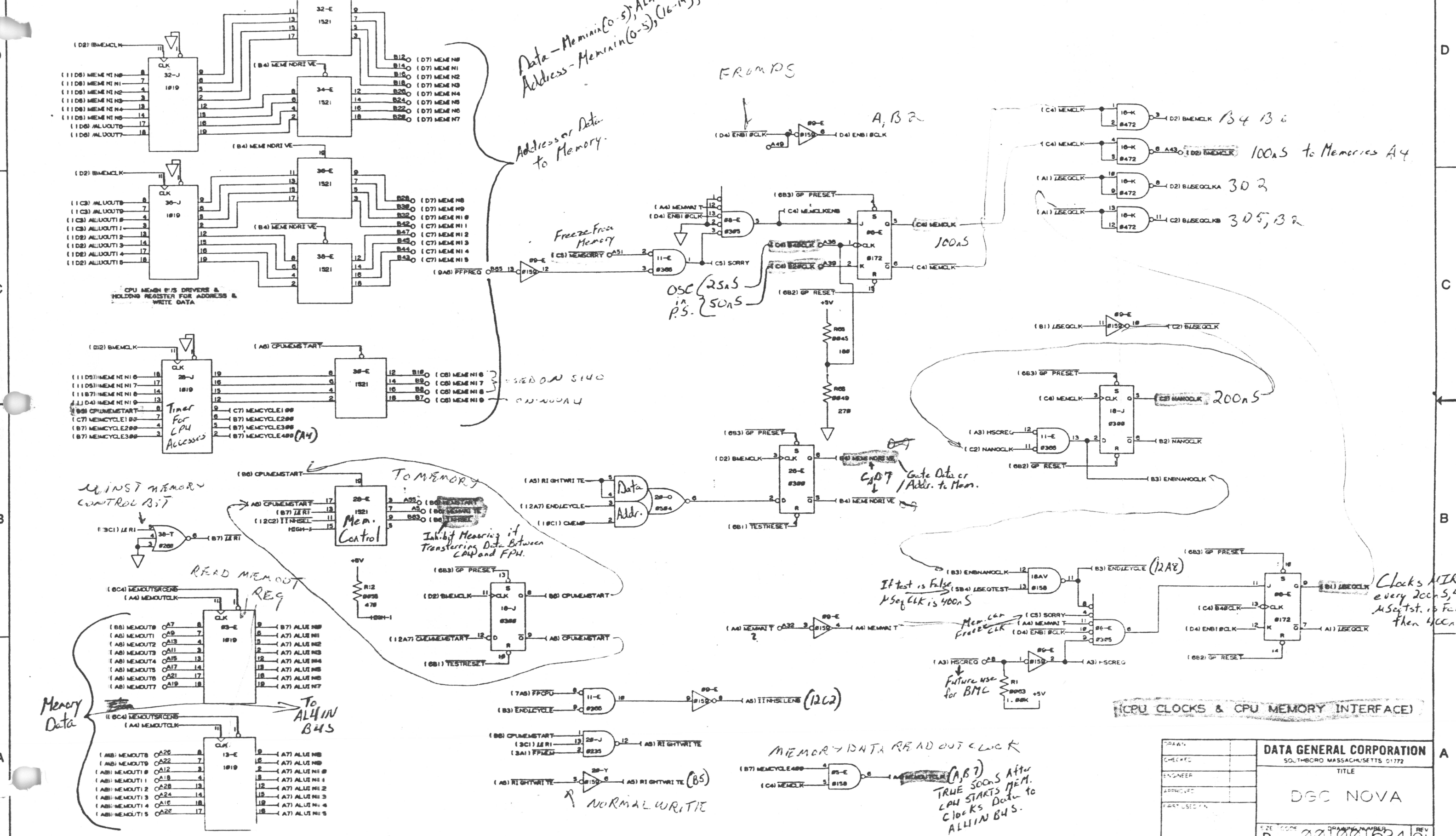
ALU PULLUPS

(CPU SLICES)

ARTWORK: 187 949	DRAWN: TCS	REV: 1	DATA GENERAL CORPORATION SOUTHBORO MASSACHUSETTS 01772
APTWORK VS SCHEMATIC	CHECKED:		
REV: SCHEMATIC REV: 151	ENGINEER: Dave Spasich	10/1/78	TITLE NOVA 4X/3 DGC NOVA
	DESIGNED BY: CAG	8/1/78	
	PREPARED BY: J. J. P. 2207-2208		SIZE: CODE
			DRAWING NUMBER: 27 20162401
			REV: 1

REVISIONS			
REV	DESCRIPTION	DRFTD	APP BY DATE

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*Data - Memory (0-5), ALLOC (E-15)
Address - Memory (0-5), (16-19), ALLOC (E-15)*

*FRONTS
A, B, C*

Address or Data to Memory

Freeze From Memory

OSC (25ns in P.S.)

SEED ON S140

MINST MEMORY CONTROL BIT

TO MEMORY

Inhibit Memory if Transferring Data Between CPU and FPU.

READ MEMOUT REG

Memory Data

To ALL IN BUS

MEMORY DATA READ OUT CLOCK

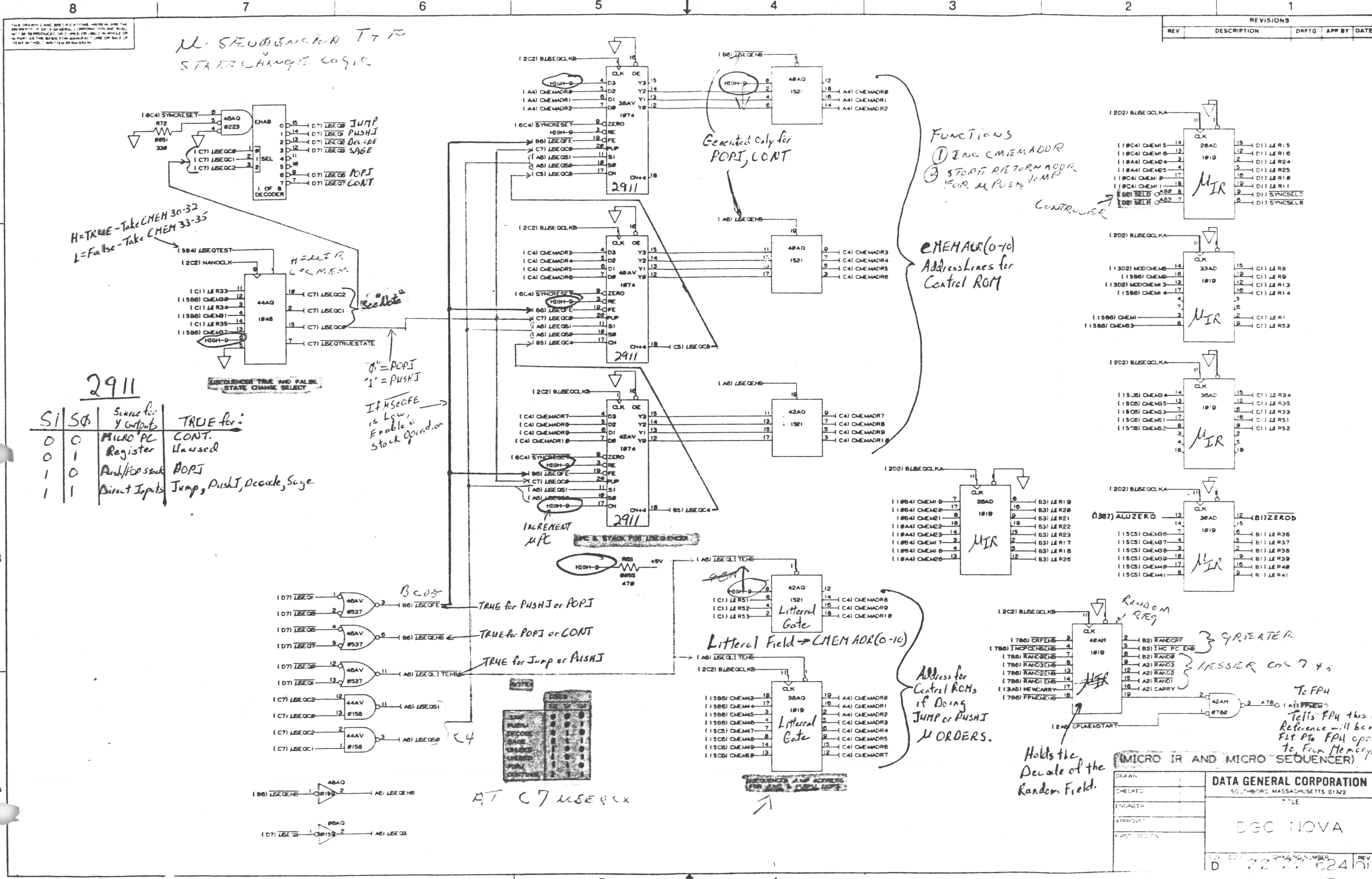
TRUE 500NS AFTER CPU STARTS MEM. CLOCKS DATA TO ALL IN BUS.

If test is false, Mem. CLK Freeze CLK. 1/2 Sec CLK is 400ns

Clocks after every 200ns, unless MSetst. is False, then 400ns

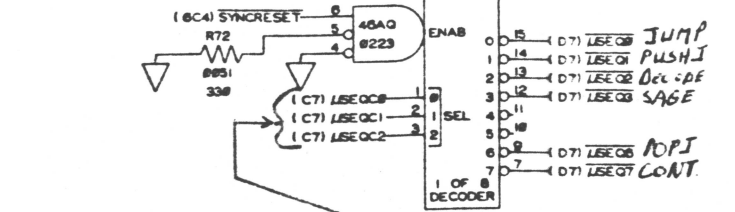
CPU CLOCKS & CPU MEMORY INTERFACE

DRAWN		DATA GENERAL CORPORATION SOUTH BORO MASSACHUSETTS 01772 TITLE DGC NOVA SIZE CODE DRAWING NUMBER D 221001624
CHECKED		
ENGINEER		
APPROVED		
PART USED IN		

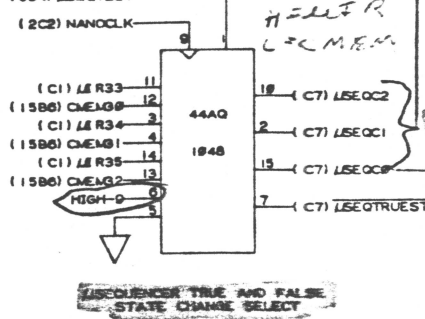


MICROSEQUENCER TRUE STATE CHANGE LOGIC

REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE



H=TRUE - Take CMEM 30-32
L=False - Take CMEM 33-35

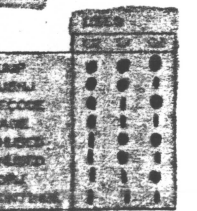


SEQUENCER TRUE AND FALSE STATE CHANGE SELECT

2911

SI	SQ	Source for Y outputs	TRUE for:
0	0	MICRO PC Register	CONT. Unused
0	1	Push/Pop stack	POPJ
1	0	Direct Inputs	Jump, PushJ, Decade, Sage
1	1	Direct Inputs	Jump, PushJ, Decade, Sage

"0" = POPJ
"1" = PUSHJ
If LSEOC0 is Low, Enable a Stack Operation



AT C7 LSEOCX

- FUNCTIONS**
- ① INC CMEM ADDR
 - ② START RETURN ADDR FOR M PUSH JUMP

CMEMADR(0-10) Address lines for Control ROM

Generated only for POPJ, CONT

Literal Field → CMEMADR(0-10)

Address for Control ROMs if doing JUMP or PUSHJ M ORDERS.

Holds the Decade of the Random Field.

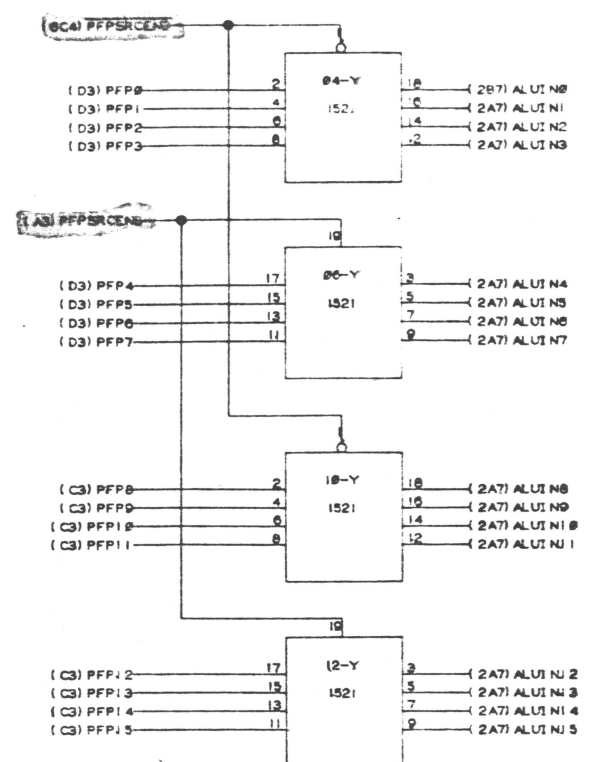
(MICRO IR AND MICRO SEQUENCER)

DRAWN	DATA GENERAL CORPORATION SOUTH BORD MASSACHUSETTS 01722 TITLE DGC NOVA
CHECKED	
ENGINEER	
APPROVED	
FIRST SECTION	
REV	REV

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

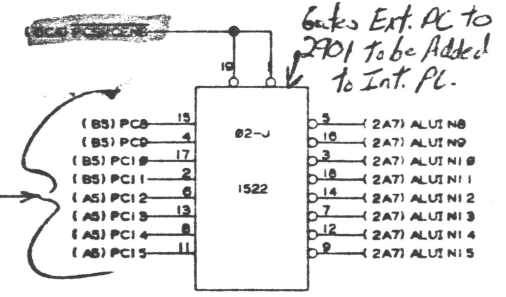
PFP BUS → ALU IN BUS



PFP BUS has two sources:
 1) Inst. Store Reg.
 2) PFP Reg.

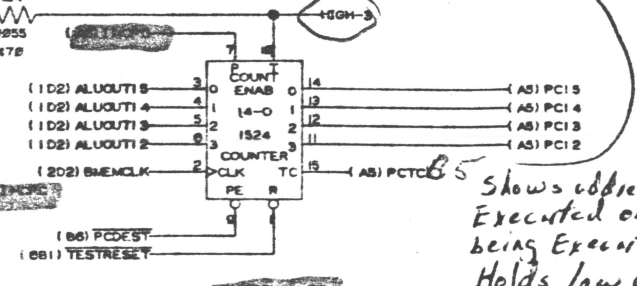
PFP ALU SOURCE
 Gates PFP BUS (usually an Inst.)
 To ALU IN - To 2901.

External PC → ALU IN BUS



Has a range of 1280 must INC IPC when you go past current block.

External PC

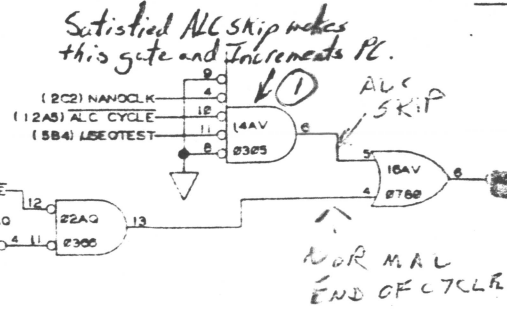


Shows address of Inst. being Executed or Next of Inst. being Executed.
 Holds low order bits of true PC.
 It is added to IPC.

UPDATE PC Logic

- 4 METHODS OF UPDATE
- 1) ALL SKIP
- 2) GREATER RANDOM
- 3) OTHER

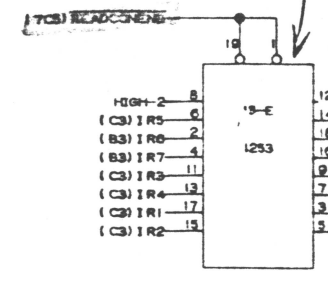
Inc. PC by Mode
 Inc PC to get next Inst. during SAGE time



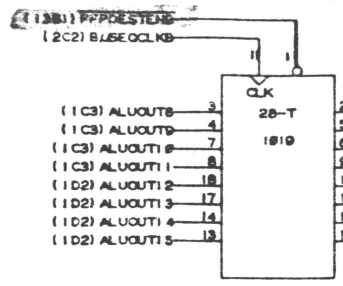
Satisfied ALL SKIP makes this gate and increments PC.

NOT MAL END OF CTCLR

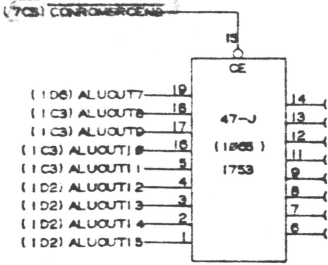
Enabled During READS TIME



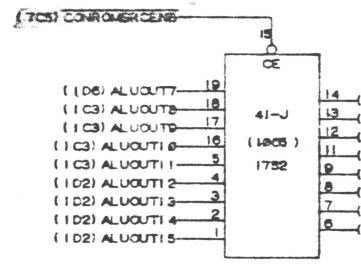
PFP Reg. - Holds Data Going to Map or Inst. from Console ROM to 6: to IR



VIA 2901 CHIPS

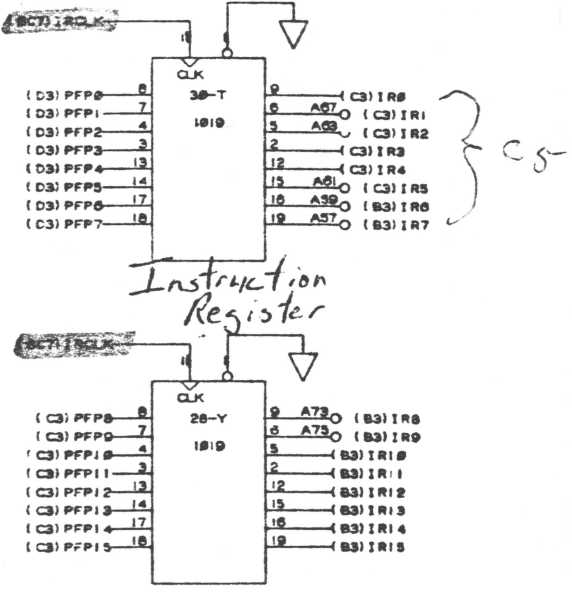


Console ROMs

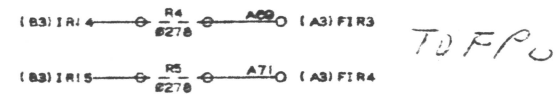


CONSOLE ROM 1512X10

Instruction Register



PFP SOURCE ENAB



TO FPU

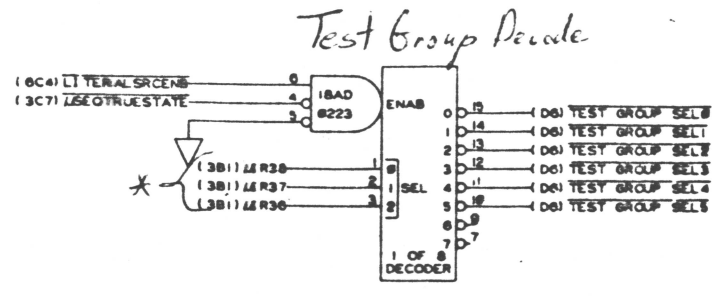
(PC, CONSOLE ROM, PFP SRC, PFP DEST, IR)

DRAWN		DATA GENERAL CORPORATION	
REVISED		SOUTHBORO MASSACHUSETTS 01772	
DESIGNED		TITLE	
APPROVED		DGC NOVA	
PROJECT NO.		SIZE CODE	
		D 00100 24 01	

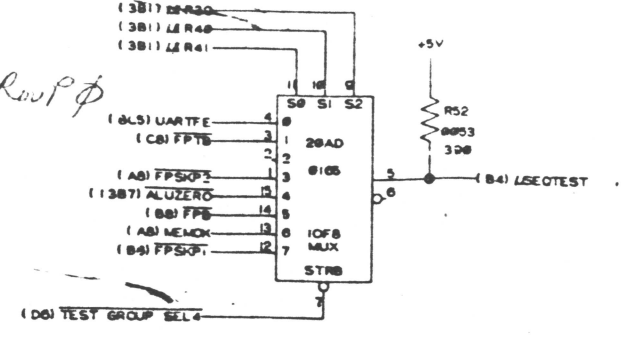
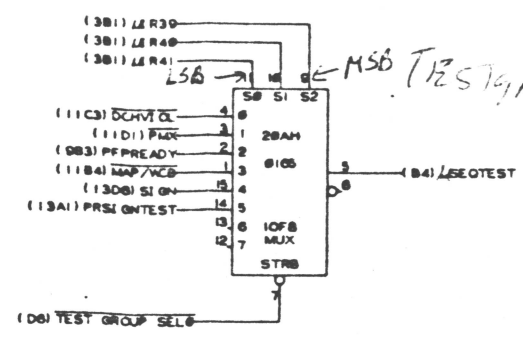
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REVISIONS			
REV	DESCRIPTION	DATE	APP BY

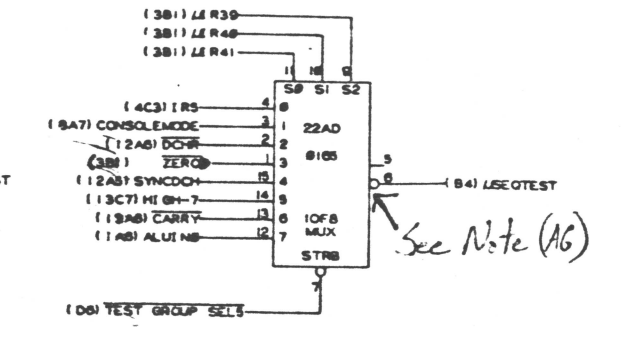
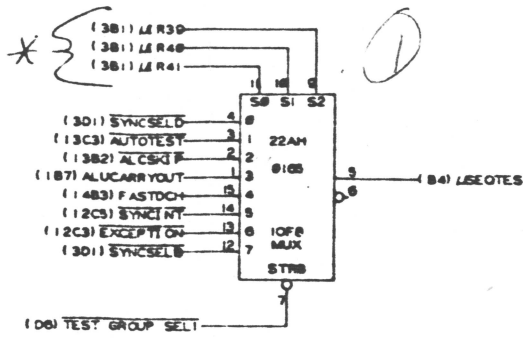
Test Mux's



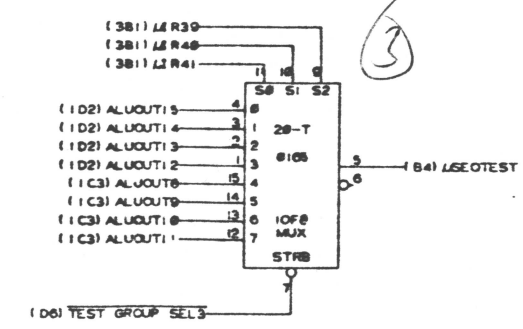
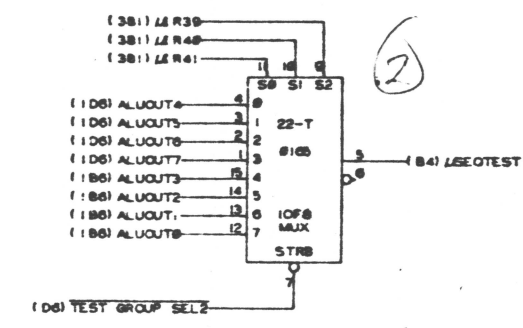
* MUX 36-41 is the Test Condition Select Field.



TRUE FIELD FAULTED
96% OF TIME



See Note (A6)



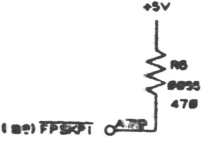
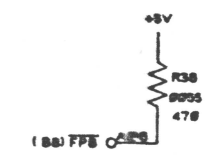
M5EOTEST	FIELD
H1	TRUE
LO	FALSE

TEST MUX - DETERMINES THE NEXT ADDRESS BASED ON DATA SUPPLIED BY

- A CONTROL STORAGE
- B M INSTR KEY
- C PFP
- D M MFP
- E 2901A
- F C.P. LOGIC GOVERNING (DGC TEST MUX AND TEST CONDITIONS)
- 1 AUTO INDEX
- 2 VIRTUAL CONSOLE
- 3 FPU
- 4 I/O

NOTE: TEST SELECTED BY THE SIGNAL TEST GROUP SELS ARE NEGATIVE ASSERTED ALL OTHER TESTS ARE POSITIVE ASSERTED.

Floating Point



DRAWN		DATA GENERAL CORPORATION SOUTHBORO MASSACHUSETTS 01172 TITLE DGC NOVA SIZE CODE DRAWING NUMBER REV D 30 001624 01
CHECKED		
ENGINEER		
APPROVED		
FIRST USE: ON		

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REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

EW4/10

EFA SIGN EXTENSION

*Output is enabled by the EFA order in the EXTRSEL FIELD
ALL HIGH ORDER bits are 0's*

Will be the Displacement

SHORT EFFECTIVE ADDRESS

Holds 8 bit Non Displacement

SHORT EFFECTIVE ADDRESS ALU INPUT SOURCE

Sign of Displacement (Bit 8)

ALU INPUT SOURCE SELECT

BYTE SWAPPER

*SWAP GATES 0-7 → 0-7
8-15 → 8-15*

IR CLOCK

CLOCK IR Generated at SAGE TIME

External Source Decode - Determines who will be on ALUIN BUS

External Source Select Field in Mode

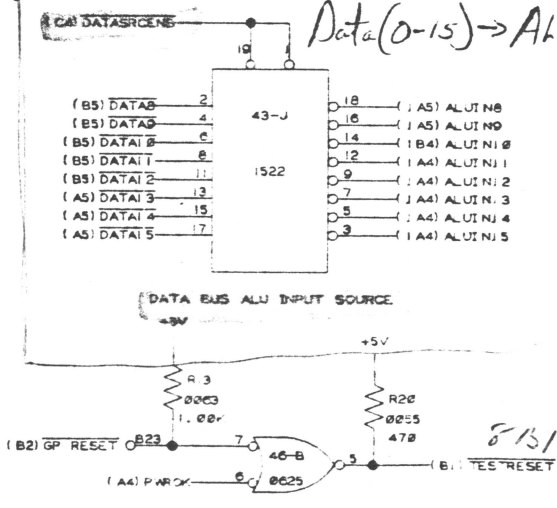
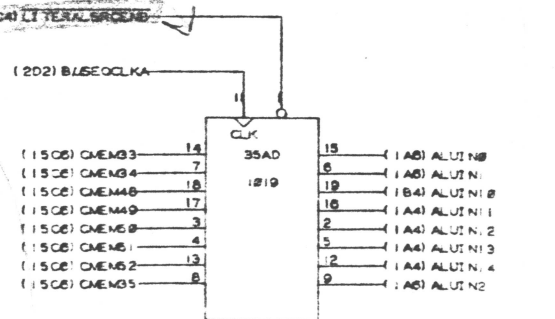
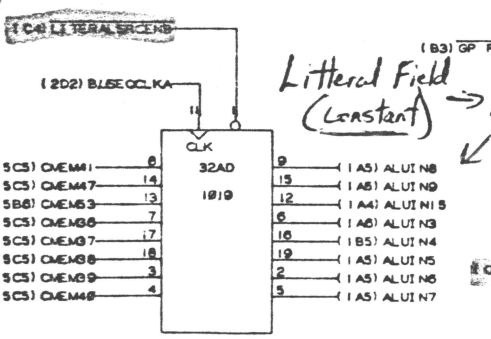
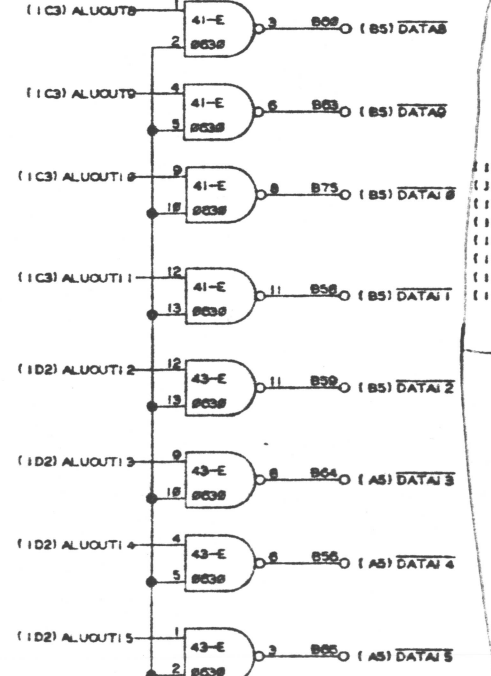
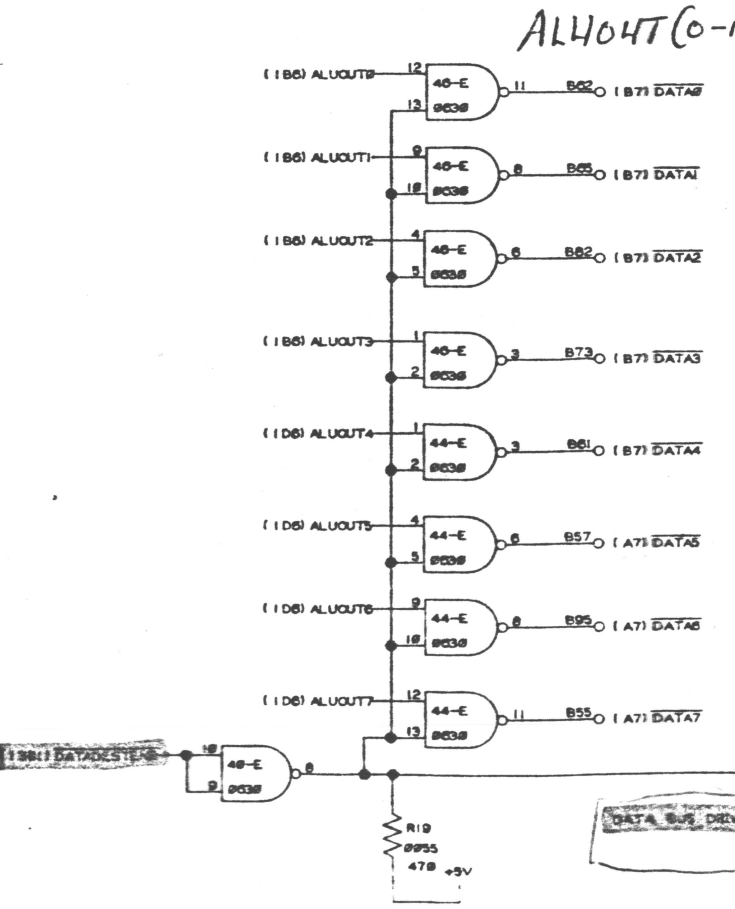
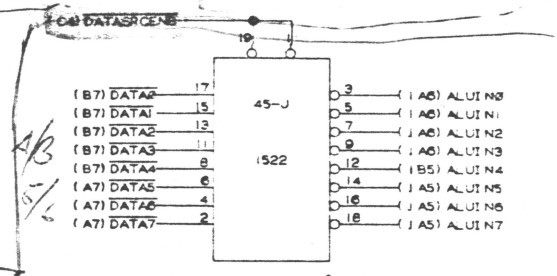
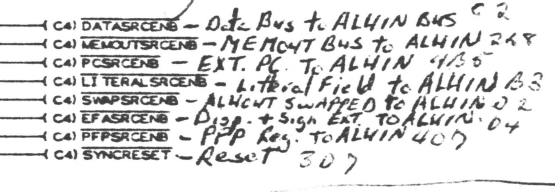
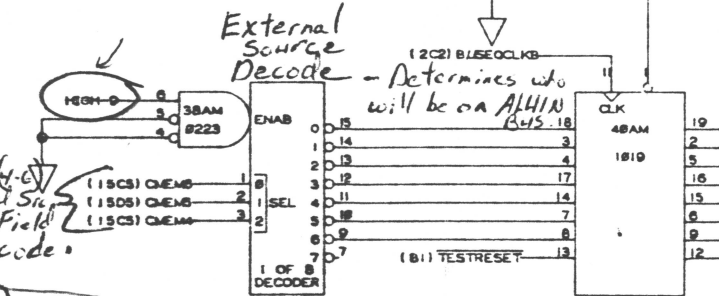
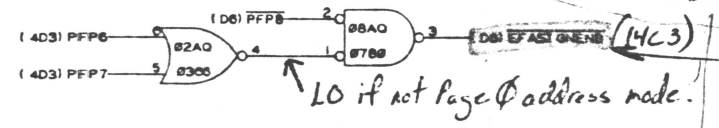
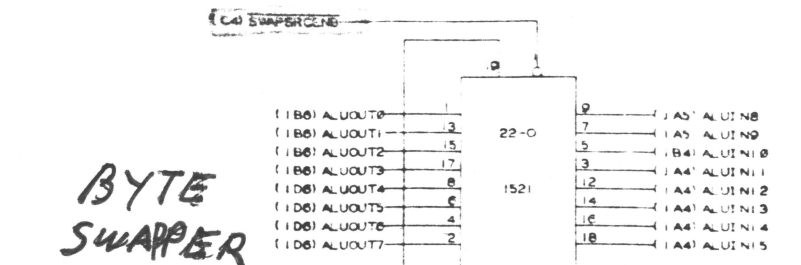
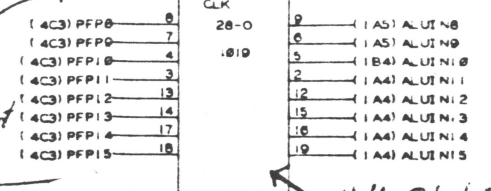
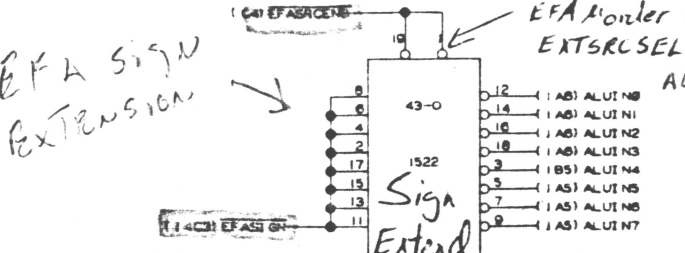
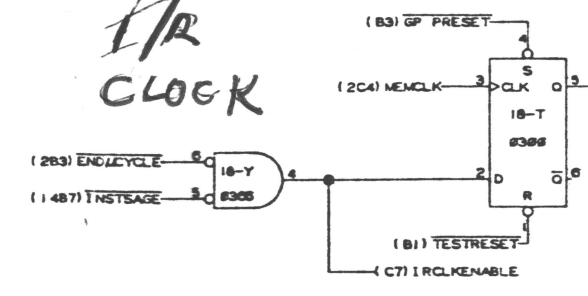
LITERAL SOURCE

Literal Field (Constant) → ALUIN

POWER OK

To Reset on Console

(SWAP AND VARIOUS IIR ENABLE DECODES)



DRAWN	DATA GENERAL CORPORATION SOUTHBORO, MASSACHUSETTS 01772
CHECKED	
ENGINEER	
APPROVED	
DATE	
TITLE	
NOVA	
SIZE	REV
D	02401

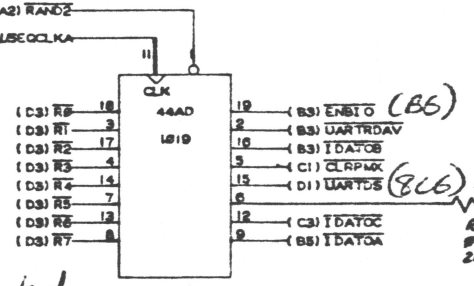
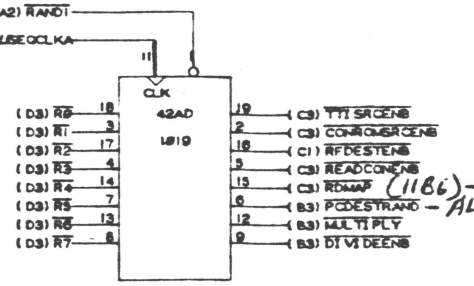
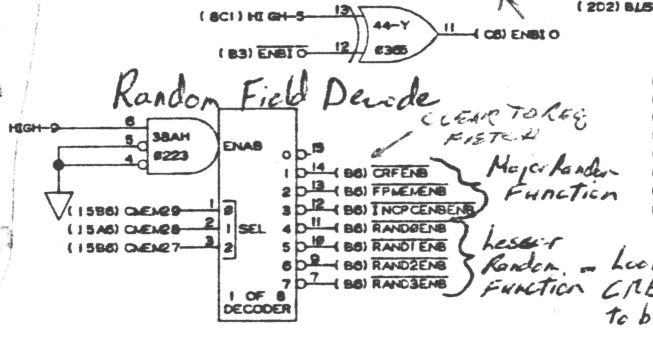
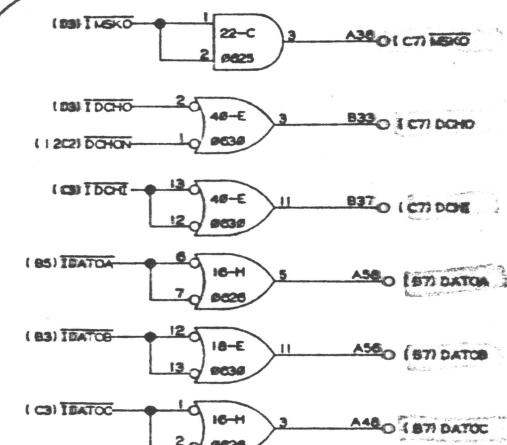
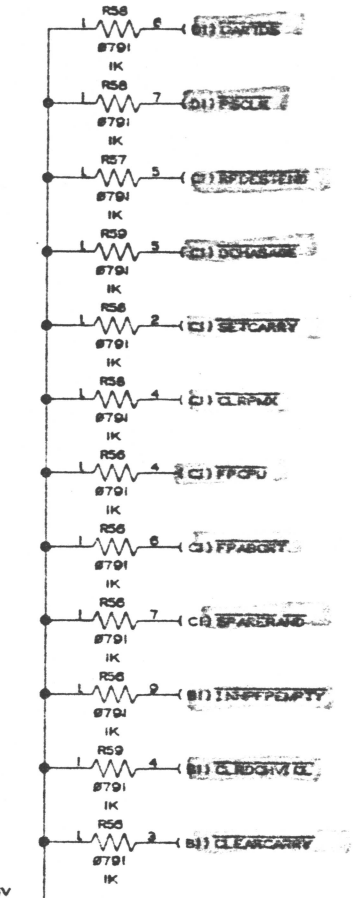
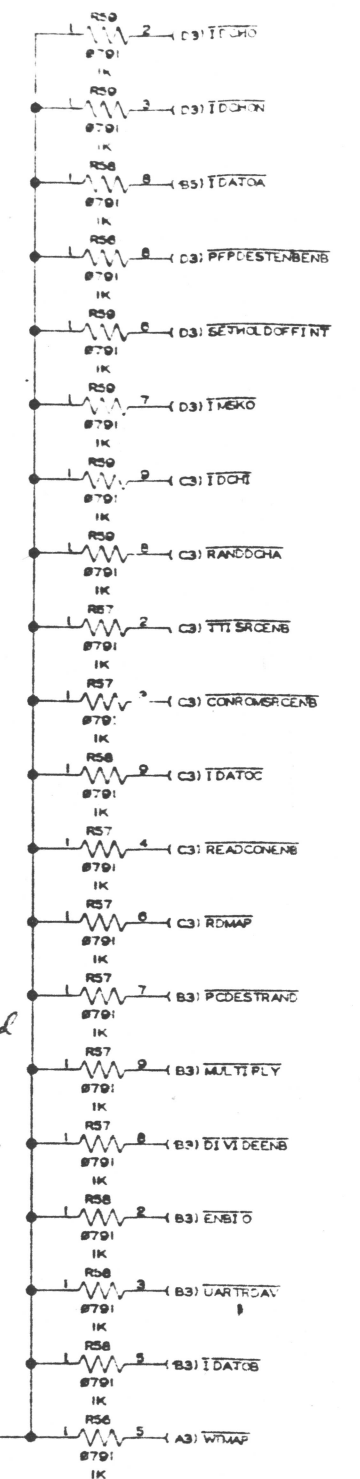
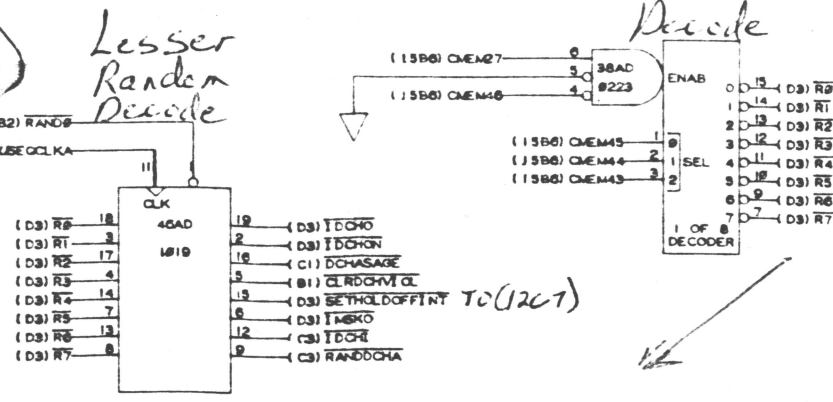
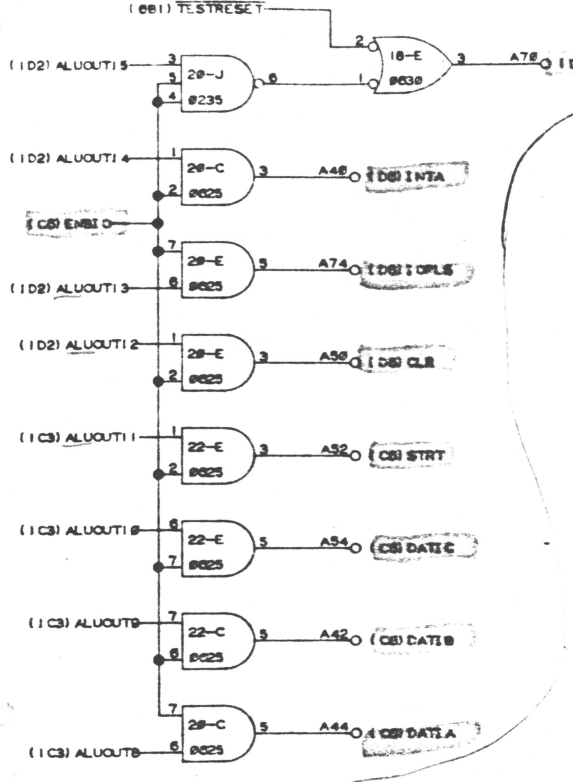
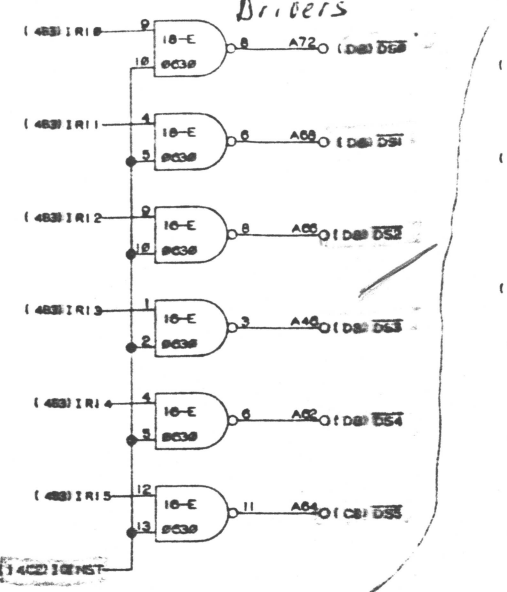
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Device select Drivers

I/O XFER CNTRL. Functions

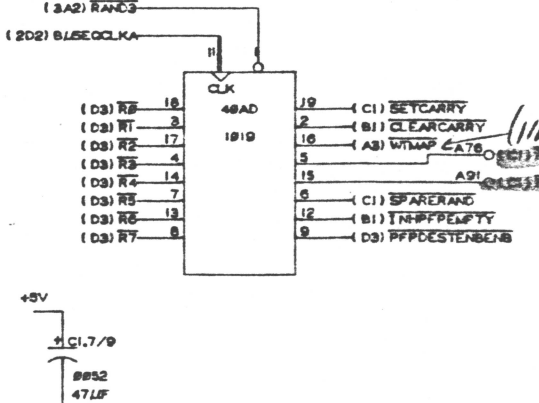
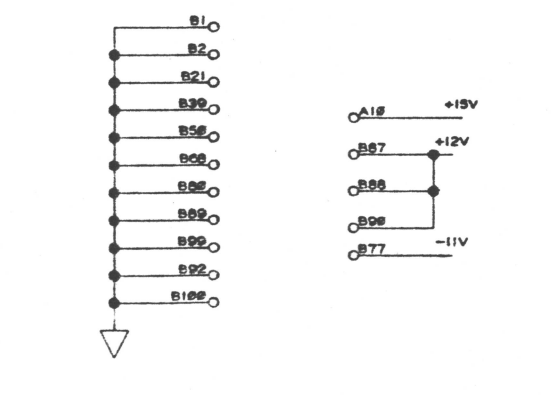
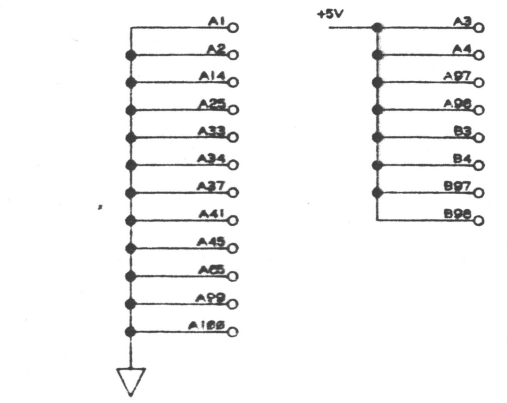
Lesser Random Decode

REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE



(B5) Enable I/O Control Signals
 (B6) Load Data into UART to be XMT'd
 (B7) Load Data into UART to be EXT. PC, PFP PC
 To Random Prog. Logic - 4186

(11B2) W. to PFP Bus into Moprans
 3 FPU



(RANDOM OPERATIONS AND I/O CONTROL SIGNALS)

DRAWN	DATA GENERAL CORPORATION
CHECKED	SOUTH BORD MASSACHUSETTS 01772
ENGINEER	TITLE
APPROVED	DGC NOVA
POST USED ON	SIZE CODE
	DRWG NUMBER
	REV

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REVISIONS				
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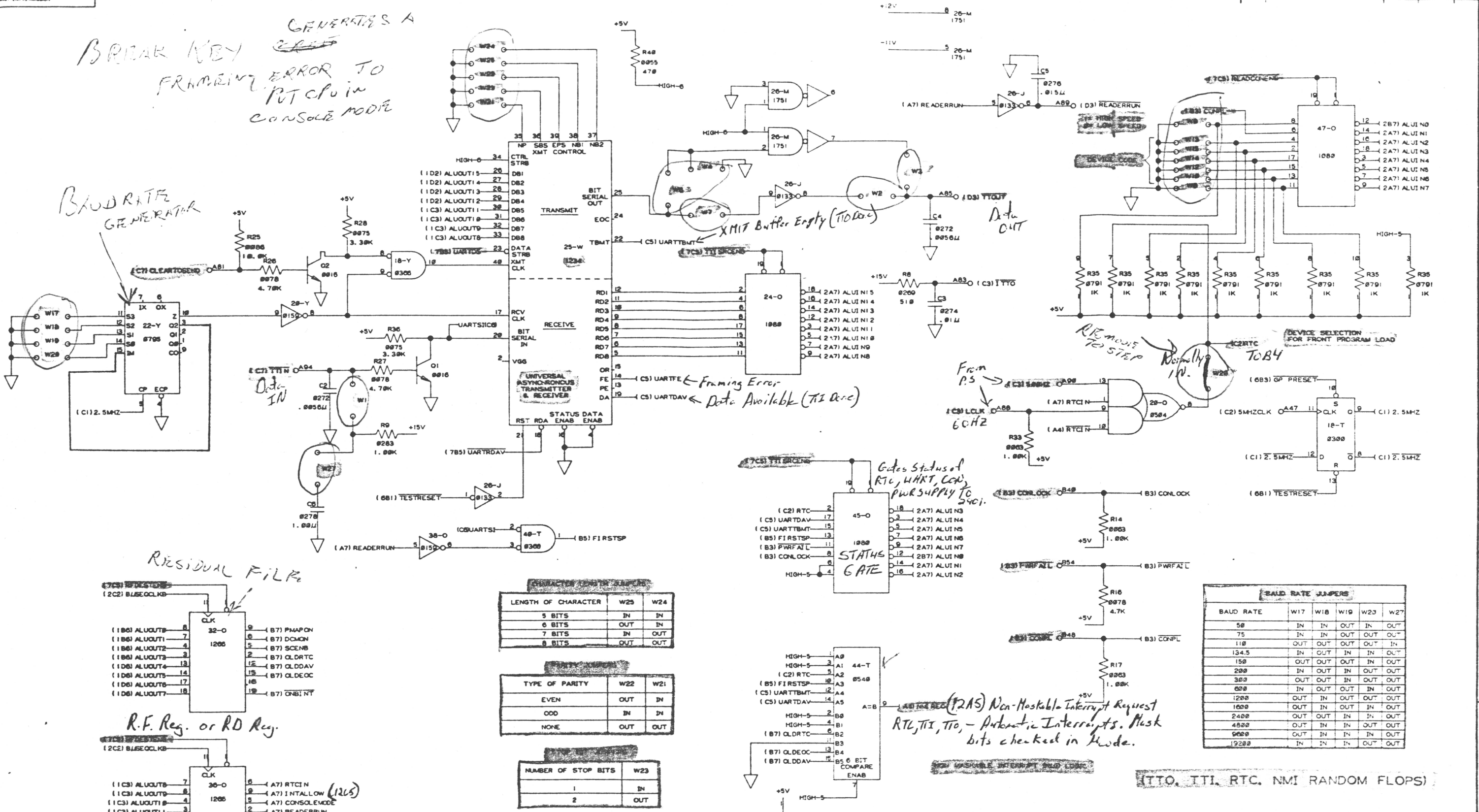
BREAK KEY GENERATES A FRAMING ERROR TO PUT CPU IN CONSOLE MODE

BAUD RATE GENERATOR

RESIDUAL FILTER

R.F. Reg. or RD Reg.

To RUN MODE LED on Console



CHARACTER LENGTH JUMPERS

LENGTH OF CHARACTER	W25	W24
5 BITS	IN	IN
6 BITS	OUT	IN
7 BITS	IN	OUT
8 BITS	OUT	OUT

PARITY JUMPERS

TYPE OF PARITY	W22	W21
EVEN	OUT	IN
ODD	IN	IN
NONE	OUT	OUT

NUMBER OF STOP BITS

NUMBER OF STOP BITS	W23
1	IN
2	OUT

BAUD RATE JUMPERS

BAUD RATE	W17	W18	W19	W23	W27
50	IN	IN	OUT	IN	OUT
75	IN	IN	OUT	OUT	OUT
110	OUT	OUT	OUT	OUT	IN
134.5	IN	OUT	IN	IN	OUT
150	OUT	OUT	OUT	IN	OUT
200	IN	OUT	IN	OUT	OUT
300	OUT	OUT	IN	OUT	OUT
600	IN	OUT	IN	OUT	OUT
1200	OUT	IN	OUT	OUT	OUT
1800	OUT	IN	OUT	IN	OUT
2400	OUT	OUT	IN	IN	OUT
4800	OUT	IN	IN	OUT	OUT
9600	OUT	IN	IN	IN	OUT
19200	IN	IN	IN	OUT	OUT

TYPE OF TRANSMISSION JUMPERS

TYPE OF TRANSMISSION	INSERT JUMPERS
20 MA CURRENT LOOP	W4, W7, W2, W...
EIA RS232-C	W6, W3

DATA GENERAL CORPORATION
SOUTHBORO MASSACHUSETTS 01772

TITLE: **DGC NOVA**

SIZE: **D** | CODE: **00100162401** | DRAWING NUMBER: **01** | REV:

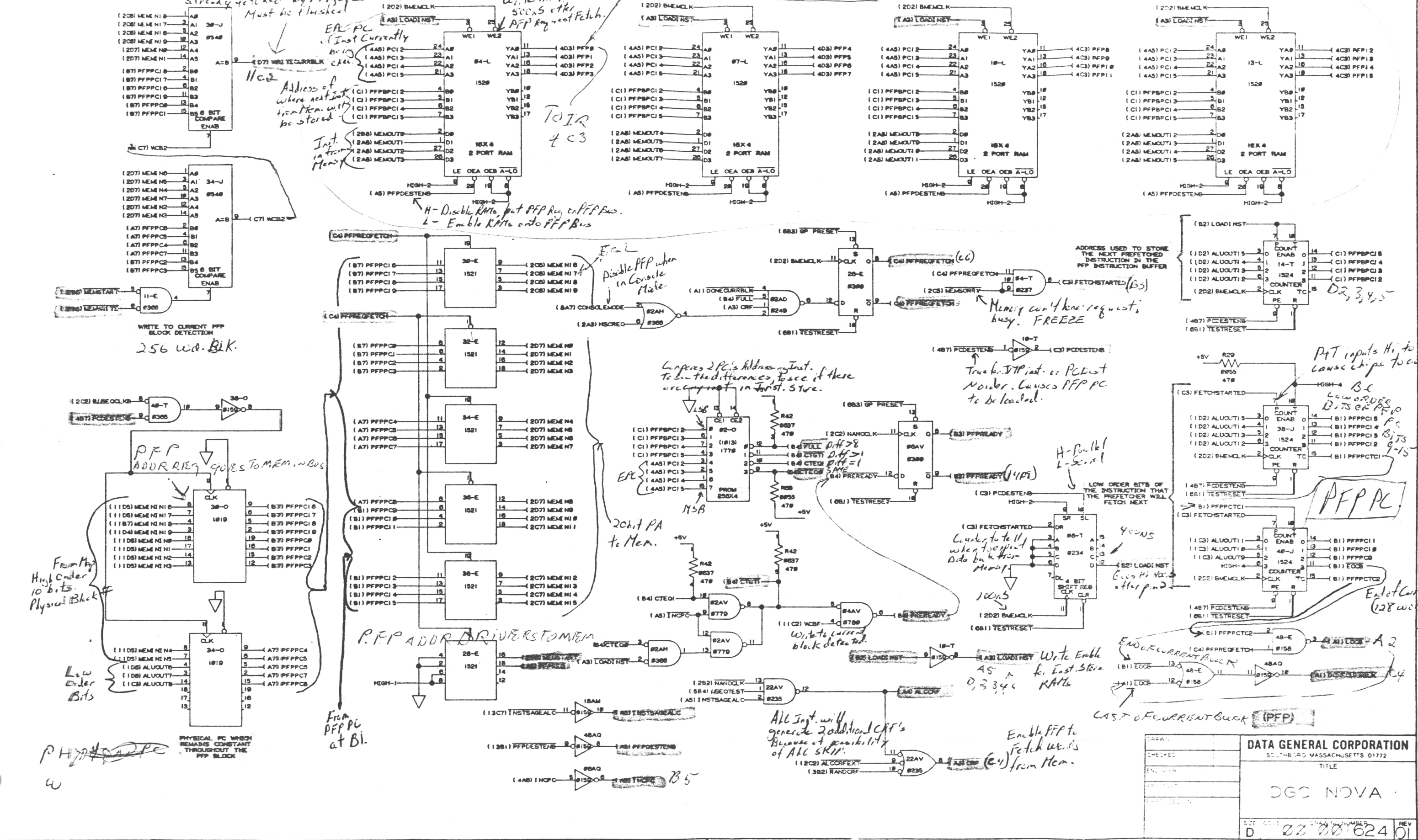
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REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY DATE

If true, CPU is writing into current block the PFP is locking it. This means that CPU may have modified an inst. already fetched by PFP, so Inst. STORE must be flushed.

PC REFS OUT INST

11 WORDS REMOVED



Address of Inst. currently being fetched from Mem. with Inst. in PFP must be stored.

Inst. in PFP must be stored.

TOIR 4 C3

H - Disable RAM, but PFP Req. on PFP Bus.
L - Enable RAM onto PFP Bus.

Disable PFP when in Console state.

Compare 2 PC's address of Inst. to see if there are any differences, to see if there are any differences in Inst. Store.

True for JTP inst. or PC Inst. Number. Causes PFP PC to be loaded.

H - Parallel L - Serial

Counter to tell when to permit Data bus to Mem.

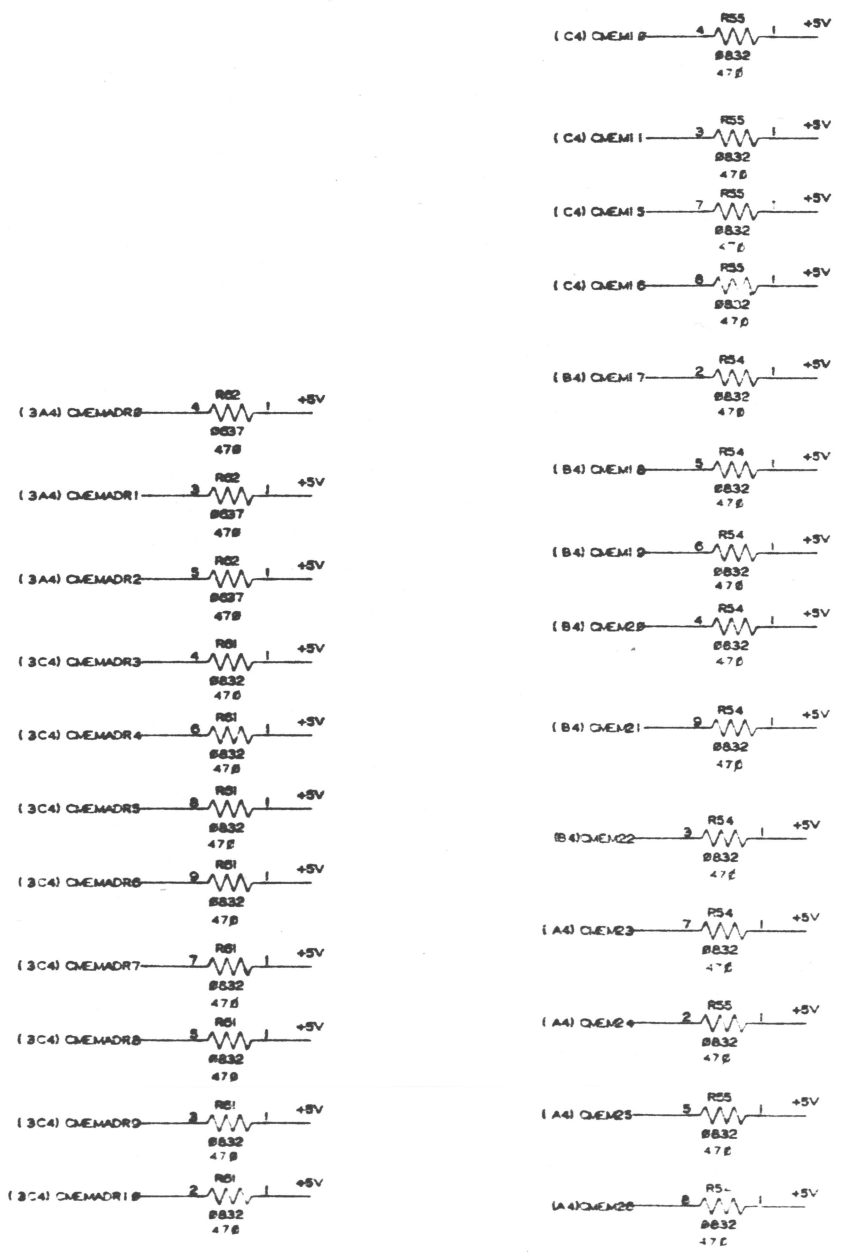
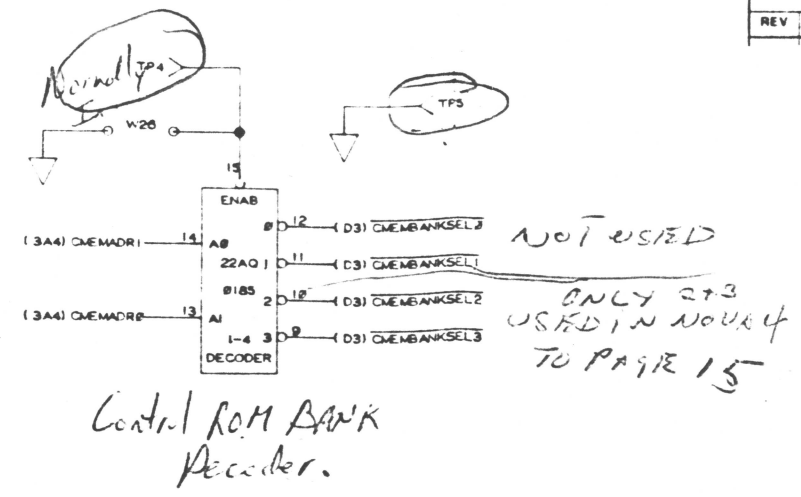
All Inst. will generate 2 additional CFF's because of possibility of ALU SKIP.

Enable PFP to Fetch ut. d's from Mem.

	DATA GENERAL CORPORATION	
	SOUTH BRIDGE MASSACHUSETTS 01772	
	TITLE	
	DGC NOVA	
	SIZE	REV
	D	02 00 624 01

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REV	DESCRIPTION	DRFTG	APP BY DATE



(CONTROL ROMARRAY)

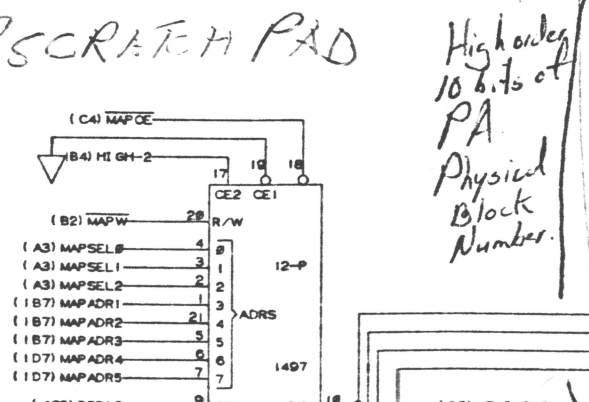
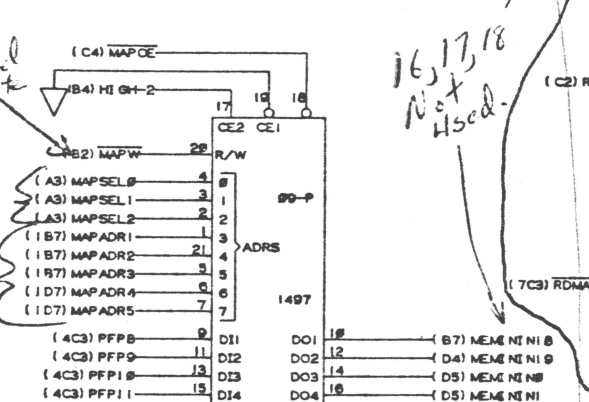
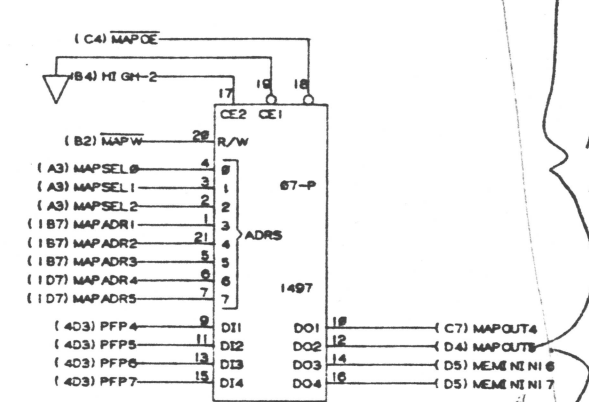
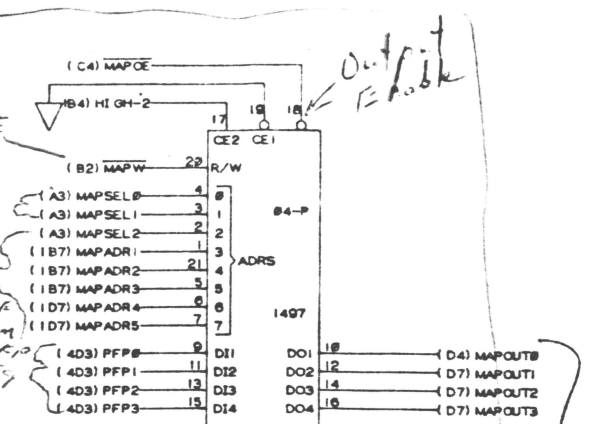
DRAWN		DATA GENERAL CORPORATION SOUTHBORO MASSACHUSETTS 01772 TITLE CONTROL ROMARRAY SIZE CODE D 071001624 01
CHECKED		
ENGINEER		
APPROVED		
TEST USED ON		REV

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REVISIONS				
REV	DESCRIPTION	DRFTG	APP BY	DATE

MapSel: 12110

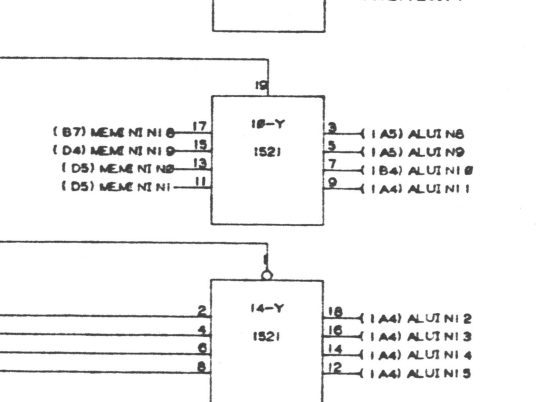
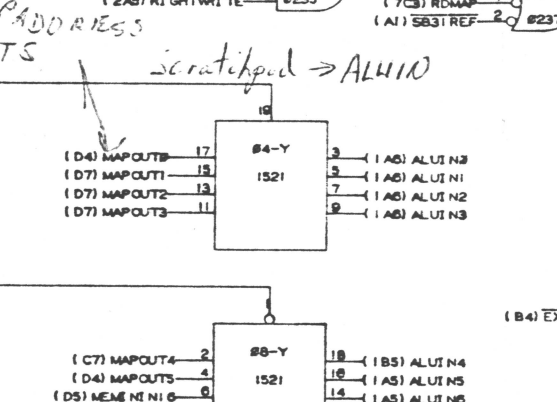
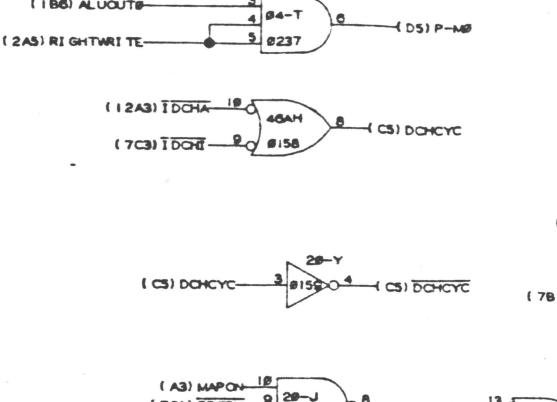
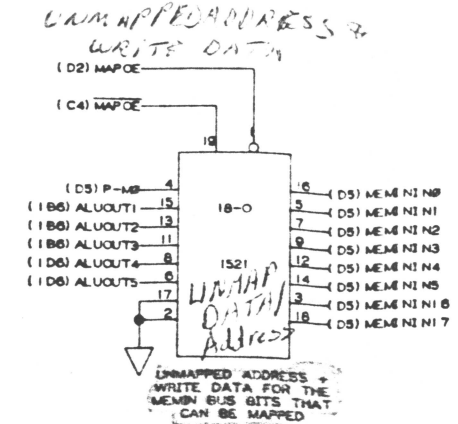
000	45cr.A
001	SCRATCH PAD
010	45cr.B
011	Unused
100	DCHMAPA
101	Unused
110	DCHMAPB
111	Unused



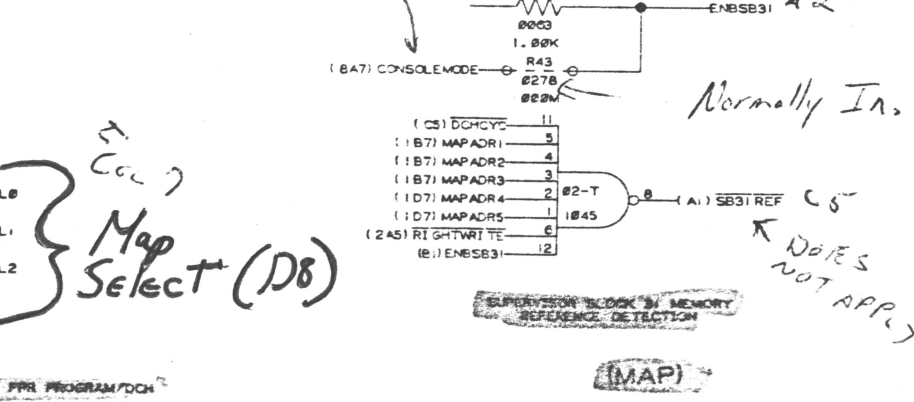
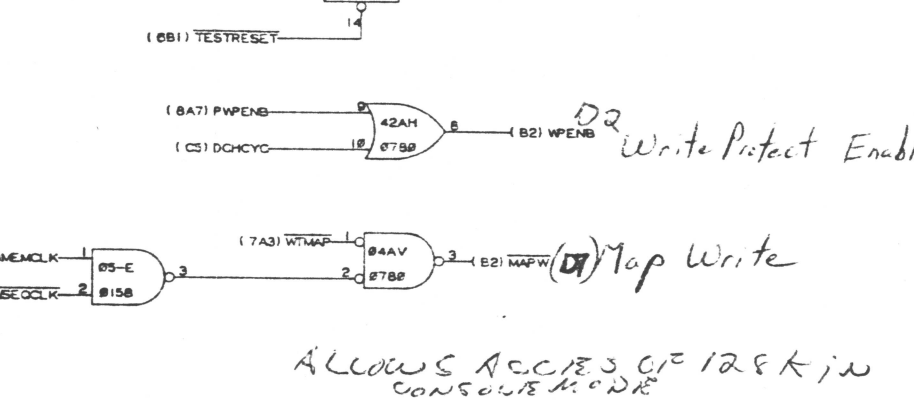
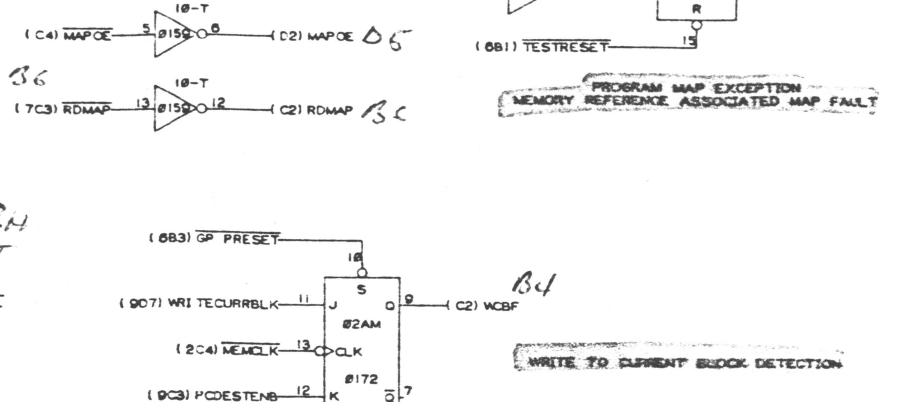
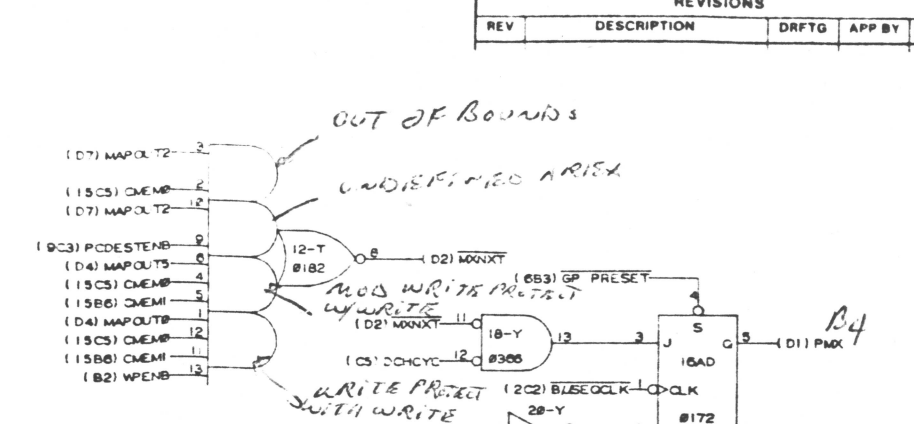
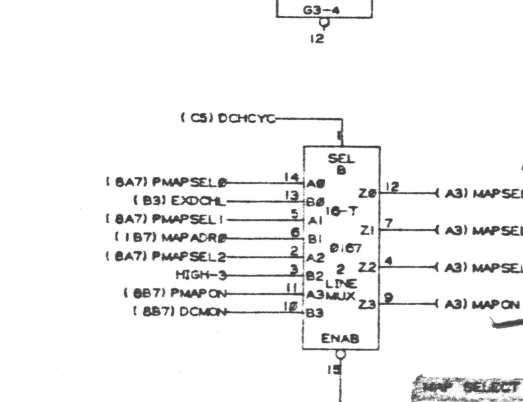
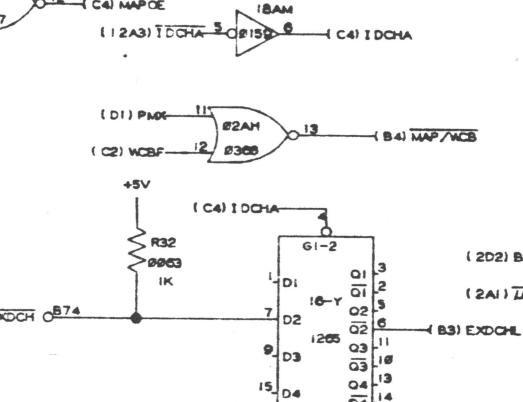
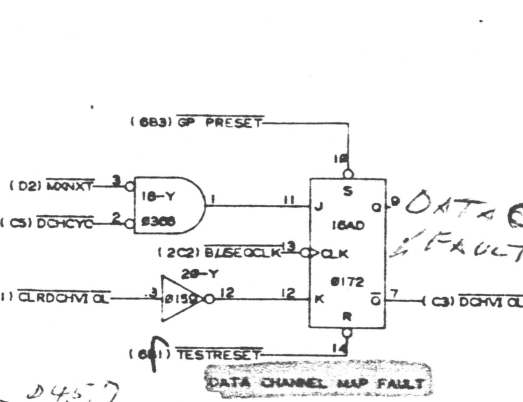
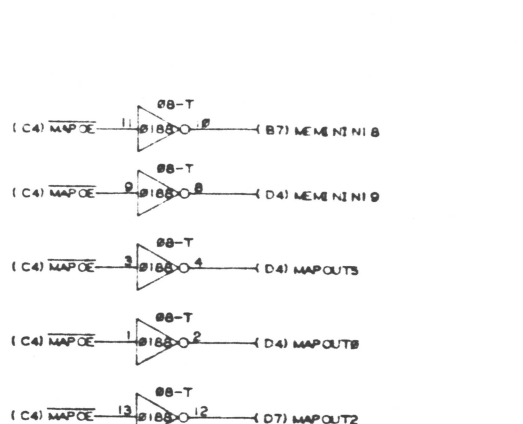
MAP SCRATCH PAD

256 x 16

SCRATCHPAD RAM EXCLUDES MAP ENTRIES



SCRATCHPAD RAM ALL INPUT SOURCE



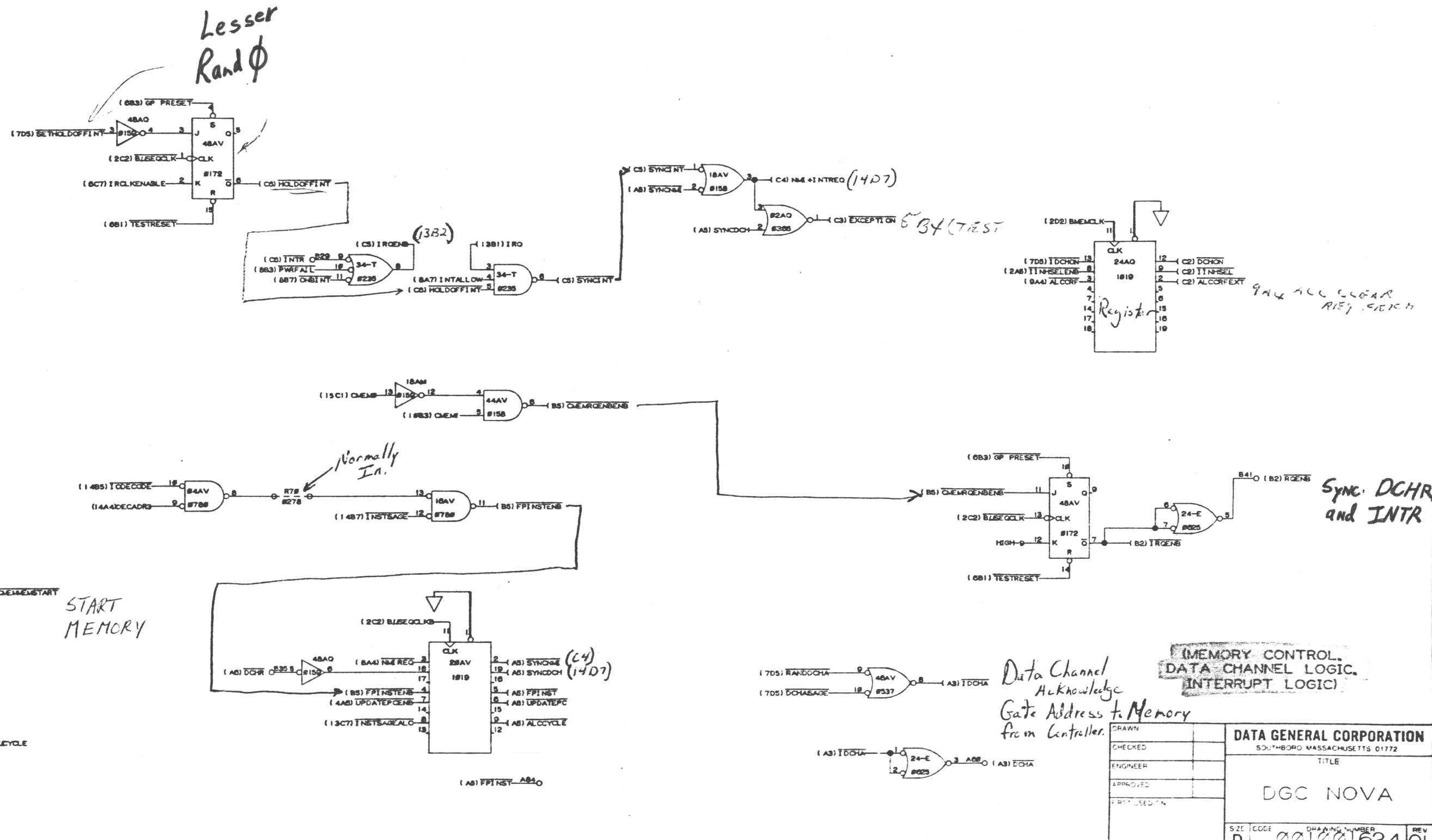
MAP SELECT FOR PROGRAM/DCH

DRAWN		DATA GENERAL CORPORATION SOUTH BORD MASSACHUSETTS 01772 TITLE DGC NOVA SIZE FOOT DRAWING NUMBER REV D 00100.024 01
CHECKED		
ENG'NEER		
APPROVED		
SHEET 11 of 5		

D
C
B
A

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MEMORY CONTROL
DATA CHANNEL LOGIC
INTERRUPT LOGIC

Data Channel Acknowledge Gate Address to Memory from Controller.

DRAWN		DATA GENERAL CORPORATION SOUTH BORD MASSACHUSETTS 01772 TITLE DGC NOVA SIZE CODE DRAWING NUMBER REV D 001001624 01
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ENGINEER		
APPROVED		
PRINTED IN		

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REVISIONS				
REV	DESCRIPTION	DRFTO	APP BY	DATE

Mul/Div

AC SOURCE

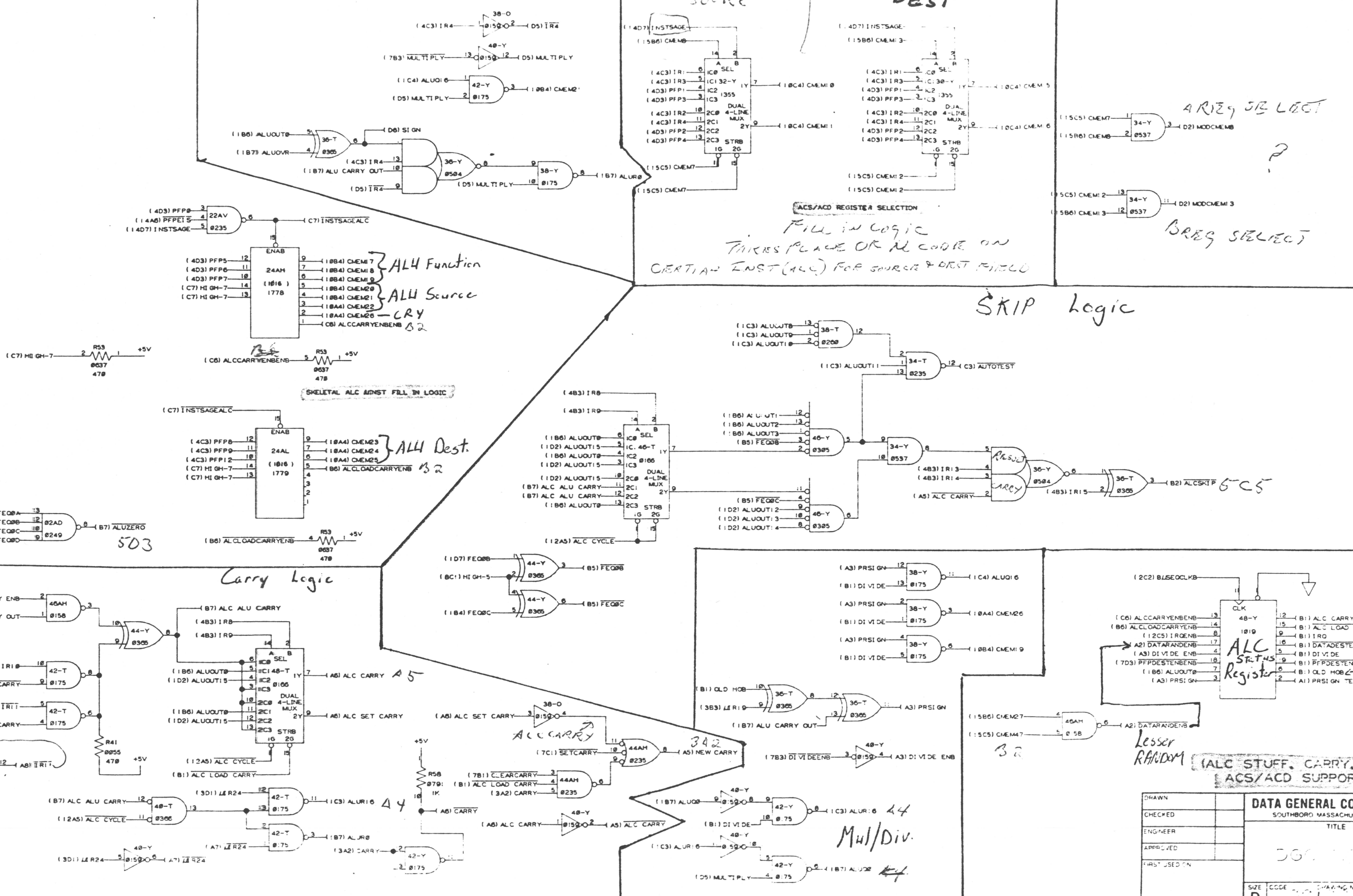
AC DEST

D

C

B

A



ACCS/ACD REGISTER SELECTION
 Fill in logic
 THIRDS PLACE OR AL CODE ON
 CERTAIN INST(ACC) FOR SOURCE & DEST FIELD

SKIP Logic

Carry Logic

ARIZY JZ LECT

BREG SELECT

ALC STUFFS Register

Lesser RANDOM (ALC STUFF, CARRY, AND ACS/ACD SUPPORT)

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CHECKED	
ENGINEER	
APPROVED	
FIRST USED ON	

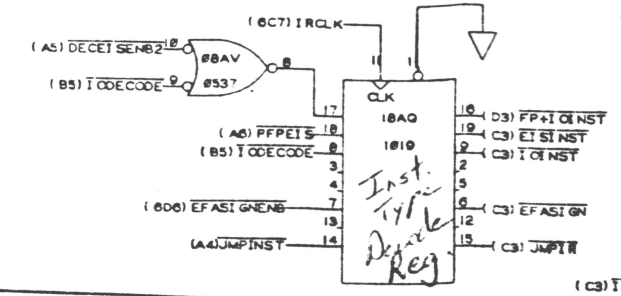
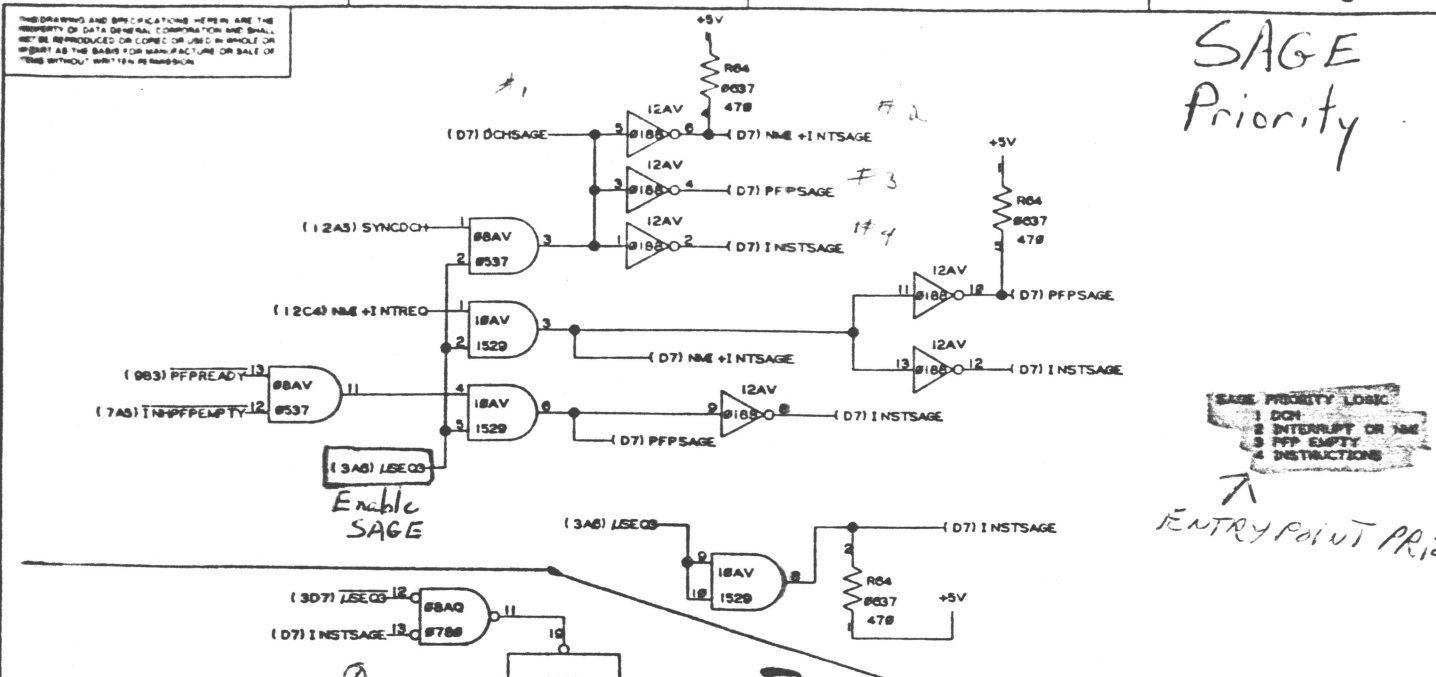
DATA GENERAL CORPORATION
 SOUTHBORO MASSACHUSETTS 01772
 TITLE
 300-1074

SIZE	CODE	DRAWING NUMBER	REV
D		300-1074	01

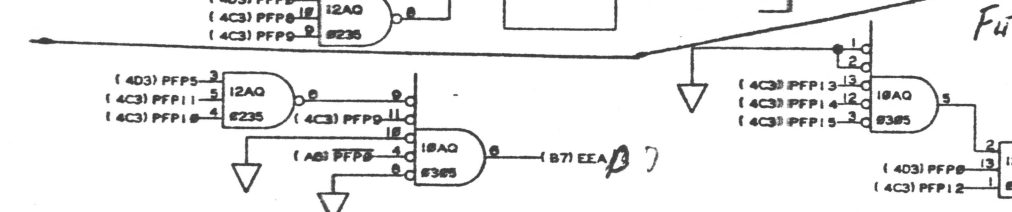
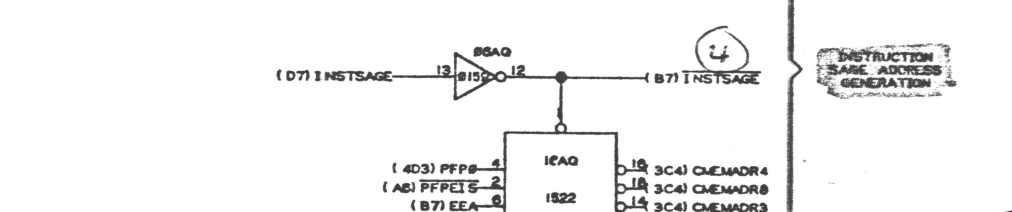
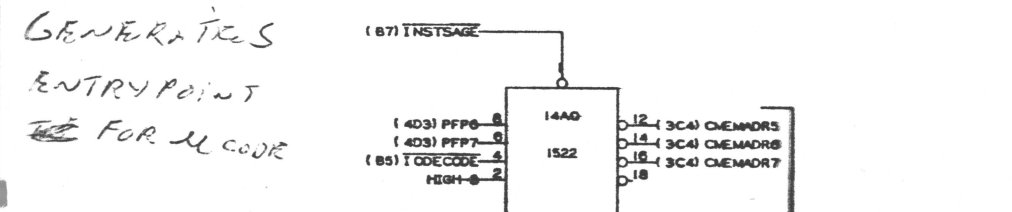
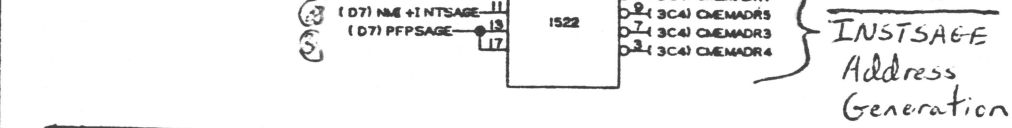
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SAGE Priority

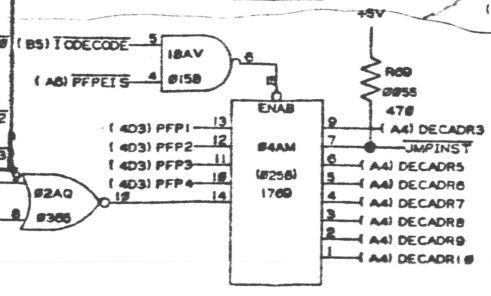
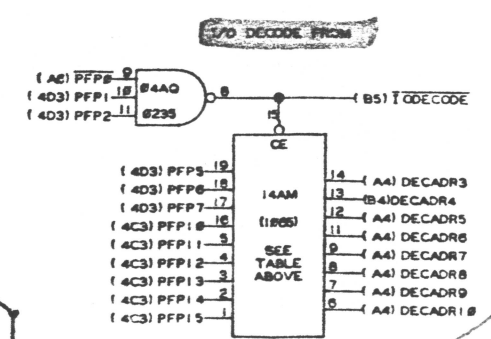


Instruction Decode

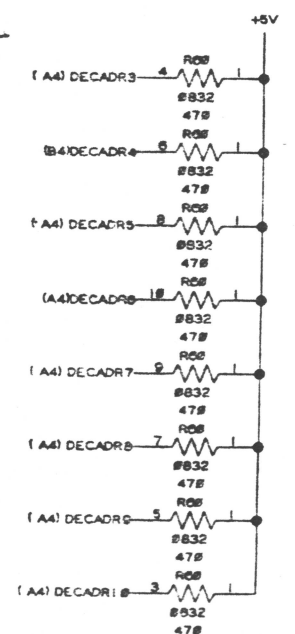
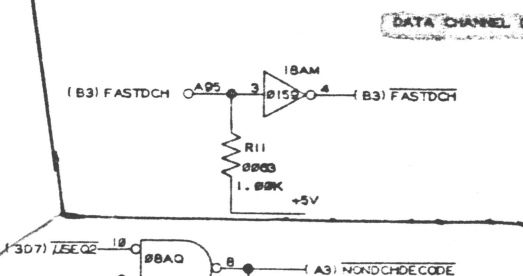
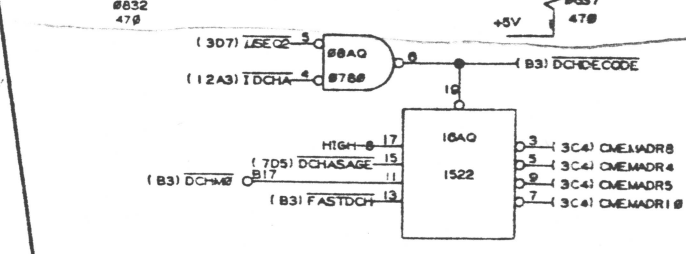
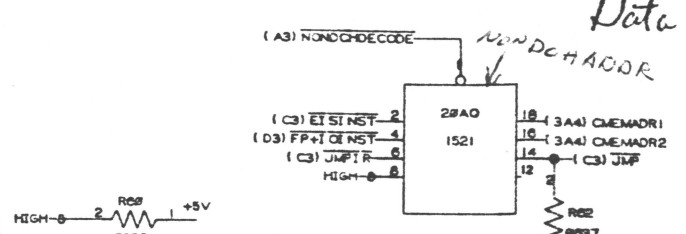


USED FOR 4 S/X AND MUL/DIV

TABLE		
005012067	-	1734
005012705	-	1780
005012787	-	1780
005012786	-	1790



Data Channel Decode Address



(DECODE SAGE)

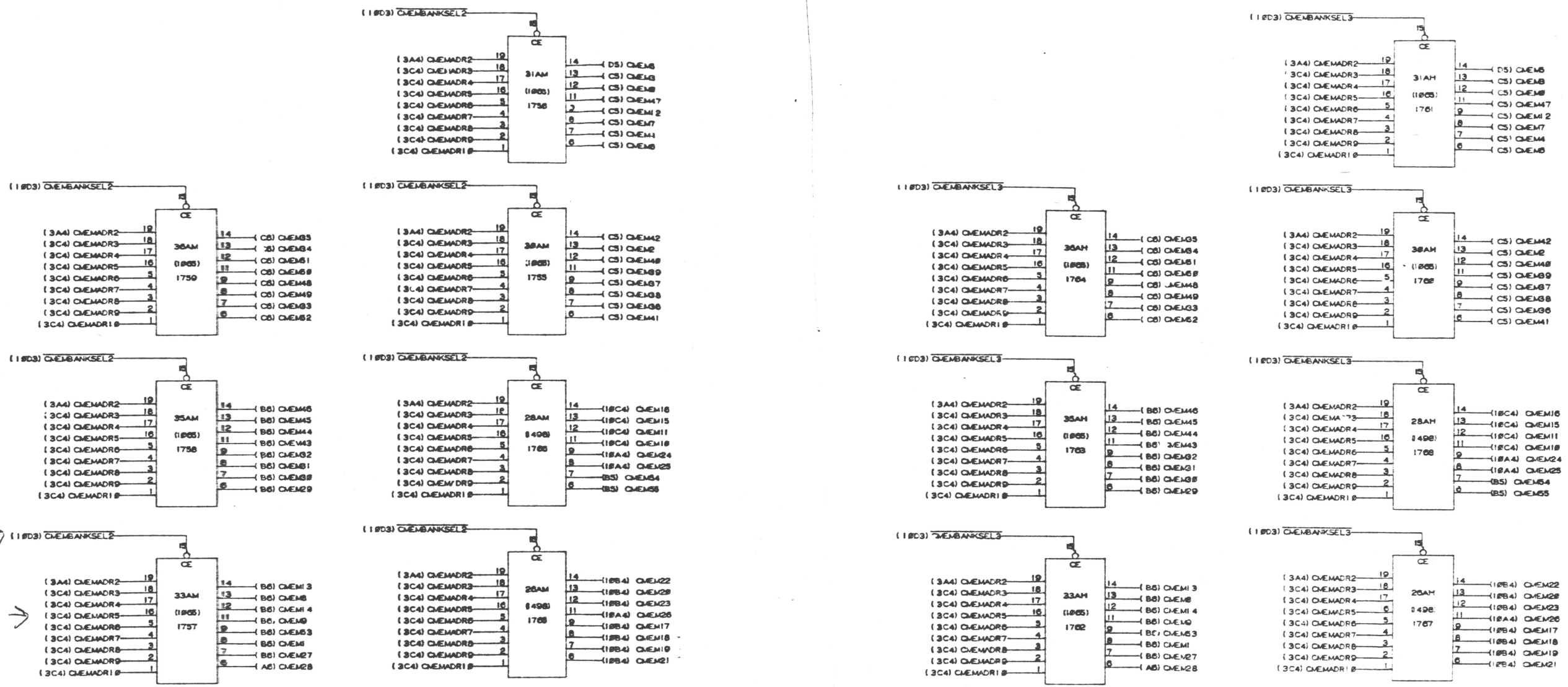
CONTROL MEM ADDR NONDCH

DRAWN		DATA GENERAL CORPORATION SOUTHBORO MASSACHUSETTS 01772 TITLE DGC NOVA SIZE CODE 00100 NUMBER 62401 REV
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ENGINEER		
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SELF TEST
 RESET RUNS PROGRAM INTO SELF TEST
 3777



RBIT BANK SEL →
 9BITSSEL →

CONTROL MEMORY ADDRESSES 3999 TO 2777

CONTROL MEMORY ADDRESSES 3999 TO 2777



(CONTROL ROMARRAY)

DRAWN		DATA GENERAL CORPORATION SOUTHBORO MASSACHUSETTS 01772 TITLE DGC NOVA SIZE CODE 20 1624 01
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		