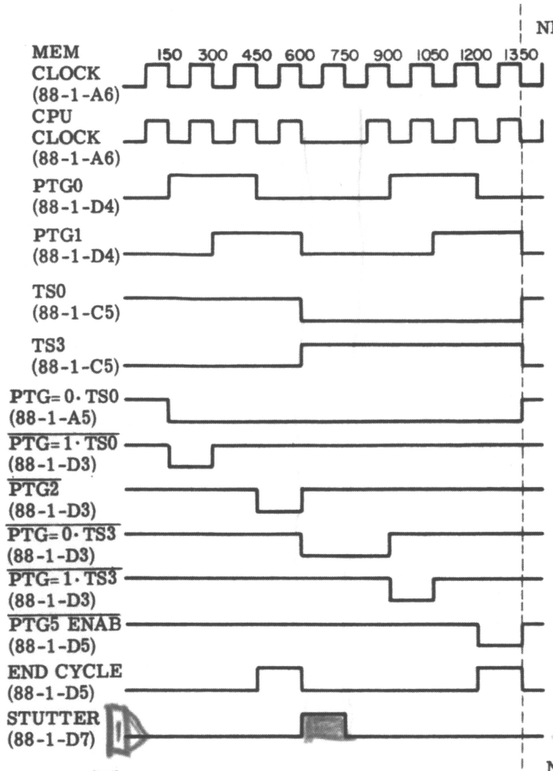


NOTE: DATA IS ON BUS FOR 1050μsec.

Figure C-2 Timing For The Processor Timing Generator During Fetch or Key

Between TS0 & TS3 have an extra 150 Ns allows time to decode Instruction and set up controls for ~~Fetch~~ that are necessary for instruction 1

Process Time
Accumulator Timing
Memory Timing Ge

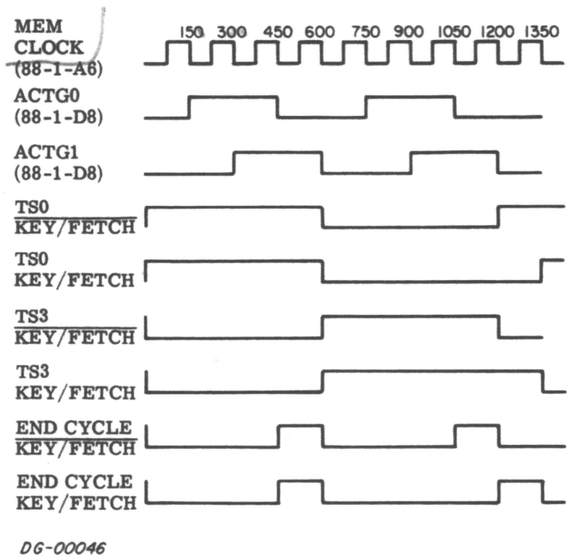
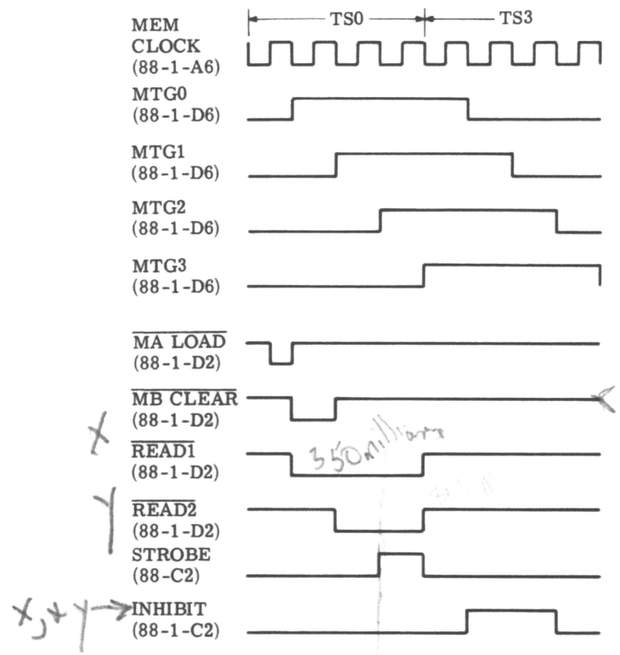


Figure C-3 Timing For The Accumulator Timing Generator

ACCUMULATOR TRUTH TABLE (88-4-B6 & B7 U124 & U123)



MEMORY TIME GEN. COUNTS

	MTG0	MTG1	MTG2	MTG3
TS0	0	0	0	0
1st CLOCK	1	0	0	0
2nd CLOCK	1	1	0	0
3rd CLOCK	1	1	1	0
4th CLOCK	1	1	1	1
SEE NOTE				
TS3	1	1	1	1
1st CLOCK	0	1	1	1
2nd CLOCK	0	0	1	1
3rd CLOCK	0	0	0	1
4th CLOCK	0	0	0	0

NOTE - IF LOOPING TS0, CLOCK FREEZES WITH ALL ONES UNTIL FIRST CLOCK IN TS3.

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Figure C-4 Timing For The Memory Timing Generator