Technical Manual

4240 INTERPROCESSOR BUS SUBSYSTEM

015-000033-00

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Model 4240

INTERPROCESSOR BUS SUBSYSTEM

DataGeneral

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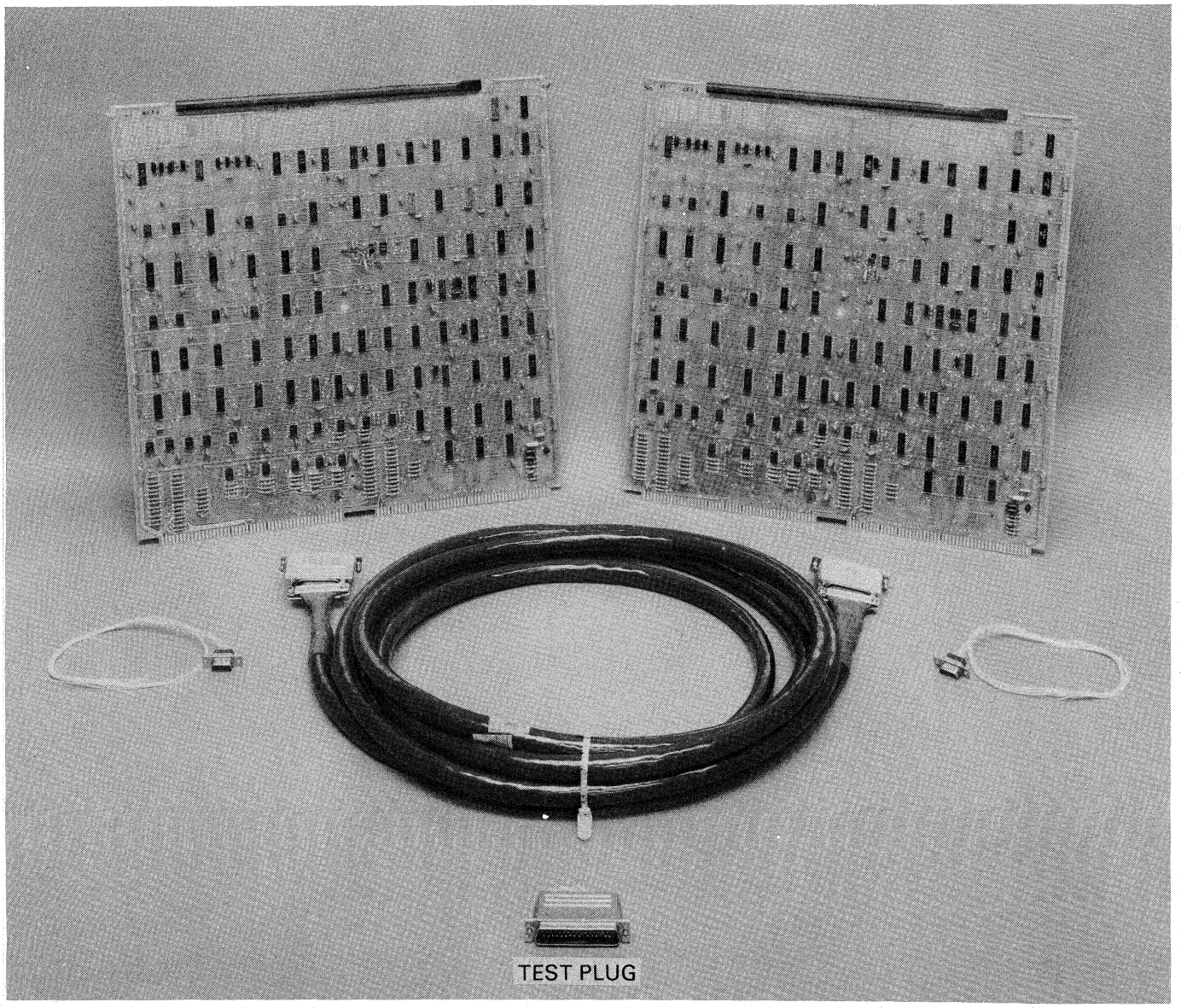


4240 SUBSYSTEM

SECTION I
OVERVIEW

INTRODUCTION

The Data General Corporation 4240 Inter-Processor Bus (IPB) subsystem provides the facilities for asynchronous communications between any two NOVA or ECLIPSE line computers. It consists of two, identical, 15" square, IPB printed circuit boards (one board installed in an I/O slot of each computer); one connecting 15' IPB external cable; and two internal cables (one cable installed in each computer) connecting the printed circuit boards to the external cable.

The IPB subsystem is under the direct program control of both computers and provides the computers with the following distinct capabilities:

- Bi-directional, full-duplex communications between computers.
- Bi-directional, half-duplex communications between computers, which may be "interlocked" with suitable software. The "interlock", consisting of interconnected status flags, allows only one processor to transmit data when the appropriate software protocol is honored by both computers.
- Program interrupt request in either computer when the other computer: 1) fails to perform as expected; or, 2) generates a signal indicating a probable "power fail" condition. This capability is implemented by missing pulse detectors and is called the Watchdog Timer facility.

The IPB transfers two types of information between processors: status information and data. Status information is transferred by the setting of Busy and Done flags. These flags are set both by programmed I/O instructions and by flag interactions between boards. Each processor is notified of status information either by means of the program interrupt facility or by flag checking software routines. Data is transferred between an accumulator in one processor and an accumulator in the other processor under direct program control, one 16-bit word at a time.

Using software routines solely dedicated to the operation of the IPB, two NOVA or ECLIPSE line computers can achieve data transfer rates exceeding 100,000 16-bit words per second. Using the program interrupt facility, the data transfer rate is limited by the time required by the interrupt handling routine in each computer.

The IPB is useful in applications where direct program control over the transfer of information is needed and where the information must be transferred rapidly. Typical applications of the IPB include: parallel processing arrangements, communications concentration systems, shared disc environments, and back-up systems. In a parallel processing arrangement or in a communications concentration system, the full-duplex communications link allows two computers to exchange data rapidly. In a shared disc environment, the "interlock" capability of the half-duplex communications link provides a means of communicating disc space reservations and actions performed on disc files. In a back-up system, the "Watchdog Timer" facility can be used to notify one computer of a possible software or hardware failure in the other computer.

Architecture

The communications capabilities of the IPB subsystem are implemented by the two IPB printed circuit boards and the IPB external cable. Although the two boards are identical, when they are connected to the IPB external cable they assume different roles. These roles are assigned by asymmetrical wiring of the "Left" and "Right" connectors of the cable. In this manual, each IPB board is referred to by its connection to the external cable; i.e., "Left" IPB board, "Right" IPB board. In data communications, the "Right" IPB board serves as the data holding area; the "Left" IPB board serves in a gating capacity. This distinction between "Left" and "Right" IPB boards does not affect the programming, operation, or communications abilities of either computer in the system.

The block diagram shows the data paths, data holding areas, missing pulse detectors, and status flags used in IPB communications.

Data Paths and Holding Areas

Data is transferred between a specified accumulator in the computer and that computer's IPB board via the I/O data bus. The data path between each processor's I/O data bus and the data holding areas of the IPB differs. On the "Right" IPB board, data is transferred directly between the "Right" processor's I/O data bus and the data holding areas. On the "Left" IPB board, data is transferred between the "Left" processor's I/O data bus and the data holding areas on the "Right" IPB board via a 16-bit, bi-directional, half-duplex, data bus in the external cable. A general purpose transmitter and a general-purpose receiver on the "Left" IPB board, which function as repeaters, form the communications link between the external cable data bus and the I/O data bus of the "Left" processor.

The data holding areas on the "Right" IPB board consist of four 16-bit storage buffers. Associated with each storage buffer is a set of 16 gates which function as a receiver. The storage buffer of this storage buffer/receiver combination is under the direct program control of one of the processors while its associated receiver is under the direct program control of the other processor. Each processor controls one full-duplex and one half-duplex storage buffer and one full-duplex and one half-duplex receiver. Each storage buffer and each receiver responds to a device code.

In full-duplex communications, the processor's full-duplex storage buffer is referred to as a 16-bit full-duplex transmitter and responds to device code 41; the processor's full-duplex receiver is referred to as a 16-bit full-duplex receiver and responds to device code 40.

In half-duplex communications, the processor's half-duplex storage buffer and half-duplex receiver are referred to as a 16-bit half-duplex transmitter/receiver and respond to the same device code, 36.

Data is loaded into a storage buffer by the execution of the appropriate I/O instruction in the transmitting processor. This data is latched at the buffer's output and is available to the receiving processor. When the receiving processor executes the appropriate I/O instruction, the associated set of receiver gates is enabled, allowing the contents of that storage buffer to pass to the receiving processor's I/O data bus.

This separate control of the storage buffer and its associated receiver allows asynchronous data communications between processors. The arrangement of the storage buffer/receiver combinations allows data to be transferred from the left processor to the right processor and from the right processor to the left processor in both full- and half-duplex communications. In full-duplex communications, the true, half-duplex character of the external cable data bus is transparent to the programmer because of the high-speed data transfer rate capability of the IPB.

Missing Pulse Detectors

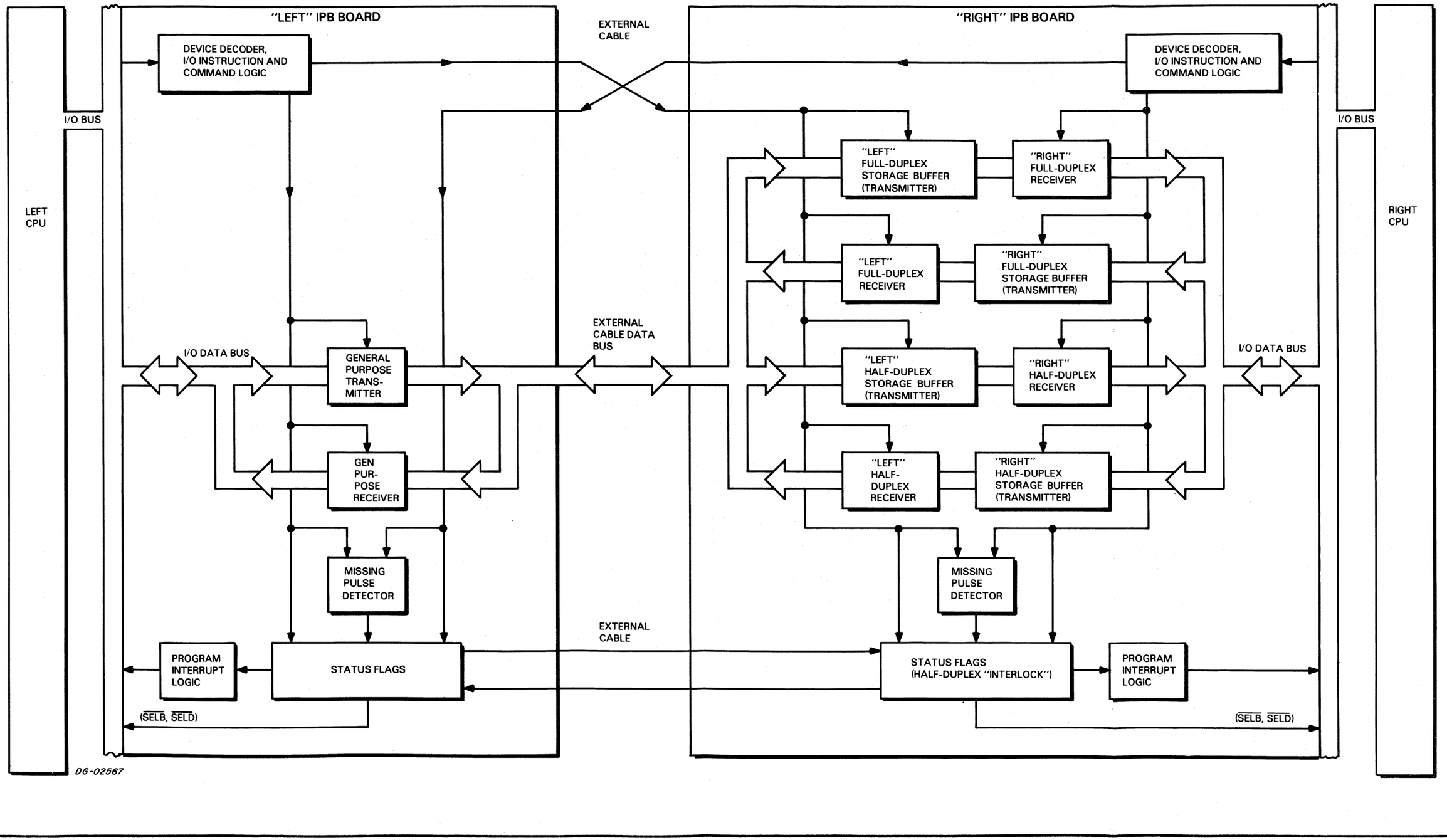
The missing pulse detectors, one on each IPB board, respond to device code 37. Each detector consists of a one-second timer which is normally restarted by the execution of the appropriate I/O instruction in the other computer at regular intervals of one second or less. When one computer fails to restart the timer in the other computer within the specified time period, that timer's Done flag is set, generating a program interrupt request in the computer in which the timer is installed. Additionally, when either computer knows that it is about to cease functioning (e.g., a power fail condition), that computer may set the other computer's timer Done flag directly by the execution of the appropriate I/O instruction.

Status Flags

Each IPB communications element, or device, has its own set of status flags. The status flags for the devices under the control of the "Left" processor are located on the "Left" IPB board; the status flags for the devices under the control of the "Right" processor are located on the "Right" IPB board. In addition, the "Right" IPB board contains the Busy flag circuitry for both half-duplex transmitter/receiver devices; this circuitry provides the software "interlock" in half-duplex communications.

When the appropriate software is used, these flags provide the processors with useful information; such as, a word is in a storage buffer, the half-duplex communications link is or is not available for transmitting data, the other processor is experiencing a probable software or hardware malfunction.

FUNCTIONAL BLOCK DIAGRAM OF THE 4240 INTER-PROCESSOR BUS SUBSYSTEM



THE IPB TECHNICAL MANUAL

The purpose of this manual is to describe the logical operation of the IPB subsystem. The information is presented in two sections:

- Section I introduces the 4240 Inter-Processor Bus subsystem and the conventions used to describe it.
- Section II describes the logical operation of the IPB.

Print References

To assist the reader in understanding the IPB subsystem, frequent references are made to the IPB logic schematic, DGC No. 001-000614. Portions of this schematic are referred to by grid reference; e.g., 2A5. The grid reference 2A5 is interpreted as follows: the first number of the reference, 2, is the page number of the schematic; the letter A refers to the row on that page; and the last number, 5, refers to the column on that page.

Nomenclature

The title blocks on each page of the IPB logic schematic refer to the communications link described on that page as follows: IPB Interlocked Comm. refers to the half-duplex communications link; IPB Non-Interlocked Chan. refers to the full-duplex communications link; and Interval Timer refers to the Watchdog Timer.

Logic Conventions

Drawings

Data General logic prints are drawn in close accordance with Mil-Std-806C. With this convention, logical functions are drawn as physically implemented. That is, where discrete gates are used to implement a function, these gates are shown. On the other hand, where a more complex integrated circuit is used, for instance a multiplexor, that function is shown as a rectangular box instead of the gates comprising the function.

Signal Levels

Throughout this manual, a distinction is frequently made between electrical levels and logical values. To minimize confusion, electrical levels are always indicated by an "H" or "L", and logical values by a "1" or "0". As an electrical level, an "H" indicates that the signal is high (greater than +2.0 volts) and an "L" indicates that it is low (less than +0.7 volts). An asserted, or true, signal is indicated by a logical "1" and a false signal by a "0".

Signal Names

The voltage level at which a signal is said to be "asserted" (true) is a matter of definition. To distinguish between signals that are asserted high (0=L, 1=H) and those that are asserted low (0=H, 1=L), a naming convention has been adopted in Data General's documentation which defines the relationship between the logical value and electrical level of a signal. If the signal name includes a horizontal bar over the name, as $\overline{\text{WRITE}}$, then that signal is asserted when it is at a low electrical level; conversely, a signal without the bar, **WRITE** is asserted when high. Logical functions may often require more than one binary signal. For instance, three lines are required to express an octal digit. Generally, these closely related signals are individually identified by effectively subscripting a common label. For instance, suppose that **BUS0** through **BUS5** are all required to completely specify a function. All or part of such a group of signals is identified by placing brackets around the range of subscripts included, as **BUS[0-5]** In this case, the suffix carries the information that there are six **BUS** lines under discussion, from **BUS0** through **BUS5**, inclusive.

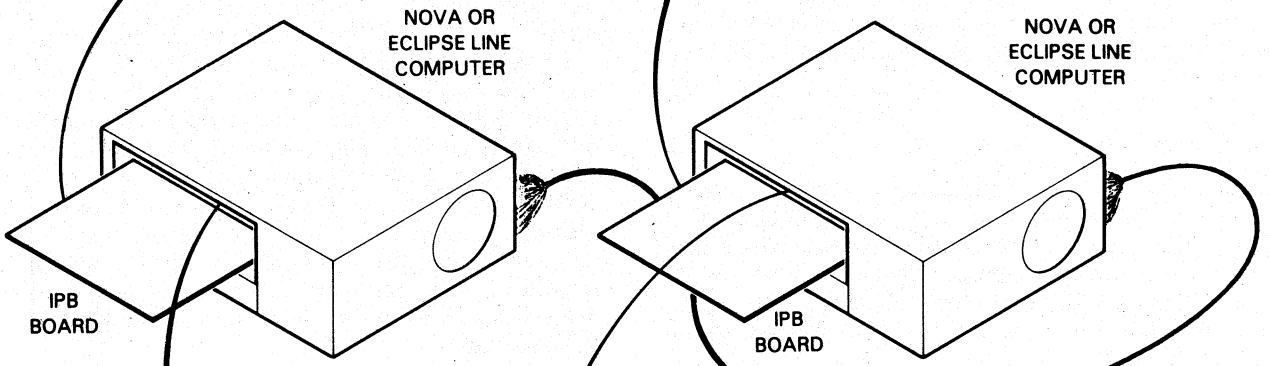
RELATED DOCUMENTS

The IPB Related Documentation diagram lists the engineering drawings and the manuals pertinent to the IPB. The ordering number of each document is listed in the diagram. The Components Guide gives logic diagrams, pin designations and truth tables for the I.C.'s used in Data General equipment. The Interface Designer's Reference, NOVA and ECLIPSE Line Computers, provides useful information concerning the processor's I/O bus and the program interrupt system. The Installation Data Sheet explains how to install the 4240 Inter-Processor Bus subsystem. The Technical Reference, 4240 Inter-Processor Bus, explains how to program the subsystem.

The documentation diagram also lists the diagnostic and reliability program tapes and listings together with the test plug wire lists.

IPB RELATED DOCUMENTATION

IPB PRINTED CIRCUIT BOARD	
IPB LOGIC SCHEMATICS	001-000614-03
IPB ILLUSTRATED PARTS LIST	016-000152-00
COMPONENTS GUIDE	015-000028
USER'S MANUAL, INTERFACE DESIGNER'S REFERENCE, NOVA AND ECLIPSE LINE COMPUTERS	015-000031
INSTALLATION DATA SHEET	010-000091
TECHNICAL REFERENCE, 4240 INTER-PROCESSOR BUS	014-000056-01



IPB EXTERNAL CABLE, MODEL	
IPB EXTERNAL CABLE, A TO A	008-000468-02
IPB EXTERNAL CABLE, A TO B	008-000469-00
IPB EXTERNAL CABLE, B TO B	008-000470-00

IPB INTERNAL CABLES	
NOVA 820, 1210, 1220	008-000194-03
NOVA 2 AND ECLIPSE LINE	008-000426-01
NOVA 800, 830, 840, 1200	008-000467-00

TEST PLUG (required to run diagnostics)	
NOVA 800, 840, 1200	008-000465-00
NOVA 820, NOVA 2, 830, 1210 1220 AND ECLIPSE LINE	008-000466-00

DIAGNOSTIC TAPES AND LISTINGS	
AB IPB DIAGNOSTIC	095-000177-01
AB IPB RELIABILITY	095-000178-02
LS IPB DIAGNOSTIC	096-000156-01
LS IPB RELIABILITY	096-000157-02

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SECTION II
THEORY OF LOGICAL OPERATION

INTRODUCTION

The IPB subsystem consists of two sets of four communications elements (one set for each computer), which are referred to as devices. These devices provide the computers with three distinct communications links:

- The 16-bit full-duplex transmitter and the 16-bit full-duplex receiver of each processor provide the full-duplex communications link between processors.
- The 16-bit half-duplex transmitter/receiver of each processor provides the half-duplex communications link between processors.
- The missing pulse detector of each processor provides a functional status communications link between processors. This is called the Watchdog Timer facility.

Since each of these communications links functions independently when used with the appropriate software, this section of the manual is presented in four subsections: the first is concerned with that information which is common to all elements of the IPB subsystem; the second is concerned with full-duplex communications between processors; the third is concerned with half-duplex communications between processors; and the fourth is concerned with the Watchdog Timer facility.

THE SUBSYSTEM

The communications capabilities of the IPB are implemented by the two IPB printed circuit boards and the IPB external cable. The internal cables, one installed in each computer, serve only as an interface between each computer's IPB printed circuit board and the external cable.

"Left" and "Right" IPB Boards

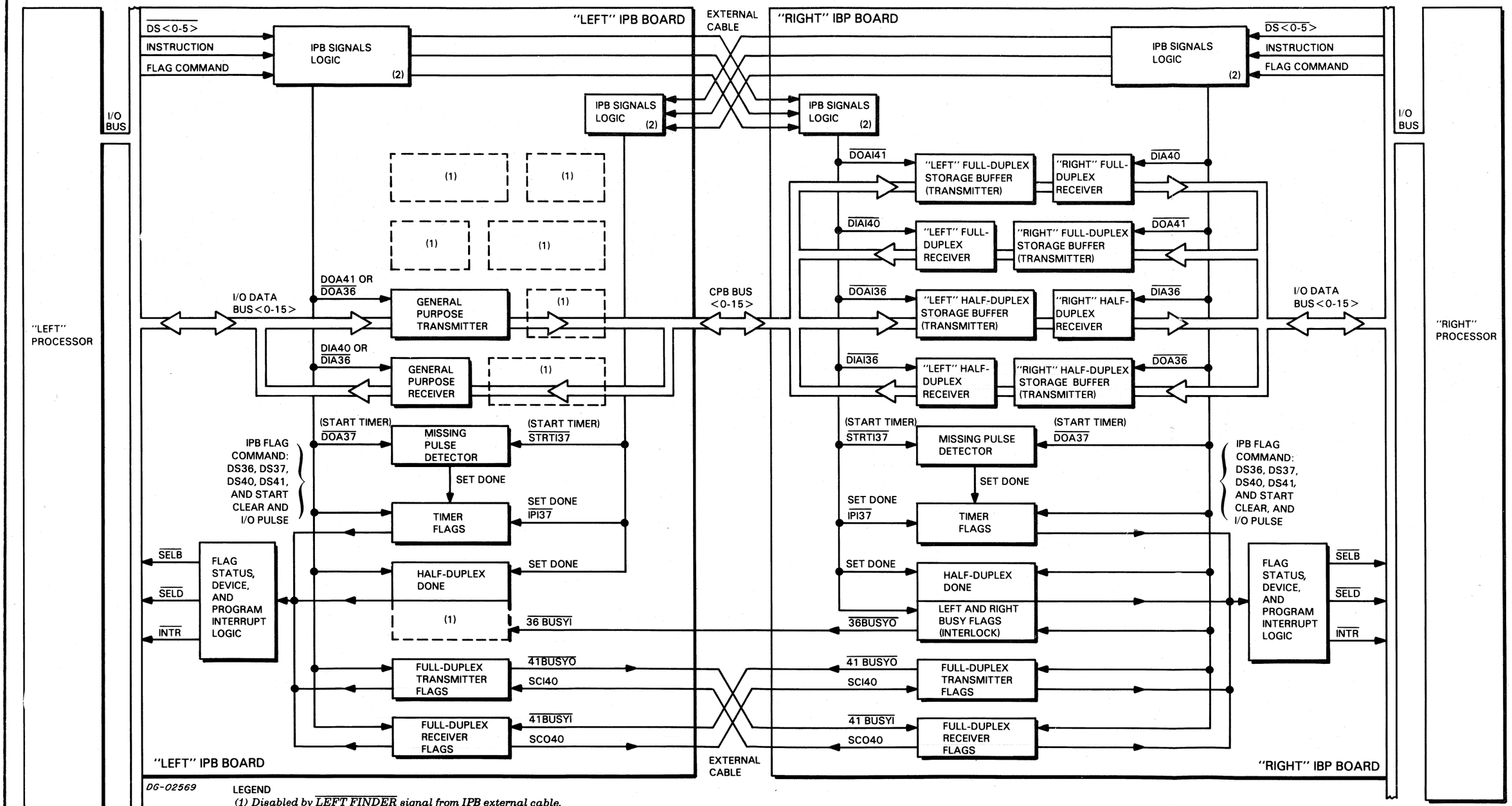
When the identical IPB printed circuit boards are connected, through the internal cables, to the external cable, the "Left" connector of the external cable partially disables the IPB board connected to it. This is accomplished by the asymmetrical wiring of the $\overline{\text{LEFT FINDER}}$ signal at the "Left" and "Right" connectors of the cable. On the "Left" IPB board, $\overline{\text{LEFT FINDER}}$ is always low; on the "Right" IPB board, $\overline{\text{LEFT FINDER}}$ is always high.

As shown in the block diagram, on the "Left" IPB board the $\overline{\text{LEFT FINDER}}$ signal disables the full-duplex storage buffer/receiver combinations. Additionally, this signal partially disables the half-duplex storage buffer/receiver combinations, allowing them to function as repeaters. In both full- and half-duplex communications, one half-duplex storage buffer/receiver combination serves as a general purpose transmitter while the other half-duplex combination serves as a general purpose receiver. The $\overline{\text{LEFT FINDER}}$ signal also disables the half-duplex Busy flag circuitry on the "Left" IPB board, which provides the software "interlock" on the "Right" IPB board.

On the "Right" IPB board, the $\overline{\text{LEFT FINDER}}$ signal enables the full-duplex storage buffer/receiver combinations and those portions of the half-duplex storage buffer/receiver combinations which are disabled on the "Left" IPB board. This arrangement allows the "Right" IPB board to serve as the data holding area for the subsystem.

The missing pulse detectors and the remaining status flags are not affected by the $\overline{\text{LEFT FINDER}}$ signal.

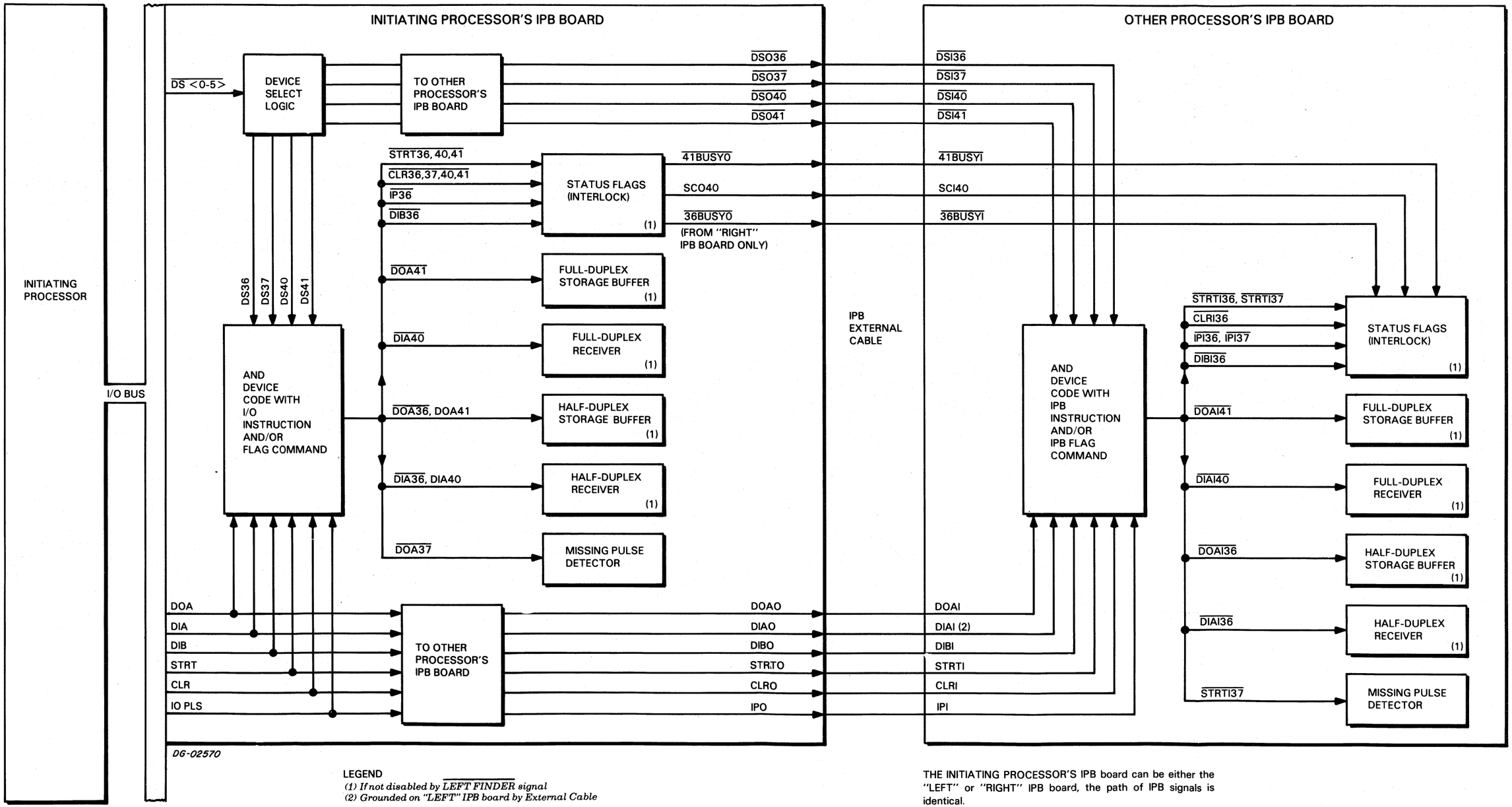
BLOCK DIAGRAM OF IPB SUBSYSTEM



LEGEND
(1) Disabled by LEFT FINDER signal from IPB external cable.
(2) Refer to the diagram, Path of IPB Signals

THE 4240 INTER-PROCESSOR BUS SUBSYSTEM transfers data and status information between any two NOVA or ECLIPSE line computers. In data communications, the "Right" IPB board serves as the data holding area; the "Left" IPB board serves in a gating capacity. The top portion of the diagram shows the data buses and storage buffer/receiver combinations used to transfer data between processors. The lower portion of the diagram shows the missing pulse detectors and status flags which are used to provide status information.

PATH OF IPB SIGNALS



LEGEND
(1) If not disabled by $\overline{\text{LEFT FINDER}}$ signal
(2) Grounded on "LEFT" IPB board by External Cable

THE INITIATING PROCESSOR'S IPB board can be either the "LEFT" or "RIGHT" IPB board, the path of IPB signals is identical.

IPB Signals

Each processor's IPB devices are controlled by signals sent to the processor's IPB board via the I/O bus. These signals are generated by the execution of the appropriate I/O instructions in the initiating processor. Three types of signals are generated by the fields of an I/O instruction which affect the IPB devices and their respective status flags:

- The device code (36, 37, 40, 41)
- The instruction (DOA, DIA, DIB)
- The flag command (Start, Clear, I/O Pulse)

When these signals are asserted and received by the initiating processor's IPB board, they generate two types of signals: first, those which affect the circuitry of the initiating processor's IPB board; and, second, those which affect the circuitry of the other processor's IPB board. Refer to the diagram showing the paths of IPB signals.

The signals which affect the circuitry of the initiating processor's IPB board have no suffix added to them; e.g., **DS40.**

The signals which affect the circuitry of the other processor's IPB board have the suffix "O" added after the last letter in the signal name; e.g., **$\overline{\text{DSO40}}$.** These signals are sent to the other processor's IPB board via the IPB external cable. When these signals are asserted on the other processor's IPB board, the suffix changes from "O" (out) to "I" (in); thus, the **$\overline{\text{DSO40}}$** signal on the initiating processor's IPB board becomes the **$\overline{\text{DSI40}}$** signal on the other processor's IPB board.

On both IPB boards, the device code is ANDed with the instruction and/or flag command. For example, the **DS40** and **DIA** signals generate the **$\overline{\text{DIA40}}$** signal on the initiating processor's IPB board; the **$\overline{\text{DSI40}}$** and **DIAI** signals generate the **$\overline{\text{DIAI40}}$** signal on the other processor's IPB board.

In addition to signals which are generated directly by the execution of an I/O instruction, three signals are generated when the appropriate status flags are set. As shown in the diagram, these signals also contain the "O" and "I" suffix.

Status Information

Status information concerning IPB operations is provided by the state (0 or 1) of each IPB device's Busy and Done flags. This information can be determined by the processor during flag checking software routines or by means of the program interrupt facility.

Flag Checking

Flag checking allows the program to ascertain the status of the Busy and Done flags of the IPB devices under the control of the processor at any time. This is accomplished by the execution of the appropriate I/O Skip instructions, which test the state of two I/O bus lines, **$\overline{\text{SELB}}$** and **$\overline{\text{SELD}}$.** Whenever the CPU issues an IPB device code, the **$\overline{\text{SELB}}$** line will be asserted if that device's Busy flag is set to 1 and the **$\overline{\text{SELD}}$** line will be asserted if that device's Done flag is set to 1.

Program Interrupt

The program interrupt facility provides the means for notifying the processor when one of its peripheral devices requires service. An IPB device requests a program interrupt by asserting the **$\overline{\text{INTR}}$** line of the I/O bus. When more than one IPB device is requesting a program interrupt, the devices are serviced according to the following priority scheme:

PRIORITY	IPB DEVICE
1	HALF-DUPLEX TRANSMITTER/RECEIVER
2	FULL-DUPLEX RECEIVER
3	FULL-DUPLEX TRANSMITTER
4	TIMER (MISSING PULSE DETECTOR)

The program interrupt system is explained in detail in the User's Manual, Interface Designer's Reference, NOVA AND ECLIPSE LINE COMPUTERS, DGC No. 015-000031.

Timing

Each IPB operation is governed by the timing of the signals received from the CPU initiating the operation. Since timing varies between computer models, it is necessary to refer to the technical manual for the particular NOVA or ECLIPSE line computers in use to determine exact timing information.

Typical timing of signals received from the CPU and typical timing of resulting IPB signals are shown in the timing diagrams. In this manual, five relative IPB time periods are defined, IPB0 through IPB4. These time periods are used only for illustrative purposes and do not relate to any timing signals.

Time Periods

IPB0 is the time period starting when the device code only is asserted (e.g., **DS40**) and ending after an instruction signal, if any, is asserted (e.g., **DIA**).

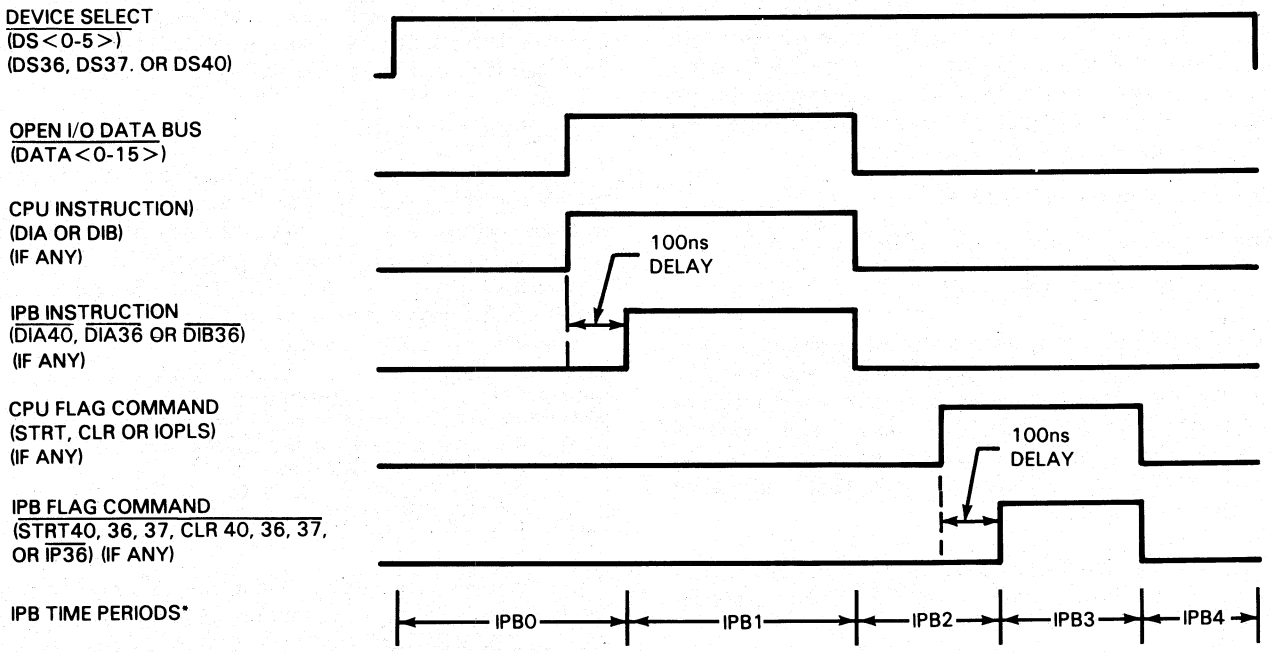
IPB1 is the time period starting when an IPB instruction signal, if any, is asserted (e.g., **$\overline{\text{DIA40}}$**) and ending when the IPB instruction ends.

IPB2 is the time period starting after the end of the IPB instruction signal, if any, and ending after a flag command signal, if any, is asserted (e.g., **CLR**).

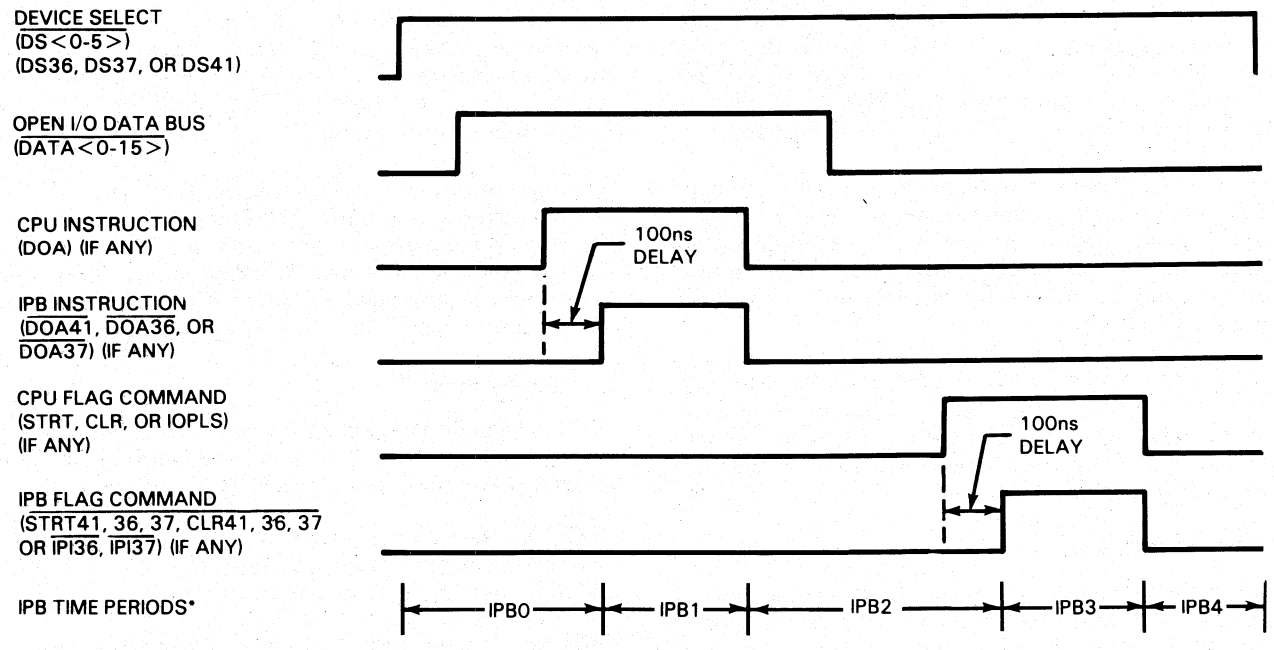
IPB3 is the time period starting when an IPB flag command signal, if any, is asserted (e.g., **$\overline{\text{CLR40}}$**) and ending when the IPB flag command signal ends.

IPB4 is the time period starting after the end of the IPB flag command signal, if any, and ending when the instruction ends.

TYPICAL PROGRAMMED IPB INPUT AND FLAG COMMAND TIMING



TYPICAL PROGRAMMED IPB OUTPUT AND FLAG COMMAND TIMING



*THESE TIME PERIODS ARE USED ONLY FOR ILLUSTRATIVE PURPOSES AND DO NOT RELATE TO ANY TIMING SIGNALS.

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FULL-DUPLEX COMMUNICATIONS

The full-duplex communications link provides the facilities for high-speed, bi-directional communications between processors. Each processor controls one full-duplex transmitter (storage buffer) and one full-duplex receiver (set of receiver gates), which allows data to be transferred from the left processor to the right processor and from the right processor to the left processor. Because of the high-speed data transfer rate capability of the IPB, this arrangement provides what appears to be a full-duplex channel to the programmer. Data is actually transferred over the half-duplex, bi-directional data bus ($\overline{\text{CPB[0-15]}}$) in the IPB external cable.

Data Transfer

Two operations are required to transfer data between processors: first, the transmitting processor sends data to the full-duplex storage buffer by executing a WRITE DATA instruction. Second, the receiving processor retrieves the data stored at the buffer's output by executing a READ DATA instruction.

Transmit

When a WRITE DATA instruction (DOA ac, DPO) is executed, the transmitting processor transfers data from the specified accumulator to the IPB board, via the I/O data bus. If the instruction was initiated by the "Right" processor, the data is loaded directly from the I/O data bus into the storage buffer. If the instruction was initiated by the "Left" processor, the data passes from the I/O data bus, through the general purpose (half-duplex) transmitter, over the **CPB** bus, and into the storage buffer.

Receive

When a READ DATA instruction (DIA ac, DPI) is executed, the receiver passes the contents of the storage buffer to the I/O data bus, and the receiving processor transfers the data into the specified accumulator. If the instruction was initiated by the "Right" processor, the receiver passes the data directly to the I/O data bus. If the instruction was initiated by the "Left" processor, the receiver passes the data to the **CPB** bus. The data passes over the **CPB** bus, through the general purpose (half-duplex) receiver, to the I/O data bus.

PROGRAMMING SUMMARY

FULL-DUPLEX

MNEMONIC (INPUT)	DPI
DEVICE CODE (INPUT)	40_8
PRIORITY MASK BIT (INPUT)	8
MNEMONIC (OUTPUT)	DPO
DEVICE CODE (OUTPUT)	41_8
PRIORITY MASK BIT (OUTPUT)	8

INSTRUCTIONS

READ DATA . . . . . DIA ac, DPI
WRITE DATA . . . . . DOA ac, DPO

FLAG COMMANDS S, C, AND P FUNCTIONS

Input

f = S In the computer executing the instruction, the DPI Busy flag is set to 1 and the DPI Done flag is set to 0. If the DPI Busy flag was 1 before this instruction was issued, then, in the other computer, the DPO Busy flag is set to 0 and the DPO Done flag is set to the prior value of the DPO Busy flag.

f = C In the computer executing the instruction, the DPI Busy and Done flags are both set to 0. In the other computer, the DPO Busy flag is set to 0 and the DPO Done flag is set to the prior value of the DPO Busy flag.

f = P This command has no effect.

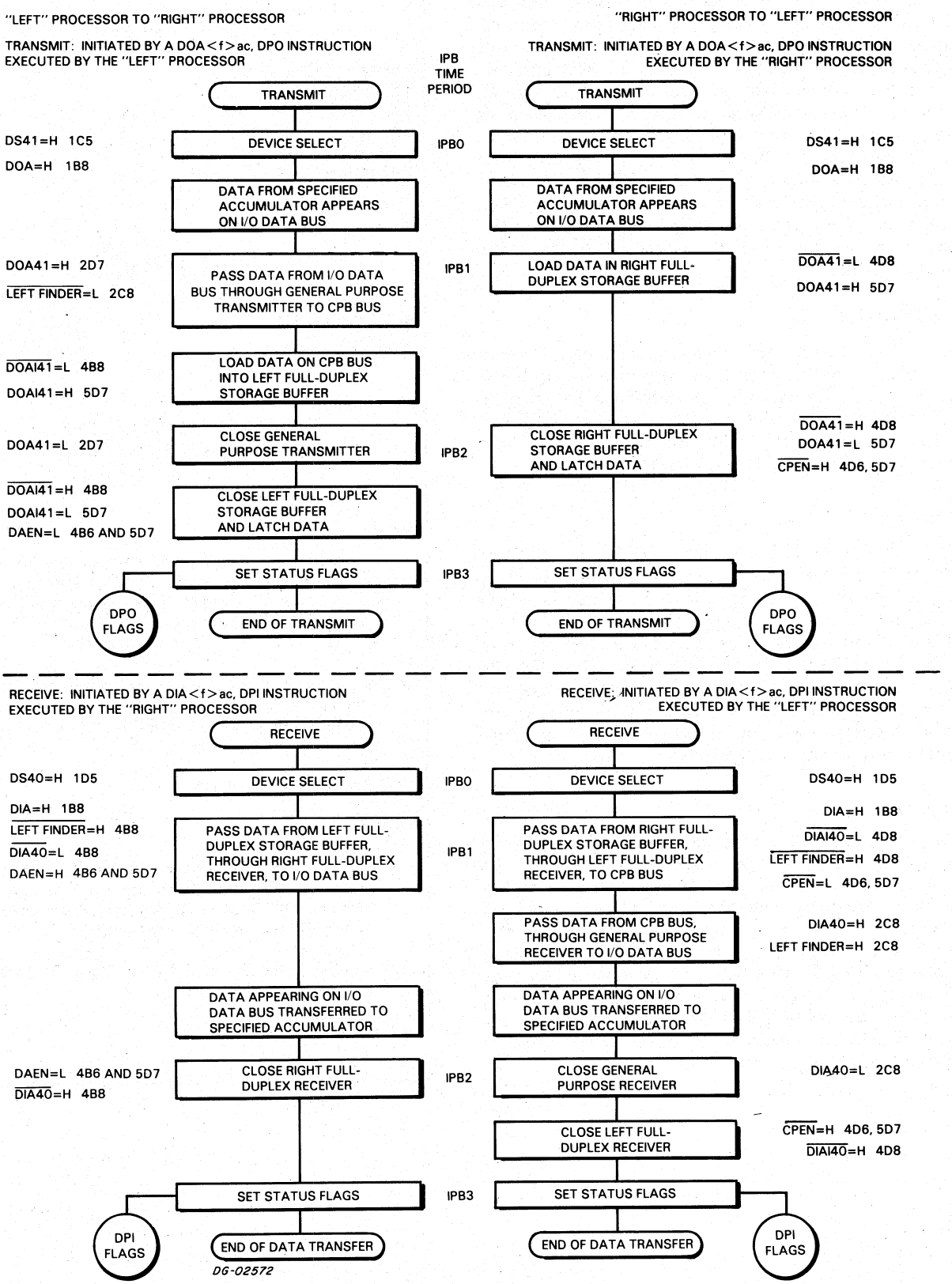
Output

f = S In the computer executing the instruction, the DPO Busy flag is set to 1 and the DPO Done flag is set to 0. In the other computer, if the DPI Busy flag is 1, the DPI Done flag is set to 1 and the DPI Busy flag remains unchanged.

f = C In the computer executing the instruction, the DPO Busy and Done flags are both set to 0.

f = P This command has no effect.

FULL-DUPLEX DATA TRANSFER



NOTE: <f> = OPTIONAL FLAG COMMAND

Status Information

Since all data transfers require the participation of both processors, each processor must be notified of the status of the data transfers. This is accomplished by manipulating the full-duplex transmitter Busy and Done flags in the transmitting processor and the full-duplex receiver Busy and Done flags in the receiving processor. The processors receive status information by means of the program interrupt facility and flag checking software routines.

The receiving processor is notified that the other processor has initiated a data transfer when the receiver Done flag is set to 1. The transmitting processor is notified that the other processor has received the data when the transmitter Done flag is set to 1.

The Busy and Done flags are set by IPB device flag commands, Start and Clear. An I/O pulse has no effect on the Busy and Done flags of the full-duplex devices.

The flags are set in the following manner:

Transmit

After data is loaded into a full-duplex storage buffer, the transmitting processor issues a Start pulse. This sets the transmitter Busy flag to 1, the transmitter Done flag to 0, and generates the **41BUSYI** signal on the other processor's IPB board.

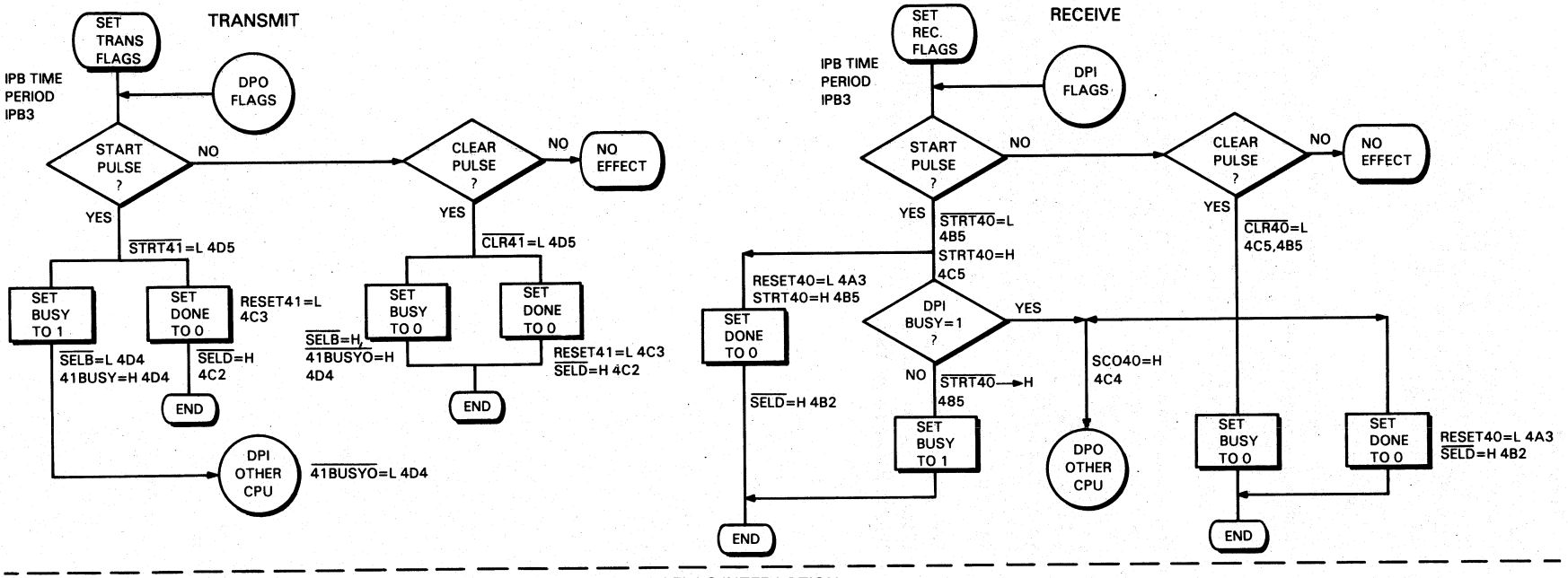
Receive

When the receiving processor is ready to receive data, it issues a Start pulse. This sets the receiver Busy flag to 1 and the receiver Done flag to 0. When the receiver Busy flag is set to 1 and the **41BUSYI** signal is asserted, the receiver Done flag is immediately set to 1.

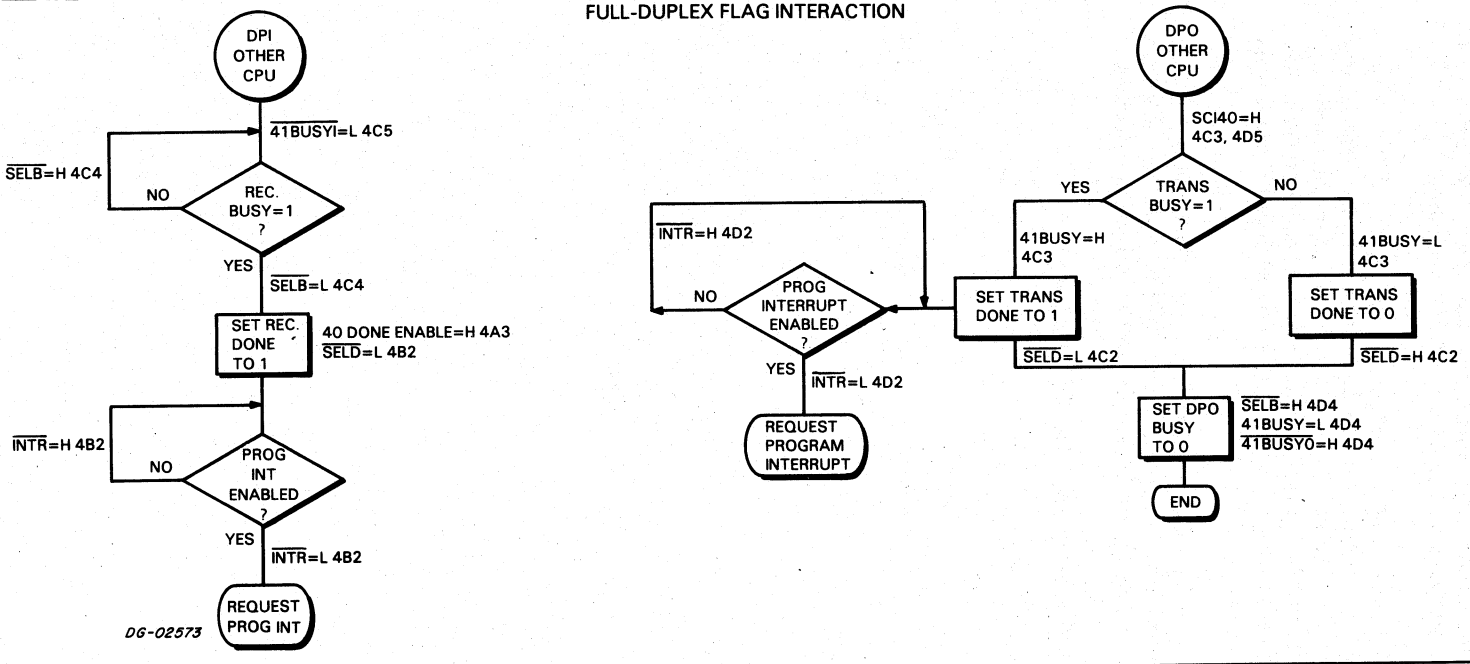
After the data in the storage buffer is retrieved, the receiving processor issues either a Start or Clear pulse. This generates the **SCI40** signal on the other processor's IPB board. If the receiving processor issues a Start pulse, the receiver Busy and Done flags are set as described above. If the receiving processor issues a Clear pulse, the receiver Busy and Done flags are both set to 0.

When the **SCI40** signal is asserted, the transmitter Done flag is set to the previous value of the transmitter Busy flag.

FULL-DUPLEX STATUS INFORMATION



FULL-DUPLEX FLAG INTERACTION



HALF-DUPLEX COMMUNICATIONS/INTERLOCKED

The half-duplex communications link provides the facilities for bi-directional, half-duplex communications between processors. Additionally, when the appropriate software is used, the circuitry which governs the setting of the Busy flags of both half-duplex devices allows the program to establish an "interlock".

Each processor controls one half-duplex transmitter/receiver device. While the transmitter/receiver is actually two separate devices, a transmitter (half-duplex storage buffer) and a receiver (half-duplex set of receiver gates), it responds to one device code and can assume only one role at a time. This arrangement allows information to be transferred either from the "Left" processor to the "Right" processor or from the "Right" processor to the "Left" processor.

Data Transfer

Two operations are required to transfer data between processors: first, the transmitting processor sends data to the half-duplex storage buffer by executing a WRITE DATA instruction. Second, the receiving processor retrieves the data stored at the buffer's output by executing a READ DATA instruction.

Transmit

When a WRITE DATA instruction (DOA ac, IPB) is executed, the transmitting processor transfers data from the specified accumulator to the IPB board, via the I/O data bus. If the instruction was initiated by the "Right" processor, the data is loaded directly from the I/O data bus into the storage buffer. If the instruction was initiated by the "Left" processor, the data passes from the I/O data bus, through the general purpose (half-duplex) transmitter, over the **CPB** bus, and into the storage buffer.

Receive

When a READ DATA instruction (DIA ac, IPB) is executed, the receiver passes the contents of the storage buffer to the I/O data bus, and the receiving processor transfers the data into the specified accumulator. If the instruction was initiated by the "Right" processor, the receiver passes the data directly to the I/O data bus. If the instruction was initiated by the "Left" processor, the receiver passes the data to the **CPB** bus. The data passes over the **CPB** bus, through the general purpose (half-duplex) receiver, to the I/O data bus.

PROGRAMMING SUMMARY

HALF-DUPLEX

MNEMONIC	IPB
DEVICE CODE	36_8
PRIORITY MASK BIT	6

INSTRUCTIONS

READ DATA	**DIA ac, IPB**
WRITE DATA	**DOA ac, IPB**
CLEAR FLAGS	**DIB ac, IPB**

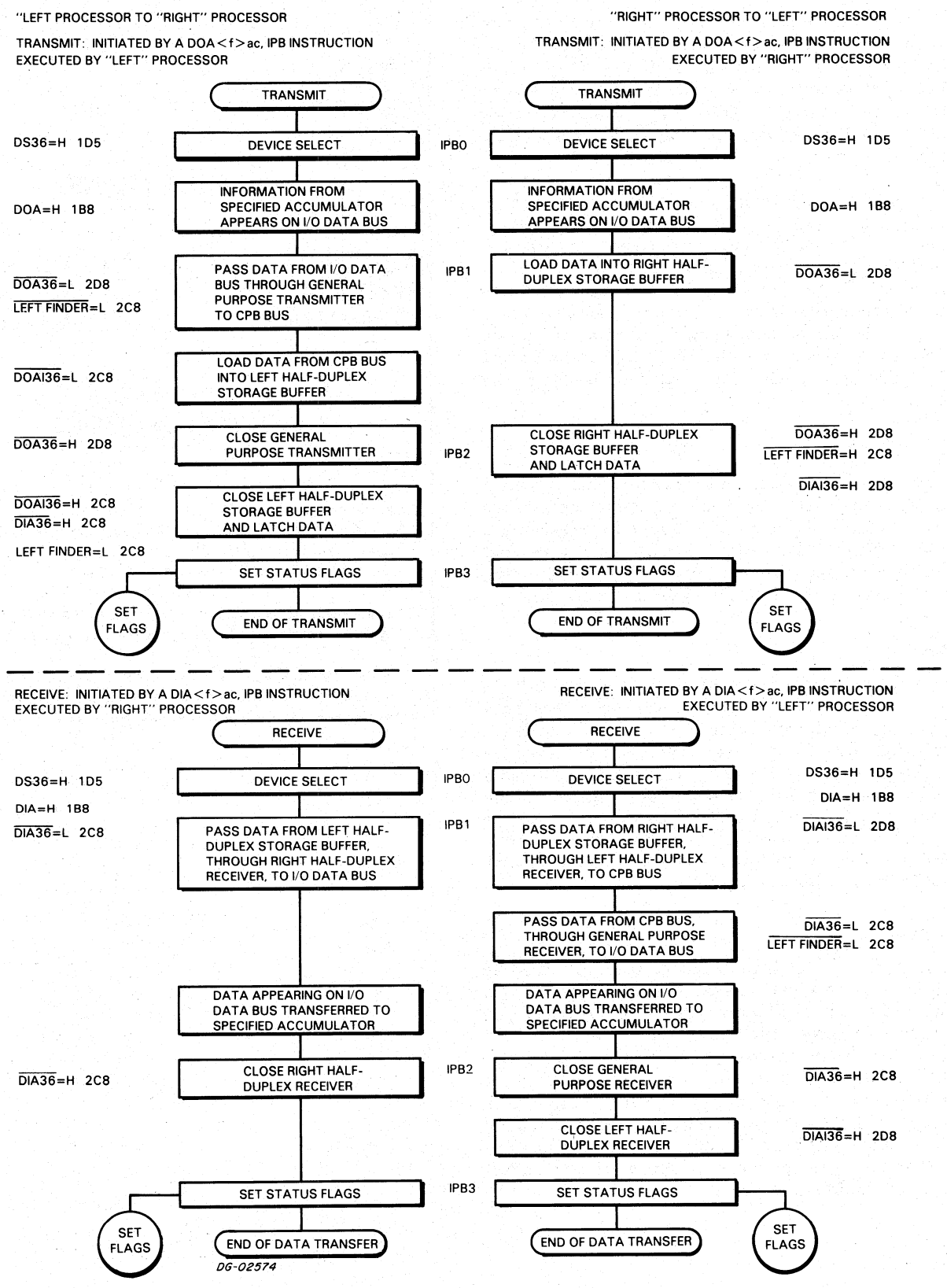
FLAG COMMANDS S, C, AND P FUNCTIONS

S In the computer executing the instruction, the IPB Busy flag is set to 1 if the IPB Busy flag of the other computer is 0. Even if both computers issue a Start at exactly the same time, only one IPB Busy flag will be set to 1.

C In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Busy flag is set to 0.

P In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Done flag is set to 1.

HALF-DUPLEX DATA TRANSFER



NOTE: <f> = OPTIONAL FLAG COMMAND

Status Information

Since all data transfers require the participation of both processors, each processor must be notified of the status of the data transfer. This is accomplished by manipulating the Busy and Done flags of the half-duplex devices of both processors. The processors receive status information by means of the program interrupt facility and flag checking software routines.

The receiving processor is notified that the other processor has initiated a data transfer when its half-duplex device Done flag is set to 1. The transmitting processor is notified that the other processor has received the data when its half-duplex device Done flag is set to 1.

The Busy and Done flags are set by IPB device flag commands, Start, Clear, and I/O Pulse. In addition, a CLEAR FLAGS instruction (DIB ac, IPB) functions as an IPB device flag command in half-duplex communications.

Interlock

The interlock allows only one processor to transmit data when the appropriate software is used, since it allows only one processor's half-duplex Busy flag to be set to 1 at any one time. This is accomplished by double-flag circuitry on the "Right" IPB board which governs the setting of the half-duplex device Busy flag of both processors. This circuitry is disabled on the "Left" IPB board by the $\overline{\text{LEFT FINDER}}$ signal.

The double-flag circuitry contains two gates; only one of these gates can be enabled at any one time. When one gate is enabled, it sets the "Left" processor's Busy flag to 1; when the other gate is enabled, it sets the "Right" processor's Busy flag to 1. A gate is enabled when the following conditions are satisfied.

- A Start pulse is issued by the appropriate processor.
- The other processor's Busy flag is set to 0.
- The gate is enabled by the output of the "W" and "X" flip-flops. These flip-flops are clocked by a 20MHz oscillator and their outputs form a 4-phase, 5MHz oscillator. The outputs of the flip-flops alternately enable the two Busy flag gates.

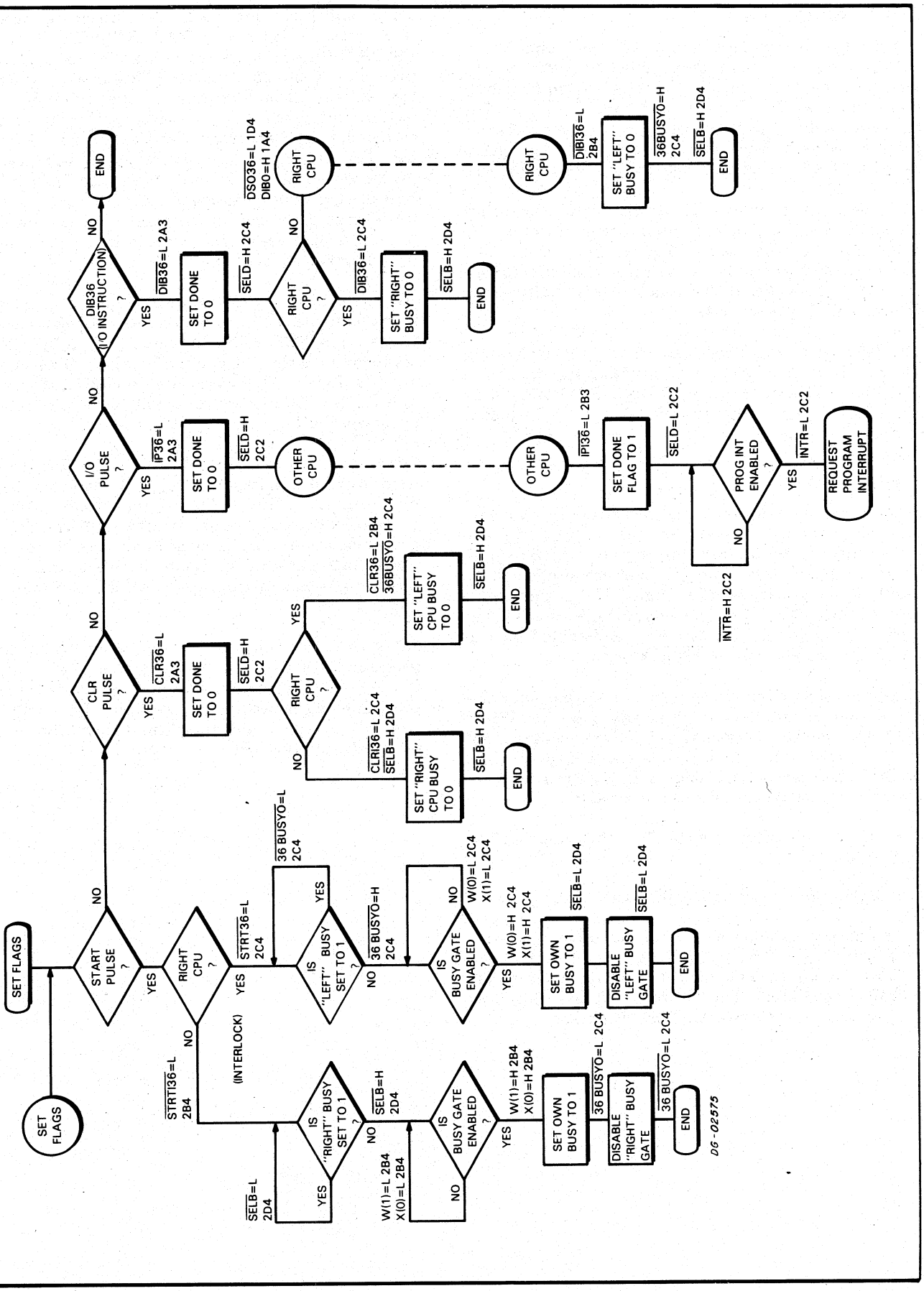
To establish an interlock, the initiating processor must first execute a REQUEST BUS instruction (NIOS IPB), which generates a Start pulse. Next, the processor must execute an I/O Skip instruction to test the state of the $\overline{\text{SELB}}$ line of the I/O bus. If the half-duplex Busy flag is set to 1, the interlock is established and the data transfer can be initiated. If the Busy flag is set to 0, it indicates that the other processor has established an interlock in the half-duplex communications link. In this case, the initiating processor must wait until the other processor releases the interlock by setting its half-duplex Busy flag to 0.

After the initiating processor establishes an interlock, it transfers data to the half-duplex storage buffer by executing a WRITE DATA instruction. After the data is loaded into the storage buffer, the processor issues an I/O Pulse. This sets the initiating processor's half-duplex Done flag to 0 and sets the receiving processor' half-duplex Done flag to 1.

When the receiving processor is notified that its half-duplex Done flag is set to 1, it retrieves the data by executing a READ DATA instruction. After the data in the storage buffer is retrieved, the receiving processor issues an I/O Pulse. This sets the receiving processor's half-duplex Done flag to 0 and sets the initiating (transmitting) processor's half-duplex Done flag to 1.

After all data transfers are completed, the initiating processor releases the interlock by executing a CLEAR FLAGS instruction (DIB ac, IPB). This sets the initiating processor's half-duplex Busy and Done flags to 0; thus, allowing the other processor to establish an interlock.

HALF-DUPLEX STATUS INFORMATION/INTERLOCK



WATCHDOG TIMER

The Watchdog Timer provides the facilities for generating a program interrupt in either computer when the other computer: 1) fails to execute a specific instruction; or, 2) generates a signal indicating a probable "power fail" condition. This capability is implemented by two missing pulse detectors, one located on each IPB board, and each detector's Timer Done flag.

Each detector consists of a one-second timer which is normally restarted by the execution of a START TIMER instruction (NIOS IVT) in the other computer at regular intervals of one second, or less. When one computer fails to restart the timer in the other computer within the specified time period, that detector's Timer Done flag is set to 1, generating a program interrupt request in the computer in which the detector is installed.

When either computer knows that it is about to cease functioning (e.g., a power fail situation), that computer may set the Timer Done flag in the other computer directly by executing a SET TIMER instruction (NIOP IVT).

When the processor is notified that the Timer Done flag is set to 1, it should take appropriate action and then execute a CLEAR TIMER instruction (NIOC IVT), setting the Timer Done flag to 0. If this instruction or an I/O Reset is not executed, the processor will continue to be notified of the failure.

PROGRAMMING SUMMARY

MNEMONIC	IVT
DEVICE CODE	37_8
PRIORITY MASK BIT	6
TIMER PERIOD (SEC)	1

INSTRUCTION

START OWN TIMER . . . . . DOA ac, IVT

FLAG COMMANDS S, C, AND P FUNCTIONS

S The timer in the other computer is started.

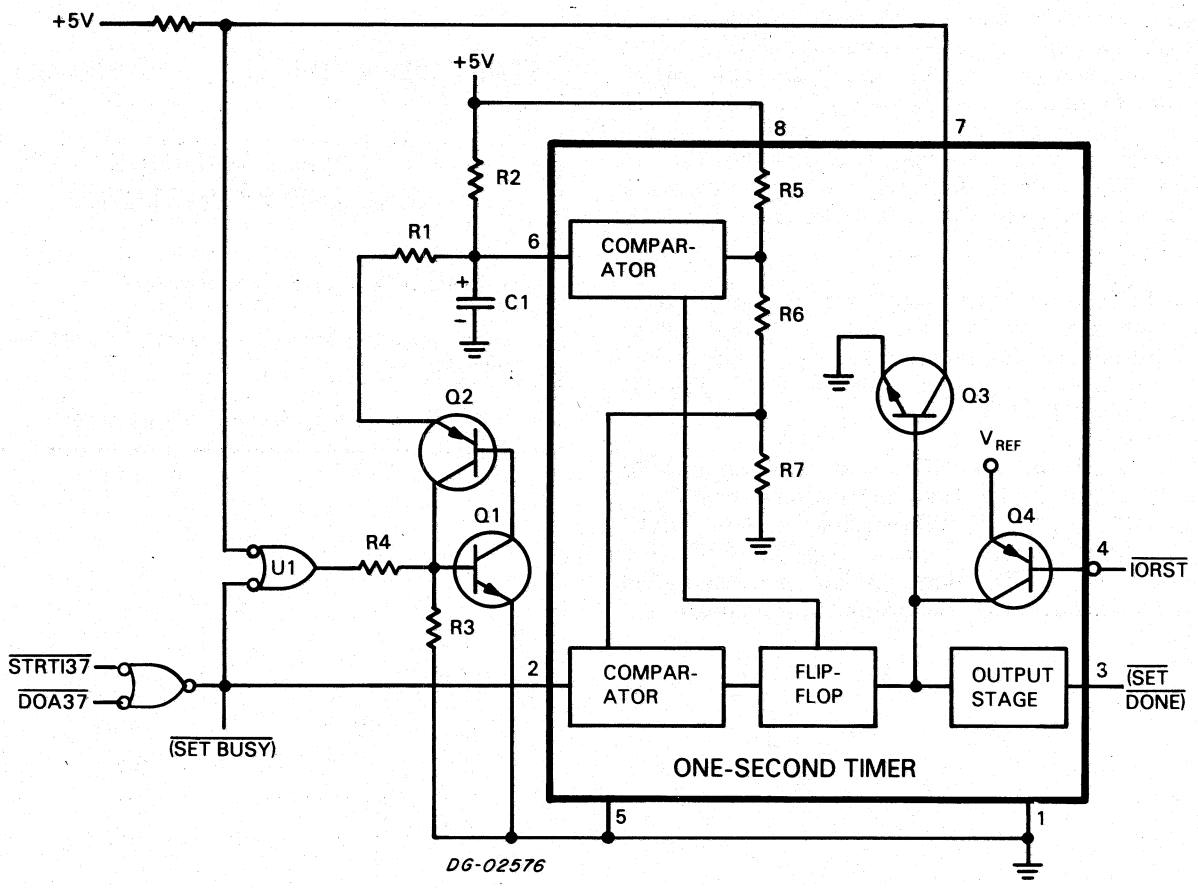
C In the computer executing the instruction, the IVT Done flag is set to 0.

P In the other computer, the IVT Done flag is set to 1.

The Timer

The one-second timer functions as a missing pulse detector. After the timer is initially started, it must be restarted at intervals of one second, or less, in order to keep its output (normally high) from changing. If the timer is allowed to run, its output changes when a comparator in the timer chip senses a predefined voltage which is stored in an external capacitor. When this occurs, the Timer Done flag is set to 1.

TIMER CIRCUIT



TIMER CIRCUIT - Either the **STRTI37** signal, generated by the execution of a START TIMER instruction in the other processor, or a **DOA37** signal, generated by the execution of a START OWN TIMER instruction (DOA ac, IVT) in the timer's processor, starts the timer and sets its Busy flag to 1. (The Timer Busy flag does not assert the **SELB** line of the I/O bus and cannot be tested by flag checking.) Either of these signals enables the timer's external gate U1, passing current to the transistor Q1. The transistor Q1 turns on transistor Q2, allowing the external capacitor C1 to discharge through the resistor R1 to ground. This keeps the output of the timer high and the Timer Done flag set to 0. (The Done flag is set to 0 after a Clear pulse or an I/O reset is issued by the timer's processor.)

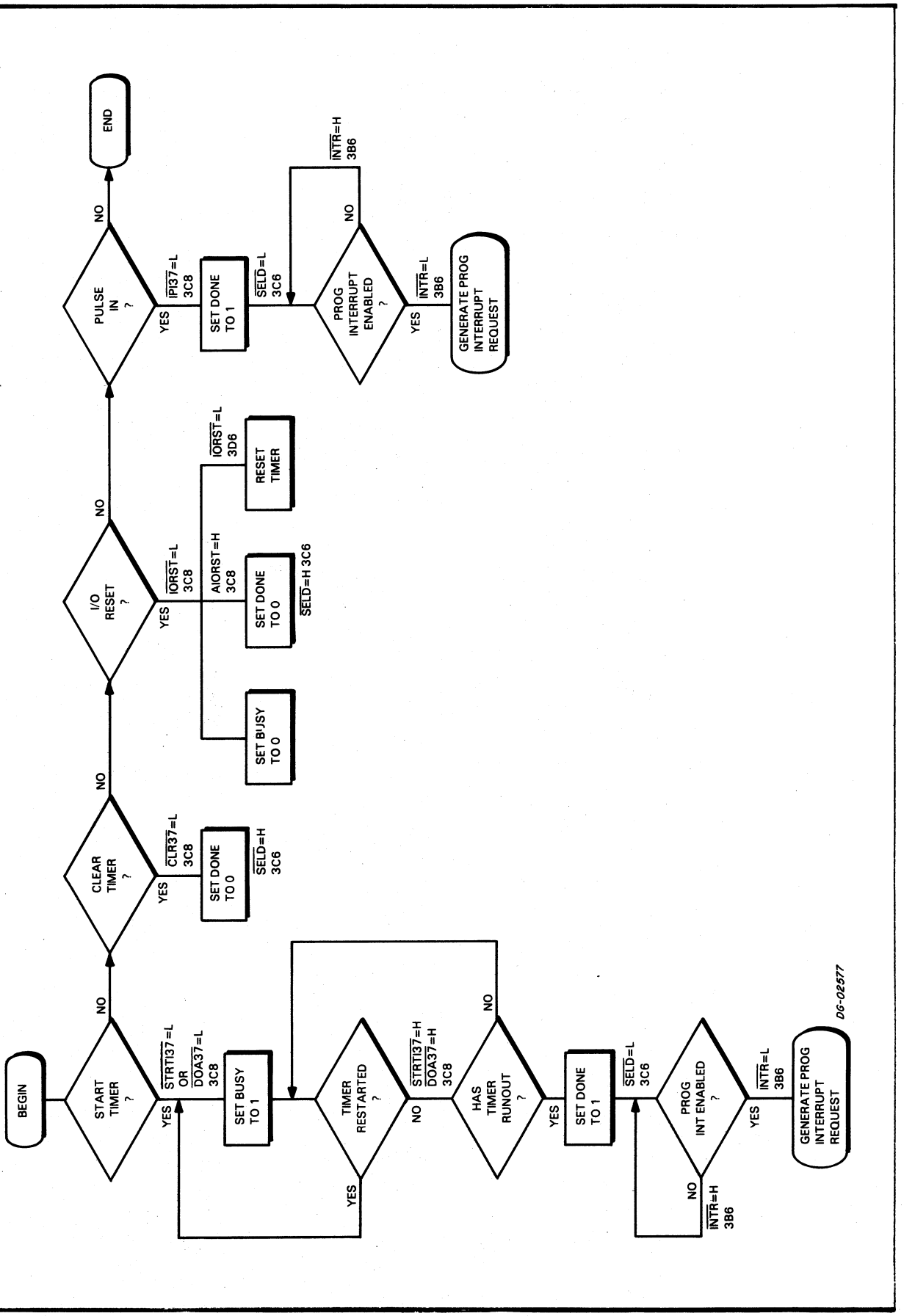
When the instruction ends, the transistors are turned off and the capacitor C1 charges through resistor R2.

If the timer is not restarted in approximately one second, the timing cycle is allowed to run and the external capacitor continues to charge. When the capacitor C1 reaches a predefined limit, the comparator senses the voltage across the capacitor, causing a flip-flop in the timer chip to toggle, and the output of the timer goes low. When this occurs, the value of the Busy flag (Busy is set to 1 after either a **STRTI37** or **DOA37** signal is asserted) is clocked into the Timer Done flip-flop, setting the Done flag to 1.

In order for the Timer Done flag to reflect the functional status of the other processor, the timer must be restarted by the **STRTI37** signal.

The **IORST** signal directly sets the Timer Done flag to 0, sets the Busy flag to 0, and resets the timer. When the timer is reset, the timer output goes high. Additionally, the **IORST** signal enables transistor Q3 in the timer chip, causing the +5 line to go low. When this occurs, the external gate U1 is enabled, allowing the capacitor C1 to discharge to ground.

WATCHDOG TIMER



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APPENDIX A
SPECIFICATIONS

4240 Inter-Processor Bus Printed Circuit Board

Size: 15" x 15"

Power Requirements: approximately 2.5 amps, 5Vdc

Space Requirements: one I/O slot in a NOVA or ECLIPSE line computer

Items Supplied on Purchase: one 15" x 15" IPB printed circuit board, one internal cable, one test plug, and one documentation package. (When ordering, specify the two computer models.)

1065 External Cable for the 4240 Inter-Processor Bus

Length: 15'

Contains 78 lines: 39 signal levels and 39 grounds

When ordering, specify the two computer models.

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