Technical Reference

4240 INTER-PROCESSOR BUS

014-000056-00

The Inter-Processor Bus (IPB) is a special purpose controller which interfaces two DGC computers, allowing the transfer of information under direct program control without an intermediate storage device. The IPB features half- and full-duplex transmission and a watchdog timer, which notifies each computer of the failure of the other.

Ordering No. 014-000056

Printed in the United States of America
Rev. 00, July 1974

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OVERVIEW

INTRODUCTION

The Data General Corporation 4240 Inter-Processor Bus (IPB) is a special purpose controller that allows any two DGC computers to transfer information back and forth without using an intermediate storage device. The IPB provides three basic functions:

a) It transmits data over a half-duplex (Interlocked) transmission line, under direct program control. This feature allows the program to establish an "interlock", i.e., only one computer is permitted to transmit over the line at any one time.

b) It transmits data over a full-duplex (Non-Interlocked) transmission line, under direct program control. This feature allows dual processor communication to be programmed in a similar manner to full-duplex communication with a Teletype®*.

c) It implements a watchdog timer which notifies each computer in the event of a failure in the other computer.

The IPB is useful in applications where direct program control of transferred information is needed and in applications where information must be transferred quickly between computers, but neither the amount of information to be transferred nor the speed with which it is to be transferred requires the use of the DGC Multiprocessor Communications Adapter (type 4038). Using routines solely dedicated to transmitting and receiving information, two DGC computers can achieve transfer rates exceeding 100,000 16-bit words per second, using the IPB. During normal program operation the information transfer rate is limited by the length of the interrupt handling routine in each computer.

Typical applications of the IPB include, shared disc environments, parallel processing arrangements, communications concentration systems, and back-up systems. In a shared disc environment, two computers share a common system's disc pack. The "interlock" on the half-duplex line of the IPB gives the two computers a foolproof system of communicating disc space reservations and actions performed on disc files.

In a parallel processing arrangement, the IPB allows the two computers to exchange data rapidly, providing a check on the results of computation. In a communications concentration system, one computer is dedicated to the handling of a large number of I/O communications to and from the system, freeing the other computer to perform calculations. The IPB allows a rapid exchange of information, under program control, in such a system. In a back-up system, computer failure is guarded against by having a back-up computer ready to assume the duties of the failing computer. The watchdog timer facility of the IPB can be used to notify the back-up computer of the failure of the other computer.

The applications mentioned above are implemented in the software of the two computers, using the hardware available in the IPB. This reference gives a brief description of the functioning of the IPB hardware and presents possible schemes of programming the computers, to implement the functions of the IPB. The design of the IPB hardware is flexible enough to allow programming schemes other than those described in this reference to alter the IPB functions.

ARCHITECTURE

The IPB communications link between two DGC computers consists of two 15-inch square IPB printed circuit boards, one in each computer, connected by a fifteen foot cable (see Figure O-1). Each IPB board contains four separate devices: a 16-bit full-duplex (Non-Interlocked) transmitter, a 16-bit full-duplex receiver, a 16-bit half-duplex (Interlocked) transmitter/receiver, and a watchdog timer.

Figure O-2 illustrates the operation of the IPB in terms of data and signal flow. Two features basic to the understanding of the IPB will be discussed in the following paragraphs. These features are the independent transfer of data and status information and the distinction between the "Left" and "Right" IPB board.

*Teletype® is a registered trademark of Teletype Corporation, Skokie, Illinois. All references to teletypes in this manual shall apply to this mark.

Two types of information are (independently) transferred through the IPB, data words and status information. Data words are transferred to and from accumulators in the two CPU's by the appropriate instructions. The data paths in the IPB are shown in the upper part of Figure O-2. Data enters from the Data (0-15) lines of the I/O bus of one computer, passes through a transmitter into the CPB (0-15) lines between the two IPB boards, and finally passes through a receiver onto the Data (0-15) lines of the I/O bus of the other computer. Associated with each transmitter and receiver is its own 16-bit storage buffer.

Status information tells whether a computer has transmitted a data word, received a data word, experienced a failure, etc. Each device in the IPB has it's own flags. (Busy and Done) which can interact with the programs of the two computers to transfer status information. Flag states are affected by commands from both computers and by the status of flags in both IPB boards. A computer receives status information by means of the program interrupt or by reading the flags. Figure O-2 illustrates the hardware separation of data and status information; all signals used in data transfer are in the upper part of the figure, all signals used in status transfer are in the lower part. The hardware independence of these two types of information transfer give a degree of flexibility to the programming of the IPB.

The IPB boards in each computer are identical, but they do not have identical roles in the transmission of information. The wiring in the IPB external cable assigns the IPB board in one computer (at the end of the cable labeled "Right") to serve as a data storage area and the other board (at the "Left" end of the cable) to serve only in a gating capacity in the transmission of data on both the full- and half-duplex lines. This means that in any data transfer, the transmitting computer writes data into one of the four buffers in the "Right" IPB board and the receiving computer reads the data from that buffer. The four data storage buffers in the "Right" IPB board latch data for the different types of data transmission in the IPB as follows:

- The buffers labeled full-duplex latch data transmitted on the full-duplex line.
- The buffers labeled half-duplex latch data transmitted on the half-duplex line.
- The receiver buffers latch data transmitted by the "Left" computer to the "Right" computer.
- The transmitter buffers latch data transmitted by the "Right" computer to the "Left" computer.

Since the "Left" IPB board is meant to serve only in a gating capacity in data transfers, only one receiver and one transmitter are necessary. The full-duplex transmitter and receiver that would be used if the board was on the "Right" side of the cable are disabled.

Another distinction between the "Left" and "Right" IPB boards is in the half-duplex Busy flags. The "Right" IPB board has a half-duplex Busy flag system containing the half-duplex Busy flags for both "Left" and "Right" computers. The corresponding logic on the "Left" IPB is disabled.

This distinction between "Right" and "Left" IPB boards are design distinction allowing the two IPB boards to be identical and does not effect the programming, operation, or communications capabilities of either computer in the system.

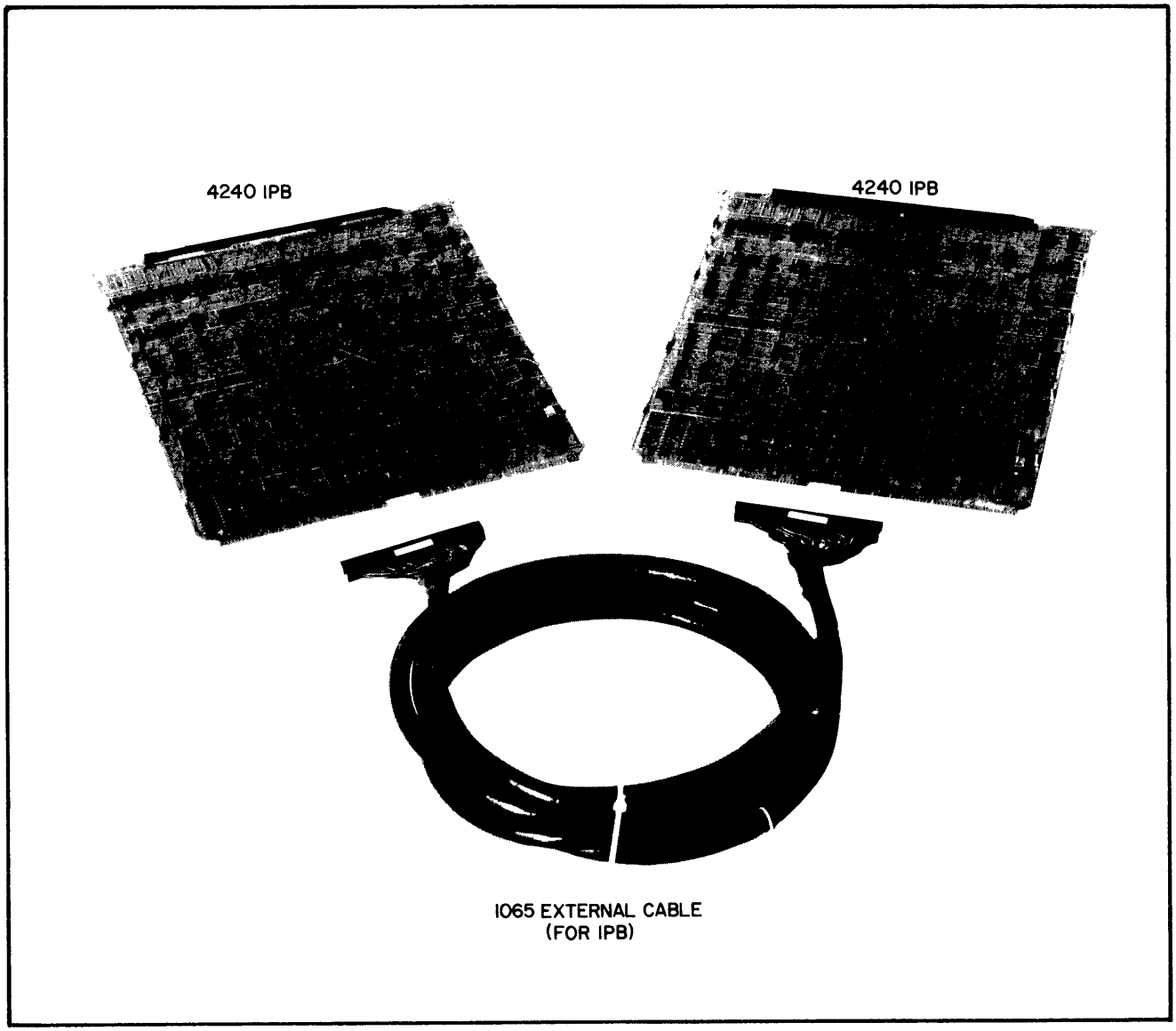
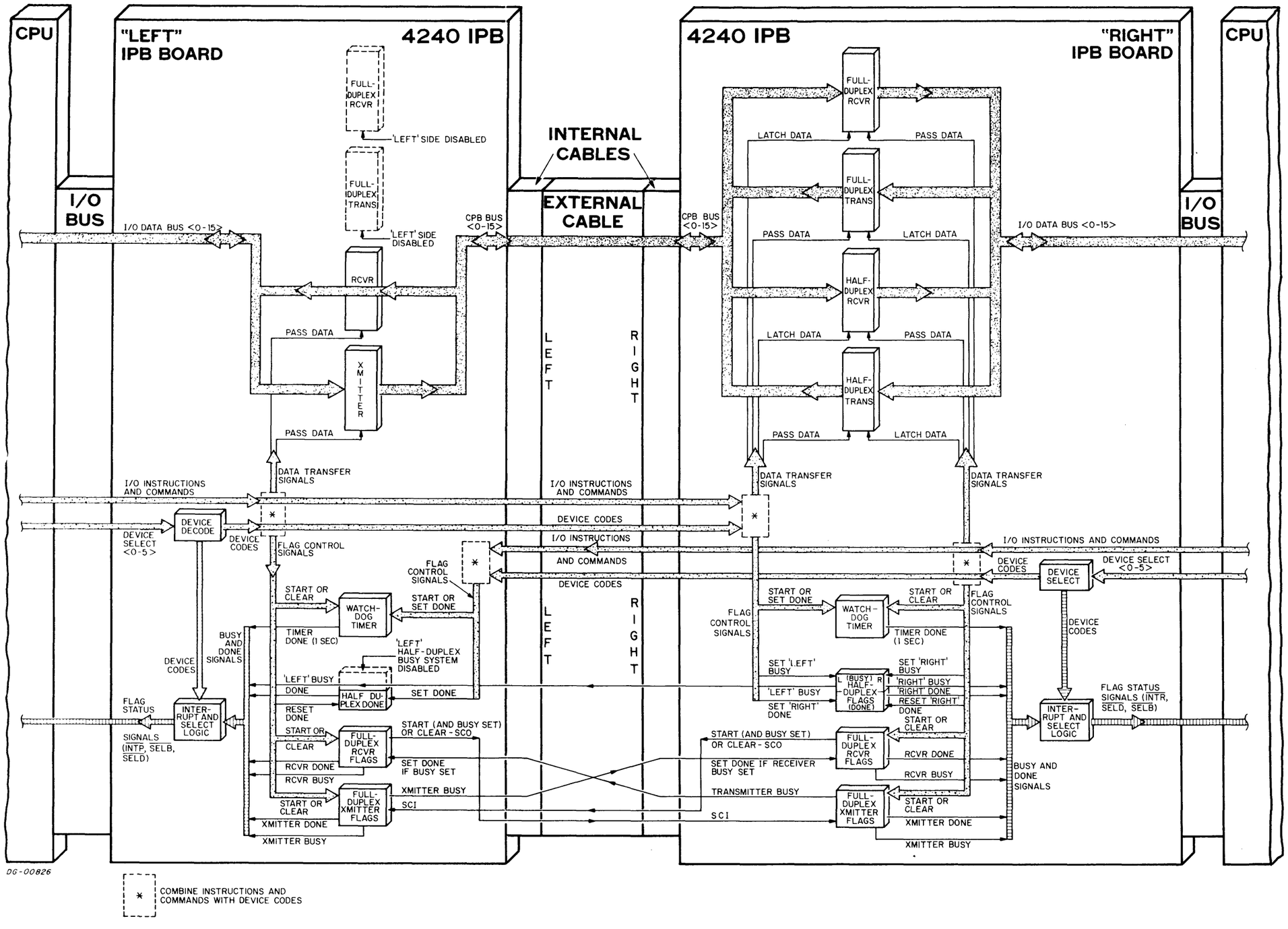


Figure O-1 Inter-Processor Bus Printed Circuit Boards and External Cable



The IPB transfers data using signals derived from the I/O instructions (top). Status information is transferred through each device by its flags (bottom) which respond to signals originating in both computers and the flags in both IPB boards. The external cable determines which board is the "Left" board and which is the "Right" board. The "Right" board stores data passing between the two computers and contains the half-duplex Busy flags for both IPB boards.

Figure O-2 Block Diagram of an IPB Communications Link

SPECIFICATIONS

4240 Inter-Processor Bus

Size: 15" x 15"

Power Requirements: approx. 2.5amps, 5Vdc

Space Requirements: 1 slot in each computer

Items Supplied on Purchase: 1 15" x 15" IPB Printed Circuit Board, 1 Internal Cable, 1 Test Plug, 1 Documentation Package

1065 External Cable for the 4240 Inter-Processor Bus (this item must be purchased separately, specify the two computer models)

Length: 15 feet

Contains 78 lines, 39 signal levels and 39 grounds

ORDERING INFORMATION

When purchasing the 4240 Inter-Processor Bus, the DGC computer model using the Inter-Processor Bus must be specified in order for the correct internal cable and test plug to be supplied. When purchasing an external cable for the 4240 IPB, the models of the two DGC computers to be linked must be specified. If an item normally supplied with the 4240 IPB needs to be purchased separately, i.e., an internal cable or test plug, the order should specify the computer it is to be used with and the fact that the item is to be used with the 4240 Inter-Processor Bus.

Item	DGC PART NUMBERS DGC Computers	DGC Part Number
4240 Inter-Processor Bus	All	005-001961
Internal Cable	NOVA 820, 1210, 1220	005-000901
	NOVA 2	005-001802
	NOVA 800, 840, 1200, 1230	005-001965
Test Plug	NOVA 800, 840, 1200, 1230	005-001963
	NOVA 820, 1210, 1220 and NOVA 2	005-001964
Documentation Package for 4240 IPB	All (specify computer to receive correct wire lists)	005-001969
External Cable	Group A to Group A*	005-001966
	Group A to Group B**	005-001967
	Group B to Group B**	005-001968

* Group A computers are NOVA 800, 840, 1200 and 1230.
**Group B computers are NOVA 820, 1210, 1220 and NOVA 2.

SECTION P
PROGRAMMING

The Data General Corporation 4240 Inter-Processor Bus (IPB) allows any two Data General computers to transfer information back and forth without using an intermediate storage device. Information transfer is accomplished via programmed I/O over either a full - or half-duplex line. In addition, the IPB provides a "watchdog timer" that will interrupt one processor if the other processor stops functioning.

The IPB is useful in applications where information must be transferred quickly between processors, but neither the amount of information to be transferred nor the speed with which it is to be transferred requires the use of the Multiprocessor Communications Adapter. The IPB is also useful in applications such as a shared disc environment where agreements must be made as to which processor has control over which files at any one point in time. The watchdog timer facility of the IPB allows this device to be used in applications where one processor must know about the failure of the other processor.

The IPB is made up of four separate devices for each computer: a 16-bit transmitter, a 16-bit receiver, a 16-bit transmitter/receiver, and a watchdog timer. The 16-bit transmitter and receiver operate together to provide a full-duplex communication link between the processors. This is functionally equivalent to a Teletype®, but is much faster. The only limit to transmission speed is the speed of the I/O interrupt handler. The 16-bit transmitter/receiver provides a half-duplex communication link between the processors. This link also provides a mechanism whereby the two processors can ensure that each one knows who is "master" of the system at any time. The watchdog timer is a one-second timer that allows either processor to be informed of a hardware or software failure in the other processor.

FULL-DUPLEX COMMUNICATION

Full-duplex communication between processors is accomplished with 4 devices: 2 transmitters and 2 receivers. Each processor in the system has a transmitter/receiver pair. Associated with each receiver is a receiver buffer. These devices are asynchronous and correspond functionally to the transmitter and receiver associated with a Teletype®. Each computer looks like a high-speed Teletype® to the other computer.

If there were not some way to prevent it, then it would be possible for one computer to transmit words faster than the other computer could receive them. So that this problem will not occur, the interaction between the transmitter of one computer and the receiver of the other computer is similar to the interaction between a computer and a Teletype® controller. When one computer transmits a word, the word is placed in the holding buffer of the other computer's receiver. The transmitting computer is not signaled that the transmission is complete until the other computer has read the word from its holding buffer into an accumulator.

Another possible problem that could occur is that a word could be lost due to the fact that the receiving computer has no way to know whether or not the other computer has already transmitted a word. Again, the interaction of the DPI Busy and Done flags of one computer with the DPO Busy and Done flags of the other computer ensures that no data will be lost due to this uncertainty. The following paragraphs describe a typical information transfer between two computers. The computer transmitting information is "computer B" and the computer receiving information is "computer A".

Before the transfer begins, computer A has no way of knowing whether or not his receiver (DPI) buffer contains meaningful information. Therefore, computer A issues an INITIATE RECEIVER instruction (NIOS DPI). The DPI Busy and Done flags of computer A will be set to 1 and 0, respectively. If computer B has not already transmitted a word, these flags will remain in this state until computer B transmits a word. When computer B finally does transmit a word, the DPI Done flag of computer A will be set to 1, signaling computer A that there is a meaningful word in its DPI buffer waiting to be read. If computer B has already transmitted a word, the DPI Done flag of computer A will be set to 1 immediately after computer A issues the INITIATE RECEIVER instruction and computer A will know that there is a meaningful word in its DPI buffer waiting to be read. Note that in the above sequence, computer A's DPI Busy flag has not been set to 0; it is still 1.

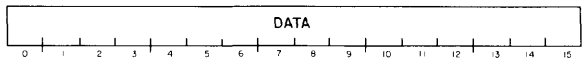
SUMMARY

FULL-DUPLEX

MNEMONIC (INPUT)	DPI
DEVICE CODE (INPUT)	40_8
PRIORITY MASK BIT (INPUT)	8
MNEMONIC (OUTPUT)	DPO
DEVICE CODE (OUTPUT)	41_8
PRIORITY MASK BIT (OUTPUT)	8

ACCUMULATOR FORMATS

READ DATA ..... (DIA)
WRITE DATA..... (DOA)



S, C, AND P FUNCTIONS

Input

S	In the computer executing the instruction, the DPI Busy flag is set to 1 and the DPI Done flag is set to 0. If the DPI Busy flag was 1 before this instruction was issued, then, in the other computer, the DPO Busy flag is set to 0 and the DPO Done flag is set to the prior value of the DPO Busy flag.
C	In the computer executing the instruction, the DPI Busy and Done flags are both set to 0. In the other computer, the DPO Busy flag is set to 0 and the DPO Done flag is set to the prior value of the DPO Busy flag.
P	This command has no effect.

Output

S	In the computer executing the instruction, the DPO Busy flag is set to 1 and the DPO Done flag is set to 0. In the other computer, if the DPI Busy flag is 1, the DPI Done flag is set to 1 and the DPI Busy flag remains unchanged.
C	In the computer executing the instruction, the DPO Busy and Done flags are both set to 0.
P	This command has no effect.

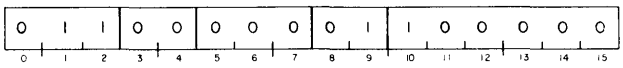
Upon learning that there is a word in its DPI buffer, computer A issues a READ DATA instruction with a Clear (DIAC ac, DPI). The word will be read into computer A's specified AC, and the DPI Busy and Done flags will both be set to 0. The DPO Busy and Done flags of computer B will be set to 0 and 1, respectively, and computer B will know that computer A received the word.

Computer B then issues a WRITE DATA instruction with a Start (DOAS ac, DPO). This instruction transfers the word to computer A's DPI buffer and sets computer B's DPO Busy and Done flags 1 and 0, respectively. When computer A is ready to receive another word, it issues another INITIATE RECEIVER instruction, and the cycle repeats. In this way, data will not be lost due to computer B transferring data so fast that computer A can not handle it or to uncertainty.

Instructions

INITIATE RECEIVER

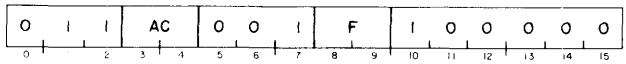
NIOS DPI



In the computer executing the instruction, the DPI Busy and Done flags are set to 1 and 0, respectively. If the DPO Busy flag of the other computer is 1, the DPI Done flag of the computer executing the instruction is set to 1 immediately. If the DPO Busy flag of the other computer is 0, the DPI Busy and Done flags of the computer executing the instruction will remain set to 1 and 0 until the DPO Busy flag of the other computer is set to 1.

READ DATA

DIA<f> ac, DPI

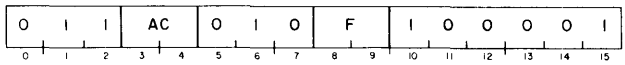


The data contained in the DPI buffer of the computer executing the instruction is placed in bits 0-15 of its specified AC. The previous contents of the specified AC are lost. The contents of the DPI buffer remain unchanged. After the data transfer, the Busy and Done flags are set according to the function specified by f.

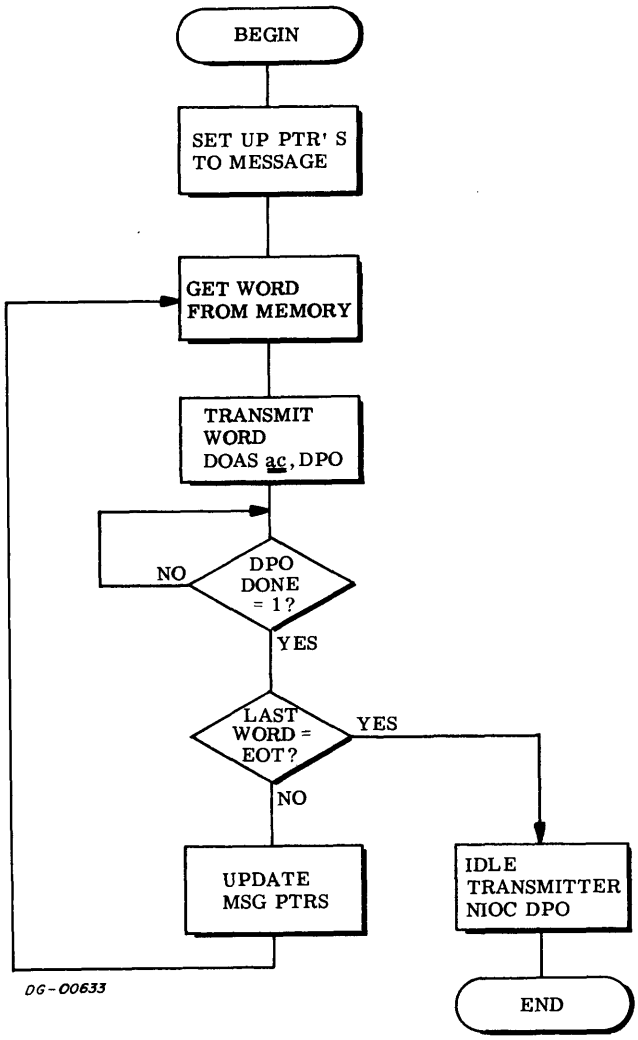
NOTE A series of DIAS instructions may be used to read a multiple word message.

WRITE DATA

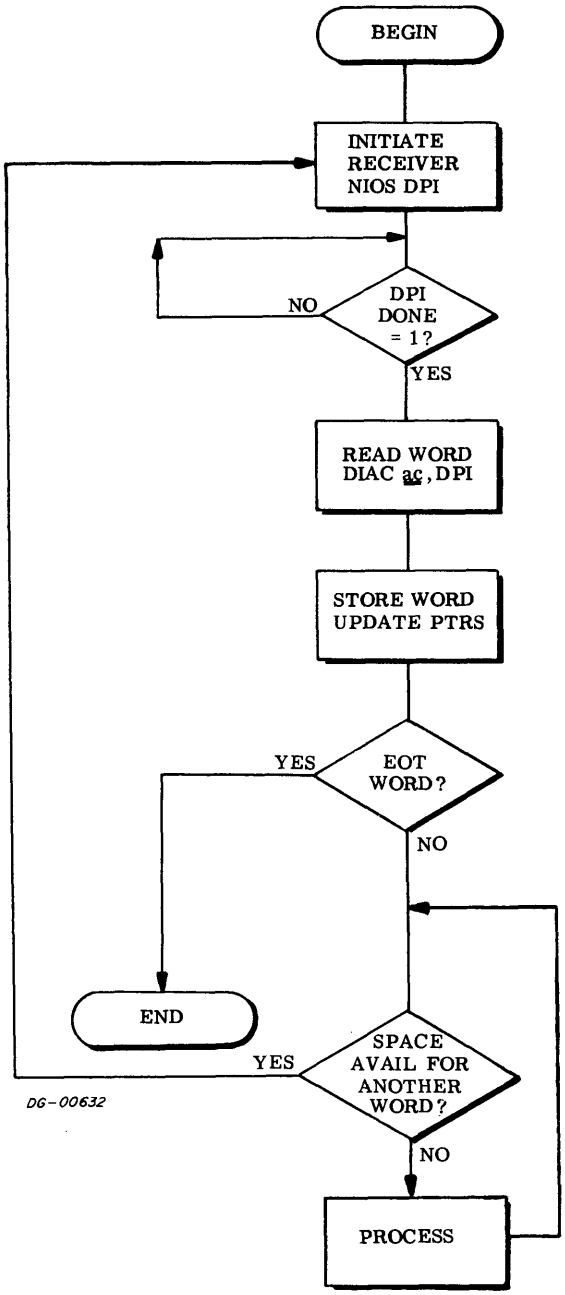
DOA<f> ac, DPO



The data contained in bits 0-15 of this specified AC is placed in the DPI buffer of the other computer in the system. The previous contents of that DPI buffer are lost. The contents of the specified AC remain unchanged. After the data transfer, the Busy and Done flags are set according to the function specified by f.



Transmission Flowchart



Reception Flowchart

HALF-DUPLEX COMMUNICATION

Half-duplex communication between processors is accomplished with two devices: one transmitter/receiver in each computer. There is one buffer which serves as the buffer for both transmitter/receivers. The devices are asynchronous and operate under program control. In addition to the communication capability, the Busy and Done flags of these devices interact with each other in such a way that an "interlock" system can be implemented with suitable software.

In a system with two processors, it is advantageous, in terms of disc space, to have the operating systems of these processors share the systems disc pack. This is known as a "shared-disc environment". It is conceivable that the systems would share not only system disc space but also user disc space. In this way, only one copy of a file would be on disc and either processor could access it. This sharing presents a problem, however. If both processors were to read the same record of the same file at the same time, update the record, and then write it back, information would be lost. The updating performed by one processor would be overlaid by the updating performed by the other processor. This is clearly an undesirable situation.

Another version of the problem has to do with disc allocation. If both systems wish to allocate new disc space on the shared disc at the same time, it is conceivable that they would both allocate the same space. The result of this would be both systems writing on the same space of the disc, thinking that this space belonged to them.

In order to prevent these events from occurring, some sort of "interlock" facility is required. Using either the full-duplex or half-duplex communication capabilities of the IPB, some sort of interlock could be implemented, but it would be complex and require much code-passing for the two processors to determine which one should have custody of which disc file. The interaction of the IPB Busy flags of the two processors gives a simple way to accomplish this interlock. One of the many ways to perform interlocking is described below. Let us call the computer wishing to establish a lock on a file "computer A" and the other computer in the system "computer B".

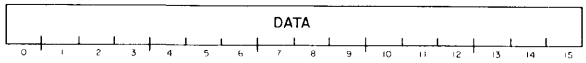
SUMMARY

HALF-DUPLEX

MNEMONIC ..... IPB
DEVICE CODE ..... 36_8
PRIORITY MASK BIT 6

ACCUMULATOR FORMATS

READ DATA ..... (DIA)
WRITE DATA ..... (DOA)



S, C, AND P FUNCTIONS

S — In the computer executing the instruction, the IPB Busy flag is set to 1 if the IPB Busy flag of the other computer is 0. Even if both computers issue a Start at exactly the same time, only one IPB Busy flag will be set to 1.

C — In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Busy flag is set to 0.

P — In the computer executing the instruction, the IPB Done flag is set to 0. In the other computer, the IPB Done flag is set to 1.

To start the lock procedure, computer A tries to set its IPB Busy flag to 1. Computer A does this by issuing a REQUEST BUS instruction (NIOS IPB). Computer A then checks to see if its IPB Busy flag is 1. If the flag is 1, computer A can continue with the procedure of establishing the desired lock. If the IPB Busy flag of computer A is 0, it means that the IPB Busy flag of computer B is 1, and computer B is about to do something in connection with either locking or unlocking a file. Computer A cannot continue the lock procedure until computer B completes its procedure.

Each computer keeps a table containing information about files in which it is interested. Each entry in the table has indicators which say whether or not this file has a lock on it and which computer has the lock. Once computer A succeeds in setting its IPB Busy flag to 1, computer A looks in its table to see whether or not computer B has a lock on the file that computer A wants. If the name of the desired file appears in this table, computer A must wait until computer B gives up its lock on the file. Note that computer A does not look in this "lock table" until it is successful in setting its IPB Busy flag to 1. If computer A looked in the table before attempting to set its IPB Busy flag to 1, it would be possible for computer B to establish a lock on the desired file between the time that computer A finished looking in the table and the time that computer A succeeded in setting its IPB Busy flag to 1.

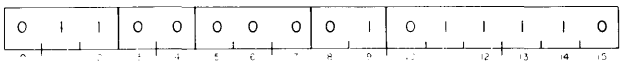
After computer A has determined that computer B does not have a lock on the desired file, computer A sends a code to computer B that means "I want to establish a lock". Computer A does this by issuing a WRITE DATA instruction with a Pulse (DOAP ac,IPB). The code word must be in the specified AC. When computer A issues this instruction, the IPB Done flag of computer B will be set to 1, signaling computer B that there is a word in its transmitter/receiver buffer waiting to be read.

Computer B reads this word by issuing a READ DATA instruction with a Pulse (DIAP ac,IPB). This instruction sets the IPB Done flag of computer B to 0. The instruction also sets the IPB Done flag of computer A to 1, signaling computer A that computer B has read the word and is ready to receive another. This sequence continues until all information pertaining to the lock desired by computer A has been transferred to computer B. After the last word has been transferred, computer A issues a CLEAR FLAGS instruction (DIB) to set its IPB Busy and Done flags to 0. The system is now ready for another lock or unlock procedure to begin. The procedure for unlocking a file is the same as the procedure described above, except that the code word sent is the code word for unlock.

Instructions

REQUEST BUS

NIOS IPB



In the computer executing the instruction, the IPB Busy flag is set to 1 if the IPB Busy flag of the other computer is 0.

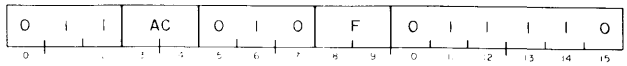
READ DATA

DIA<u>f</u> <u>ac</u>,IPB

The contents of the IPB buffer are placed in bits 0-15 of the specified AC in the computer executing the instruction. The previous contents of the specified AC are lost. The contents of the IPB buffer remain unchanged. After the data transfer, the Busy and Done flags are set according to the function specified by f.

WRITE DATA

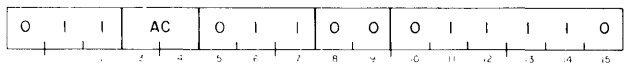
DOA<u>f</u> <u>ac</u>,IPB



Bits 0-15 of the specified AC in the computer executing the instruction are placed in the IPB buffer. The previous contents of the IPB buffer are lost. The contents of the specified AC remain unchanged. After the data transfer, the Busy and Done flags are set according to the function specified by f.

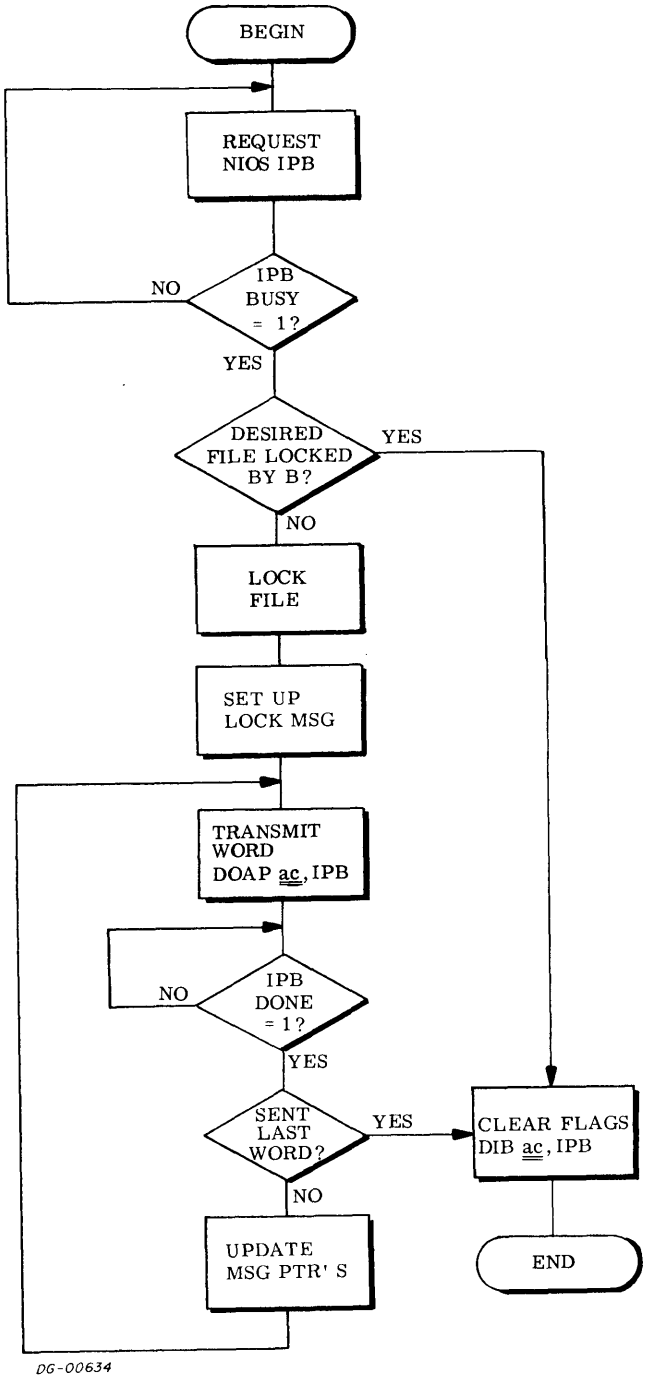
CLEAR FLAGS

DIB <u>ac</u>,IPB

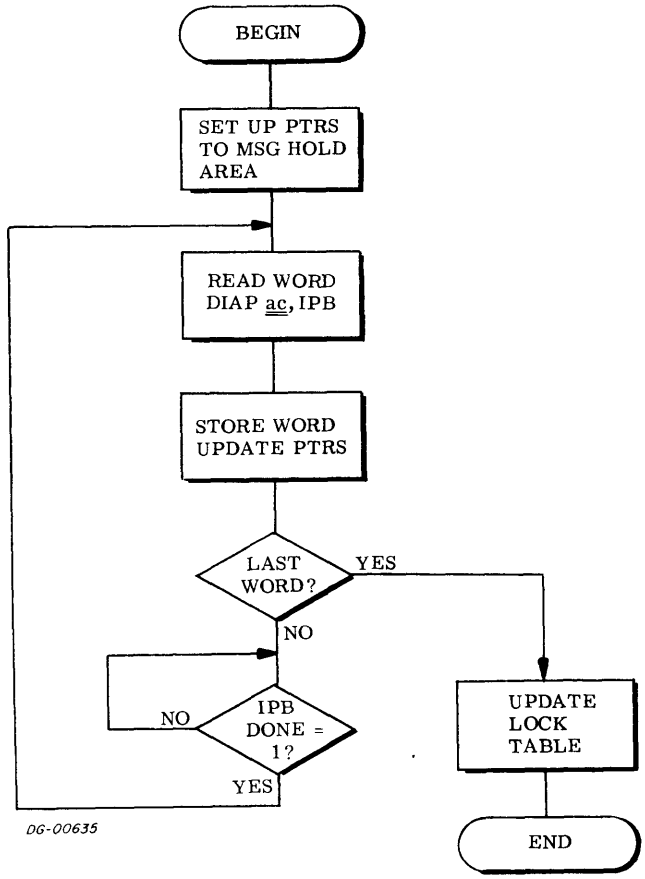


The IPB Busy and Done flags in the computer executing the instruction are both set to 0. The contents of the specified AC are lost.

NOTE None of the optional mnemonics specified by f should be coded with this instruction. If any of the three optional mnemonics are coded, results will be unpredictable.



Transmission Flowchart Computer A



Reception Flowchart Computer B

WATCHDOG TIMER

The watchdog timer facility of the IPB consists of two timers. One timer is placed in each computer in the system. The timers are so constructed that if they are allowed to run for approximately one second without being restarted, they will initiate a program interrupt request in the computer in which they are installed.

The watchdog timer facility is useful in multiprocessor configurations for indicating to one processor whether or not the other processor is still functioning. If either processor does not start its timer at intervals of less than one second, the other processor will receive an indication of this fact. If a timer is allowed to run for approximately one second without being restarted, it indicates a failure of some sort in the processor which is connected to that timer.

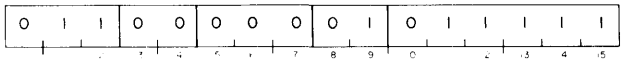
To use the watchdog timer facility, each processor must issue a START TIMER instruction at least once per second. This instruction starts the timer in the other processor. If a timer is allowed to run for one second without being restarted, its Done flag will be set to 1. This indicates to the processor in which the timer is installed that the other processor has ceased to function. If a processor receives this indication, it should take appropriate action and then issue a CLEAR TIMER instruction. If the processor that is still functioning does not issue a CLEAR TIMER instruction, then it will continue to report the failure of the other processor.

In the event of one processor knowing that it is about to cease functioning, (i.e., a Power Fail situation) that processor can indicate this situation to the other processor by issuing a SET TIMER instruction. This instruction will immediately set the IVT Done flag in the other processor to 1.

Instructions

START TIMER

NIOS IVT



The one-second timer in the other processor is started.

SUMMARY	
MNEMONIC	IVT
DEVICE CODE	37_8
PRIORITY MASK BIT	6
TIMER PERIOD (SEC)	1

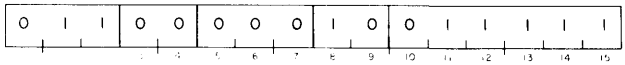
ACCUMULATOR FORMATS
(none)

S, C, AND P FUNCTIONS

S	The timer in the other computer is started.
C	In the computer executing the instruction, the IVT Done flag is set to 0.
P	In the other computer, the IVT Done flag is set to 1.

CLEAR TIMER

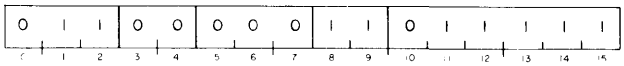
NIOC IVT



In the computer executing the instruction, the IVT Done flag is set to 0.

SET TIMER

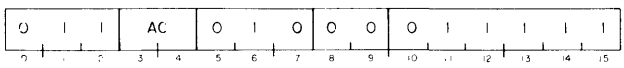
NIOP IVT



The IVT Done flag in the other processor is set to 1.

START OWN TIMER

DOA ac, IVT



In the computer executing the instruction, the timer is started. The contents of the specified AC remain unchanged.

SECTION I

INSTALLATION

INTRODUCTION

A dual DGC computer system requires the following items for an IPB communications link: two DGC computers, two 15-inch square 4240 Inter-Processor Bus printed circuit boards (one in each computer), two internal cables (one for each IPB board in each computer) and one external cable. These items can be purchased separately (an internal cable is supplied when a 4240 IPB printed circuit board is purchased), or as part of a complete minicomputer system. When items are purchased separately the installation procedure will include all the tasks outlined in this section. In the case where the IPB is purchased as part of a complete system, the system will be shipped in a partially or completely assembled state, eliminating some of the tasks outlined in this section. The considerations involved in the installation of the IPB can be divided into inspection, unpacking, positioning of boards and cabling.

INSPECTION

Inspection is performed in three stages: before unpacking, after unpacking, and through the Diagnostic and Reliability Programs. Before unpacking, all shipping containers should be inspected for signs of damage incurred in transit. After unpacking, items should be inspected for damage incurred in transit; if damage has occurred in either of these cases, both Data General Corp. and the carrier should be notified immediately. After installation, the IPB Diagnostic and Reliability Programs can be run as a final inspection. The Diagnostic Program can be run as described in the diagnostic listing whenever a single IPB board is ready to be installed. The Reliability Program is run when the two IPB boards, internal cables, and external cables have all been installed.

UNPACKING

Caution The primary consideration in unpacking is to avoid damage to the equipment being unpacked. Tapes sealing a container or folder should be cut with scissors or slit in such a manner as to avoid damage to the items inside. Avoid flexing or bending printed circuit boards. Save all packing materials.

The unpacking procedure for a computer containing boards and internal cables is given in the technical manual for that computer. Printed circuit boards shipped separately are packed in cardboard folders within a carton. Cables are shipped in several ways: in position when part of an assembled system, in the same carton as the printed circuit boards when part of a small shipment, or in a package containing several cables. The unpacking procedure for a package containing printed circuit boards or cables is as follows:

1) Open the cardboard carton, avoiding damage to its contents, and remove the loose "flow-pack" and any cables shipped in the package.
2) Remove the folders containing printed circuit boards. Avoid bending the boards.
3) Open each folder using scissors to cut the tape. Avoid stabbing or bending the folder.
4) Remove the printed circuit board from the folder and open the plastic bag containing the board.

POSITIONING THE IPB BOARD

The slots available in any DGC computer for the IPB will depend on the computer, its options, and the other I/O devices in use. The installation section of the computer technical manual (and some of the I/O controller manuals) should be consulted for specific rules and some recommendations on board placement. Some general rules concerning the occupation of slots in DGC computers are: Slot 1 always has a CPU board; Slot 2 has either a CPU board, a memory, or a Multiply/Divide option; depending on the computer and its options; Slot 3 is wired for the basic I/O devices (Teletype® or CRT display, Paper Tape Punch and Paper Tape Reader) using the 4007 I/O interface subassembly, but can also have a memory board. Also, the Data General convention is to install memory boards from lower numbered slots up and I/O controllers from the highest slot down.

In spite of the rules given above, the task of choosing a slot in the computer chassis in which to place the IPB board is not necessarily trivial. The major user criterion for choosing a slot in which to place the IPB board, is the priority for interrupt service relative to other controllers he wishes to assign the IPB. The Program Interrupt priority chain is

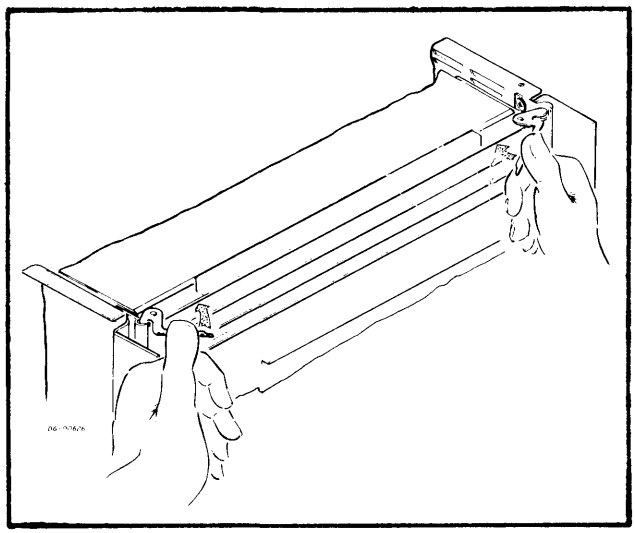
hardwired so that device controllers in lower slots have a higher priority in responding to INTERRUPT ACKNOWLEDGE instructions. Within the IPB board itself there is an internal interrupt priority chain that goes from highest priority to lowest as follows: half-duplex line, full-duplex receiver, full-duplex transmitter, watchdog timer.

A related consideration in choosing the slot of the IPB board is the continuity of the Program Interrupt and Data Channel priority chains. These chains are independent of each other and operate by passing an enabling signal from slot to slot through each board in the chain. A controller can be recognized for Data Channel service or Interrupt service only when the enabling signal, $\overline{\text{DCHP}}$ or $\overline{\text{INTP}}$, respectively, is low. The lowest controller requesting service is recognized and removes the enabling signal level from other controllers further along the chain. All DGC boards maintain the continuity of both chains by either participating in the chain or having internal jumpers passing the enabling signals through the board. If a slot is empty (or contains a board not manufactured by Data General Corp., which does not maintain Data Channel and Interrupt continuity) controllers located in higher slots will not receive the Program Interrupt and Data Channel enabling signals, unless the continuity is maintained by jumpering the enabling signals over the empty slot(s) to the next DGC board.

The continuity of the Program Interrupt enabling signal ($\overline{\text{INTP}}$) is maintained by placing a jumper from pin A96 of the lowest slot in a sequence of empty slots (or slots containing boards which do not pass the signal) to pin A96 of the next slot containing a DGC board. This jumpering is required for each set of slots which do not pass $\overline{\text{INTP}}$. Similarly, for the Data Channel enabling signal ($\overline{\text{DCHP}}$), a jumper is placed from pin A94 of the lowest slot in a sequence of slots that do not pass the $\overline{\text{DCHP}}$ signal to pin A94 of the next slot containing a DGC board.

When the IPB board is placed in a previously empty slot that has been correctly jumpered over to maintain the Data Channel and Program Interrupt priority chain continuity, the jumpers must be removed or rewired to reflect the new arrangement.

Once the slot has been chosen for the IPB board, the remaining tasks are cabling the system and inserting the IPB board in the slot. The IPB board is placed in a slot by carefully sliding it, component side facing up, into the guides on each side of the chassis. The locking tabs at the corners of the board are used to provide leverage to completely seat the board in the two connectors in the slot. The board is plugged into the connectors by pressing the locking tabs towards the board and is unplugged by releasing the locking tabs as shown below.



CABLING

The cables in the IPB communications link pass data and signals between the two IPB boards. Two internal cables are needed (one for each computer) to link the back panel pins of the slot occupied by an IPB board to an external cable connecting the two computers.

Internal Cables

The types of cables required by different systems are determined by the internal cable connector mounting schemes used in different DGC computer models. DGC computers having 7 or 17 slots (i. e., NOVA computer, SUPERNOVA computer, NOVA 800, 840, 1200, and 1230 computers) are designated group A; these computers have a cable mounting area on the chassis which is suitable for internal cables using female socket connectors. DGC computers having 4 or 10 slots (i. e., NOVA 820, 1210, 1220, and NOVA 2 computers) are designated group B; these computers mount paddleboard connectors for internal cables on standoffs next to other paddleboard connectors on the chassis.

When an IPB board is purchased, the DGC model computer it is to be used in must be specified so that the correct internal cable can be shipped with the board. The internal cable is installed by mounting the connector in the cable mounting area of the chassis and wire wrapping the cable wires to the appropriate back panel pins of the slot holding the IPB board. The one exception to this procedure is on Slot 9 of all 10 slot DGC computers (NOVA 820, 1220 and NOVA 2/10 computers) where an internal cable is etch wired onto the back panel in the factory. The correct back panel pin for each wire is indicated by a tag on the wire and also in the wire list (see below). Pins with an A label are

on the left side of the back panel; pins with a B label are on the right side; odd pins are on the upper row; even pins are on the lower row; pin numbering is from left to right.

Caution The pins on the back panel are fragile and damaging any of them may lead to particularly expensive repairs or replacements. The internal cable leads should be connected to the back panel pins by wire wrapping only, and absolutely NOT by soldering. Data General strongly recommends that its field service personnel install all wire wrap connections to the back panel.

External Cable

When an IPB external cable is purchased, the model numbers of the DGC computers it is to connect must be specified so that the correct external cable will be sent. There are three types of external cable: cables with two male socket connectors for connecting two group A computers, cables with two female edge connectors for connecting two group B computers, and cables with one male socket connector and one female edge connector for connecting a group A computer to a group B computer. The cabling of the IPB communications link is completed by the plugging of the external cable connectors into the connectors of the internal cables going to the slots containing the IPB boards in the two computers.

Caution The external cable and all device cables should be secured and strain relieved at each computer. Failure to do so may result in damage to the back panel pins.

DIAGNOSTIC AND RELIABILITY PROGRAMS

The IPB documentation package includes a Diagnostic Program Tape, a Reliability Program Tape and listings giving operating procedures for these tapes. The diagnostic program is used to test a single IPB board; it requires a special test plug supplied with the board. The reliability program tests the various types of transfers between two computers carried out through the IPB.

REFERENCES

Wire Lists

008-000194 wire list for internal cable (general purpose) for NOVA 1210, 1220 and 820 computers.

008-000426 wire list for internal cable (general purpose) for NOVA 2 computer.

008-000467 wire list for internal cable for NOVA 1200, 1230, 800, 840 computers.

008-000468 wire list for external IPB cable (group A to group A).

008-000469 wire list for external IPB cable (group A to group B).

008-000470 wire list for external IPB cable (group B to group B).

Diagnostics

095-000177 absolute binary IPB diagnostic tape.

095-000178 absolute binary IPB reliability tape.

096-000156 listing for the IPB diagnostic tape.

096-000157 listing for the IPB reliability tape.

CUT ALONG DOTTED LINE

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