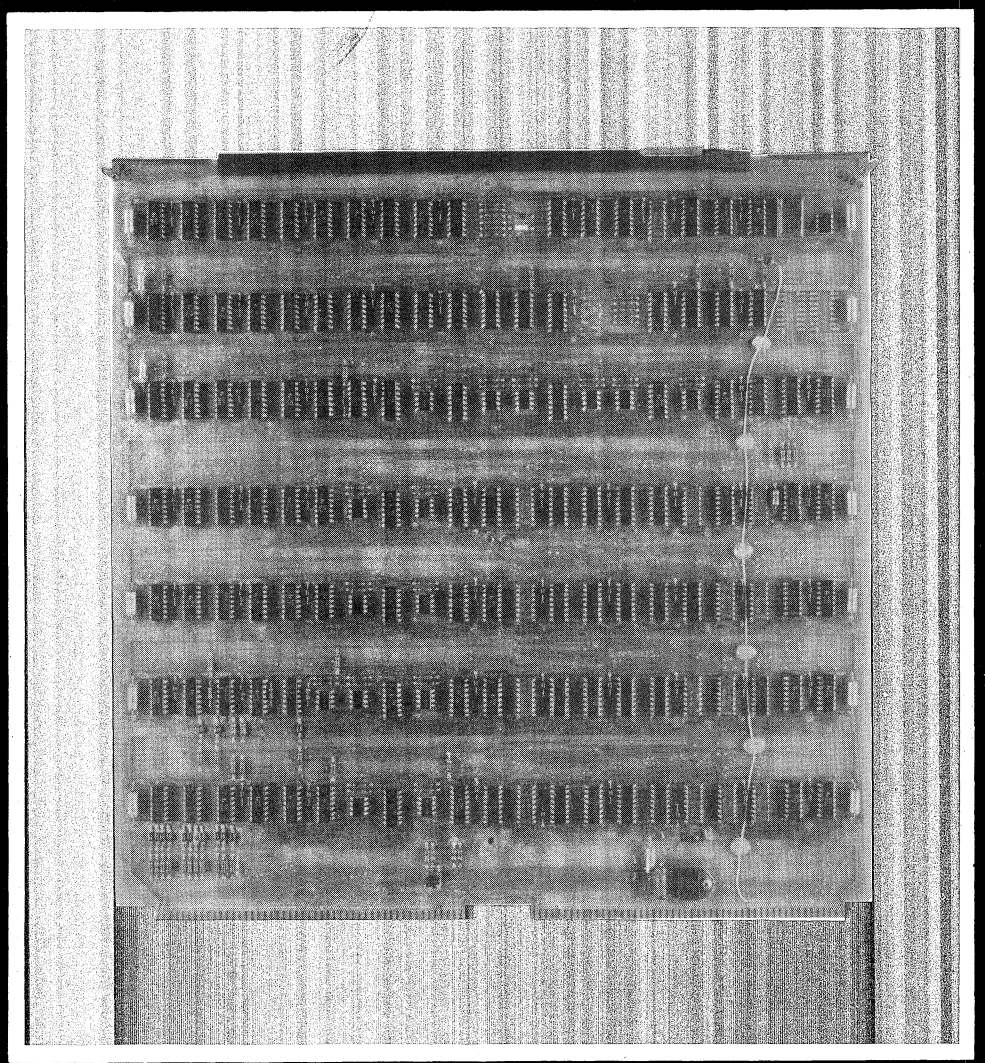
Maintenance Service Guide

MULTIPROCESSOR COMMUNICATIONS ADAPTER



Data General

Data General Service, Inc.
A Subsidiary of Data General Corporation

MAINTENANCE
SERVICE GUIDE
FOR
MULTIPROCESSOR COMMUNICATIONS ADAPTER

MODEL 4206

015-000200

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SECTION 1

INTRODUCTION

The Multiprocessor Communications Adapter (MCA), subsystem Model 4206, depicted in Figure 1-1, can connect up to fifteen NOVA® and/or ECLIPSE® -line computers in daisy chain fashion, to form a multiprocessor system. Blocks of data can be transferred from one computer to another, at either standard or high-speed rates, through the computer's data channel facilities, and a communications bus.

The MCA subsystem may be used whenever it is convenient to partition a job. For example, one CPU might handle a number of data communication lines, while another preprocesses data, and a third performs actual computations. Since several compatible processors are used, the system may also provide its own backup, in case of failure.

1.1 MCA SUBSYSTEM COMPONENTS

The MCA subsystem consists of a common communications bus, and an adapter board for each NOVA or ECLIPSE-line CPU in the system. An internal cable connects the communications bus to the back panel of the CPU. These components are discussed in detail below.

1.1.1 Communications Bus - The communications bus is an external, bidirectional cable that connects the adapters of each CPU in the system in a daisy chain fashion. Data is transmitted via the bus to specified destinations. The bus is time division multiplexed, providing sequenced time slots for each adapter. For example, if there are four logical links established, and communications are proceeding on all, each link receives 1/4 of the communications bus time. Any of the interconnected computers can be stopped, or have its power switched off, without affecting the other computers still in operation. Internal cables connect the bus to the back panel.

1.1.2 Multiprocessor Communications Adapter PCB - The MCA PCB is a 15 inch square resident in any I/O slot of either a NOVA or ECLIPSE-line CPU chassis. Each adapter board connects a single CPU to the communications bus, and is assigned a unique jumper-selectable identifying number, ranging from 1 to 15. This number identifies the adapter when data is transferred to and from other CPUs in the multiprocessor system.

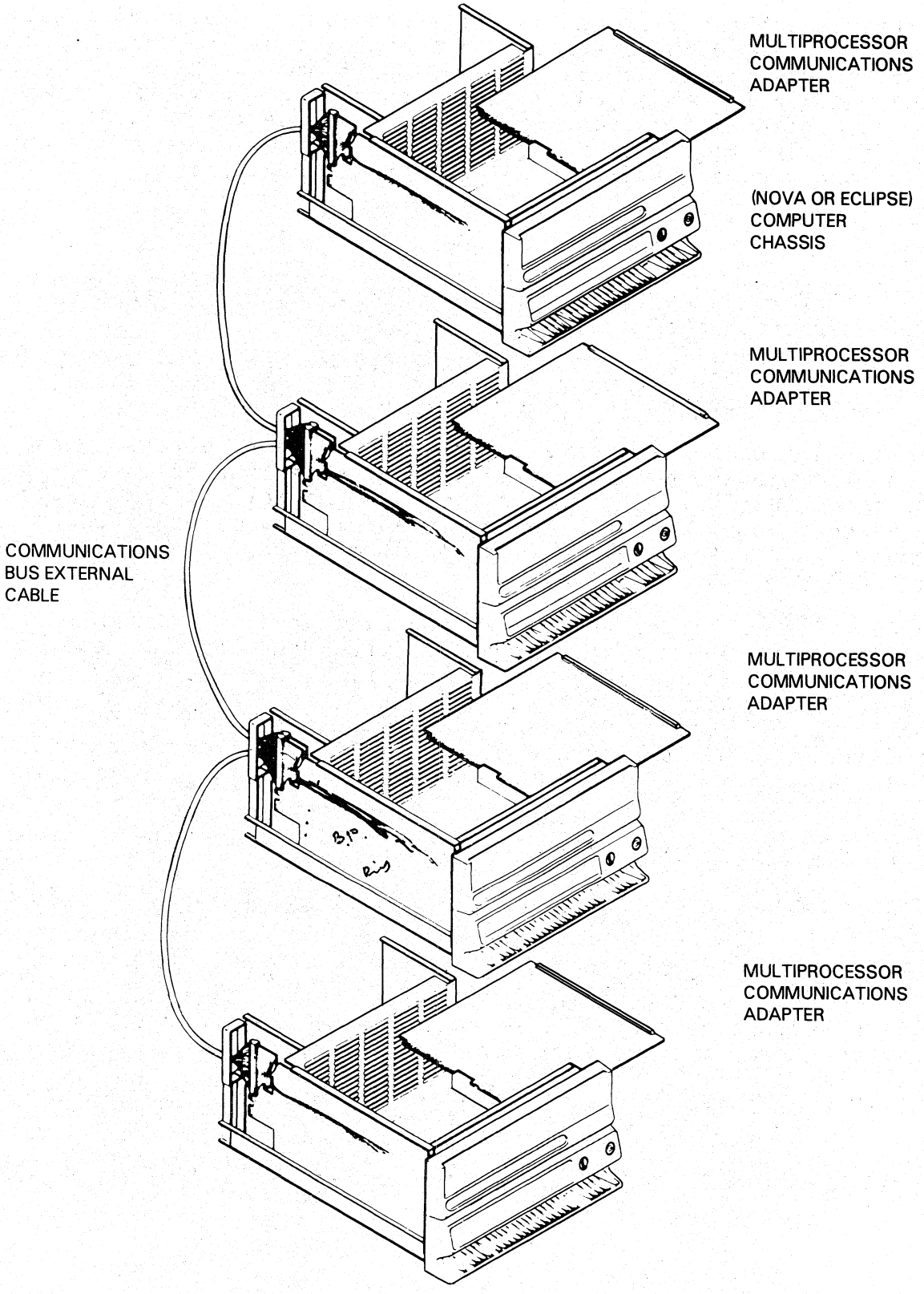


Figure 1-1. Multiprocessor Communications Adapter Subsystem

Internal cables wire the communications bus to the back panel of the MCA slot in the CPU chassis. Each MCA can be connected to the communications bus via two ports: the OUT port and the IN port. The OUT port of one MCA is connected to the IN port of the next MCA in the daisy chain, via the communications bus. Note that the terms "OUT" and "IN" do not describe the direction of the data transfer. Since the bus is bidirectional, data travels in and out of either port.

NOTE

A leftmost adapter has a terminator, instead of another adapter plugged into its IN port.

A rightmost adapter has a terminator, instead of another adapter plugged into its OUT port.

An adapter contains both a transmitter and a receiver. These two devices allow independent transmission and reception of data. Each device is connected separately to the data channel. The MCA software first selects and prepares a device, transmitter, or receiver, to send or receive data. All transfers to and from memory are then handled automatically by the data channel.

A CPU with an adapter board can establish a link between its transmitter, and any receiver it designates (provided that the receiving adapter has been initialized for reception). When receiving the first data word from a transmitting adapter, the receiver locks onto that transmitter, and subsequently accepts further data only from that transmitter. To unlock the receiver so that it can receive data from another transmitter, an I/O instruction must be issued by the receiving CPU.

1.2 MCA CONFIGURATIONS

The following two rules are important for configuring an MCA subsystem:

1. The distance from the first MCA to the second, must be less than or equal to 6.09 meters (20 feet). The remaining MCAs may be distributed in any manner over the bus, as long as the total length of the bus does not exceed 42.67 meters (140 feet).

2. For systems with only two MCAs, the distance between the two MCAs can be up to 150 feet.

Refer to Figure 1-2 and Table 1-1 for MCA configuration specifications.

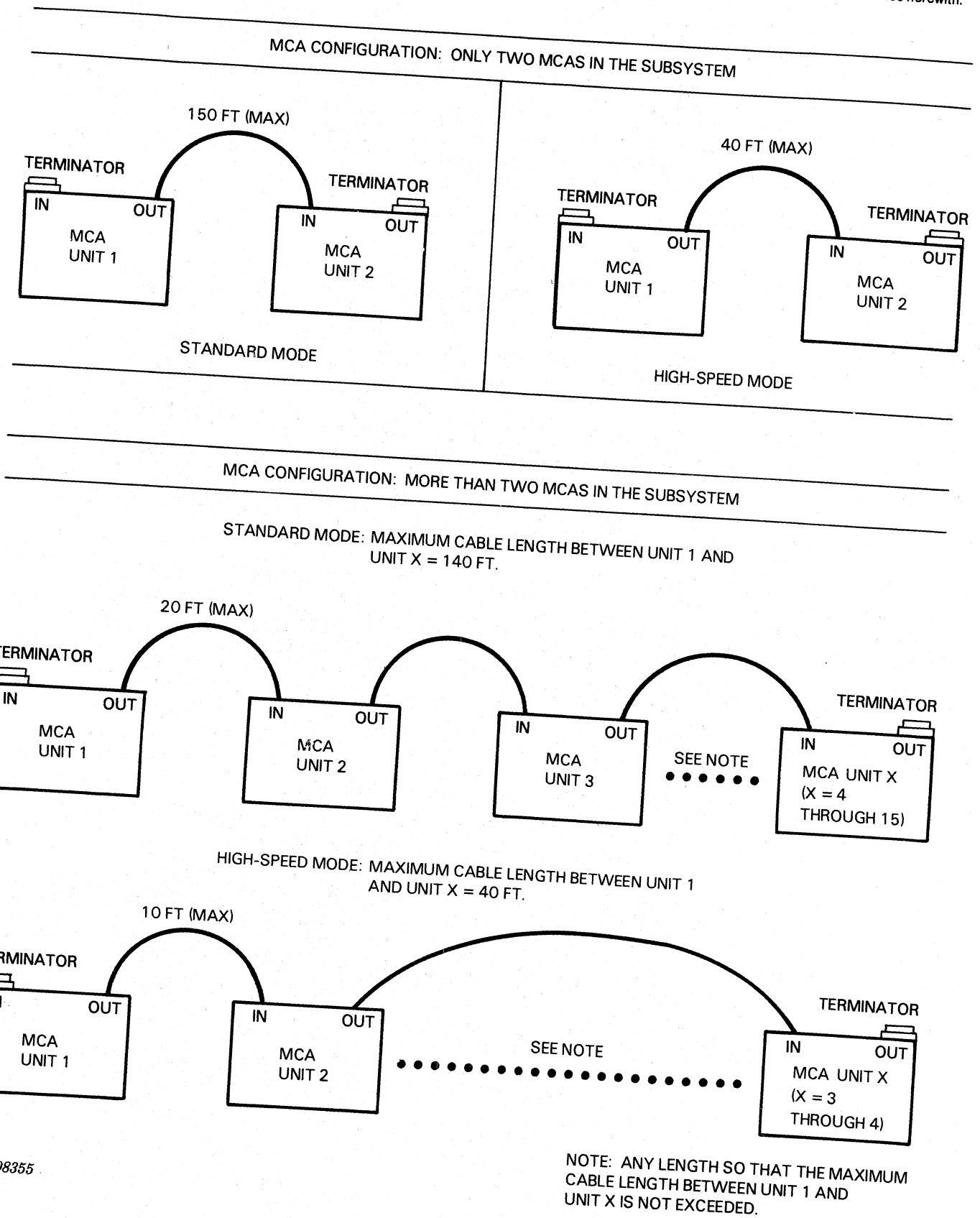


Figure 1-2. MCA Configurations

Table 1-1. MCA Configuration Specifications

SPECIFICATION	STANDARD MODE	HIGH-SPEED MODE
MCAs in a System	Up to 15.	Up to 4.
Bus Length (Max):		
Only Two MCAs	45.72 m (150 ft)	12.19 m (40 ft)
More Than Two MCAs	42.67 m (140 ft)	12.19 m (40 ft)
Distance Between First Two MCAs in a System:		
Only Two MCAs (in the System:	45.72 m (max) (150 ft)	12.19 m (max) (40 ft)
Three or More MCAs (in the System)	6.09 m (max) (20 ft)	3.05 m (max) (10 ft)
Distance Between the Remaining MCAs:	The remaining MCAs may be distributed in any way, but can not exceed the maximum total bus length.	

1.3 DATA BLOCKS

The size and form of the data transmission can follow any convention established by the user. In a relatively simple system, in which the size and nature of the data blocks to be transferred is always known in advance, the receiver can initialize itself to accept the data block at the completion of the previous transmission.

If the exact size and nature of the data blocks has not been predetermined, a control block specifying the nature of a transfer is transmitted before the actual data block. With such a convention, the receiver initializes itself. The first word transferred to the receiver, locks it to the sending transmitter until explicitly unlocked by the program. Thus, once the first word in a control block is received, the receiver is locked to that transmitter, and is initialized to accept subsequent data blocks from that transmitter.

Alternatively, the control block from adapter A to adapter B can be a request for data. Adapter B's transmitter can start sending the desired data while its receiver is reinitialized to accept a new control block. The hardware does not distinguish between data and control blocks.

1.4 MCA SPECIFICATIONS

Table 1-2 below summarizes MCA subsystem specifications according to operating mode, standard or high-speed.

Table 1-2. MCA Subsystem Specifications

SPECIFICATION	STANDARD	HIGH-SPEED
Data Transfer Rates* (words/second)	Up to 312,500	Up to 500,000
Maximum Allowable Programmed I/O Latency	Infinite (msecs)	Infinite (msecs)
Controller's +5 V Current Draw	3.5 A	3.5 A

* Data transfer rates are determined by the response time of the processor's data channel facilities. Whether the MCA is operating in standard or high-speed mode, is also a factor.

1.5 FIELD REPLACEABLE UNITS

The Field Replaceable Units (FRUs) comprising the MCA are listed in Table 1-3 below.

Table 1-3. MCA Field Replaceable Units

DGC PART NO.	FRU
005-006732	Assembly Main PCB MCA
	Non FCC-Compliant Cables and Terminators
005-007058	MCA External Cable (Cannon to Cannon) Model 1106AA
005-007068	MCA External Cable (Cannon to Edge) Model 1106AB
005-007060	MCA External Cable (Edge to Edge) Model 1106BB
005-007062	Internal Cable (IN) Cannon
005-007063	Internal Cable (OUT) Cannon
005-007064	Internal Cable (IN) Edge
005-007065	Internal Cable (OUT) Edge
005-007067	Test Plug Cannon Model 4206A
005-007072	Edge Conn. Test Plug 4206A Terminator
005-012585	MCA Bus Internal Cable (IN & OUT) (Push-on)

Table 1-3. MCA Field Replaceable Units (Continued)

DGC PART NO.	FRU
	FCC-Compliant Cables and Terminators
	FCC-Compliant to FCC-Compliant Connectors (Model 1106HH SubD to SubD)
005-18617	10 ft External Cable
005-19421	20 ft External Cable
005-19276	40 ft External Cable
005-20131	75 ft External Cable
005-19485	140 ft External Cable
005-19484	Internal Cable for FCC-Compliant Connection
005-20329	Terminator for FCC-Compliant Connection
	FCC-Compliant to Non FCC-Compliant Connector (Model 1106BH - Edge to SubD)
005-19488	10 ft External Cable
005-20130	20 ft External Cable
005-19263	40 ft External Cable
005-20129	75 ft External Cable
005-19487	140 ft External Cable
005-12585	Internal Cable for Edge Connector
005-07064	Internal Cable for Wire-Wrap Connection
005-07065	
005-19484	Internal Cable for FCC-Compliant Connection
005-07072	Terminator for Edge Connector
005-20329	Terminator for FCC-Compliant Connection
	FCC-Compliant to Non FCC-Compliant Connector (Model 1106AH Cannon to SubD)
005-19483	10 ft External Cable
005-20128	20 ft External Cable
005-19482	40 ft External Cable
005-20127	75 ft External Cable
005-19486	140 ft External Cable
005-07062	Internal Cable for Cannon Connector
005-07063	
005-19484	Internal Cable for FCC-Compliant Connection
005-07067	Terminator for Cannon Connector
005-20329	Terminator for FCC-Compliant Connector

SECTION 2

OPERATING CONTROL AND PROCEDURES

There are no operating controls or procedures for the Model 4206 MCA.

SECTION 3

THEORY OF OPERATION

The MCA, which consists of an adapter board and a communication bus, transfers data from one computer to another, through the computer's data channels. The adapter board is attached to the I/O bus of each computer in the system. In turn, all the adapter boards in the system are attached to one another by a common communications bus. Both the major MCA logic blocks and the MCA operations, are discussed in detail below.

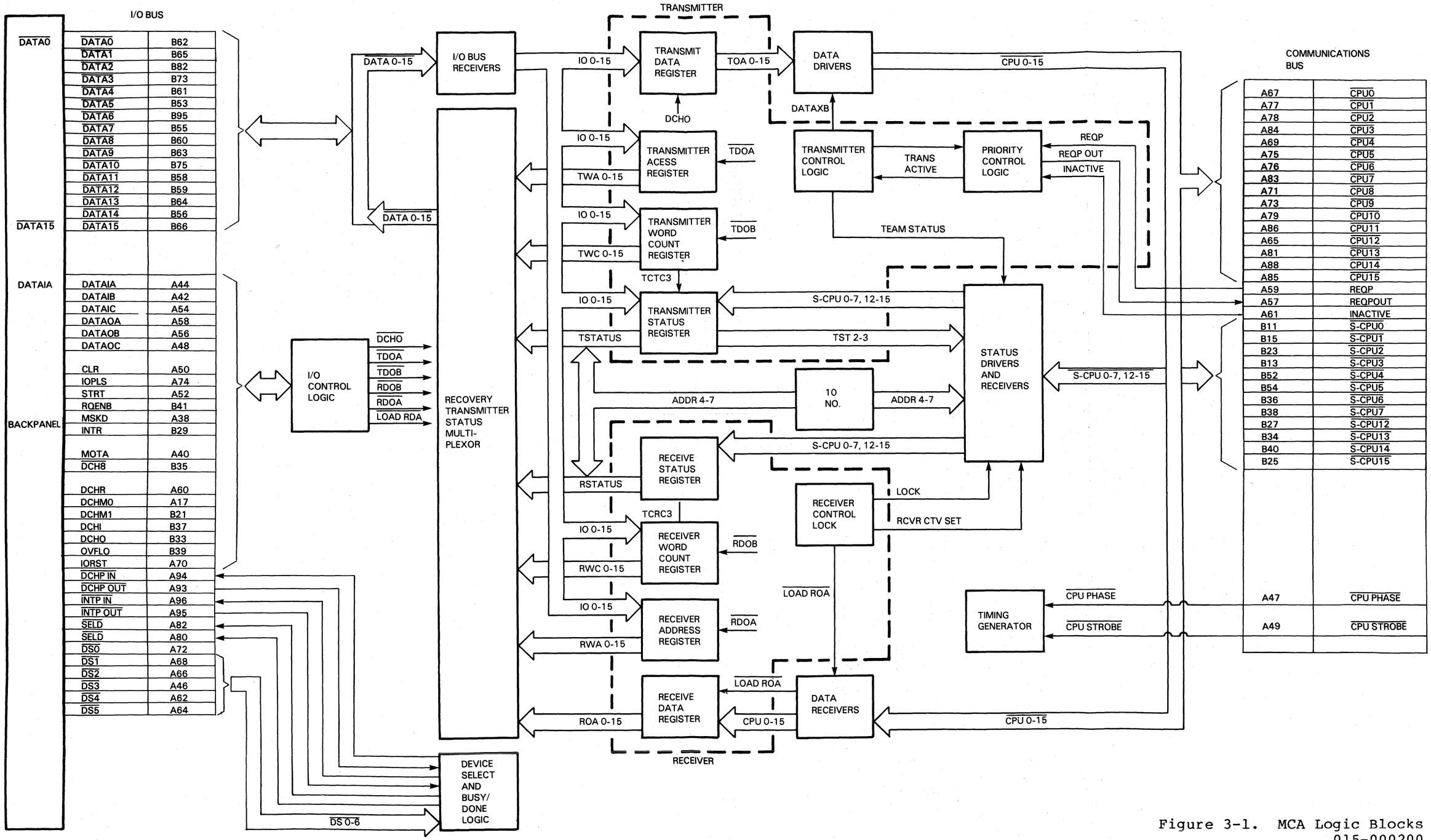
3.1 MCA LOGIC BLOCK DESCRIPTION

The major MCA logic blocks, and their interrelationships, are shown in the MCA major block diagram, Figure 3-1. These blocks, which are listed and defined in detail below, fall under the following categories:

- Transmitter logic blocks and registers
- Receiver logic blocks and registers
- I/O control logic
- Busy/Done logic
- Timing generator
- Receiver/transmitter status multiplexor
- Identifying logic
- Drivers
- Receivers

3.1.1 Transmitter - The transmitter contains the following logic blocks:

- Transmit data register
- Transmitter address register
- Transmitter word count register
- Transmitter status register
- Transmitter control logic
- Priority control logic



* OVFLO IS NOT AVAILABLE IN THE ECLIPSE LINE

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Figure 3-1. MCA Logic Blocks

3.1.1.1 Transmit Data Register - Contains a 16-bit data word that has been transferred from the I/O bus (via the data channel) over the I/O<0-15> lines. This word is then transmitted over the TDA<0-15> lines, to the data drivers.

3.1.1.2 Transmitter Address Register - Contains the memory location of the first word to be transferred. This location is transferred from the I/O Bus Receivers over the I/O<0-15> lines, and is then sent over the TWA<0-15> lines to the I/O Bus Multiplexor.

3.1.1.3 Transmitter Word Count Register - Contains the two's complement of the number of words to be transferred. This number is transferred from the I/O Bus Receivers over the I/O<0-15> lines and is then sent over the TWC<0-15> lines to the I/O Bus Multiplexor. (The number is also sent to the Transmitter Status Register via the TCTC3 line.)

3.1.1.4 Transmitter Status Register - Contains the status of the transmitter. This information includes:

1. the identifying number of the receiver to which transmissions are directed.

2. the identifying number of this transmitter.

3. the status of the selected receiver (whether the selected receiver is locked to either this transmitter or some other transmitter).

4. the status of the transmitter (whether the transmitter has sent the last word of a block as specified by its Word Count Register).

The Transmitter Status Register receives input from the I/O<0-3> lines, the TCTC3 lines, and the Status Drivers and Receivers. The receiver sends signals over the TST<0-3> lines to the Status Drivers and Receivers. It also outputs to the I/O Bus Control Multiplexor.

3.1.1.5 Transmitter Control Logic - Maintains the transmitter's address, word count, and status registers, (including a timeout indicator), coordinates the transmitter's data channel activities, and generates requests to use the communications bus.

3.1.1.6 Priority Control Logic - This circuitry determines which transmitter in the MCA network has access to the shared communications bus at any given time.

3.1.2 Receiver - The receiver contains the following logic blocks:

- Receiver control logic
- Receive data register
- Receiver address register
- Receiver word count register
- Receiver status register

3.1.2.1 Receive Data Register - Contains the data word transferred from the Data Receivers over the CPU<0-15> lines. The word is then transferred to the I/O Bus Control Multiplexor over the RDA<0-15> lines.

3.1.2.2 Receiver Word Count Register - Contains the two's complement of the number of words yet to be received. Receives its input over the I/O>0-15> lines and outputs to the I/O Bus Control Multiplexor over the RWC<0-15> lines as well as to the Receiver Status Register over the TCRC3 line.

3.1.2.3 Receiver Address Register - Contains the location in memory where the next word to be received will be stored. Receives its input over the I/O<0-15> lines and outputs to the I/O Bus Control Multiplexor over the TWA<0-15> lines.

3.1.2.4 Receiver Status Register - Contains the status of the receiver. This information includes:

- the identifying number of this receiver.
- the identifying number of the transmitter to which the receiver is or was most recently locked.
- receiver status:

  a. whether this receiver is locked to the specified transmitter
  b. whether the receiver has received the last word of a block

- whether the transmitter has sent the last word of a block as specified by its Word Count Register.

The register receives signals from the Status Drivers and Receivers and outputs to the I/O Bus Control Multiplexor, the Status Drivers, and Status Receivers.

3.1.2.5 Receiver Control Logic - The three main functions of the receiver control logic are as follows:

1. To maintain the receiver's Address, Word Count, and Status Registers, including a lock and a timeout indicator.

2. To coordinate the receiver's data channel activities.

3. To monitor the status portion of the communications bus for requests to transmit data to this receiver.

3.1.3 I/O Control Logic - Coordinates and synchronizes the transfer of data from the receiver or the transmitter to the data channel of the I/O bus.

3.1.4 Busy/Done Logic - Allows the program to determine in detail the status of the MCA subsystem.

3.1.5 Timing Generator - The generator, located on the leftmost MCA in the system, coordinates the activities of the transmitters and receivers in the MCA network.

3.1.6 Receiver/Transmitter Status Multiplexor - This multiplexor stores data to be transferred once data channel has been granted.

3.1.7 Identifying Logic - Contains the logic and jumpers necessary to identify the adapter during data transfers to and from other computers in the multiprocessor system.

3.1.8 Drivers - The two types of drivers, data and status, boost the small drive current to a higher value suitable for driving a large number of devices simultaneously.

3.1.9 Receivers - The following are the three types of receivers for the I/O bus signals:

1. I/O Bus Receivers
2. Status Receivers
3. Data Receivers

3.2 MCA BUSSES AND SIGNALS

There are two busses that allow the MCA to communicate with the host CPU and the other MCA PCBs in the subsystem, the I/O bus, and the communications bus.

3.2.1 The I/O Bus - The host CPU communicates with its MCA thru the back panel. In addition to the data signals, there are three types of signals appearing on the I/O bus:

- I/O Control
- Device Select
- Busy/Done

Table 3-1 lists and defines the I/O signals and back panel pin number.

Table 3-1. NOVA/ECLIPSE I/O Bus Signals

SIGNAL NAME	BACKPANEL PIN	DESCRIPTION
$\overline{\text{DATA 0 - 15}}$	B62, B65, B82, B73 B61, B57, B95, B55 B60, B63, B75, B58 B59, B64, B56, B66	Data. All data and addresses, for both data channel and Processor I/O (PIO) are transferred between the interface and the processor via these 16 bidirectional lines.
$\overline{\text{DS 0-5}}$	A72, A68, A66, A46 A62, A64	Device Select. These lines carry the six low order bits of the I/O instruction currently being executed.
DATIA	A44	Data In A. Asserted by the processor during the execution of a DIA instruction.
DATIB	A42	Data In B. Asserted by the processor during the execution of a DIB instruction.
DATIC	A54	Data In C. Asserted by the processor during the execution of a DIC instruction.
DATOA	A58	Data Out A. Asserted by the processor during the execution of a DOA instruction.
DATOB	A56	Data Out B. Asserted by the processor during the execution of a DOB instruction.

Table 3-1. NOVA/ECLIPSE I/O Bus Signals (Continued)

SIGNAL NAME	BACKPANEL PIN	DESCRIPTION
DATOC	A48	Data Out C. Asserted by the processor during the execution of a DOC instruction.
STRT	A52	Start. Asserted by the processor during the execution of an I/O instruction in which bits 8 and 9 = 01.
CLR	A50	Clear. Asserted by the processor during the execution of an I/O instruction in which bits 8 and 9 = 10.
IOPLS	A74	I/O Pulse. Asserted by the processor during the execution of an I/O instruction in which bits 8 and 9 = 11.
$\overline{\text{SELB}}$	A82	Selected Busy. Asserted by the interface if its Done flag is set to 1.
$\overline{\text{SELD}}$	A80	Selected Done. Asserted by the interface if its Busy flag is set to 1.
$\overline{\text{INTR}}$	A29	Interrupt Request. Asserted by the interface to request program interrupt service.
$\overline{\text{MSKO}}$	A38	Mask Out. Asserted by the processor during the execution of a MSKO instruction.
$\overline{\text{INTP IN \& OUT}}$	A96, A95	Interrupt Priority. Asserted by the first interface on the I/O bus using the program interrupt facility.
INTA	A40	Interrupt Acknowledge. Asserted by the processor during the execution of a INTA instruction.
$\overline{\text{DCHR}}$	B35	Data Channel Request. Asserted by the interface when it requires data channel service.
$\overline{\text{DCHP IN \& OUT}}$	A94, A93	Data Channel Priority. Asserted by the first data channel interface on the I/O bus.

Table 3-1. NOVA/ECLIPSE I/O Bus Signals (Continued)

SIGNAL NAME	BACKPANEL PIN	DESCRIPTION
$\overline{\text{DCHA}}$	A60	Data Channel Acknowledge. Asserted by the processor at the beginning of each data channel cycle.
$\overline{\text{DCHM0-DCHM1}}$	B17, B21	Data Channel Mode. Asserted by the interface whose DCH SEL flip flop is set, to inform the processor of the type of cycle being performed.
DCHI	B37	Data Channel In. Asserted by the processor for data channel input.
DCHO	B33	Data Channel Out. Asserted by the processor for data channel output.
IORST	A70	I/O Reset. Asserted by the processor during the execution of an I/O Reset (IORST) instruction, or when the console RESET switch is activated.
PWR ON	any +5V Pin	Power-On. A +5 volt signal that is asserted when the computer is on.
$\overline{\text{RQENB}}$	B41	Request Enable. Asserted by the processor to synchronize program interrupt and data channel requests from all interfaces.
*OVFLO	B39	Overflow.

* Not available on the ECLIPSE line.

3.2.2 The Communications Bus - The MCA PCBs exchange data and signals over an external cable known as the communications bus. The communications bus links the OUT port of one MCA PCB with the IN port of another MCA PCB. Table 3-2 describes the communications bus signal, and lists the back panel pin numbers. Table 3-3 indicates the location of the signals on the external connectors.

Table 3-2. Communications Bus Signals

SIGNAL NAME	BACK PANEL PIN	DESCRIPTION
$\overline{\text{S-CPU 0-7}}$	B11, B15, B23, B13 B52, B54, B36, B38	Status CPU. Establish transmitter/ receiver pairings and transfer status information from one CPU another.
$\overline{\text{S-CPU 12-15}}$	B27, B34, B40, B25	
$\overline{\text{CPU 0-15}}$	A67, A77, A78, A84 A69, A75, A76, A83 A71, A73, A79, A86 A65, A81, A86, A85	Data. Transmit 16 data bits in parallel from one CPU to another.
$\overline{\text{CPU PHASE}}$	A47	Timing. Composed of two other timing signals: STATUS PHASE (low) and DATA PHASE (low). Ensure that only one transmitter/ receiver pair is using the communications bus at any given time.
$\overline{\text{CPU STROBE}}$	A49	Timing. Composed of two other timing signals: STATUS STROBE and DATA STROBE. Control the transfer of status information and data between that pair of CPUs.
REQP	A59	Priority Control. Determines which of the active transmitters will be given access to the communications bus by using a round-robin priority scheme.
REQP OUT	A57	Priority Control. Same as above.
GND	A1, A2, A99 A100, B1, B2, B100, B48, B50, B99	Ground.
+V TERM	A89, A90, A91	Power.
RETURN	A92	Status. Used to determine whether the adapter can access the communications bus.
INACTIVE	A61	Status. Used to determine whether the adapter can access the communications bus.
SPARE	A63	Reserved for future use.

Table 3-3. Internal Cable Connections for MCA IN and OUT Ports

SIGNAL	BACK PANEL PIN NO.	EXTERNAL CONNECTOR PIN NO. @1	@2	SIGNAL	BACK PANEL PIN NO.	EXTERNAL CONNECTOR PIN NO. @1	@2
GND	A1	A	1	GND	B100	b	24
+V TERM	A89	C	3	$\overline{\text{CPU 1}}$	A77	c	25
+V TERM	A90	D	4	$\overline{\text{CPU 2}}$	A78	d	26
+V TERM	A91	E	5	$\overline{\text{CPU 10}}$	A79	e	27
RETURN	A92	F	6	$\overline{\text{CPU 13}}$	A81	f	28
INACTIVE	A61	H	7	$\overline{\text{CPU 7}}$	A83	h	29
GND	A2	J	8	$\overline{\text{CPU 3}}$	A84	j	30
$\overline{\text{CPU STROBE}}$	A49	K	9	$\overline{\text{CPU 15}}$	A85	k	31
GND	A99	L	10	$\overline{\text{CPU 11}}$	A86	l	32
$\overline{\text{CPU PHASE}}$	A47	M	11	$\overline{\text{CPU 14}}$	A88	m	33
GND	A100	N	12	$\overline{\text{S-CPU 0}}$	B11	p	35
SPARE	A63	P	13	$\overline{\text{S-CPU 3}}$	B13	r	36
REQP*	A59	R	14	$\overline{\text{S-CPU 1}}$	B15	s	37
REQP OUT**	A57	R	14	$\overline{\text{S-CPU 2}}$	B23	t	38
GND	B1	S	15	$\overline{\text{S-CPU 15}}$	B25	u	39
GND	B2	T	16	$\overline{\text{S-CPU 12}}$	B27	v	40
$\overline{\text{CPU 12}}$	A65	U	17	$\overline{\text{S-CPU 13}}$	B34	w	41
$\overline{\text{CPU 0}}$	A67	V	18	$\overline{\text{S-CPU 6}}$	B36	x	42
$\overline{\text{CPU 4}}$	A69	W	19	$\overline{\text{S-CPU 7}}$	B38	y	43
$\overline{\text{CPU 8}}$	A71	X	20	$\overline{\text{S-CPU 14}}$	B40	z	44
$\overline{\text{CPU 9}}$	A73	Y	21	GND	B48	AA	45
$\overline{\text{CPU 5}}$	A75	Z	22	$\overline{\text{S-CPU 4}}$	B52	AB	46
$\overline{\text{CPU 6}}$	A76	a	23	$\overline{\text{S-CPU 5}}$	B54	AC	47
* IN port only ** OUT port only. @1 = Edge Connector @3 = Socket Connector				GND	B50	AD	48
				GND	B99	AF	50

3.3 MCA OPERATION OVERVIEW

The PCBs, in the MCA subsystem, exchange data over the communications bus. Although the external connectors of each PCB are labeled as IN ports or OUT ports, signals travel in both directions between boards. To transmit data, the MCA board must have both I/O bus and communications bus priority. Note that within any MCA board, the receiver has priority over the transmitter.

3.3.1 I/O Bus Priority - I/O bus priority is determined by the proximity to the CPU board with the nearest board having highest priority and the farthest board having the lowest.

3.3.2 Communications Bus Priority - The OUT port of one MCA board is connected to the IN port of the MCA board with the next highest priority. In the MCA subsystem the leftmost board with the next highest priority has one external cable connected to the OUT port and a terminator connected to the IN port. The rightmost board with the lowest priority has one external cable connected to the IN port, and a terminator connected to the OUT port (see Figure 3-2). Priority advances board by board from highest to lowest, and then cycles back to the highest board until a request for service is found. When the board is finished, priority steps down to the next lower board, completing the cycle.

3.3.3 MCA Data Transfer - The following flow chart (Figure 3-3) shows how data is transferred over the communications bus, from one CPU to another.

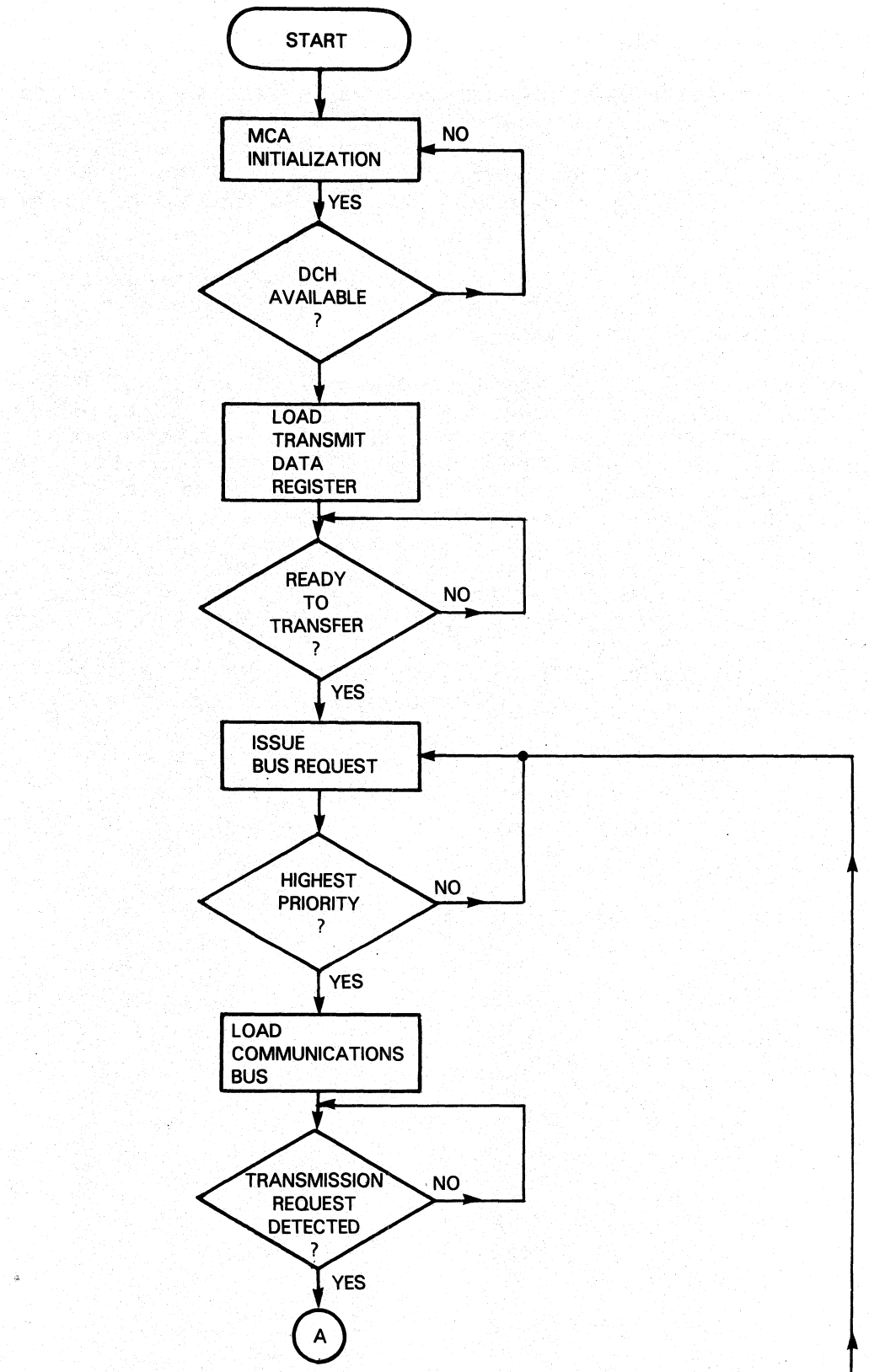

Figure 3-2. Data Transfer Flow Chart (Sheet 1 of 3)

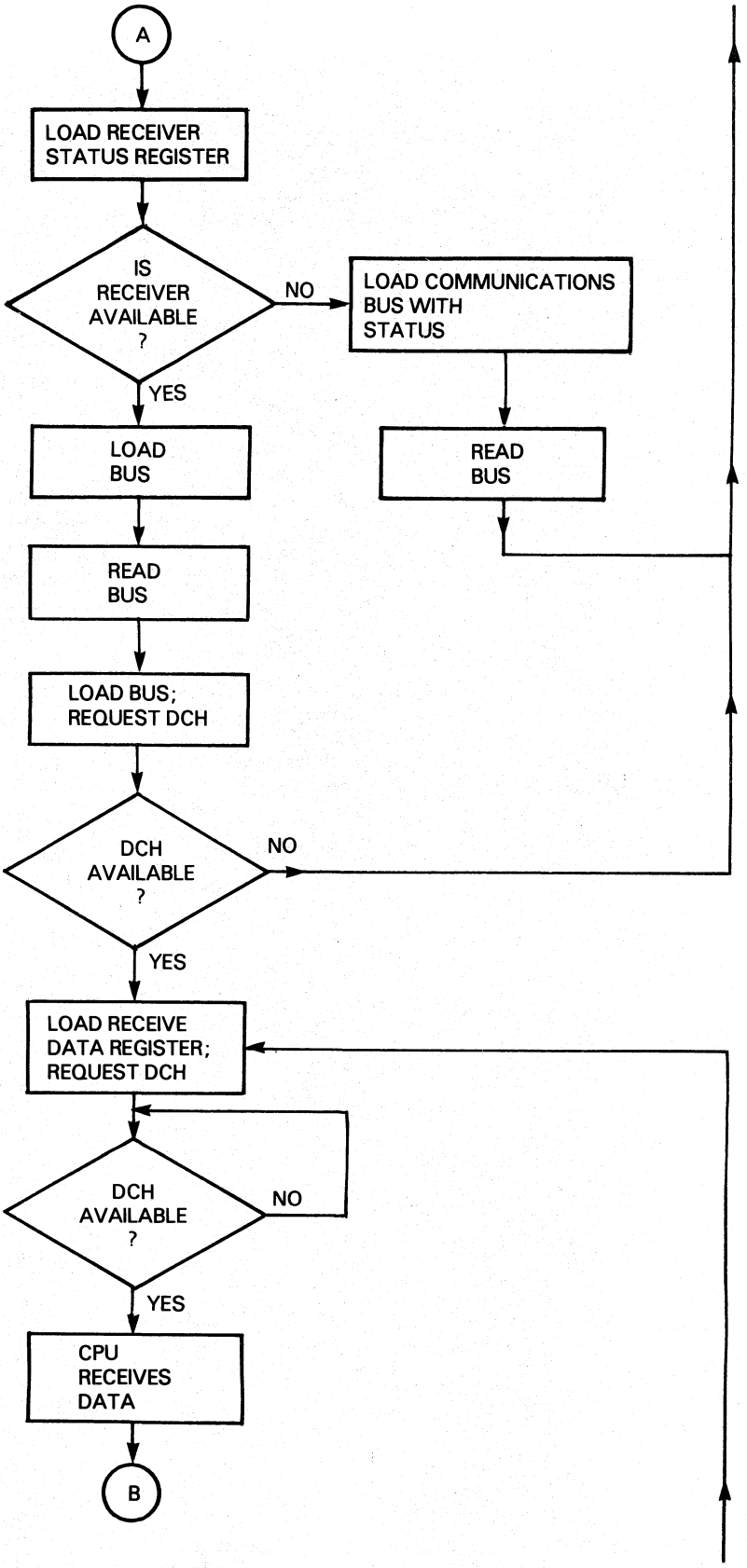

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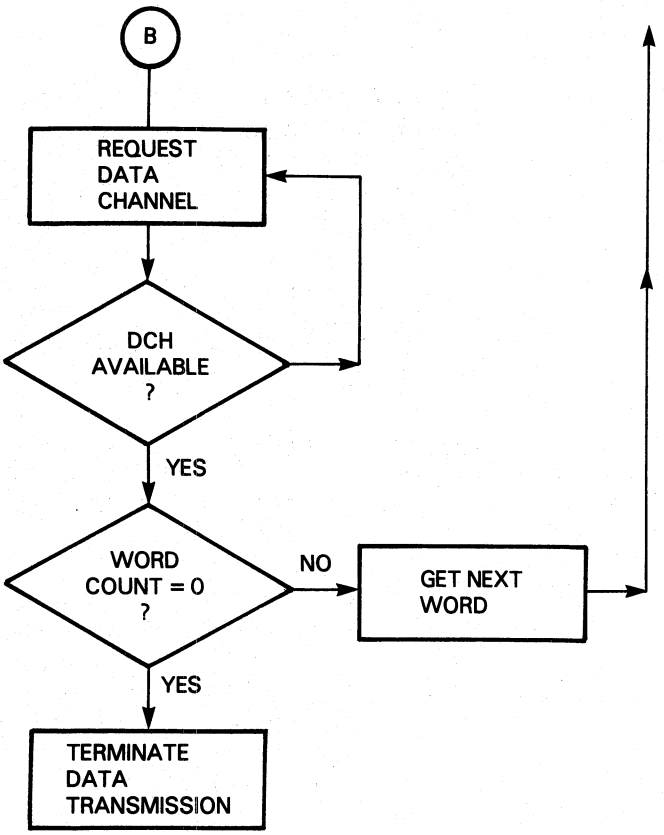
Figure 3-2. Data Transfer Flow Chart (Sheet 2 of 3)



FS-08357 (3 of 3)

Figure 3-2. Data Transfer Flow Chart (Sheet 3 of 3)

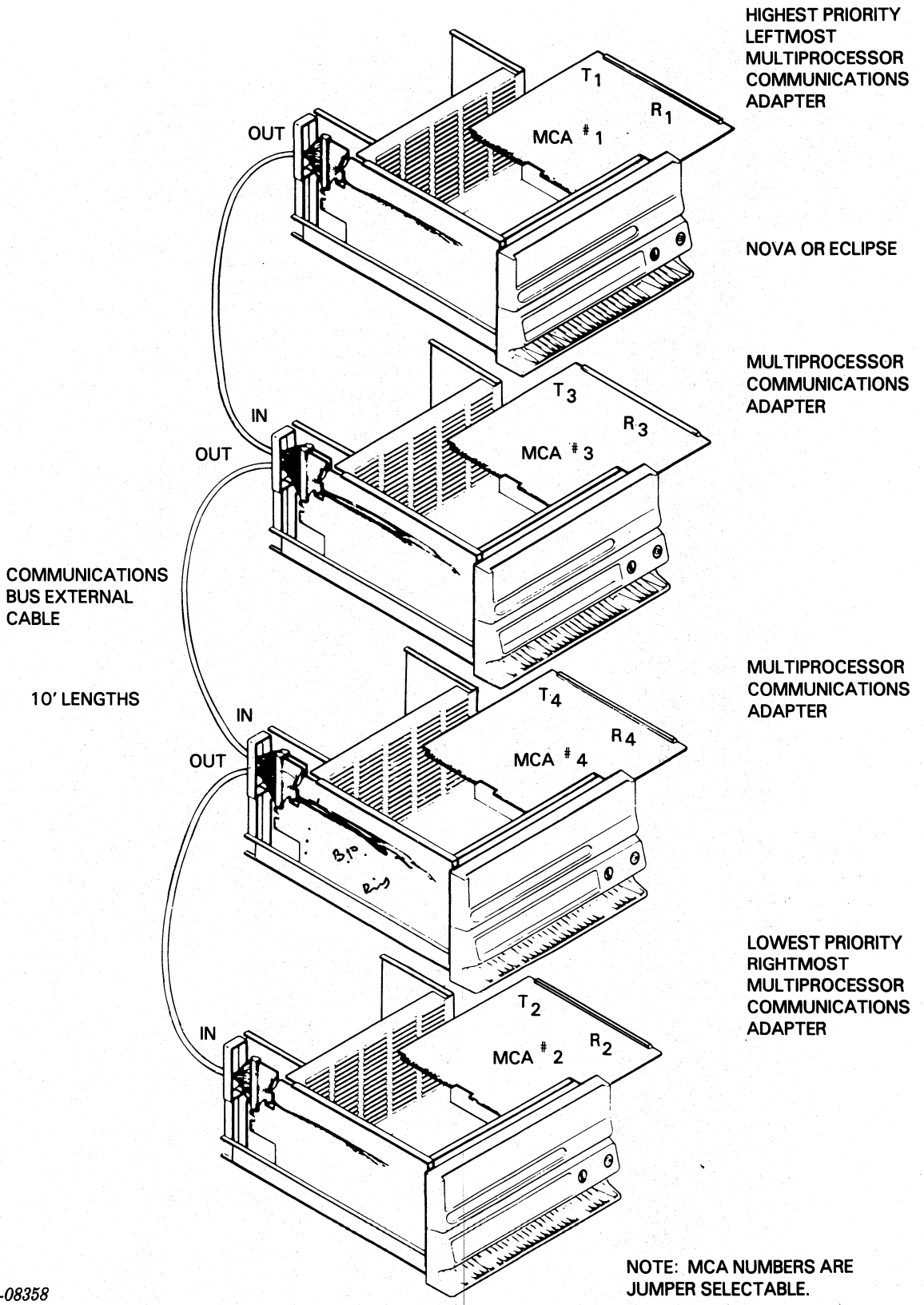


Figure 3-3. MCA Method of Bus Priority

SECTION 4

FAULT DIAGNOSIS

4.1 DIAGNOSTIC PROGRAMS AND LISTINGS

The diagnostic programs and listings used to test the MCA subsystem are listed in Table 4-1.

Table 4-1. MCA Diagnostic Programs and Listings

DGC PART NO.	DESCRIPTION
096-000034	MCA RELI, Listing
096-000397	MCA 4206, Listing

4.2 SPECIAL TOOLS AND EQUIPMENT

Proper diagnostic troubleshooting requires the use of either of three MCA terminators: Cannon (DGC P/N 005-007067), Edge (DGC P/N 005-007072), or SubD (DGC P/N 005-020329). The MCA 4206 diagnostic program is run with a terminator on either the IN port or the OUT port. The MCA RELI diagnostic program is run with a terminator on the IN port of the leftmost MCA, and a terminator on the OUT port of the rightmost MCA.

4-3 MCA 4206: 096-000397

MULTIPROCESSOR COMMUNICATIONS ADAPTER 4206 DIAGNOSTIC

System Requirements: NOVA/ECLIPSE FAMILY CPU; 4K WORDS OF MEMORY (MINIMUM); TERMINATOR P/N 005-007072; OPERATOR'S CONSOLE

Estimated Program Run Time: 1st pass = 2 seconds; 2nd pass = 3 minutes

The MCA 4206 diagnostic is a maintenance program that tests and aids in diagnosing problems in a single MCA PCB. The program runs with the MCA bus disconnected. Standard device codes for the MCA transmitter/receiver are 6/7; MCA 4206 also supports alternate device codes 46/47.

- RESTRICTIONS AND TESTING NOT PERFORMED

MCA 4206 does not test communication between multiple MCA PCBs in an MCA network. Use diagnostic MCA RELI to test interprocessor communication.

- STARTING ADDRESS OR TEST IDENTIFICATION

200 - auto run

- UNIQUE SWITCHES AND CONTROL CODES

The switch settings in MCA 4206 are the standard DTOS switch settings except for the following:

BIT	SET TO	FUNCTION
7	1	Causes the CPU to halt, allowing entry of a different device code from the switch register as follows: AC0 contains the old transmitter code, AC1 contains the new transmitter code.

- OPERATING PROCEDURE

1. On each Model 4206 MCA PCB to be tested, insert the jumpers to select the appropriate device code (refer to Figure 4-1 for jumper locations):

DEVICE CODE 6/7 (XMT/RCV) (PRIMARY)

IN = W1
OUT = W2, W17

DEVICE CODE 46/47 (XMT/RCV) (SECONDARY)

IN = W2, W17
OUT = W1

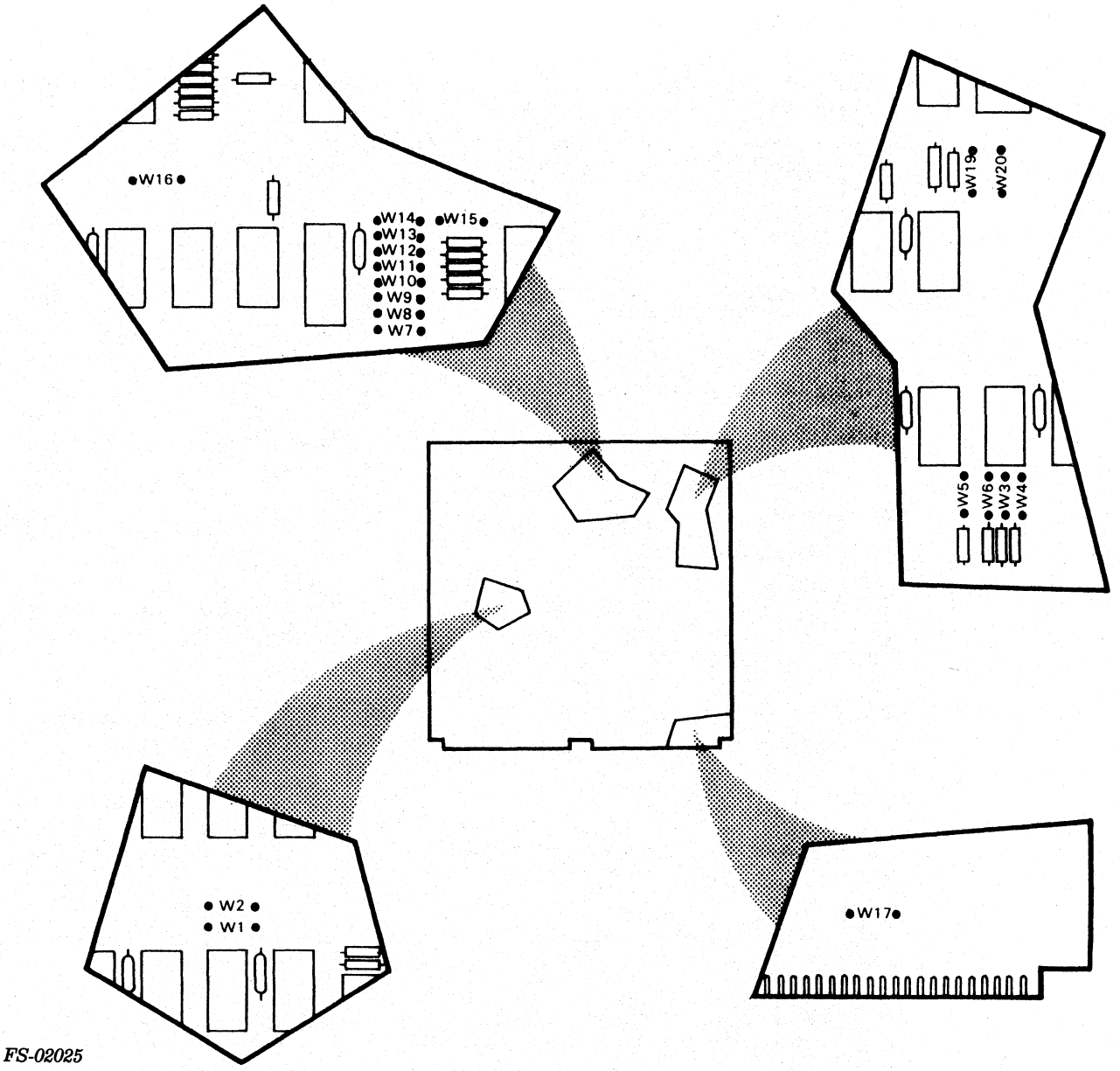


Figure 4-1. Jumper Locations On Model 4206 MCA PCB

2. Note whether the MCA PCB is set up for "normal" or "fast" mode of operation. Write down whether jumper W15 is in ("normal") or out ("fast").

   JUMPERING FOR NORMAL MODE OPERATION

   IN = W8, W10, W12, W14, W15
   OUT = W7, W9, W11, W13

   JUMPERING FOR FAST MODE OPERATION

   IN = W7, W9, W11, W13
   OUT = W8, W10, W12, W14, W15

3. Make sure that jumper W16 is out (jumper W16 generates timing signals).

4. Insert the MCA PCB to be tested into its appropriate slot in the processor.

5. Disconnect the external MCA bus cable (refer to Figure 4-2 for cabling diagram and information regarding the "left-most" computer in an MCA network).

6. Attach the terminator (DGC P/N 005-007072) to the external cable connector.

7. Turn on the power.

8. If jumper W15 is IN ("normal" mode of operation), deposit "1" at location 150.

9. Load the diagnostic MCA 4206 using standard DTOS procedures (refer to Section 2.0).

10. MCA 4206 starts automatically at starting address 200 with the message:

    SET DATA SWITCHES, HIT CONTINUE

    Set the console data switches to 000000, press CONTINUE.

11. Press RESET and START at location 200.

The program is now running. Allow MCA 4206 to run until two PASS messages have printed. The first PASS message prints after approximately two seconds, the second PASS message appears after approximately three minutes.

12. On loading, the transmitter has a device code of 6; the receiver has a device code of 7. To change device codes to alternate values, do the following:

    Start MCA 4206 at starting address 200.

    The program will halt and ask the operator to set the data switches.

    Enter the old transmitter code into AC0.

    Enter the new transmitter code into AC1.

    Put console data switch 7 to "1".

    Press CONTINUE. This device code routine changes all of the transmitter I/O instructions to the new transmitter device code. Additionally, all of the receiver I/O instructions are changed to the transmitter code + 1.

- ERROR INDICATIONS

  If the program detects an error, it halts at location ERR1 + 1. AC3 contains the location of the error + 1. Examine the listing to determine if other accumulator contents are relevant. Switch settings may be changed when the program halts.

- ODT AND COMMAND STRING - MCA 4206 does not include either the standard DTOS ODT utility or the Command String Interpreter.

The MCA bus is time-division multiplexed among MCAs. The priority on the bus proceeds from the leftmost CPU to the rightmost CPU along the MCA bus. If, for example, (Figure 4-2) MCA #1 has the bus, MCA #3 has next priority. However, assuming MCA #3 does not need the bus and MCA #4 does, MCA #4 will get the bus. MCA #3 will not have an opportunity to get the MCA bus again until MCA #2 and MCA #1 have had opportunity to get the bus.

A further description of the theory of operation of the MCA can be found in technical reference manual 014-000072.

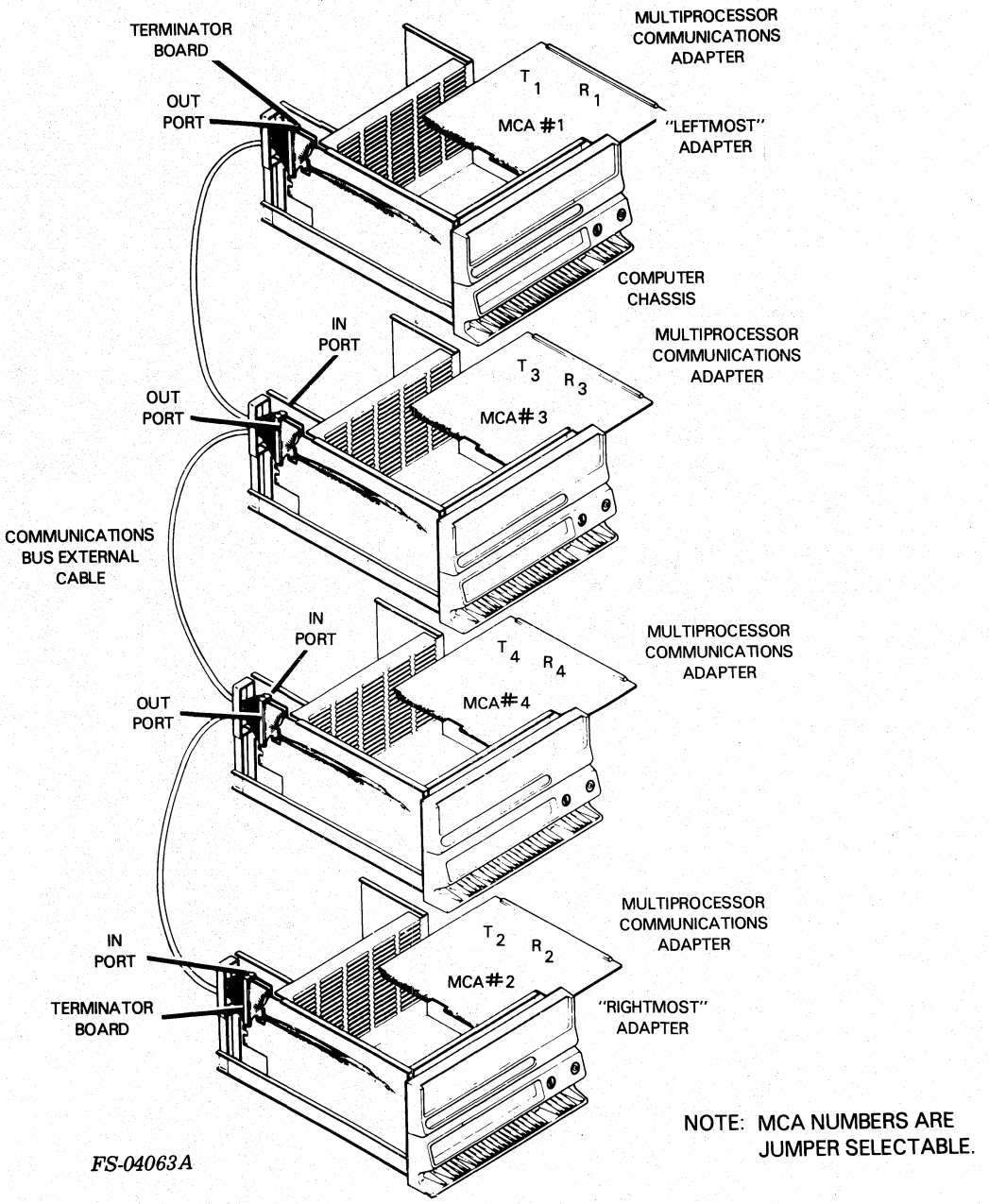


Figure 4-2. Model 4206 MCA Network Cabling and Terminator Placement

4.4 MCA RELI, 096-000034

MULTIPROCESSOR COMMUNICATIONS ADAPTER RELIABILITY	
System Requirements:	NOVA/ECLIPSE-FAMILY CPU; 4K WORDS OF MEMORY (MINIMUM) FOR EACH CPU; OPERATOR'S CONSOLE ("master" processor must have console; console is optional on "slave" processors)
Estimated Program Run Time:	DEPENDENT ON NUMBER OF CPU'S BEING TESTED

The diagnostic MCA RELI is a maintenance program designed to assure reliable simultaneous operation of from one to fifteen Model 4038 or 4206 MCA PCBs interconnected to a like number of NOVA/ECLIPSE computers. MCA RELI supports both primary device code networks (device code 6/7) and seccondary device code networks (device code 46/47).

The three modes of operation for this program are:

- RANDOM EXERCISE MODE

  In the random exercise mode, psuedo-random length blocks of pseudo-random data are sent randomly from each computer to all other computers in the MCA network.

- OPERATOR SELECTABLE WORD COUNT MODE

  The operator may select a word count of from 1 to 2000 words of random data to send between computers in the operator selectable word count mode.

- OPERATOR SELECTABLE DATA

  In the operator selectable data mode, the word count is forced to 1 and the operator may select any data pattern to send between computers.

While running the diagnostic, the user will be performing three different tests: 1) an automatic program load test, 2) a power down test, 3) and an interprocessor test. MCA RELI supports both a primary and a secondary network of MCA PCBs. The standard device code for the primary network is 6, the standard secondary device code is 46.

The program selects, at random, a receiver to which to transmit. It also selects a random location above the program as the transmitter buffer (the length of the buffer is a random selection, from 2 to 2000 words). The length of the buffer - 1 is used to compute the first number to be placed in the buffer. The first number in the buffer is used to compute the second, and so on. These "pseudo-random values are computed by the subroutine RAND, and each number is based on the previous number. Note that the first number is not the word count - 1, but the output of the random number generator when the word count - 1 is used as the base.

The transmitter begins transmission. It waits for one of three states: DONE, transmitter time-out, or neither of the first two states and a time lapse of 100 milliseconds. If DONE occurs, the program returns to its pseudo-random number generation. If a transmitter time-out occurs, the program restarts transmission, theorizing that the receiver was tied up with printouts. The program tolerates only 1024 of these (between 10 seconds and two minutes) before it prints out an error message and returns to its pseudo-random number generation. If the program finds neither a DONE or a transmitter time-out and more than 100 milliseconds elapse, it prints a message indicating the failure of the MCAs time-out logic, then goes back to its pseudo-random number generation.

After sending a block of information to a receiver, the transmitter will not send any more until a one-word acknowledgement block comes back from that MCA.

The PASS message types only if 512 blocks are sent and acknowledged from each MCA whose octal ID code has been entered, and if no errors are detected.

If an error is detected either in the transmitter itself or in the linked receiver (as reported in the acknowledgement word), then all future transmissions will consist of the same data from the same length buffer that caused the error. The transmitter buffer is frozen. The core location is also frozen, but not always in the same location as when the error occurred.

Each MCA receiver is always open for reception from any transmitter. When an incoming data block is complete, an interrupt occurs and the data is verified before the main program resumes. After the main program resumes, a one-word acknowledgement is sent off to the transmitter if it is on the list of typed in codes. Otherwise, no acknowledgement occurs. This lack of acknowledgement curtails any further communication from that MCA. The acknowledgement word contains the number of words received - 1 in bits 6 to 15, the occurrence of data errors in bit 0, and the occurrence of receiver status errors in bit 1. One word blocks are never acknowledged.

If the transmitter "talks" to its own receiver, no acknowledgement word is sent back since both the transmitter program and receiver program have complete access to each other.

The data block is checked for errors by verifying that each word received equals the number produced by the subroutine RAND when the word before it is used as the base. The first base value is simply the block length - 1. Even if only two data words are correct, the entire buffer can be reconstructed and the correct length computed. This can also be done if the length is correct and all of the data is bad. If the length is wrong and two good words do not exist, however, the printout will be meaningless.

- RESTRICTIONS AND TESTING NOT PERFORMED

Prior to running this diagnostic, the operator may run the diagnostic program MCA 4206.

The following configuration rules apply:

- In the NORMAL mode of operation, up to 15 NOVA and/or ECLIPSE processors may be interconnected with one MCA for each processor.
- In the FAST mode of operation, up to 4 NOVA and/or ECLIPSE processors may be interconnected with one MCA for each processor.
- An MCA PCB requires one slot per processor.
- In the normal mode of operation, the distance between the "leftmost" CPU and the next CPU is 20 feet, maximum (a "leftmost" CPU is the CPU which contains the MCA board with no MCA connected to its "in" port). This MCA also has jumper W16 OUT which designates it as the "leftmost" CPU.
- MCAs other than the first two may be distributed in any manner along the 140 foot MCA bus length.
- The maximum total MCA bus length is 140 feet for NORMAL mode operation, and 40 feet for FAST mode operation.
- Models 4038 and 4206 MCA PCBs cannot be intermixed on the same MCA bus.
- Both Models 4206 and 4038 MCA PCBs are data channel devices.
- MCA PCBs other than the "leftmost" and "rightmost" in a configuration must have their terminators removed (a "rightmost" CPU is the CPU which contains the MCA board with no MCA connected to its "out" port).

- OPTIONAL EQUIPMENT

  If there are fewer TTY/DASHER devices than processors, a TTY/DASHER device can be connected to each processor one at a time for input and/or output. Always keep console data switch 3 set to "1" for any processor which has an unconnected TTY/DASHER. Those processors will signal any need for such a device with a blinking CARRY light.

- STARTING ADDRESS OR TEST IDENTIFICATION

  2 (Starting location 4 is also used during the automatic program load test).

- UNIQUE SWITCHES AND CONTROL CODES

  Setting console data switch 0 to "1" indicates one or more "slave" processors either are not configured with a TTY/DASHER device, or that the device is not activated. Switch 0 set to "1" overrides the effects of switch 2 set to "1".

  Setting console data switch 3 to "1" stops the program before printouts occur. Setting console data switch 3 to "0" allows printouts to occur.

  Any time after the message "TYPE OCTAL CODES", the operator may type a one- or two-digit octal code followed by a carriage return. This adds the code of some MCA to the list and communication will start to that MCA.

  Typing a minus sign (-) and a one- or two-digit code followed by a carriage return will stop communication to that MCA.

  Typing an octal number between 1 and 2000 followed by the letter "B" and a carriage return forces the block length of the transmission to the value typed. The word "CYCLE" will be printed. Note, that one word blocks are never acknowledged. If the user types "1B", operation proceeds as normal, but the success message "CYCLE" is not printed. Normal status and data checks are made.

  Typing an octal number between 0 and 177777 followed by the letter "D" forces the block length of transmissions to one word. The value of the single data word is the value typed. This mode of operation is intended for situations where a particular data pattern is failing or one bit is being dropped. The receiver continuously indicates an error condition which shows the transmitted word as 033031 and the received word as the data word selected and typed in. Note, that this is the normal operation in this mode.

  Typing CTRL R (^R) interrupts the program and restarts it at location 2.

- OPERATING PROCEDURE

1. Make sure proper jumpers are inserted to select the proper device code and non-zero MCA octal ID code. Each MCA PCB in a given network must have a different MCA octal ID code. Refer to Figure 4-1 for jumper locations.

NOTE

Refer to Figure 4-2 for information for locating the "leftmost" CPU in an MCA network.

2. Insert jumpers on the MCA PCB in the network's leftmost CPU to select either the FAST or NORMAL operating mode (refer to the diagnostic restrictions portion of this section). The settings of these jumpers are irrelevant on MCA PCBs other than the MCA PCB in the leftmost CPU.

NOTE

For ECLIPSE S250, ECLIPSE C350, and ECLIPSE M600 systems, select only the NORMAL mode of operation.

3. On Model 4206 MCA networks, remove jumper W16 from the MCA PCB in the leftmost CPU. On all other Model 4206 MCA PCBs in the network, insert jumper W16.

4. Install a terminator (DGC P/N 005-007072) on the IN port of the leftmost MCA PCB, and on the OUT port of the rightmost MCA PCB.

5. With the power off, install each MCA PCB into its processor.

6. Interconnect the MCA PCBs with the proper cables (refer to Figure 4-2).

7. Power-up the system.

8. Select one processor to be the "master" processor. No particular processor must be used; the term only distinguishes between the MCA PCB transmitting the downline load (master) and the MCA PCBs receiving the load (slaves).

9. At the "master" processor, load MCA RELI.

NOTE

If a CPU with a secondary MCA is selected as the "master" CPU, insert the following patch to execute the downline load:

LOCATION	FROM	TO
3560	61206	61246
3562	62006	62046
3563	73106	73146
3564	63606	63646

10. At each of the "slave" processors, do the following:

Press RESET.

Set the console data switches to 100007(octal), and press PROGRAM LOAD. This will initiate a data channel load through the receivers of the primary MCA PCBs.

NOTE

For NOVA 4 and ECLIPSE S/140 (no front panel switches), set SWREG bit 11 (A) to a "1".

For secondary MCA PCBs, set the console data switches to 100047(octal), and press PROGRAM LOAD.

For any "slave" processors that are not equipped with the program load feature, enter the following routine and START at location 3605:

LOCATION	DATA	
3605	102400	
3606	061207	(primary)
	or	
	061247	(secondary)
3607	062107	(primary)
	or	
	062147	(secondary)
3610	000400	

11. Start the "master" processor at starting address 4. It will halt.

12. Set all console data switches of the "master" processor to "0", except for the console data switches which correspond to the MCA octal ID codes of each of the MCA PCBs that will be receiving the downline load. For example, console data switch 1 = MCA octal code 1, console data switch 2 = MCA octal code 2, console data switch 15 = MCA octal ID code 17, etc.

13. At the "master" processor, press CONTINUE. The "slave" processors that contain the MCA PCBs specified by the "master" processor's console data switches receives the program, then halts. When the downline load has completed, the "master" processor also halts.

14. Verify the halt at each of the "slave" processors. Also, verify that each of the "slave" processors loaded the program. Each "slave" processor must stop at location 3602 (good data). Location 3604 contains any bad data.

15. If any "slave" processor did not correctly load the program, return to the "master" processor and set all of the console data switches to "0" except the console data switch that corresponds to the MCA octal ID code of the failing "slave" processor. At the "master" processor, press CONTINUE. The "slave" processor should receive the downline load and halt at location 3602(octal).

16. When each of the "slave" processors has successfully loaded the program, set the console data switches of the "master" processor to 000002(octal).

17. If the "slave" processors have no TTY/DASHER, set console data switch 0 on the "master" processor to "1". If all of the "slave" processors have TTY/DASHER attached, set console data switch 0 to "0".

18. At the "master" processor, press START.

19. For TTY/DASHER configured processors the program prints:

CORE, MCA #: XXXX Y

where XXXX = last available memory location + 1
Y = MCA octal ID code

TYPE OCTAL CODES

Type: XXXX) where XXXX is the same octal ID code that shows on the printout. This will initiate operation in the loopback mode. Each MCA will transmit to its own receiver.

For processors with no TTY/DASHER:

"Slave" processors with no TTY/DASHER will halt to allow entry of MCA octal ID code. When this halt occurs, AC0 contains the last memory location + 1, and AC1 contains that "slave" processor's MCA octal ID code. Set the console data switches of each of these "slave" processors to equal its own MCA octal ID code (located in AC1). Press CONTINUE.

20. For TTY/DASHER configured processors:

    Allow MCA RELI to run until two PASS messages print out.

    For processors with no TTY/DASHER:

    By the time the "master" processor has typed out two PASS messages, the "slave" processors should also have completed two passes. The location tagged in XPCNT may be examined to check the pass count.

21. Perform the power off test. With MCA RELI running, select any processor and turn its power off. Observe that all other processors in the MCA network continue to run. Turn the power back on, start the program at starting address 2, and re-enter the processor's own MCA octal ID code for loopback operation. Note, if a processor with SC memory is powered down, the program must be reloaded. A downline load may be performed to load the program.

22. Perform the power off test described above for each processor in the MCA network.

23. Perform the interprocessor test. Stop each processor.

For TTY/DASHER configured processors:

Restart each processor at starting address 2. The program will type:

```
CORE, MCA #: XXXX      Y
TYPE OCTAL CODES
```

Type: the MCA octal ID codes of each of the other MCAs in the network. Separate each of the MCA octal ID codes by a comma, then type a carriage return.

EXAMPLE: In a six processor MCA network with MCA octal ID codes 1, 2, 3, 4, 5, and 6, make the entries as follows:

```
At # 1: 2,3,4,5,6
   # 2: 1,3,4,5,6
   # 3: 1,2,4,5,6
   # 4: 1,2,3,5,6
   # 5: 1,2,3,4,6
   # 6: 1,2,3,4,5
```

NOTE

Once a single entry is made, do not press RESET on any processor in the MCA network. If an incorrect entry, is made, type in random entries until the program responds with "?", then make the entries again.

Once the first entry is made selecting MCA octal ID codes, all entries must be made within 75 seconds or timeouts will occur.

For processors with no TTY/DASHER:

Start each processor at starting address 2, with console data switch 0 set to "1". The processor halts to allow for manual entry of the MCA octal ID codes of each of the other MCAs in the network. For example, console data switches 1, 3, 5, and 15 set to "1" select transmission to MCA octal ID codes 1, 3, 5, and 17.

After the console data switches have been set, press CONTINUE.

24. The test is now running. The time interval between passes depends on the type of processor that contains the left-most MCA and on the total number of MCAs in the network. For example, in a network where the left-most MCA is in an ECLIPSE system and where there is a total of three MCAs in the network, there will be an interval of about 10 seconds between passes. For each additional processor (MCA) added to this network, expect the time interval to increase by about five seconds.

    For TTY/DASHER configured processors:

    When all of the processors in the MCA network are transmitting to all other processors in the network, allow the test to run until at least two PASS messages are printed.

    For processors with no TTY/DASHER:

    By the time the "master" processor has typed PASS more than twice, each "slave" processor has probably completed two passes. To check the pass count of any "slave", examine the location tagged XPCNT.

After testing is completed, remove the terminator and return the system to its original configuration.

- ERROR INDICATIONS

For processors with a TTY/DASHER device, an error printout is the first indication of an error. If there is no TTY/DASHER device, the program proceeds through the normal error path, but instead of generating an error printout, the program issues a halt. The user may repeat the failing sequence by pressing CONTINUE.

Any interpretation of error printouts should be done with these considerations:

- Following a successful transmit sequence:

  XMITTER DIA = Address of the next word to be transmitted
  XMITTER DIB = 2s complement of the number of words remaining to be transferred

- Following a successful receive sequence:

  REC DIA = Address of the next word to be stored
  REC DIB = 2s complement of the number of words remaining to be received

- For both a receive and transmit sequence:

  DIB should = 0, indicating that all words were in fact transmitted/received
  DIA should = Buffer address + 2s complement of the block length

  For example: Buffer address = 2000, Block length = 17600, DIA address should = 5000.

- In a case where the entire block is not transmitted/received, the address read by the DIA should equal the buffer address + the 2s complement of the block length + the word count read by the DIB.

  For example: Buffer address = 3000, Block length = 176000, DIB read 177777. Address read should equal 3000 + 2000 + (-1) = 4777.

- In a case where a status error occurs, the expected status and the actual status are provided.

- Data or word count (block length) errors are itemized at the receiving end of a bad transmission, unless no lock-on was established. The same data block will be transmitted repeatedly thereafter.

  For example:

	RCVD: 4	SENT: 1
WC-1 =	000244	000243
1	000000	031332
2	031332	125440
3	125440	134507
4	134507	126717

  If the receiver equals the transmitter, the transmitter buffer address - 1 is also printed. The first location of the transmitter buffer is the printed address + 1 (7315).

  Next, the actual word count received - 1 is printed, then the computer word count transmitted - 1.

  The numbers at the far left of the sample are the offsets from the base address of the buffer. For example, 1 represents the first location in the buffer.

In the sample printout on the previous page, note that one more word was received than was transmitted. Following that, the first four nonmatching data words are printed. In the sample, an extra word of zeros was received; all of the subsequent data words are mismatched.

- Data or word count (block length) errors are reported at the transmitting end of a bad transmission. The same data will be transmitted repeatedly thereafter.

NOTE

In PRCVD is the address where WC-1 is stored (word #0).
In PRBUF is the address of the receiver buffer (word #1).
In PXBUF is the address of the transmitter buffer.
BUFL = 2000 the length of both buffers.

- Other failures may result in one of these messages:

```
STATUS ERROR, RCVR 4
ADDRESS   -WD CNT   STATUS
004502    17600     040406
DIA-R     DIB-R     DIC-R
006502    000000    040405

ADDRESS ERROR, RCVR 4
ADDRESS   -WD CNT   STATUS
4502      17600     040406
DIA-R     DIB-R     DIC-R
6506      000000    040406
```

Under ADDRESS are the contents of PRBUF which is the address of the receiver buffer word # 1. Under -WD CNT is the contents of MBUFL which is the length of the MCA word count. Under STATUS is what the status should be. The next two lines present the pertinent receiver registers as read. DIA-R equals the MCA receiver address register, DIB-R equals the MCA receiver word count register, and DIC-R equals the MCA receiver status register.

RECEIVER STATUS REGISTER

```
 R RRR TTT T00 000 11C
```

BITS	
0,1,2,3	RCVR Code
4,5,6,7	Transmitter link
12	Time-out error
13	Lock-on (RCVR is locked to XMTR link)
14	XMTR count done
15	RCVR count done

```
STATUS ERROR,XMTR 4
ADDRESS -WD CNT STATUS
002505  177000  040406
DIA-X   DIB-X   DIC-X
004505  000000  040410

ADDRESS ERROR,XMTR 4
ADDRESS -WD CNT STATUS
2505    177000  040406
DIA-X   DIB-X   DIC-X
2505    000000  040406

WORD COUNT ERROR,XMTR 4
ADDRESS -WD CNT STATUS
2505    177000  040406
DIA-X   DIB-X   DIC-X
4505    177777  040406
```

Under ADDRESS are the contents of ADR, which is the address of the transmitter buffer. Under -WD CNT is the contents of MWC, which is the block length. Under STATUS is what the status should be. The next two lines present the pertinent transmitter registers as read: DIA-X equals the MCA transmitter address register; DIB-X equals the MCA transmitter word count; DIC-X equals the MCA transmitter status register.

TRANSMITTER STATUS REGISTER

```
R RRR TTT T00 000 11C
```

BITS	
0,1,2,3	RCVR link
4,5,6,7	Transmitter link
10	Diagnostic status phase
11	Diagnostic mode
12	Time-out
13	Lock (state of RCVR before last word)
14	XMTR count done
15	RCVR count done

- ODT AND COMMAND STRING INTERPRETER - MCA RELI contains the standard DTOS Octal Debug Tool (ODT). MCA RELI does not contain Command String Interpreter.

SECTION 5

REMOVAL, REPLACEMENT, AND ADJUSTMENT

This section provides procedures for removal, replacement, and adjustment of MCA PCBs, internal cables, and the external communication bus cable.

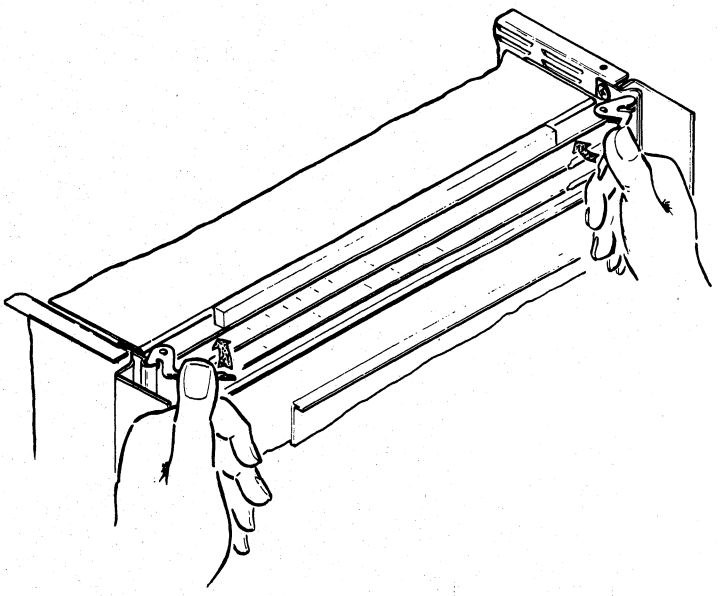
5.1 MCA PCB REMOVAL AND REPLACEMENT

Use the following steps to remove and replace the MCA PCB.

1. Power-down the CPU, and remove the power cord according to the procedure in the appropriate CPU PIP.

2. Accessing the card cage varies according to the CPU being used. Either open the front panel of the cabinet, remove the front panel and EIA shield, if any, or slide the chassis out until the card cage is exposed.

3. Locate and remove the MCA PCB by pulling the ejector tabs, as illustrated in Figure 5-1.



FS-06239

Figure 5-1. PCB Removal

4. Before installing the replacement PCB, match the configuration of the previous PCB by inserting the required jumpers. See Figure 5-2 for jumper locations.

5. Insert the replacement PCB in the same slot from which you remove the previous board.

6. Close up the CPU by either sliding the chassis into the cabinet, closing the cabinet door, or reinstalling the front panel and any EMI shield.

7. Power-up the system according to the appropriate CPU PIP.

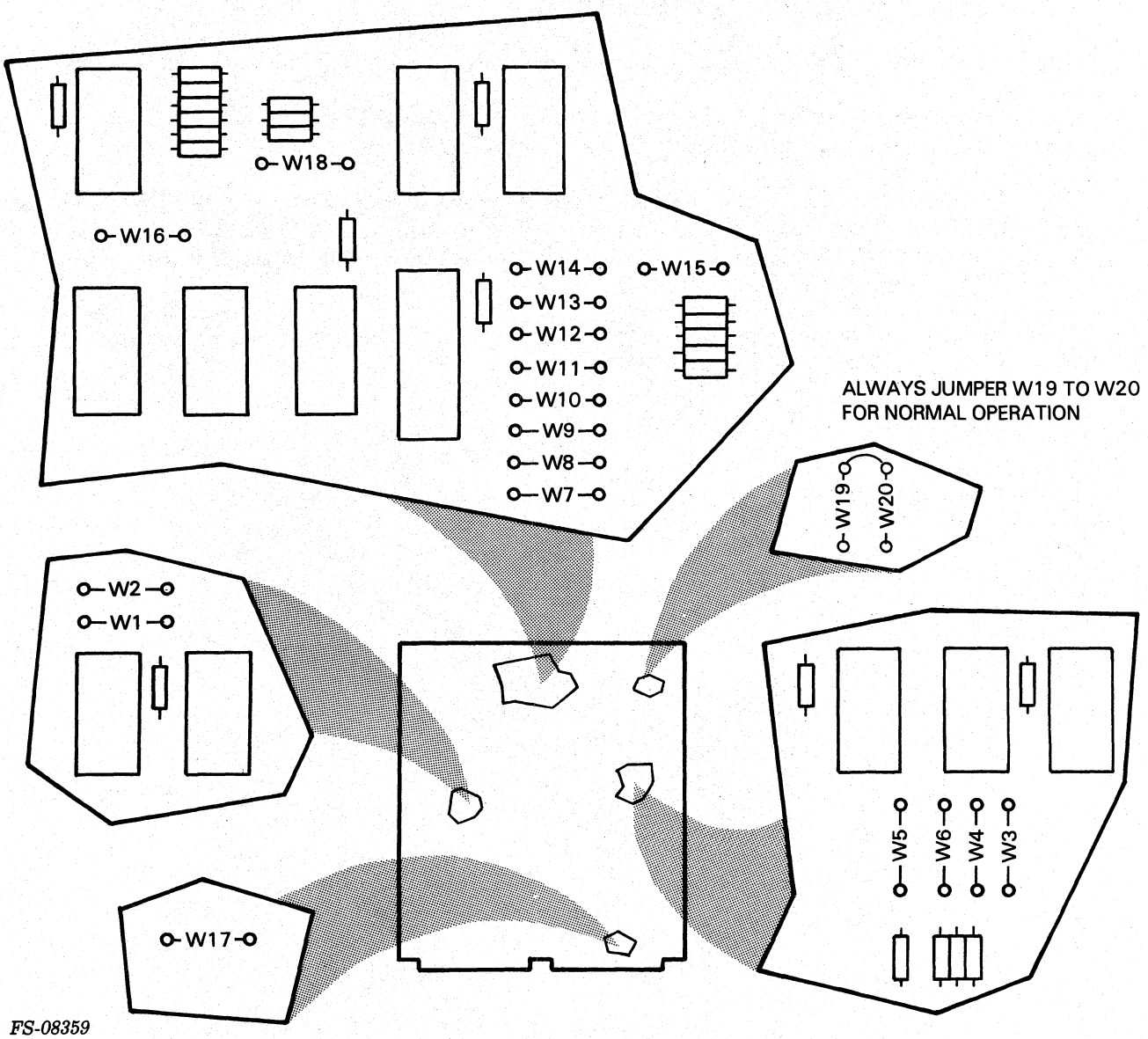


Figure 5-2. Jumper Locations on the MCA PCB

5.2 EXTERNAL CABLE REMOVAL AND REPLACEMENT

Before replacing the external cable (the communications bus), check the new cable's part number against that of the old cable's. Use the following steps to replace the external cable.

1. Power-down the CPUs at each end of the external cable, using the procedure in the appropriate CPU PIP.

2. Working on one CPU at a time, open the cabinet's rear panel to access the cable bulkhead. Locate and remove the external cable by either unscrewing the retaining screws, or clipping the cable tie and pulling the connector loose. Save all hardware for the replacement cable. See Figures 5-3 and 5-4.

3. Attach the connector of the replacement cable to the mating connector of the MCA internal cable. Secure the external cable with a cable tie, or with the two screws just removed.

4. Detach the other end of the old cable from the other CPU, and connect the new cable as per steps 2 and 3, above.

5. Close the rear panel on both cabinets, and power-up each CPU.

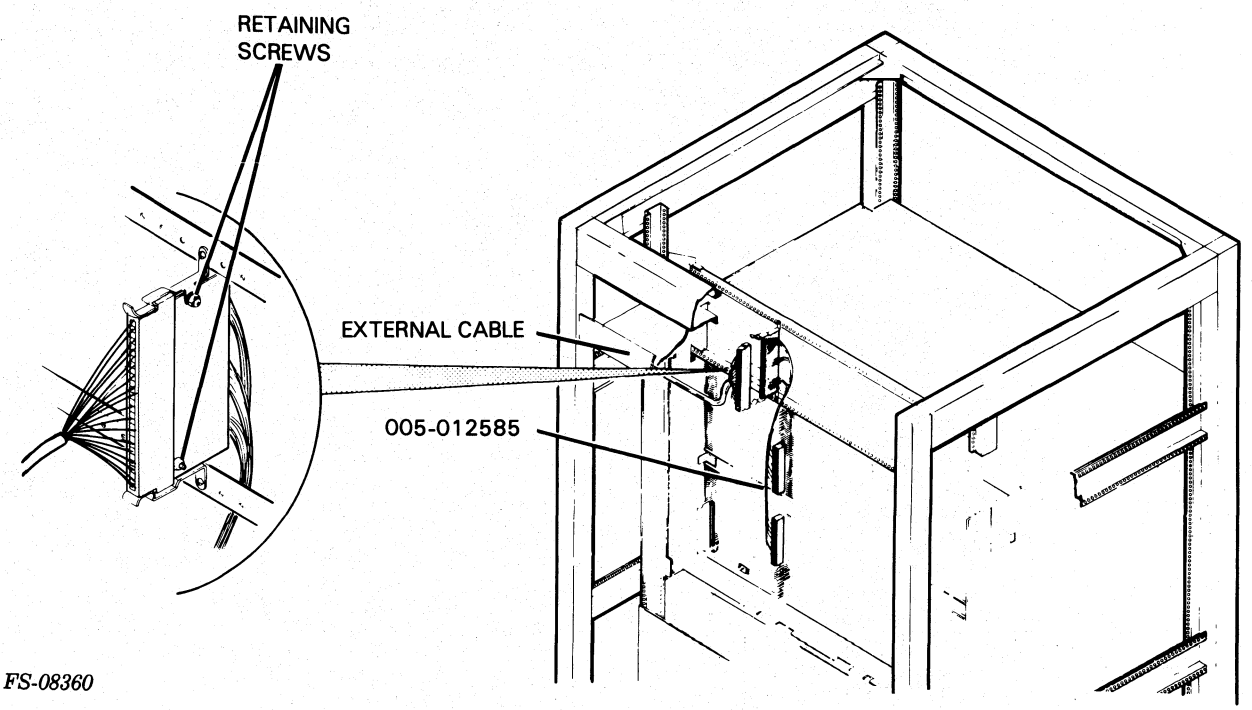


Figure 5-3. External Cabling with Edge Connectors

5.3 INTERNAL CABLE REMOVAL AND REPLACEMENT

Internal cable replacement varies according to the type of CPU being used. The four categories of internal cables are listed below in the order in which they are presented.

1. Back panel plug-on connectors with subD bulkhead connectors for FCC compliant chassis.

2. Back panel plug-on connectors with paddleboard connectors for NOVA 4 computer and ECLIPSE C350, ECLIPSE S240, ECLIPSE S250 and ECLIPSE M600 computers.

3. Wirewrapped back panel with paddleboard connectors for NOVA 2 and NOVA 3 computers, and ECLIPSE C330, ECLIPSE S230, ECLIPSE S130, ECLIPSE C150, ECLIPSE S200, and ECLIPSE C300 computers.

4. Wirewrapped back panel with Cannon connectors for NOVA 1200 and NOVA 800 computers.

Note that a wirewrapped back panel requires two internal cables, one for the OUT port and one for the IN port. See Table 5-1 for internal cable part numbers.

Table 5-1. Internal Cable Part Numbers

CABLE PART NO.	PORT	WIRE RUN LIST	TYPE OF EXTERNAL CONNECTOR	USED ON
005-007062 005-007063	IN OUT	008-000899 008-000900	Cannon	NOVA 1200, NOVA 800, NOVA 830, NOVA 840, NOVA SuperNOVA computers
005-007064 005-007065	IN OUT	008-000901 008-000902	Edge	NOVA 2, NOVA 3, NOVA 820, NOVA 1210, NOVA 1220 computers ECLIPSE AP130, ECLIPSE C300, ECLIPSE C330, ECLIPSE S130, ECLIPSE S150, ECLIPSE S200, ECLIPSE S230 computers

Table 5-1. Internal Cable Part Numbers (Continued)

CABLE PART NO.	PORT	WIRE RUN LIST	TYPE OF EXTERNAL CONNECTOR	USED ON
005-012585	IN & OUT	Push on connector	Paddleboard	Noncompliant versions of NOVA 4, ECLIPSE C350, ECLIPSE M600, ECLIPSE S120,ECLIPSE S140, ECLIPSE S250, ECLIPSE MV/FAMILY computers
005-019484	IN & OUT	Push on connector	SubD	Compliant versions of NOVA 4 and ECLIPSE computers

5.3.1 Back Panel Plug-on Connectors With SubD Bulkhead Connectors - Use the following steps to remove and replace the internal cable.

1. Access the cable bulkhead by opening the rear panel of the cabinet.
2. Unscrew and detach the MCA external cables, or cable and terminator, saving the hardware for reinstallation.
3. Swing the cable bulkhead down and locate the MCA internal cable.
4. Unscrew the subD connectors from the bulkhead, and detach the other end from the backpanel (see Figure 5-5).
5. Connect the backpanel connectors of the internal cable to the back panel, plug the two subD connectors into the cable bulkhead, and secure with the screws previously removed.
6. Swing the cable bulkhead into place and secure.
7. Reconnect the external cables, and any terminator to the internal cables. Secure with the screws removed earlier.
8. Close the rear panel of the cabinet and power-up the system.

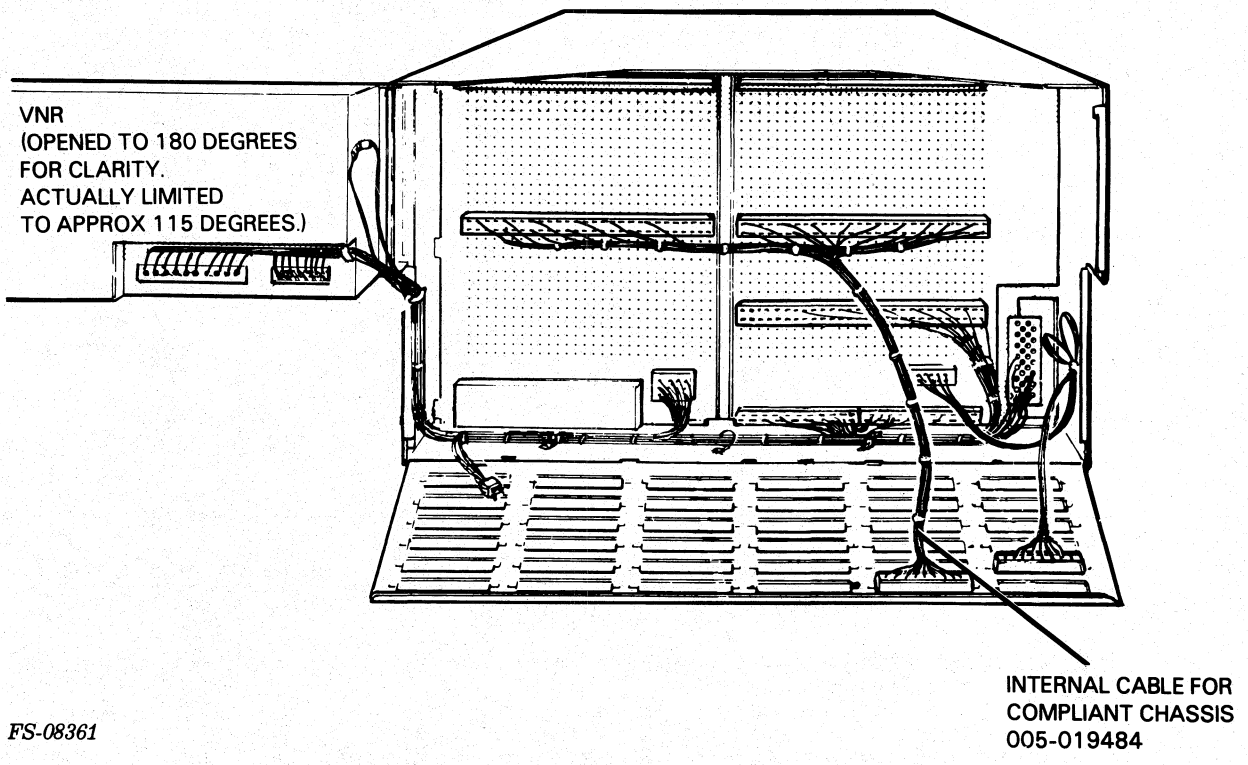


Figure 5-4. Back Panel and EMI Cable Bulkhead

5.3.2 Back Panel Plug-on Connectors with Paddleboard Connectors - Use the following steps to replace the internal cable.

1. Power-down the system according to the instructions in the appropriate CPU PIP.
2. Access the back panel and paddleboard by opening the rear door of the cabinet.
3. Locate and disconnect the MCA external cables, or cable and terminator.
4. Remove the screws which secure the two paddleboard connectors to the chassis frame (see Figures 5-6 and 5-7).
5. Unplug the other end of the internal cable from the back panel.
6. Plug the replacement cable onto the back panel where the previous internal cable was connected.
7. Secure the two paddleboard connectors to the chassis, using the screws and spacers previously removed.

8. Connect the MCA external cables, or cable and terminator, to the paddleboard. Close the rear door of the cabinet.

9. Power-up the system.

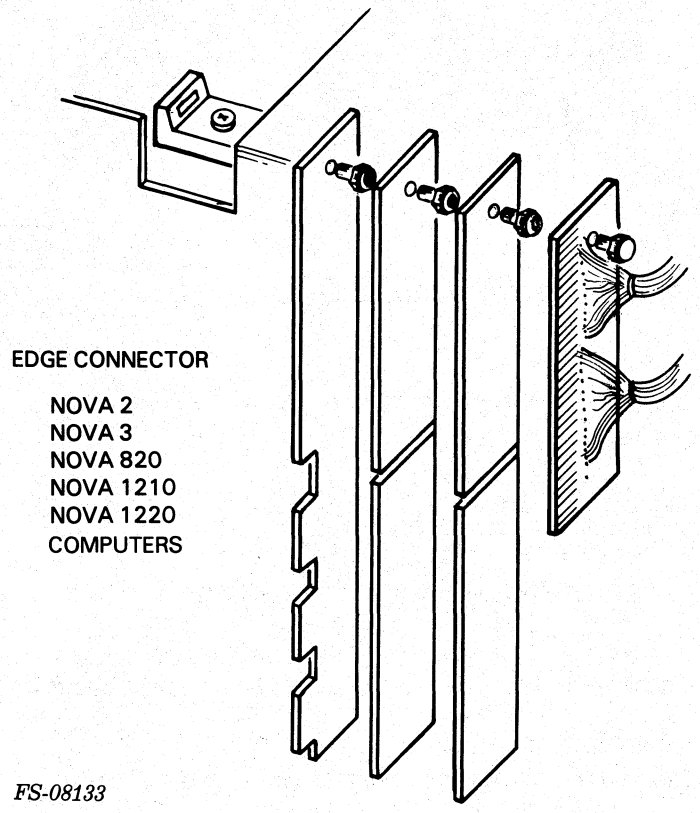


Figure 5-5. Edge Connectors

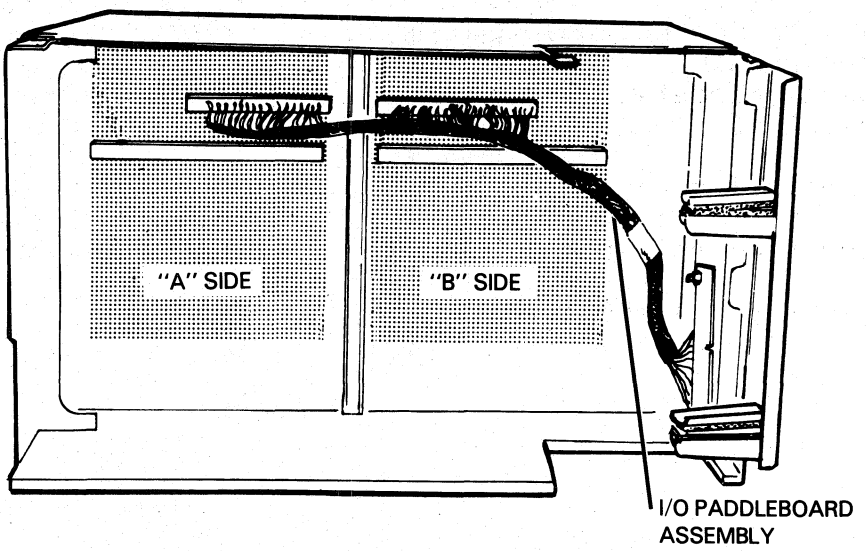


Figure 5-6. Edge Connectors in Side Mounted Paddleboard

5.3.3 Wirewrapped Back Panel with Paddleboard Connectors - Use the following steps to replace the internal cable.

1. Power-down the system using the procedure in the appropriate CPU PIP.

2. Label and remove all external cables and terminators from the CPU.

3. Remove the CPU chassis from the cabinet.

CAUTION

To prevent injury to the FE, at least two people should be present to remove the CPU from its cabinet.

4. Locate the two MCA internal cables which are wirewrapped to the back panel where the MCA PCB is located. Note that there are two cables, one for the IN port and one for the OUT port of the MCA PCB.

5. Using an unwrap tool, remove all the cable wirewraps from the back panel pins of the MCA slot. Be careful not to remove power, ground, or priority wires.

6. Remove the two screws and spacers which secure the two paddleboard connectors to the chassis (see Figure 5-7).

7. Check the new cable's part number against that of the old cable's.

8. Connect the paddleboard connectors to the chassis using the screws and spacers previously removed.

9. Using wirelist 008-000901 for the IN port cable and 008-000902 for the OUT port cable, wirewrap the internal cable to the back panel. Cut the wires leaving enough for a service loop. Use an ohmmeter to verify that the cable has been correctly installed.

10. Reinstall the CPU in the equipment cabinet.

11. Reconnect all external cables and close the cabinet rear panel.

12. Power-up the system.

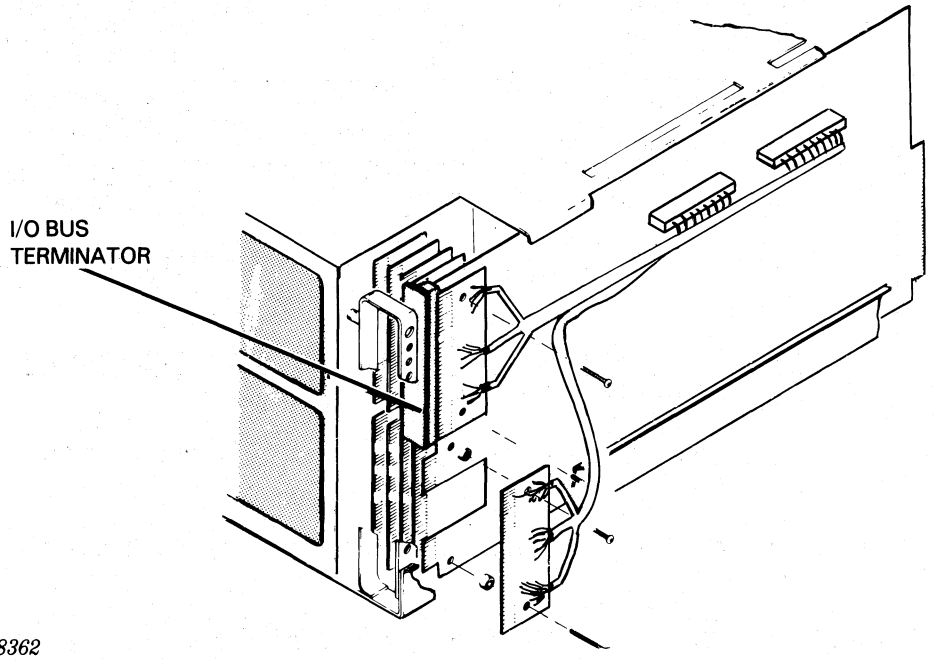


Figure 5-7. Edge Connectors with Wirewrapped Back Panel

5.3.4 Wirewrapped Back Panel with Cannon Connectors - Use the following steps to replace the internal cable.

1. Power-down the system using the procedure in the appropriate CPU PIP.

2. Label and remove all external cables from the CPU.

3. Remove the CPU chassis from the cabinet.

CAUTION

To prevent injury to the FE, at least two people should be present to remove the CPU from its cabinet.

4. Locate the MCA internal cables which are wirewrapped to the back panel where the MCA PCB is located. Note that there are two cables, one for the IN port and one for the OUT port of the MCA PCB.

5. Using an unwrap tool, remove all the cable wirewraps from the back panel pins of the MCA slot. Be careful not to remove power, ground, or priority wires.

6. Remove the two screws that secure the two Cannon connectors to the chassis (see Figure 5-8).

7. Check the new cable's part number against that of the old cable's.

8. Connect the Cannon connectors to the chassis using the screws previously removed.

9. Using wirelist 008-000899 for the IN port cable and 008-000900 for the OUT port cable, wirewrap the internal cable to the back panel. Cut the wires leaving enough for a service loop. Use an ohmmeter to verify that the cable has been correctly installed.

10. Reinstall the CPU in the equipment cabinet.

11. Reconnect all external cables and close the cable rear panel.

12. Power-up the system.

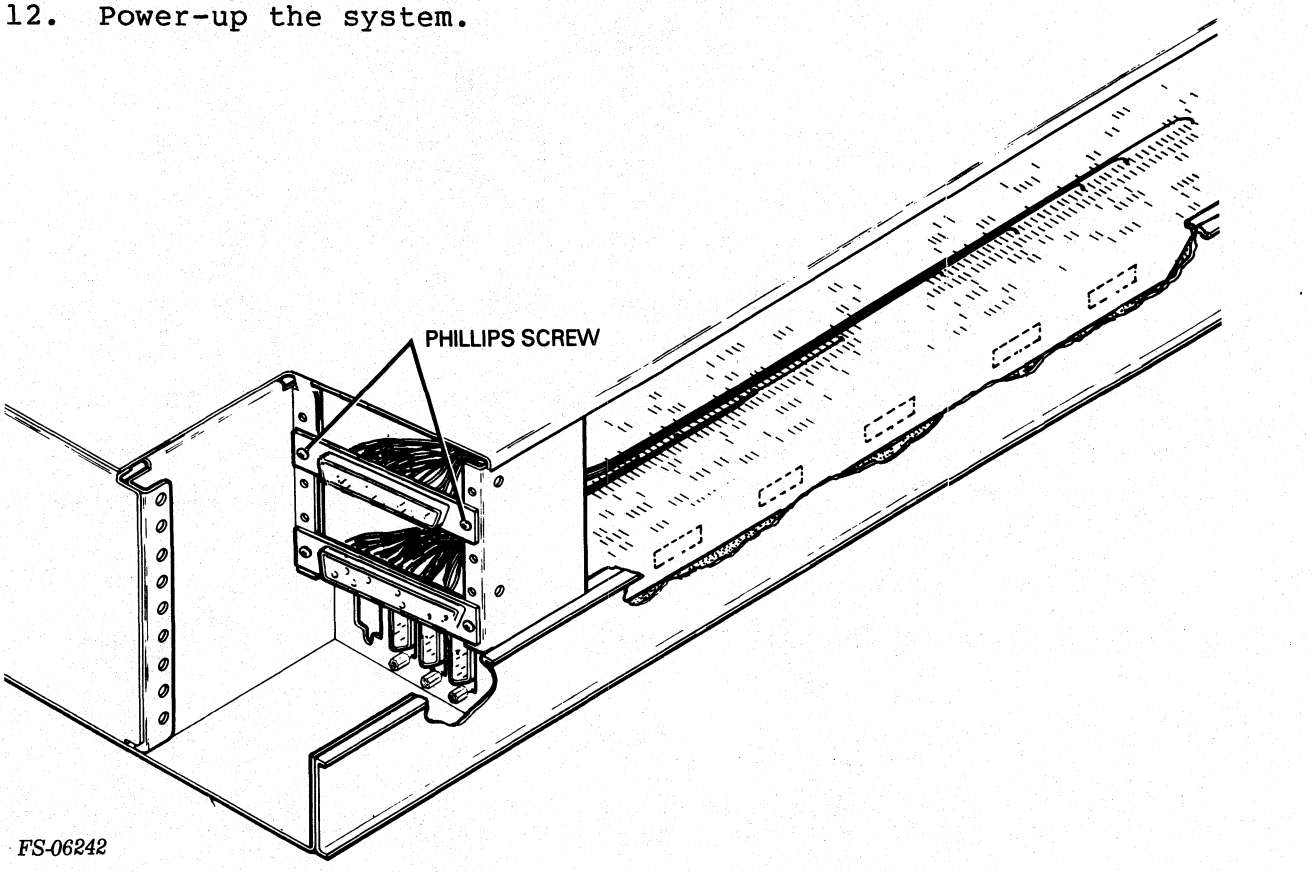


Figure 5-8. Cannon Connectors with Wirewrapped Back Panel

SECTION 6

INSTALLATION/REMOVAL

6.1 INTRODUCTION

An MCA subsystem consists of the following hardware:

- An adapter for each computer in the network.
- A common communications bus.
- Terminators: one for the IN port of the leftmost adapter, and one for the OUT port of the rightmost adapter.
- IN port and OUT port internal cables.

NOTE

An MCA which does not have another MCA connected to its IN port is referred to as the leftmost adapter. The MCA which does not have another MCA connected to its OUT port is referred to as the rightmost adapter.

CAUTION

MCAs from the Model 4206 series should not be used in the same network with MCAs from the Model 4308 series.

6.2 SITE PREPARATION REQUIREMENTS

The site preparation requirements are listed below.

Table 6-1. MCA Dimensions

MCA Board	WIDTH	DEPTH
Millimeter	381.0	381.0
Inches	(15.0)	(15.0)
External Cable Length		
Standard Mode (Maximum):	140 ft, 150 ft (2 MCAs in system)	
High-Speed Mode:	40 ft	
Electrical Characteristics	**SUPPLY VOLTAGE**	**CURRENT**
	+ 5.0 (Vdc)	3.400 (Amps)

6.3 CONFIGURATION REQUIREMENTS

Table 6-1 specifies the limits for the distance between MCAs. The critical limits are the distance between the first and second MCA boards, and the total length of the communications bus (see Figure 6-1). The first and last MCA boards have terminators in one of their ports. The first MCA board, designated as the leftmost, has a terminator in the IN port. The last MCA board, designated as the rightmost, has a terminator in the OUT port.

Table 6-2. MCA Configuration Requirements

SPECIFICATION	STANDARD MODE	HIGH-SPEED MODE
Total MCAs in a System	Up to 15	Up to 4
Total Bus Length (Max):		
Only Two MCAs	45.72 m (150 ft)	12.19 m (40 ft)
More Than Two MCAs	42.67 m (140 ft)	12.19 m (40 ft)
Distance Between First Two MCAs in a System:		
Only Two MCAs (in the system)	45.72 m (max) (150 ft)	12.19 m (max) (40 ft)
Three or More MCAs (in the system)	6.09 m (max) (20 ft)	3.05 m (max) (10 ft)
Distance Between the Remaining MCAs:	The remaining MCAs may be distributed in any way, but can not exceed the maximum total bus length.	

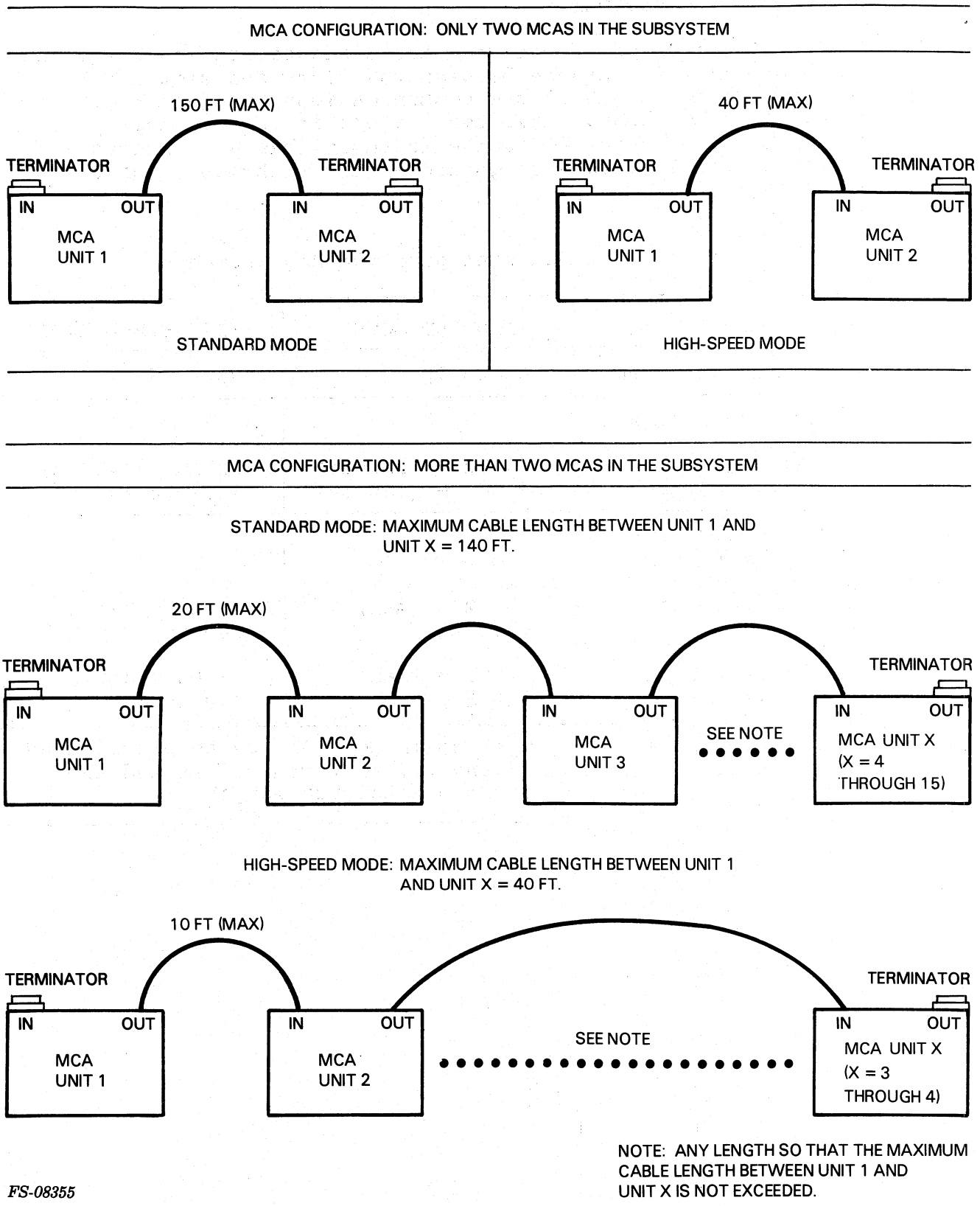


Figure 6-1. MCA Configurations

6.4 MCA SUBSYSTEM INSTALLATION

If the MCA subsystem has been factory installed in the CPUs, proceed to the section on installing the external cables. For on-site installation, the procedure is presented in the following order:

1. Unpacking the MCA subsystem.
2. Preparing the board.
3. Selecting the chassis slot.
4. Installing internal cables.
5. External cables and terminators.

These procedures are described in detail below

6.4.1 Unpacking - The MCA is shipped in the packing kit shown in Figure 6-2 below.

NOTE

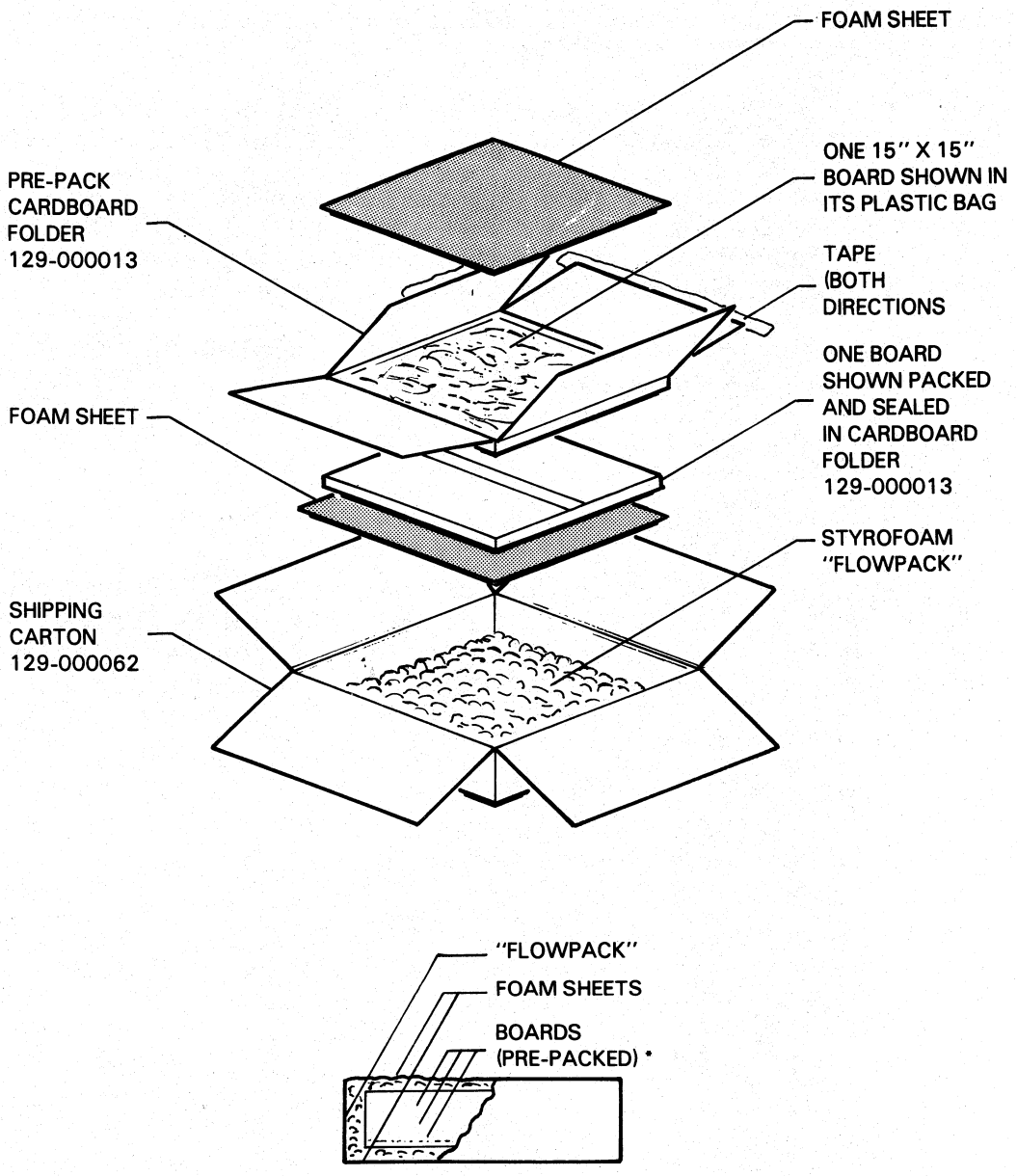
Do not unpack cartons damaged in shipping unless specifically directed to do so by a representative of the carrier or by the Data General Corporation.

Open the shipping container, check the contents against the packing list(s), and note any damaged or missing parts (save the packing material for possible future use).

CAUTION

Metal-Oxide Semiconductor (MOS) IC chips may be damaged by static electricity. When handling PCBs, the customer service personnel should proceed as follows:

1. Before removing the PCB from the protective shipping bag, touch a solid ground to eliminate any static charge.
2. Handle the PCB as little as possible when it is out of the protective shipping bag. Handle the PCB only by the edges.
3. Avoid carpeted floors when handling the PCB especially in low humidity.



* MULTIPLE PACKING--UP TO THREE (3) 15 IN. X 15 IN. BOARDS. ENCLOSED IN PLASTIC BAGS AND SEALED IN PRE-PACKED FOLDERS AS SHOWN, CAN BE PUT IN SHIPPING CARTON NUMBER 129-000062. FOR FOUR (4) TO SEVEN (7) BOARDS. USE SHIPPING CARTON NUMBER 129-000012.

FS-08363

Figure 6-2. MCA Packing Kit

6.4.2 Board Preparation - Before installing the MCA PCB, check both power requirements and jumpering on the board.

6.4.2.1 Power Requirements - Each MCA board draws 3.4 amps of current at +5 Vdc. Before installing the MCA board in the CPU chassis, refer to the appropriate PIP, and locate the installation drawings of each particular CPU for the chassis loading rules. Using the installation drawings, determine the following:

- the total +5 V current drawn by the boards in that chassis to ensure that sufficient +5 V current is available for the MCA.
- whether the CPU chassis has separate fuses for groups of adjacent slots. If so, ensure that the +5 V current drawn by the boards in the group of slots in which the MCA is placed does not exceed the rating of the fuse for that group of slots.

6.4.2.2 Jumper Configuration - The jumpers located on the MCA board are used to select the following parameters:

1. device code
2. identifying number
3. operating mode
4. leftmost and rightmost processor

Figure 6-3 shows the locations of the various jumpers on the MCA board. Note that jumpers W19 and W20 are configured for normal operation as shown in the figure below. Other configurations for these two jumpers are for in-house testing only.

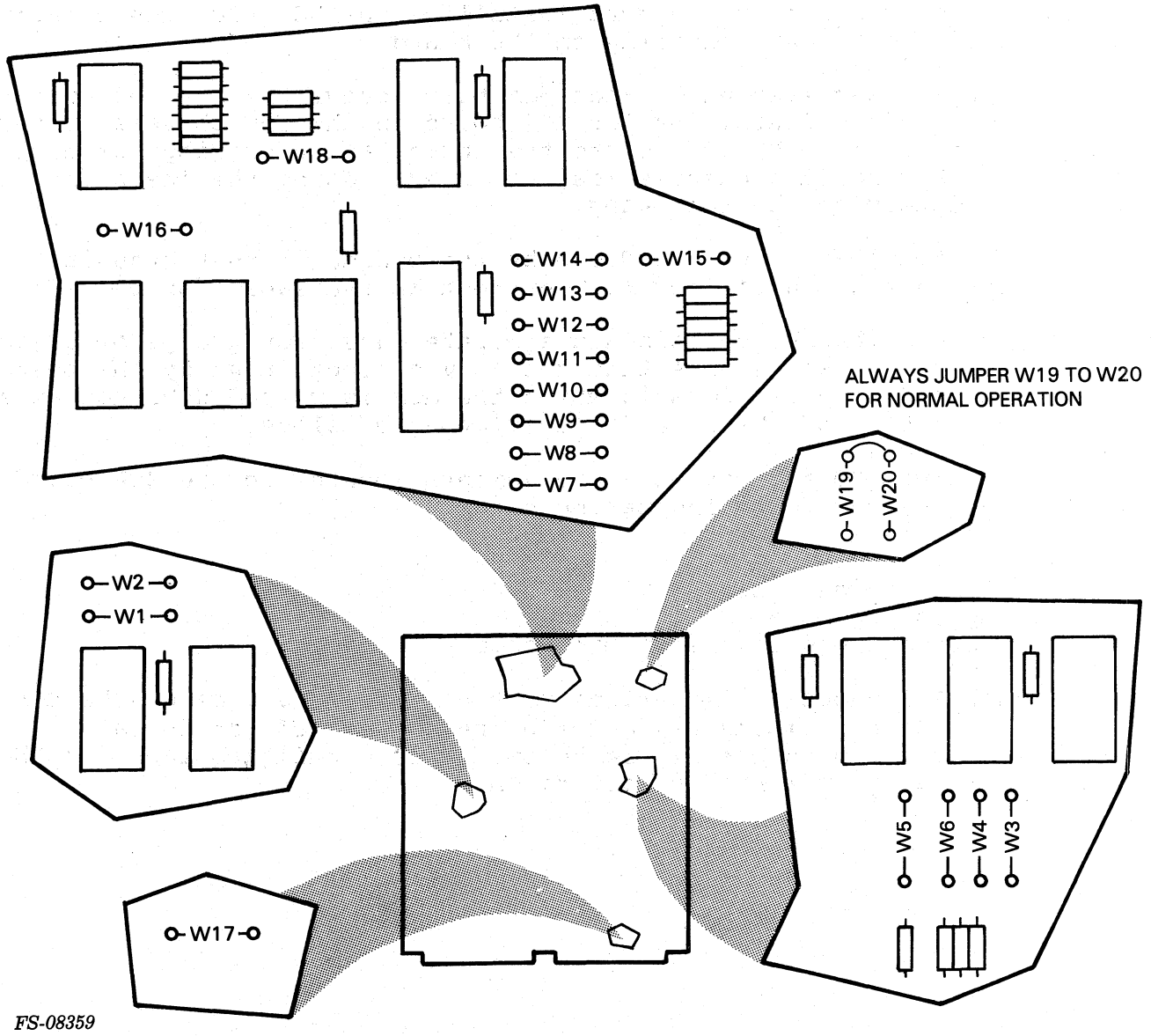


Figure 6-3. MCA Jumper Locations

A. Device Code Select Jumpers - Use device codes 6 and 7 for the first MCA in a computer. Use secondary device codes 46 (octal) and 47 (octal) if a second MCA is installed in the computer. Jumper configurations are listed in Table 6-3 below.

Table 6-3. Device Code Select Jumper Configuration

DEVICE CODE	INSERT JUMPERS
6/7 (MCAT/MCAR)	W1
46/47 (MCAT1/MCAR)	W2, W17

B. Identifying Number Jumpers - Four jumpers are used to specify the binary representation of the selected identifying number. Jumper configurations are listed in Table 6-4 below.

NOTE

Although 0 is a valid identifying number within an MCA network, 0 is not a valid identifying number with Data General's Real-time Disc Operating Systems (RDOS).

Table 6-4. Identifying Number Jumper Configuration

Bit Positions of Identifying No.	MSB 0	1	2	LSB 3
Insert Jumper to Indicate 1 in Required Bit Position	W5	W6	W3	W4

C. Operating Mode Jumpers - Configure jumpers on the leftmost adapter to select either standard or high-speed mode. When selecting high-speed mode, remember that the MCA network contains a maximum of four CPUs when operating in high-speed mode. (The operating mode jumpers on all but the leftmost adapters are used to select the operating mode of the adapter when it is removed from the MCA network and placed in diagnostic mode.) Jumper configurations are listed in Table 6-5 below.

Table 6-5. Operating Mode Jumper Configuration

MODE OF OPERATION	INSERT JUMPERS
Standard	W8, W10, W12, W14, W15
High-Speed	W7, W9, W11, W13

D. Leftmost and Rightmost Processor Jumpers - The leftmost processor jumper, W16, disables the internal clocks of the MCA. Insert jumper W16 in all the adapters in the network, except the leftmost adapter. Do not insert jumper W16 on the leftmost adapter.

The rightmost processor jumper, W18, disables the return of communictions bus priority to the leftmost MCA PCB from all adapters in the network, except the rightmost MCA PCB. Insert jumper W18 in all adapters in the network, except the rightmost adapter. Omit jumper W18 on the rightmost adapter.

NOTE

Newer Rev boards do not have a W18. Rightmost is not relevant to these boards, and can be ignored.

6.4.3 Chassis Slot Selection - The MCA can be placed in any available I/O slot of a NOVA or ECLIPSE CPU. Refer to the PIP for each particular model CPU to determine the locations of the I/O slots.

6.4.3.1 Priority Within the CPU - The proximity to the CPU board determines the interrupt priority within a computer chassis. The boards closest to the CPU board have the highest priority. An open slot must be jumpered to allow boards located beyond that point to request service. Table 6-6 indicates jumper connections for empty I/O slots. Figure 6-4 shows a back panel with jumpers installed.

6.4.3.2 Priority Within NOVA 2, 3, and 800 Series CPUs - The enabling signals in the data channel priority chain are also used by the CPU to determine either high-speed or standard data channel mode. A branch in the priority chain returns the signal to the processor, and any controller requesting data channel service that is connected beyond the branch in the priority chain receives standard data channel service. Normally, the Data Channel Priority (DCHP) (low) signal is returned to the processor on CPU pin A95, through the back panel etch, from DCHP OUT (low) of the top slot of the chassis.

Table 6-6. Jumper Connections For Empty I/O Slots

SIGNAL	ON PIN	TO SIGNAL	ON PIN
$\overline{\text{INTP IN}}$	A96	$\overline{\text{INTP OUT}}$	A95
$\overline{\text{DCHP IN}}$	A94	$\overline{\text{DCHP OUT}}$	A93

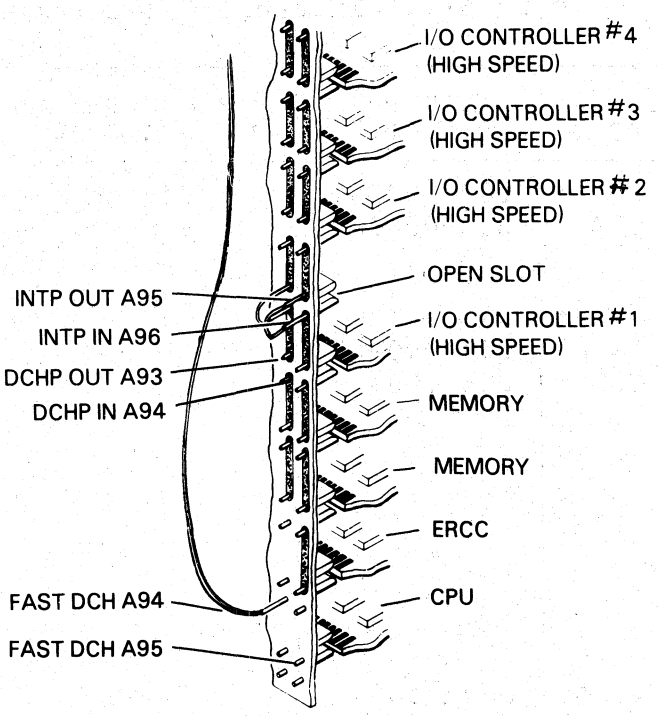


Figure 6-4. Back Panel Interrupt Jumpering

6.4.4 Internal Cable Installation - Internal cable installation varies according to the type of CPU being used. The four categories of internal cables are listed below in the order in which they are presented in this section.

1. back panel plug-on connectors with subD bulkhead connectors for FCC compliant chassis.

2. back panel plug-on connectors with paddleboard connectors for NOVA 4 and ECLIPSE C350, ECLIPSE S140, ECLIPSE S250, and ECLIPSE M600 computers.

3. wirewrapped back panel with paddleboard connectors for NOVA 2, NOVA 3, and ECLIPSE C330, ECLIPSE S230, ECLIPSE S130, ECLIPSE C150, ECLIPSE S200, and ECLIPSE C300 computers.

4. wirewrapped back panel with Cannon connectors for NOVA 1200 and NOVA 800 computers.

Note that a wirewrapped back panel requires two internal cables, one for the OUT port and one for the IN port. See Table 6-7 for internal cable part numbers.

Table 6-7. Internal Cable Part Numbers

CABLE PART NUMBER	PORT	WIRE RUN LIST	TYPE OF EXTERNAL CONNECTOR	USED ON
005-007062 005-007063	IN OUT	008-000899 008-000900	Cannon	NOVA 1200,NOVA 800,NOVA 830,NOVA 840,NOVA Super-NOVA
005-007064 005-007065	IN OUT	008-000901 008-000902	Edge	NOVA 2,NOVA 3,NOVA 820,NOVA 1210, NOVA 1220 ECLIPSE AP130 ECLIPSE C300 ECLIPSE C330 ECLIPSE S130 ECLIPSE S150 ECLIPSE S200 ECLIPSE S230
005-012585	IN & OUT	Push on connector	Edge	Noncompliant versions of NOVA 4, ECLIPSE C350,ECLIPSE M600, ECLIPSE S120 ECLIPSE S140 ECLIPSE S250 ECLIPSE MV/FAMILY Computers
005-019484	IN & OUT	Push on connector	SubD	Compliant versions of NOVA 4 and ECLIPSE Computers

6.4.4.1 Back Panel Plug-on Connectors With SubD Bulkhead Connectors - Use the following steps to install the internal cable.

1. Access the cable bulkhead by opening the rear panel of the cabinet.

2. Swing the cable bulkhead down, and locate the back panel pins for the MCA slot.

3. Connect the back panel connectors of the internal cable to the back panel and plug the two subD connectors into the cable bulkhead. Secure with the screws provided (see Figure 6-5).

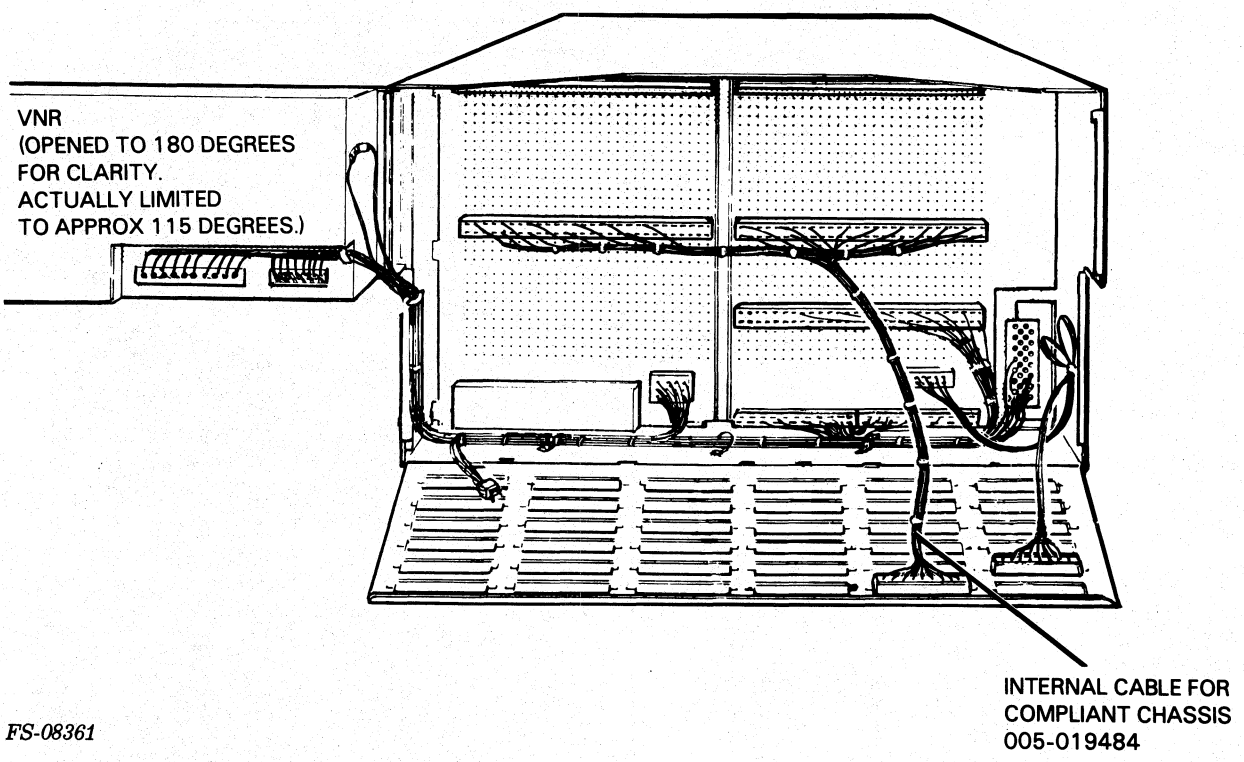


Figure 6-5. Back Panel and EMI Cable Bulkhead

6.4.4.2 Back Panel Plug-on Connectors with Paddleboard Connectors - Use the following steps to install the internal cable.

1. Access the back panel and paddleboard by opening the rear door of the cabinet.
2. Locate the back panel pins for the slot occupied by the MCA board.
3. Plug the internal cable onto the back panel where the MCA is located.
4. Secure the two paddleboard connectors to the chassis using the screws and spacers provided (see Figures 6-6 and 6-7).

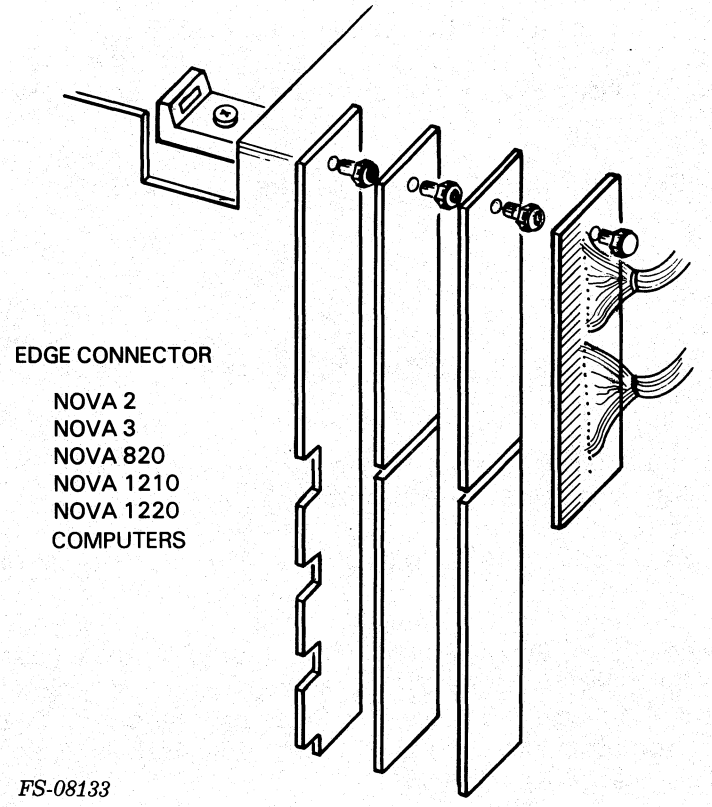


Figure 6-6. Edge Connectors

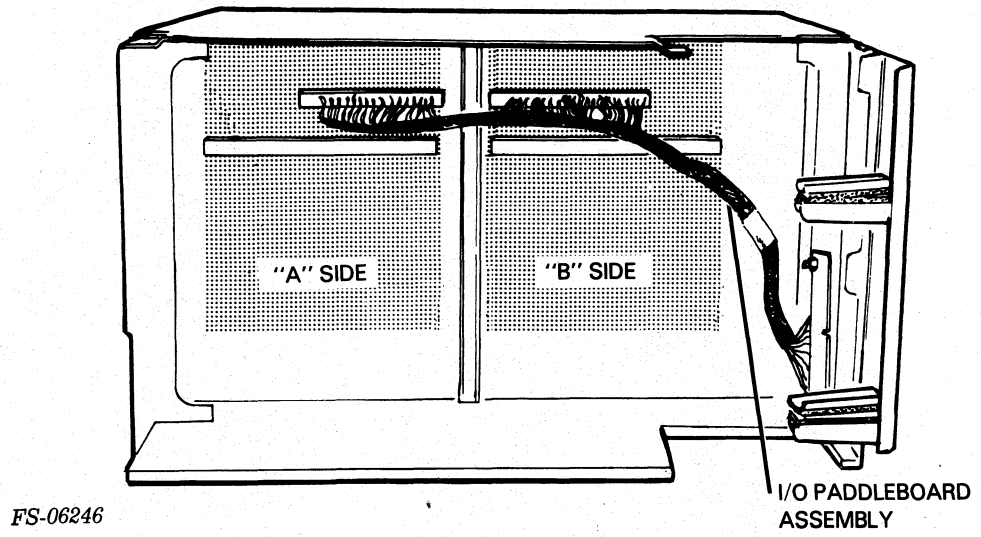


Figure 6-7. Edge Connectors with Side Mounted Paddleboards

6.4.4.3 Wirewrapped Back Panel with Paddleboard Connectors - Use the following steps to install the internal cable.

1. Label and remove all external cables and any terminators from the CPU.

2. Remove the CPU chassis from the cabinet.

CAUTION

To prevent injury to the FE at least two people should be present to remove the CPU from its cabinet.

3. Connect the paddleboard connectors to the chassis using the screws and spacers previously removed.

4. Locate the back panel pins for the slot occupied by the MCA board.

5. Using wirelist 008-000901 for the IN port cable and 008-000902 for the OUT port cable, wirewrap the internal cable to the back panel. Cut the wires leaving enough for a service loop. Use an ohmmeter to verify that the cable has been correctly installed (see Figure 6-8).

6. Reinstall the CPU in the equipment cabinet.

7. Reconnect all external cables.

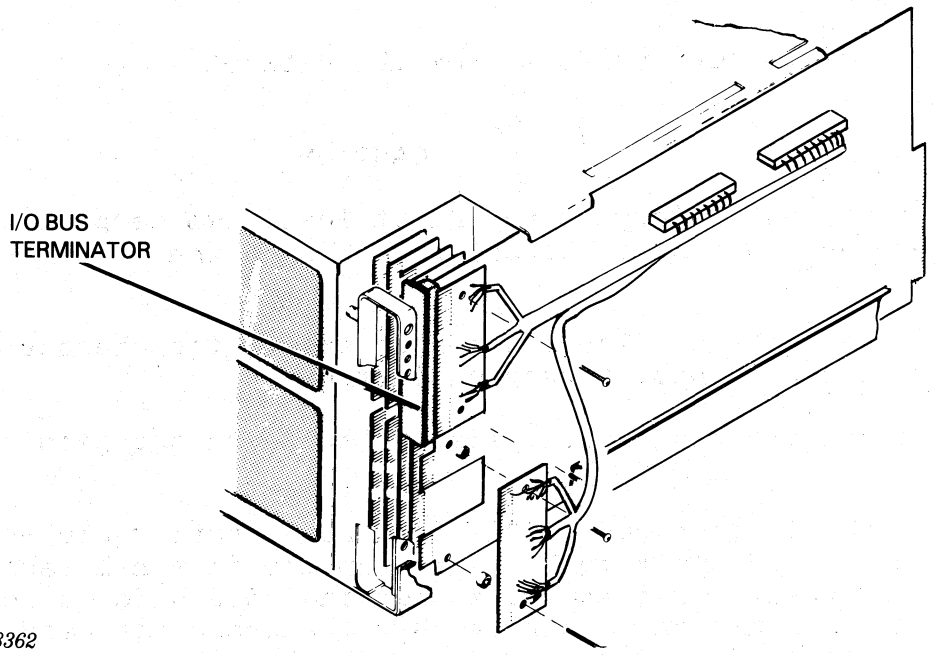


Figure 6-8. Edge Connectors with Wirewrapped Back Panel

6.4.4.4 Wirewrapped Back Panel with Cannon Connectors - Use the following steps to install the internal cable.

1. Label and remove all external cables from the CPU.
2. Remove the CPU chassis from the cabinet.

CAUTION

To prevent injury to the Service Personnel, at least two people should be present to remove the CPU from its cabinet.

3. Connect the Cannon connectors to the chassis using the screws provided.
4. Locate the back panel pins for the slot occupied by the MCA board.
5. Using wirelist 008-000899 for the IN port cable and 008-000900 for the OUT port cable, wirewrap the internal cable to the back panel. Cut the wires leaving enough for a service loop. Use an ohmmeter to verify that the cable has been correctly installed (see Figure 6-9).

6. Reinstall the CPU in the equipment cabinet.

7. Reconnect all external cables.

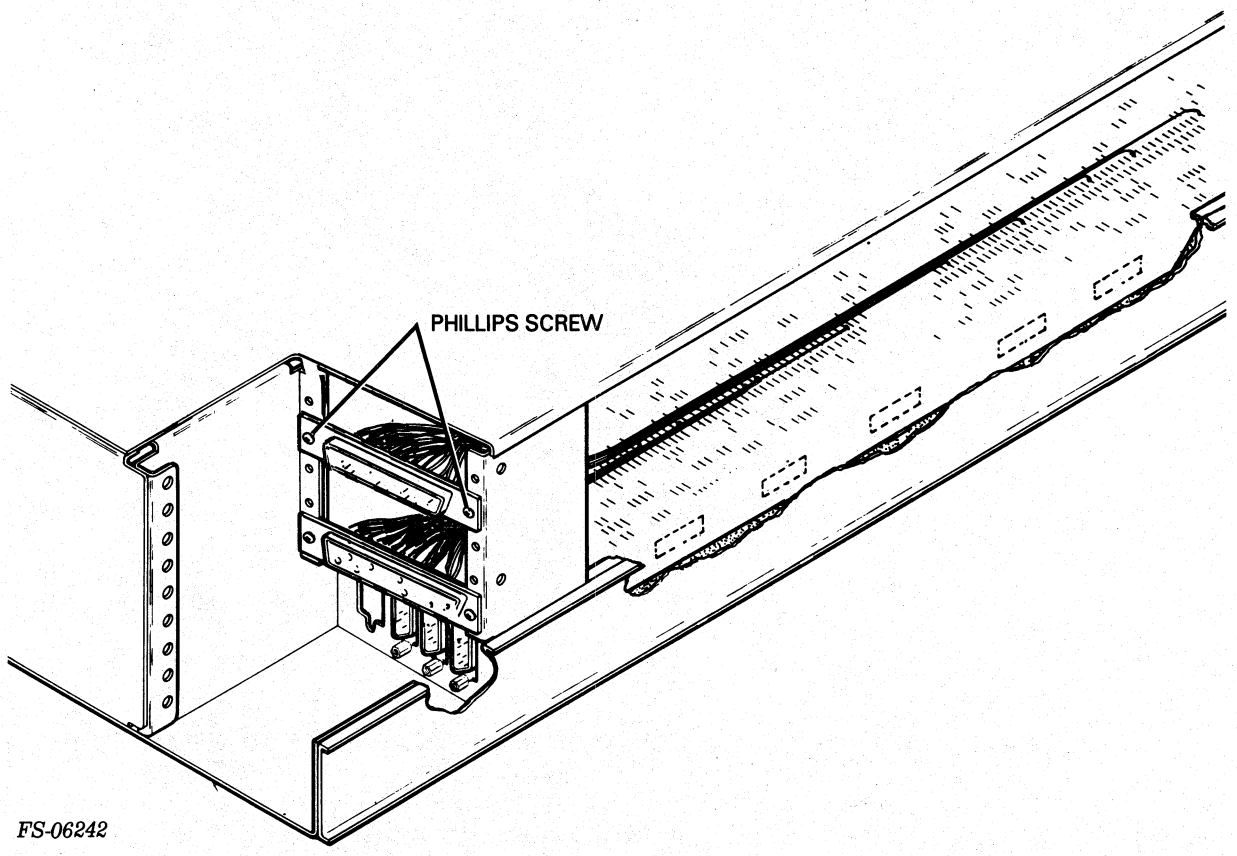


Figure 6-9. Cannon Connectors with Wirewrapped Back Panel

6.4.5 External Cabling and Terminators - All MCA boards except the leftmost and the rightmost require two external cables. The leftmost board has a terminator connected to the IN port and the rightmost board has a terminator in the OUT port. Use the procedure below to install the external cables and terminators.

1. Using the configuration guidelines in Section 6.3, determine the location of the MCA board within the MCA subsystem.

2. Locate the OUT port. If the board is not a rightmost MCA board, connect the appropriate external cable to the port and connect the other end of the cable to the IN port of the next MCA in the subsystem. If the board is the rightmost MCA board, install a terminator in the port.

3. Locate the IN port. If the board is not a leftmost MCA board, connect the appropriate external cable to the port and connect the other end of the cable to the OUT port of the next MCA in the subsystem. If the board is the leftmost MCA board install a terminator in the port.

4. Use steps 1 thru 3 for the remaining MCA boards.

5. When all MCA boards in the subsystem have been connected, close the back panel of the equipment cabinet, and power-up the various CPUs according to the appropriate CPU PIP.

Data General Service, Inc.

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